

# TPD6S300 USB Type-C™ 端口保护器: $V_{BUS}$ 短路过压和 IEC ESD 保护

## 1 特性

- 4 通道  $V_{BUS}$  短路过压保护 (CC1、CC2、SBU1、SBU2) : 24  $V_{DC}$  容差
- 6 通道 IEC 61000-4-2 ESD 保护 (CC1、CC2、SBU1、SBU2、DP、DM)
- CC1、CC2 过压保护 FET 600mA, 能够通过  $V_{CONN}$  电源
- 集成 CC 无电电池电阻器, 可用于处理移动设备中的无电电池用例
- 3mm x 3mm WQFN 封装

## 2 应用

- 笔记本电脑
- 平板电脑
- 智能手机
- 监视器和电视
- 扩展坞

## 3 说明

TPD6S300 是一种单芯片 USB Type-C 端口保护解决方案, 可提供 20V  $V_{BUS}$  短路过压和 IEC ESD 保护。

自从 USB Type-C 连接器发布以来, 已经发布了很多不符合 USB Type-C 规格的 USB Type-C 的产品和配件。其中的一个示例就是仅在  $V_{BUS}$  线路上布设 20V 电压的 USB Type-C 电力输送适配器。USB Type-C 的另一个问题是, 由于此小型连接器中的各引脚极为靠近, 因此连接器的机械扭转和滑动可能使引脚短路。这可能导致 20V  $V_{BUS}$  与 CC 和 SBU 引脚短路。此外, 由于 Type-C 连接器中的各引脚极为靠近, 所以存在碎屑和水汽导致 20V  $V_{BUS}$  引脚与 CC 和 SBU 引脚短路的严重问题。

这些非理想的设备和机械事件使得 CC 和 SBU 引脚必须具有 20V 容差, 即使它们仅在 5V 或更低电压下工作。TPD6S300 通过在 CC 和 SBU 引脚上提供过压保护, 可以使 CC 和 SBU 引脚实现 20V 容差, 同时不会干扰正常工作。该器件将高压 FET 串联放置在 SBU 和 CC 线路上。当在这些线路上检测到高于 OVP 阈值的电压时, 高压开关被打开, 并且将系统的其余部分与连接器上存在的高压状态隔离。

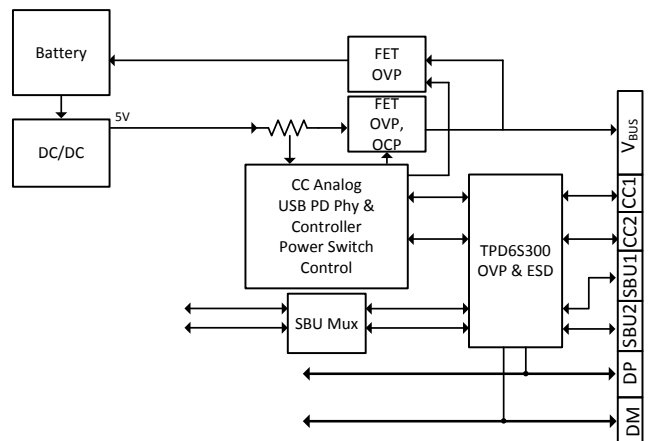
最后, 大多数系统都需要为其外部引脚应用 IEC 61000-4-2 系统级 ESD 保护。TPD6S300 为 CC1、CC2、SBU1、SBU2、DP、DM 引脚集成 IEC 61000-4-2 ESD 保护, 并且无需在连接器上通过外部放置高压 TVS 二极管。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TPD6S300	WQFN (20)	3.00mm x 3.00mm

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

### 应用图表



Copyright © 2016, Texas Instruments Incorporated



## 目录

<b>1</b>	特性 .....	<b>1</b>	8.3	Feature Description .....	<b>16</b>
<b>2</b>	应用 .....	<b>1</b>	8.4	Device Functional Modes .....	<b>19</b>
<b>3</b>	说明 .....	<b>1</b>	<b>9</b>	<b>Application and Implementation</b> .....	<b>20</b>
<b>4</b>	修订历史记录 .....	<b>2</b>	9.1	Application Information .....	<b>20</b>
<b>5</b>	<b>Device Comparison Table</b> .....	<b>3</b>	9.2	Typical Application .....	<b>20</b>
<b>6</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>10</b>	<b>Power Supply Recommendations</b> .....	<b>25</b>
<b>7</b>	<b>Specifications</b> .....	<b>5</b>	<b>11</b>	<b>Layout</b> .....	<b>26</b>
7.1	Absolute Maximum Ratings .....	<b>5</b>	11.1	Layout Guidelines .....	<b>26</b>
7.2	ESD Ratings—JEDEC Specification .....	<b>5</b>	11.2	Layout Example .....	<b>26</b>
7.3	ESD Ratings—IEC Specification .....	<b>5</b>	<b>12</b>	器件和文档支持 .....	<b>27</b>
7.4	Recommended Operating Conditions .....	<b>5</b>	12.1	文档支持 .....	<b>27</b>
7.5	Thermal Information .....	<b>6</b>	12.2	接收文档更新通知 .....	<b>27</b>
7.6	Electrical Characteristics .....	<b>6</b>	12.3	社区资源 .....	<b>27</b>
7.7	Timing Requirements .....	<b>8</b>	12.4	商标 .....	<b>27</b>
7.8	Typical Characteristics .....	<b>10</b>	12.5	静电放电警告 .....	<b>27</b>
<b>8</b>	<b>Detailed Description</b> .....	<b>15</b>	12.6	Glossary .....	<b>27</b>
8.1	Overview .....	<b>15</b>	<b>13</b>	机械、封装和可订购信息 .....	<b>27</b>
8.2	Functional Block Diagram .....	<b>16</b>	13.1	.....	<b>27</b>

## 4 修订历史记录

<b>Changes from Revision B (November 2016) to Revision C</b>		<b>Page</b>
•	Changed units from $\mu$ s to ns for OVP_RESPONSE in the <i>Timing Requirements</i> table .....	<b>8</b>

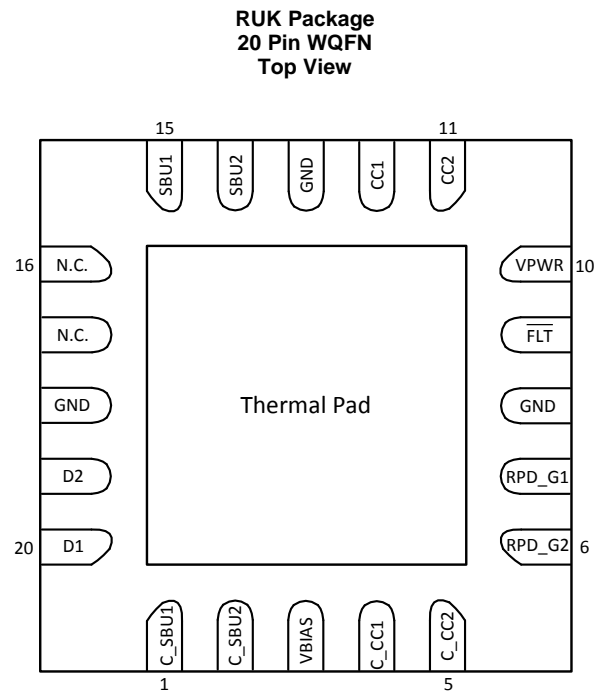
  

<b>Changes from Revision A (September 2016) to Revision B</b>		<b>Page</b>
•	首次公开发布产品说明书 .....	<b>1</b>

## 5 Device Comparison Table

Part Number	Over Voltage Protected Channels	IEC 61000-4-2 ESD Protected Channels
TPD6S300	4-Ch (CC1, CC2, SBU1, SBU2)	6-Ch (CC1, CC2, SBU1, SBU2, DP, DM)
TPD8S300	4-Ch (CC1, CC2, SBU1, SBU2)	8-Ch (CC1, CC2, SBU1, SBU2, DP_T, DM_T, DP_B, DM_B)

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C_SBU1	I/O	Connector side of the SBU1 OVP FET. Connect to either SBU pin of the USB Type-C connector
2	C_SBU2	I/O	Connector side of the SBU2 OVP FET. Connect to either SBU pin of the USB Type-C connector
3	VBIAS	Power	Pin for ESD support capacitor. Place a 0.1- $\mu$ F capacitor on this pin to ground
4	C_CC1	I/O	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector
5	C_CC2	I/O	Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector
6	RPD_G2	I/O	Short to C_CC2 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND
7	RPD_G1	I/O	Short to C_CC1 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND
8	GND	GND	Ground
9	FLT	O	Open drain for fault reporting
10	V_PWR	Power	2.7-V-3.6-V power supply

**Pin Functions (continued)**

PIN		TYPE	DESCRIPTION
NO.	NAME		
11	CC2	I/O	System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller
12	CC1	I/O	System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller
13	GND	GND	Ground
14	SBU2	I/O	System side of the SBU2 OVP FET. Connect to either SBU pin of the SBU MUX
15	SBU1	I/O	System side of the SBU1 OVP FET. Connect to either SBU pin of the SBU MUX
16	N.C.	I/O	Unused pin. Connect to Ground
17	N.C.	I/O	Unused pin. Connect to Ground
18	GND	GND	Ground
19	D2	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector
20	D1	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector
—	Thermal Pad	GND	Internally connected to GND. Used as a heatsink. Connect to the PCB GND plane

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>I</sub>	Input voltage	V <sub>PWR</sub>	-0.3	5	V
		RPD_G1, RPD_G2	-0.3	24	V
V <sub>O</sub>	Output voltage	$\overline{\text{FLT}}$	-0.3	6	V
		VBIAS	-0.3	24	V
V <sub>IO</sub>	I/O voltage	D1, D2	-0.3	6	V
		CC1, CC2, SBU1, SBU2	-0.3	6	V
		C_CC1, C_CC2, C_SBU1, C_SBU2	-0.3	24	V
T <sub>A</sub>	Operating free air temperature	-40	85	°C	
T <sub>stg</sub>	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings—JEDEC Specification

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

### 7.3 ESD Ratings—IEC Specification

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge <sup>(1)</sup>	IEC 61000-4-2, C_CC1, C_CC2, D1, D2	Contact discharge	±8000
			Air-gap discharge	±15000
		IEC 61000-4-2, C_SBU1, C_SBU2	Contact discharge	±6000
			Air-gap discharge	±15000

- (1) Tested on the [TPD6S300 EVM](#) connected to the [TPS65982 EVM](#).

### 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
V <sub>I</sub>	Input voltage	V <sub>PWR</sub>	2.7	3.3	4.5	V
		RPD_G1, RPD_G2	0		5.5	V
V <sub>O</sub>	Output voltage	$\overline{\text{FLT}}$ pull-up resistor power rail			5.5	V
V <sub>IO</sub>	I/O voltage	D1, D2	-0.3		5.5	V
		CC1, CC2, C_CC1, C_CC2	0		5.5	V
		SBU1, SBU2, C_SBU1, C_SBU2	0		4.3	V
I <sub>VCONN</sub>	V <sub>CONN</sub> current	Current flowing into CC1/2 and flowing out of C_CC1/2, VCCx – VC_CCx ≤ 250 mV			600	mA
I <sub>VCONN</sub>	V <sub>CONN</sub> current	Current flowing into CC1/2 and flowing out of C_CC1/2, T <sub>J</sub> ≤ 105°C			1.25	A

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
External components <sup>(1)</sup>	FLT pull-up resistance	1.7		300	kΩ
	VBIAS capacitance <sup>(2)</sup>		0.1		μF
	V <sub>PWR</sub> capacitance	0.3	1		μF

- (1) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented must be within the minimum and maximums listed in the table.
- (2) The VBIAS pin requires a minimum 35-V<sub>DC</sub> rated capacitor. A 50-V<sub>DC</sub> rated capacitor is recommended to reduce capacitance derating. See the [VBIAS Capacitor Selection](#) section for more information on selecting the VBIAS capacitor.

## 7.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD6S300	UNIT
		RUK (WQFN)	
		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	45.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	48.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.6	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CC OVP SWITCHES</b>						
R <sub>ON</sub>	On resistance of CC OVP FETs, T <sub>J</sub> ≤ 85°C	CCx = 5.5 V		278	392	mΩ
	On resistance of CC OVP FETs, T <sub>J</sub> ≤ 105°C	CCx = 5.5 V		278	415	mΩ
R <sub>ON(FLAT)</sub>	On resistance flatness	Sweep CCx voltage between 0 V and 1.2 V			5	mΩ
C <sub>ON_CC</sub>	Equivalent on capacitance	Capacitance from C <sub>CCx</sub> or CCx to GND when device is powered. VC <sub>CCx</sub> /VCCx = 0 V to 1.2 V, f = 400 kHz	60	74	120	pF
R <sub>D</sub>	Dead battery pull-down resistance (only present when device is unpowered). Effective resistance of R <sub>D</sub> and FET in series	V <sub>C<sub>CCx</sub></sub> = 2.6 V	4.1	5.1	6.1	kΩ
V <sub>TH_DB</sub>	Threshold voltage of the pulldown FET in series with RD during dead battery	I <sub>CC</sub> = 80 μA	0.5	0.9	1.2	V
V <sub>OVPCC</sub>	OVP threshold on CC pins	Place 5.5 V on C <sub>CCx</sub> . Step up C <sub>CCx</sub> until the FLT pin is asserted	5.75	6	6.2	V
V <sub>OVPCC_HYS</sub>	Hysteresis on CC OVP	Place 6.5 V on C <sub>CCx</sub> . Step down the voltage on C <sub>CCx</sub> until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C <sub>CCx</sub>		50		mV
BW <sub>ON</sub>	On bandwidth single ended (–3 dB)	Measure the –3-dB bandwidth from C <sub>CCx</sub> to CCx. Single ended measurement, 50-Ω system. V <sub>cm</sub> = 0.1 V to 1.2 V		100		MHz

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>STBUS_CC</sub>	Short-to-VBUS tolerance on the CC pins	Hot-Plug C <sub>CCx</sub> with a 1 meter USB Type C Cable, place a 30-Ω load on CCx			24	V
V <sub>STBUS_CC_CL AMP</sub>	Short-to-VBUS system-side clamping voltage on the CC pins (CCx)	Hot-Plug C <sub>CCx</sub> with a 1 meter USB Type C Cable. Hot-Plug voltage C <sub>CCx</sub> = 24 V. VPWR = 3.3 V. Place a 30-Ω load on CCx		8		V
<b>SBU OVP SWITCHES</b>						
R <sub>ON</sub>	On resistance of SBU OVP FETs	SBUx = 3.6 V. -40°C ≤ T <sub>J</sub> ≤ +85°C		4	6.5	Ω
R <sub>ON(FLAT)</sub>	On resistance flatness	Sweep SBUx voltage between 0 V and 3.6 V. -40°C ≤ T <sub>J</sub> ≤ +85°C		0.7	1.5	Ω
C <sub>ON_SBU</sub>	Equivalent on capacitance	Capacitance from SBUx or C <sub>SBUx</sub> to GND when device is powered. Measure at VC <sub>SBUx</sub> /V <sub>SBUx</sub> = 0.3 V to 3.6 V		6		pF
V <sub>OVP SBU</sub>	OVP threshold on SBU pins	Place 3.6 V on C <sub>SBUx</sub> . Step up C <sub>SBUx</sub> until the FLT pin is asserted	4.35	4.5	4.7	V
V <sub>OVP SBU_HYS</sub>	Hysteresis on SBU OVP	Place 5 V on C <sub>CCx</sub> . Step down the voltage on C <sub>CCx</sub> until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C <sub>SBUx</sub>		50		mV
BW <sub>ON</sub>	On bandwidth single ended (-3 dB)	Measure the -3-dB bandwidth from C <sub>SBUx</sub> to SBUx. Single ended measurement, 50-Ω system. V <sub>cm</sub> = 0.1 V to 3.6 V		1000		MHz
X <sub>TALK</sub>	Crosstalk	Measure crosstalk at f = 1 MHz from SBU1 to C <sub>SBU2</sub> or SBU2 to C <sub>SBU1</sub> . V <sub>cm1</sub> = 3.6 V, V <sub>cm2</sub> = 0.3 V. Be sure to terminate open sides to 50 Ω		-80		dB
V <sub>STBUS_SBU</sub>	Short-to-VBUS tolerance on the SBU pins	Hot-Plug C <sub>SBUx</sub> with a 1 meter USB Type C Cable. Put a 100-nF capacitor in series with a 40-Ω resistor to GND on SBUx			24	V
V <sub>STBUS_SBU_C LAMP</sub>	Short-to-VBUS system-side clamping voltage on the SBU pins (SBUx)	Hot-Plug C <sub>SBUx</sub> with a 1 meter USB Type C Cable. Hot-Plug voltage C <sub>SBUx</sub> = 24 V. VPWR = 3.3 V. Put a 150-nF capacitor in series with a 40-Ω resistor to GND on SBUx		8		V
<b>POWER SUPPLY and LEAKAGE CURRENTS</b>						
V <sub>PWR_UVLO</sub>	V <sub>PWR</sub> under voltage lockout	Place 1 V on VPWR and raise voltage until SBU or CC FETs turnon	2.1	2.3	2.5	V
V <sub>PWR_UVLO_HYS</sub>	V <sub>PWR</sub> UVLO hysteresis	Place 3 V on VPWR and lower voltage until SBU or CC FETs turnoff; measure difference between rising and falling UVLO to calculate hysteresis	100	150	200	mV
I <sub>VPWR</sub>	V <sub>PWR</sub> supply current	VPWR = 3.3 V (typical), VPWR = 4.5 V (maximum). -40°C ≤ T <sub>J</sub> ≤ +85°C.		90	135	μA
I <sub>CC_LEAK</sub>	Leakage current for CC pins when device is powered	VPWR = 3.3 V, VC <sub>CCx</sub> = 3.6 V, CCx pins are floating, measure leakage into C <sub>CCx</sub> pins. Result must be same if CCx side is biased and C <sub>CCx</sub> is left floating			5	μA

**Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SBU\_LEAK}$	Leakage current for SBU pins when device is powered	VPWR = 3.3 V, VC_SBUx = 3.6 V, SBUx pins are floating, measure leakage into C_SBUx pins. Result must be same if SBUx side is biased and C_SBUx is left floating. $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$			3	$\mu\text{A}$
$I_{C\_CC\_LEAK\_OV\_P}$	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_CCx = 24 V, CCx pins are set to 0 V, measure leakage into C_CCx pins			1200	$\mu\text{A}$
$I_{C\_SBU\_LEAK\_OV\_VP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_SBUx = 24 V, SBUx pins are set to 0 V, measure leakage into C_SBUx pins			400	$\mu\text{A}$
$I_{CC\_LEAK\_OVP}$	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_CCx = 24 V, CCx pins are set to 0 V, measure leakage out of CCx pins			30	$\mu\text{A}$
$I_{SBU\_LEAK\_OVP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_SBUx = 24 V, SBUx pins are set to 0 V, measure leakage out of SBUx pins	-1		1	$\mu\text{A}$
$I_{Dx\_LEAK}$	Leakage current for Dx pins	V_Dx = 3.6 V, measure leakage into Dx pins			1	$\mu\text{A}$
<b>FLT PIN</b>						
$V_{OL}$	Low-level output voltage	IOL = 3 mA. Measure the voltage at the FLT pin			0.4	V
<b>OVER TEMPERATURE PROTECTION</b>						
$T_{SD\_RISING}$	The rising over-temperature protection shutdown threshold		150	175		$^{\circ}\text{C}$
$T_{SD\_FALLING}$	The falling over-temperature protection shutdown threshold		130	140		$^{\circ}\text{C}$
$T_{SD\_HYST}$	The over-temperature protection shutdown threshold hysteresis			35		$^{\circ}\text{C}$
<b>Dx ESD PROTECTION</b>						
$V_{RWM\_POS}$	Reverse stand-off voltage from Dx to GND	Dx to GND. $I_{Dx} \leq 1 \mu\text{A}$			5.5	V
$V_{RWM\_NEG}$	Reverse stand-off voltage from GND to Dx	GND to Dx			0	V
$V_{BR\_POS}$	Break-down voltage from Dx to GND	Dx to GND. $I_{BR} = 1 \text{ mA}$	7			V
$V_{BR\_NEG}$	Break-down voltage from GND to Dx	GND to Dx. $I_{BR} = 8 \text{ mA}$	0.6			V
$C_{IO}$	Dx to GND or GND to Dx	f = 1 MHz, VIO = 2.5 V		1.7		pF
$\Delta C_{IO}$	Differential capacitance between two Dx pins	f = 1 MHz, VIO = 2.5 V		0.02		pF
$R_{DYN}$	Dynamic on-resistance Dx IEC clamps	Dx to GND or GND to Dx		0.4		$\Omega$

**7.7 Timing Requirements**

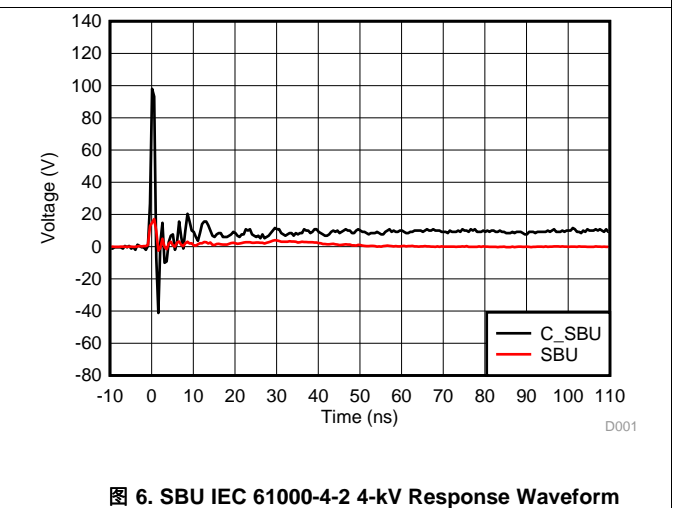
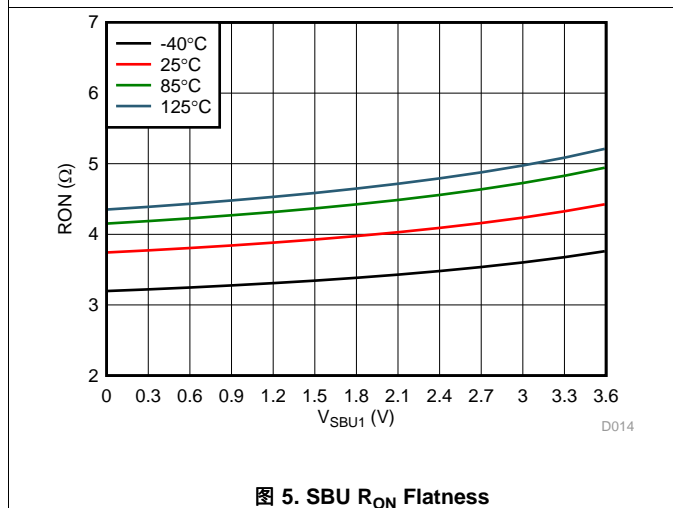
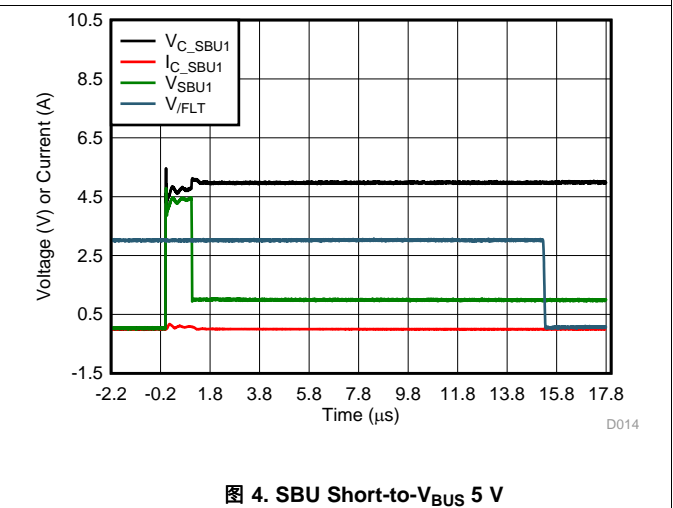
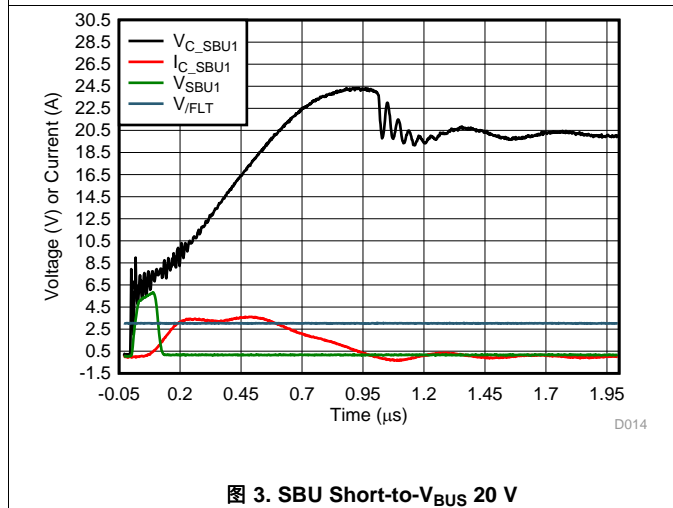
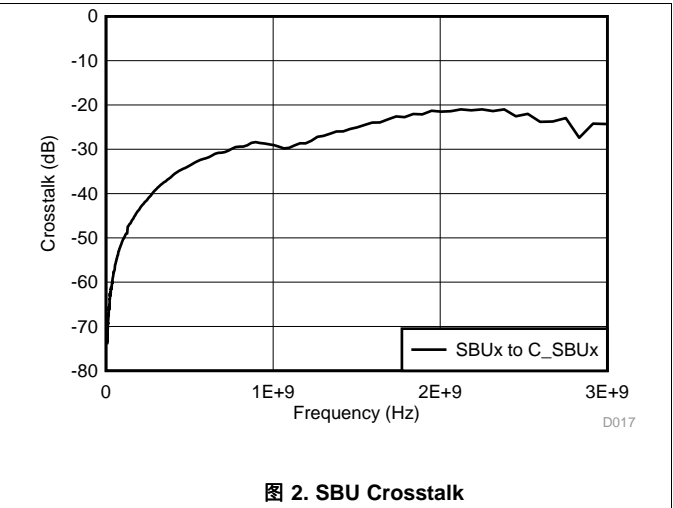
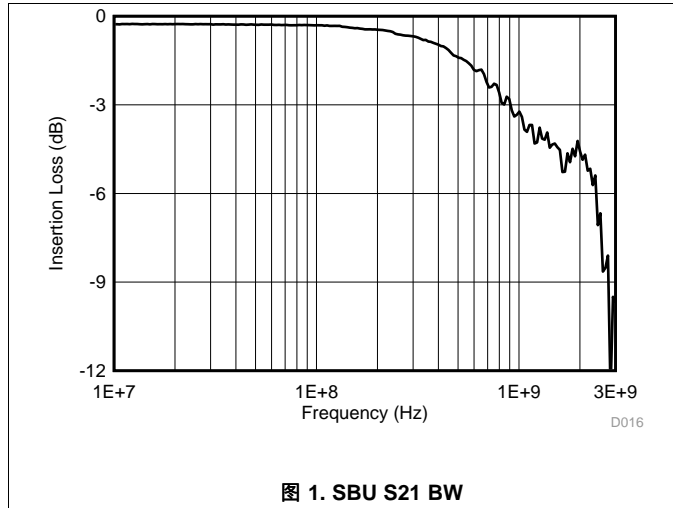
		MIN	NOM	MAX	UNIT
<b>POWER-ON and Off TIMINGS</b>					
$t_{ON}$	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on			3.5	ms
$dV_{PWR\_OFF}/dt$	Minimum Slew rate allowed to guarantee CC and SBU FETs turnoff during a power off	-0.5			V/ $\mu\text{s}$
<b>OVER VOLTAGE PROTECTION</b>					
$t_{OVP\_RESPONSE\_CC}$	OVP response time on the CC pins. Time from OVP asserted until OVP FETs turnoff		70		ns



**Timing Requirements (continued)**

		<b>MIN</b>	<b>NOM</b>	<b>MAX</b>	<b>UNIT</b>
$t_{\text{OVP\_RESPONSE\_SBU}}$	OVP response time on the SBU pins. Time from OVP asserted until OVP FETs turnoff		80		ns
$t_{\text{OVP\_RECOVERY\_CC\_1}}$	OVP recovery time on the CC pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on. OVP must be removed for CC FETs to turn back on	21	29	39	ms
$t_{\text{OVP\_RECOVERY\_SBU\_1}}$	OVP recovery time on the SBU pins. Once an OVP has occurred, the minimum time duration until the SBU FETs turn back on. OVP must be removed for SBU FETs to turn back on	21	29	39	ms
$t_{\text{OVP\_RECOVERY\_CC\_2}}$	OVP recovery time on the CC pins. Time from OVP Removal until CC FET turns back on, if device has been in OVP > 40 ms		0.5		ms
$t_{\text{OVP\_RECOVERY\_SBU\_2}}$	OVP recovery time on the SBU pins. Time from OVP Removal until SBU FET turns back on, if device has been in OVP > 40 ms		0.5		ms
$t_{\text{OVP\_FLT\_ASSERTION}}$	Time from OVP asserted to $\overline{\text{FLT}}$ assertion		20		$\mu\text{s}$
$t_{\text{OVP\_FLT\_DEASSERTION}}$	Time from CC FET turnon after an OVP to $\overline{\text{FLT}}$ deassertion		5		ms

### 7.8 Typical Characteristics



Typical Characteristics (接下页)

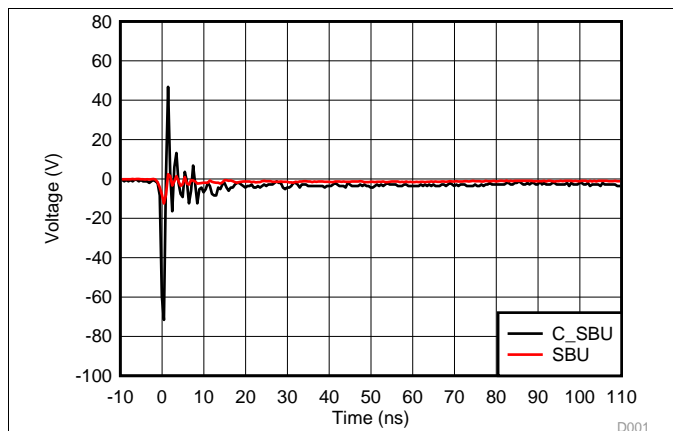


图 7. SBU IEC 61000-4-2 -4-kV Response Waveform

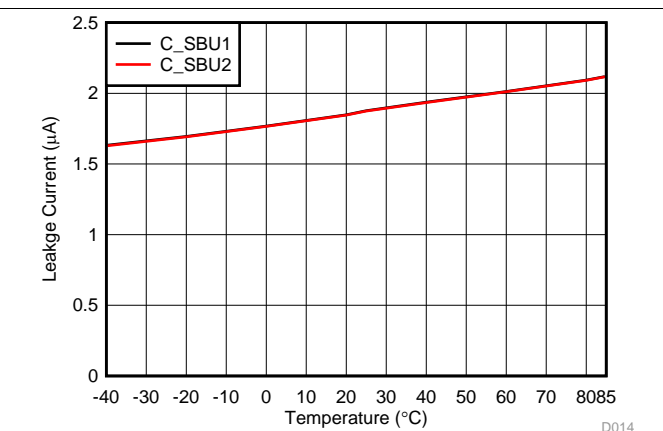


图 8. SBU Path Leakage Current vs Ambient Temperature at 3.6 V

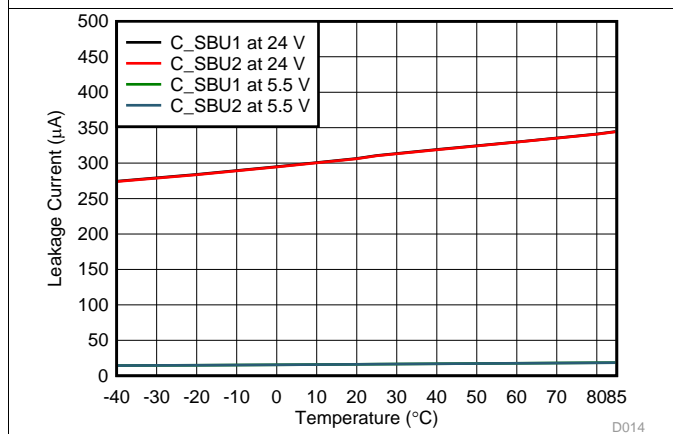


图 9. C\_SBU OVP Leakage Current vs Ambient Temperature at 5.5 V and 24 V

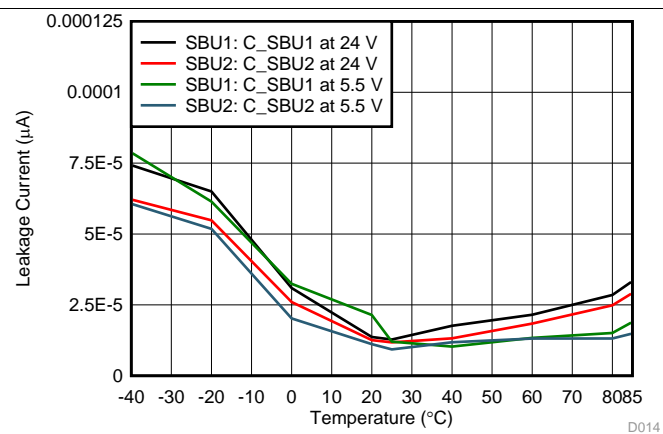


图 10. SBU OVP Leakage Current vs Ambient Temperature at 5.5 V and 24 V

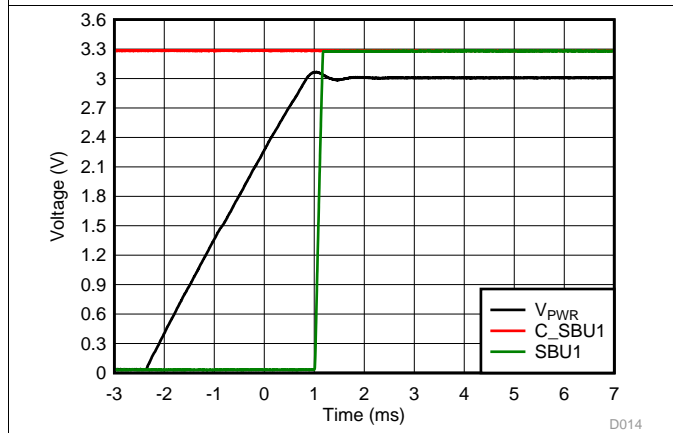


图 11. SBU FET Turnon Timing

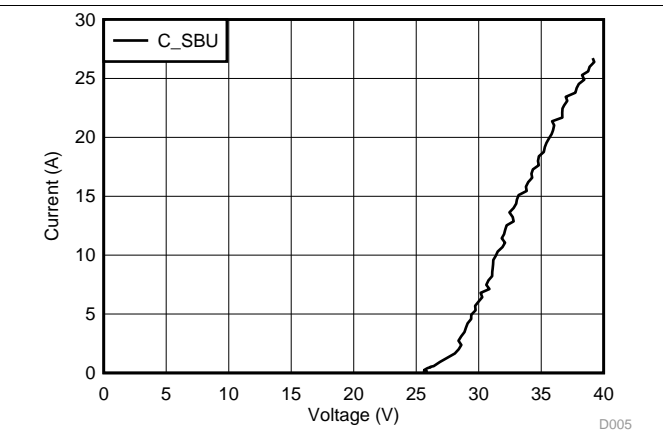


图 12. C\_SBU TLP Curve Unpowered

Typical Characteristics (接下页)

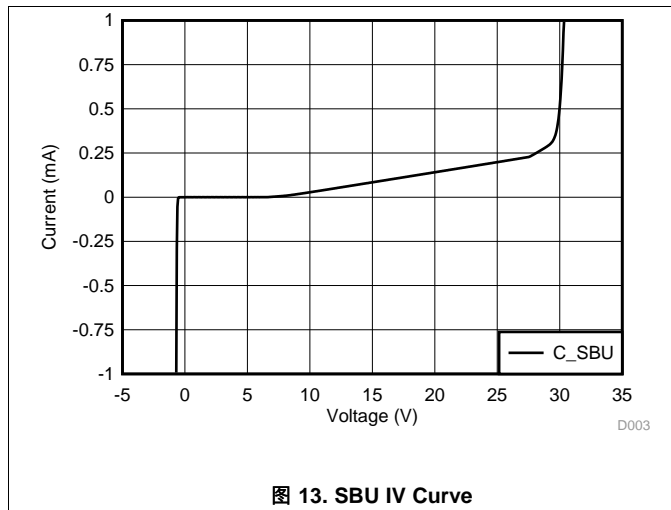


图 13. SBU IV Curve

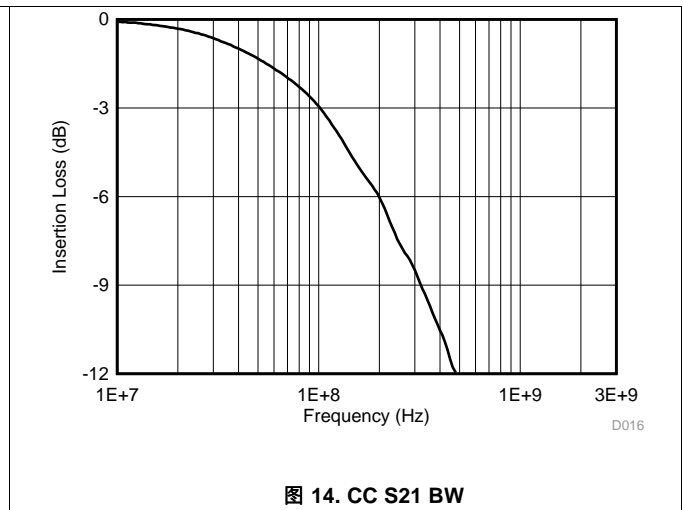


图 14. CC S21 BW

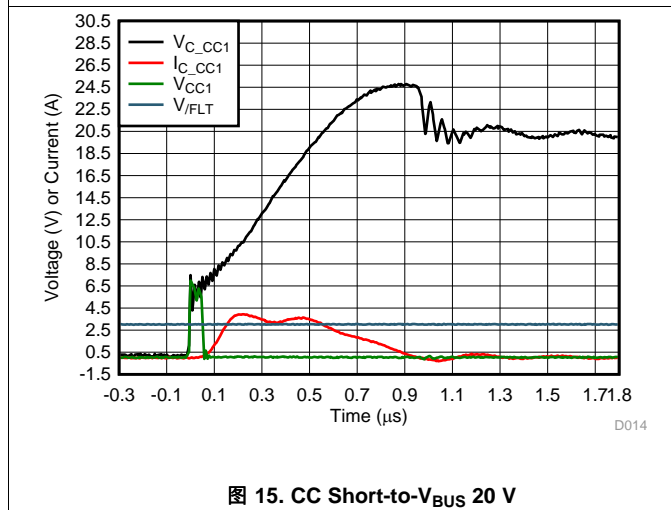


图 15. CC Short-to-V<sub>BUS</sub> 20 V

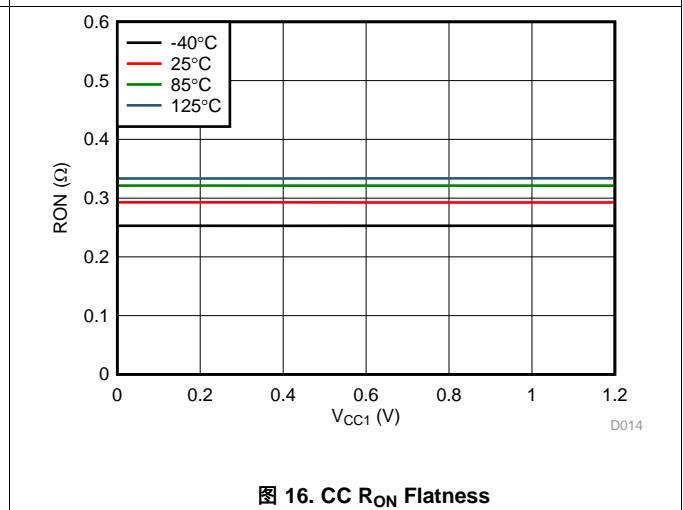


图 16. CC R<sub>ON</sub> Flatness

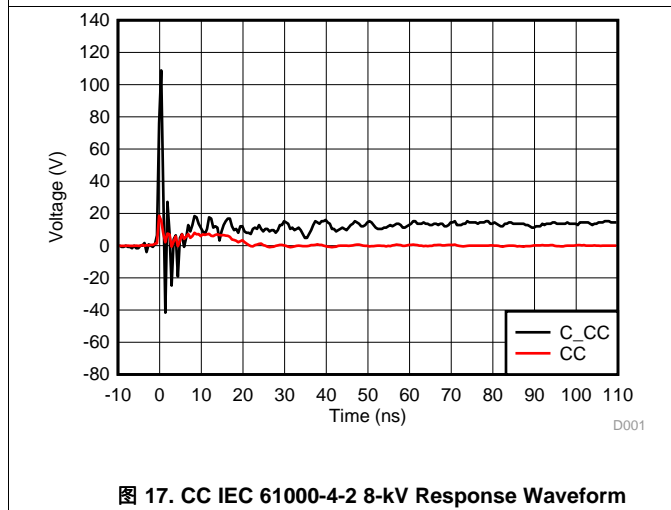


图 17. CC IEC 61000-4-2 8-kV Response Waveform

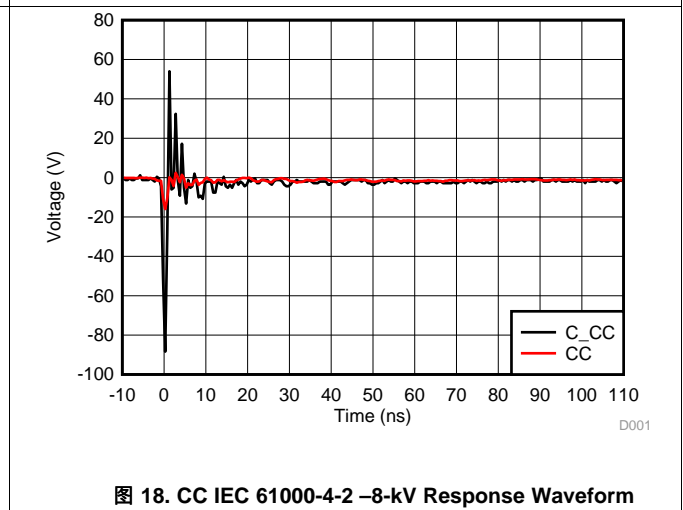


图 18. CC IEC 61000-4-2 -8-kV Response Waveform

Typical Characteristics (接下页)

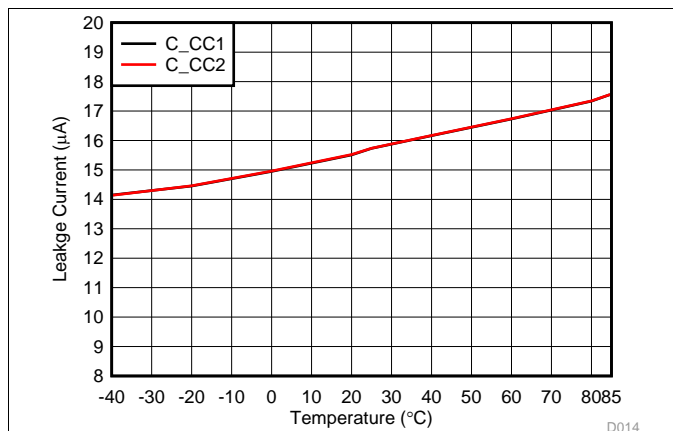


图 19. C\_CC Path Leakage Current vs Ambient Temperature at C\_CC = 5.5 V

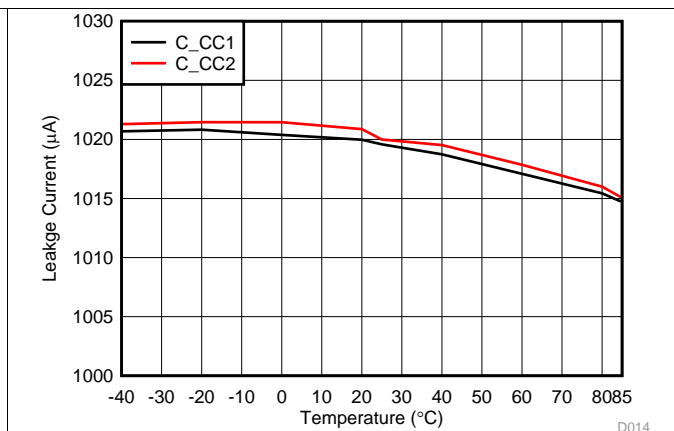


图 20. C\_CC OVP Leakage Current vs Ambient Temperature at C\_CC = 24 V

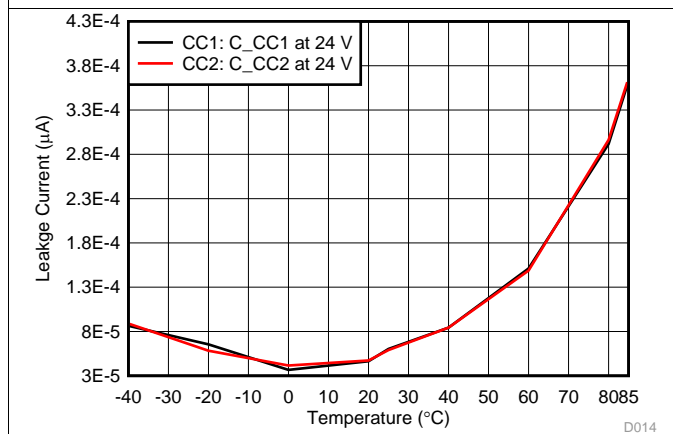


图 21. CC OVP Leakage Current vs Ambient Temperature at C\_CC = 24 V

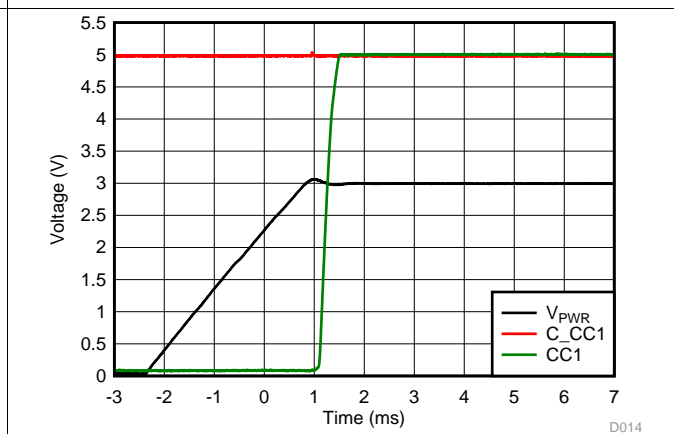


图 22. CC FET Turnon Timing

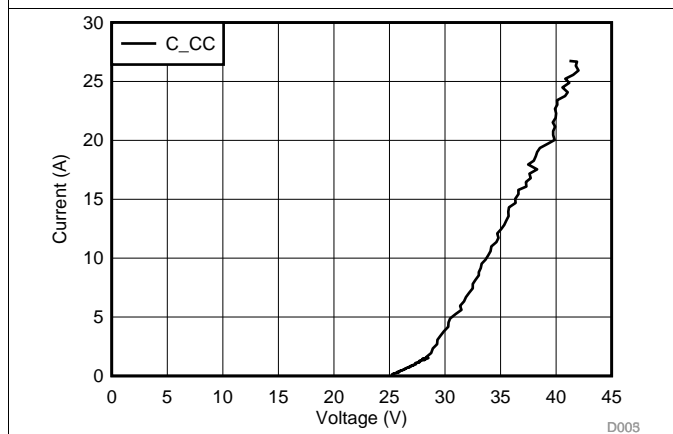


图 23. C\_CC TLP Curve Unpowered

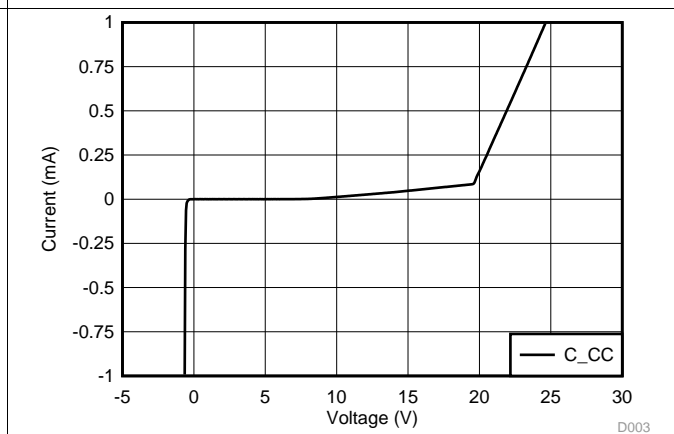
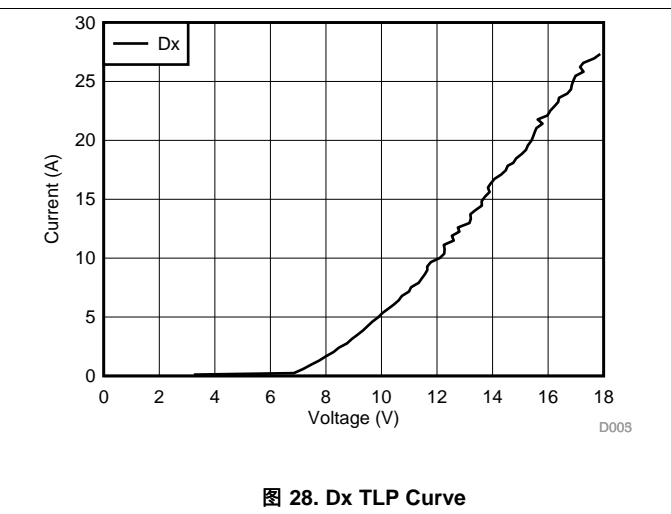
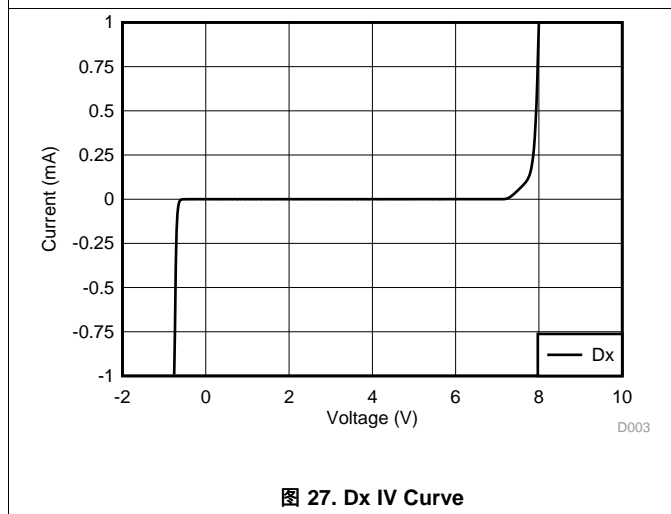
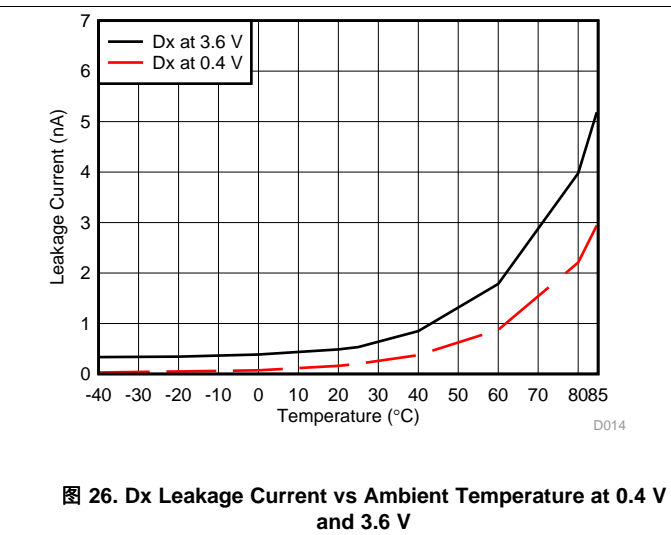
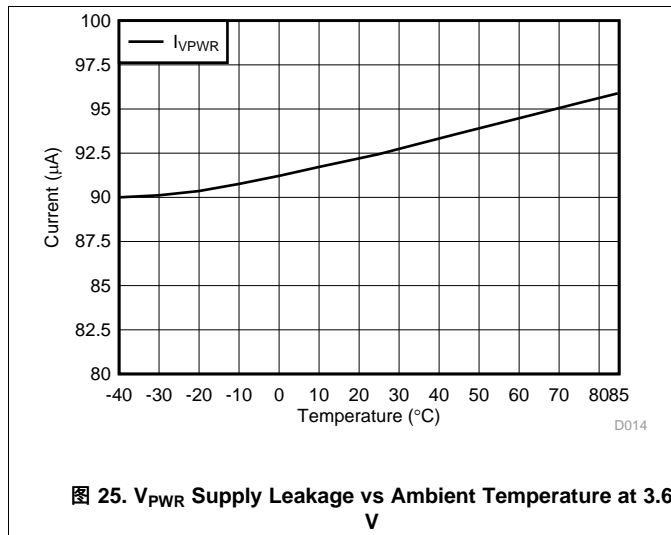


图 24. C\_CC IV Curve

Typical Characteristics (接下页)



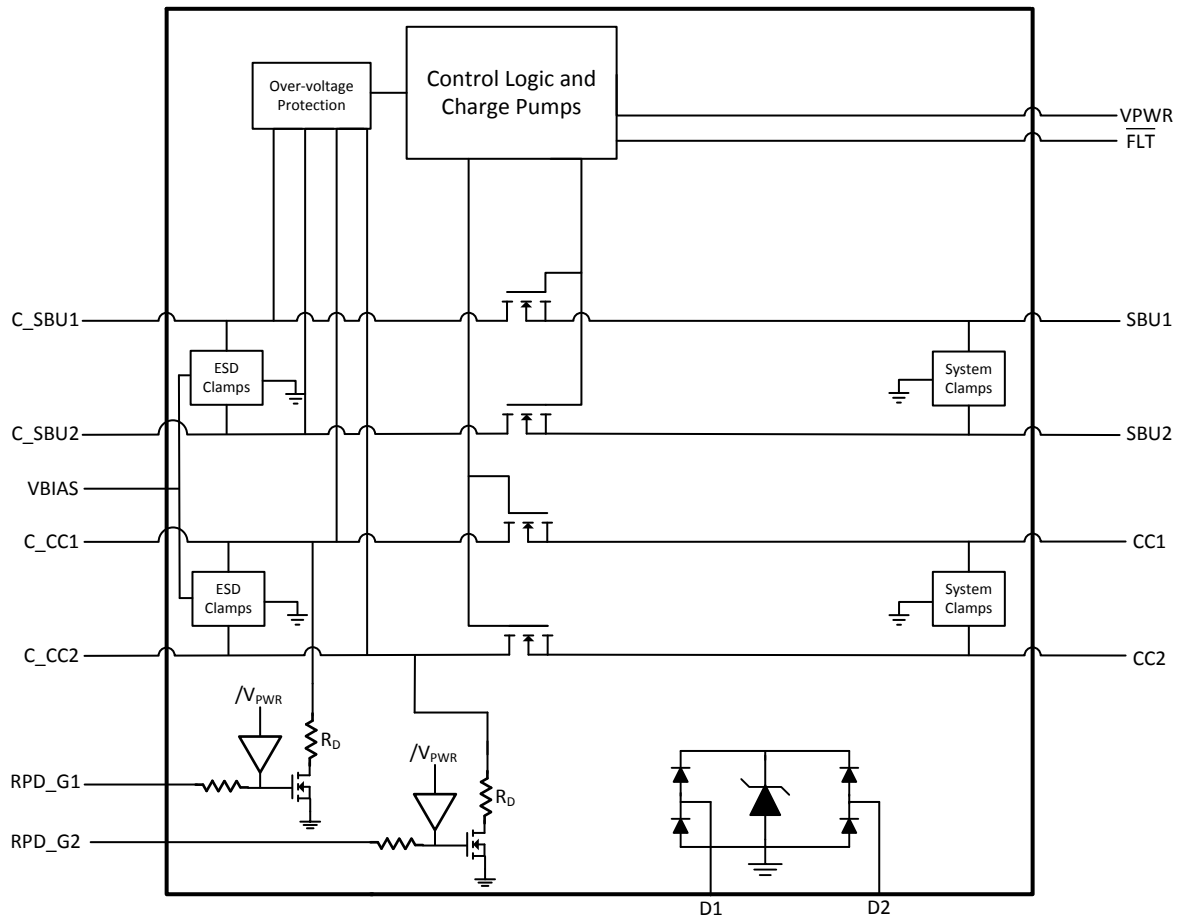
## 8 Detailed Description

### 8.1 Overview

The TPD6S300 is a single chip USB Type-C port protection solution that provides 20-V Short-to- $V_{BUS}$  overvoltage and IEC ESD protection. Due to the small pin pitch of the USB Type-C connector and non-compliant USB Type-C cables and accessories, the  $V_{BUS}$  pins can get shorted to the CC and SBU pins inside the USB Type-C connector. Because of this short-to- $V_{BUS}$  event, the CC and SBU pins need to be 20-V tolerant, to support protection on the full USB PD voltage range. Even if a device does not support 20-V operation on  $V_{BUS}$ , non-complaint adaptors can start out with 20-V  $V_{BUS}$  condition, making it necessary for any USB Type-C device to support 20 V protection. The TPD6S300 integrates four channels of 20-V Short-to- $V_{BUS}$  overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector.

Additionally, IEC 61000-4-2 system level ESD protection is required in order to protect a USB Type-C port from ESD strikes generated by end product users. The TPD6S300 integrates eight channels of IEC61000-4-2 ESD protection for the CC1, CC2, SBU1, SBU2, DP\_T (Top side D+), DM\_T (Top Side D–), DP\_B (Bottom Side D+), and DM\_B (Bottom Side D–) pins of the USB Type-C connector. This means IEC ESD protection is provided for all of the low-speed pins on the USB Type-C connector in a single chip in the TPD6S300. Additionally, high-voltage IEC ESD protection that is 22-V DC tolerant is required for the CC and SBU lines in order to simultaneously support IEC ESD and Short-to- $V_{BUS}$  protection; there are not many discrete market solutions that can provide this kind of protection. This high-voltage IEC ESD diode is what the TPD6S300 integrates, specifically designed to guarantee it works in conjunction with the overvoltage protection FETs inside the device. This sort of solution is very hard to generate with discrete components.

## 8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

## 8.3 Feature Description

### 8.3.1 4-Channels of Short-to- $V_{BUS}$ Overvoltage Protection (CC1, CC2, SBU1, SBU2 Pins): 24- $V_{DC}$ Tolerant

The TPD6S300 provides 4-channels of Short-to- $V_{BUS}$  Overvoltage Protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector. The TPD6S300 is able to handle 24- $V_{DC}$  on its C\_CC1, C\_CC2, C\_SBU1, and C\_SBU2 pins. This is necessary because according to the USB PD specification, with  $V_{BUS}$  set for 20-V operation, the  $V_{BUS}$  voltage is allowed to legally swing up to 21 V, and 21.5 V on voltage transitions from a different USB PD  $V_{BUS}$  voltage. The TPD6S300 builds in tolerance up to 24- $V_{BUS}$  to provide margin above this 21.5 V specification to be able to support USB PD adaptors that may break the USB PD specification.

When a short-to- $V_{BUS}$  event occurs, ringing happens due to the RLC elements in the hot-plug event. With very low resistance in this RLC circuit, ringing up to twice the settling voltage can appear on the connector. More than 2x ringing can be generated if any capacitor on the line derates in capacitance value during the short-to- $V_{BUS}$  event. This means that more than 44 V could be seen on a USB Type-C pin during a Short-to- $V_{BUS}$  event. The TPD6S300 has built in circuit protection to handle this ringing. The diode clamps used for IEC ESD protection also clamp the ringing voltage during the short-to- $V_{BUS}$  event to limit the peak ringing to around 30 V. Additionally, the overvoltage protection FETs integrated inside the TPD6S300 are 30-V tolerant, therefore being capable of supporting the high-voltage ringing waveform that is experienced during the short-to- $V_{BUS}$  event. The well designed combination of voltage clamps and 30-V tolerant OVP FETs insures the TPD6S300 can handle Short-to- $V_{BUS}$  hot-plug events with hot-plug voltages as high as 24- $V_{DC}$ .



## Feature Description (接下页)

The TPD6S300 has an extremely fast turnoff time of 70 ns typical. Furthermore, additional voltage clamps are placed after the OVP FET on the system side (CC1, CC2, SBU1, SBU2) pins of the TPD6S300, to further limit the voltage and current that are exposed to the USB Type-C CC/PD controller during the 70 ns interval while the OVP FET is turning off. The combination of connector side voltage clamps, OVP FETs with extremely fast turnoff time, and system side voltage clamps all work together to insure the level of stress seen on a CC1, CC2, SBU1, or SBU2 pin during a short-to- $V_{BUS}$  event is less than or equal to an HBM event. This is done by design, as any USB Type-C CC/PD controller will have built in HBM ESD protection.

图 29 is an example of the TPD6S300 successfully protecting the TPS65982, the world's first fully integrated, full-featured USB Type-C and PD controller.

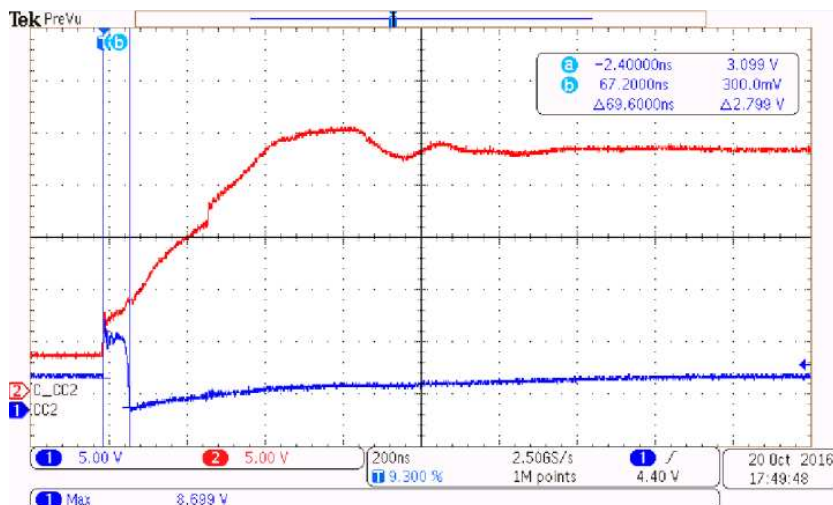


图 29. TPD6S300 Protecting the TPS65982 During a Short-to- $V_{BUS}$  Event

### 8.3.2 8-Channels of IEC 61000-4-2 ESD Protection (CC1, CC2, SBU1, SBU2, DP\_T, DM\_T, DP\_B, DM\_B Pins)

The TPD6S300 integrates 8-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, SBU2, DP\_T (Top side D+), DM\_T (Top Side D-), DP\_B (Bottom Side D+), and DM\_B (Bottom Side D-) pins. USB Type-C ports on end-products need system level IEC ESD protection in order to provide adequate protection for the ESD events that the connector can be exposed to from end users. The TPD6S300 integrates IEC ESD protection for all of the low-speed pins on the USB Type-C connector in a single chip. Also note, that while the RPD\_Gx pins are not individually rated for IEC ESD, when they are shorted to the C\_CCx pins, the C\_CCx pins provide protection for both the C\_CCx pins and the RPD\_Gx pins. Additionally, high-voltage IEC ESD protection that is 24-V DC tolerant is required for the CC and SBU lines in order to simultaneously support IEC ESD and Short-to- $V_{BUS}$  protection; there are not many discrete market solutions that can provide this kind of protection. The TPD6S300 integrates this type of high-voltage ESD protection so a system designer can meet both IEC ESD and Short-to- $V_{BUS}$  protection requirements in a single device.

### 8.3.3 CC1, CC2 Overvoltage Protection FETs 600 mA Capable for Passing VCONN Power

The CC pins on the USB Type-C connector serve many functions; one of the functions is to be a provider of power to active cables. Active cables are required when desiring to pass greater than 3 A of current on the  $V_{BUS}$  line or when the USB Type-C port uses the super-speed lines (TX1+, TX2-, RX1+, RX1-, TX2+, TX2-, RX2+, RX2-). When CC is configured to provide power, it is called VCONN. VCONN is a DC voltage source in the range of 3 V-5.5 V. If supporting VCONN, a VCONN provider must be able to provide 1 W of power to a cable; this translates into a current range of 200 mA to 333 mA (depending on your VCONN voltage level). Additionally, if operating in a USB PD alternate mode, greater power levels are allowed on the VCONN line.

## Feature Description (接下页)

When a USB Type-C port is configured for VCONN and using the TPD6S300, this VCONN current flows through the OVP FETs of the TPD6S300. Therefore, the TPD6S300 has been designed to handle these currents and have an RON low enough to provide a specification compliant VCONN voltage to the active cable. The TPD6S300 is designed to handle up to 600 mA of DC current to allow for alternate mode support in addition to the standard 1 W required by the USB Type-C specification.

### 8.3.4 CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices

An important feature of USB Type-C and USB PD is the ability for this connector to serve as the sole power source to mobile devices. With support up to 100 W, the USB Type-C connector supporting USB PD can be used to power a whole new range of mobile devices not previously possible with legacy USB connectors.

When the USB Type-C connector is the sole power supply for a battery powered device, the device must be able to charge from the USB Type-C connector even when its battery is dead. In order for a USB Type-C power adaptor to supply power on  $V_{BUS}$ , RD pull-down resistors must be exposed on the CC pins. These RD resistors are typically included inside a USB Type-C CC/PD controller. However, when the TPD6S300 is used to protect the USB Type-C port, the OVP FETs inside the device isolate these RD resistors in the CC/PD controller when the mobile device has no power. This is because when the TPD6S300 has no power, the OVP FETs are turned off to guarantee overvoltage protection in a dead battery condition. Therefore, the TPD6S300 integrates high-voltage, dead battery RD pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection.

If dead battery support is required, short the RPD\_G1 pin to the C\_CC1 pin, and short the RPD\_G2 pin to the C\_CC2 pin. This connects the dead battery resistors to the connector CC pins. When the TPD6S300 is unpowered, and the RP pull-up resistor is connected from a power adaptor, this RP pull-up resistor activates the RD resistor inside the TPD6S300. This enables  $V_{BUS}$  to be applied from the power adaptor even in a dead battery condition. Once power is restored back to the system and back to the TPD6S300 on its VPWR pin, the TPD6S300 removes its RD pull-down resistor and turn on its OVP FETs within 3.5 ms to guarantee the RD pull-down resistor inside the CC/PD Controller is exposed within 10 ms. This is by design, because if the RD pull-down resistor is not exposed within 10 ms, the power adaptor can legally interpret this behavior as a port disconnect and remove  $V_{BUS}$ .

If desiring to power the CC/PD controller during dead battery mode and if the CC/PD Controller is configured as a DRP, it is critical that the TPD6S300 be powered before or at the same time that the CC/PD controller is powered. It is also critical that when unpowered, the CC/PD controller also expose its dead battery resistors. When the TPD6S300 gets powered, it exposes the CC pins of the CC/PD controller within 3.5 ms. Once the TPD6S300 turns on, the RD pull-down resistors of the CC/PD controller must be present immediately, in order to guarantee the power adaptor connected to power the dead battery device keeps its  $V_{BUS}$  turned on. If the power adaptor sees any change to its CC voltage for more than 10 ms, it can disconnect  $V_{BUS}$ . This removes power from the device with its battery still not sufficiently charged, which consequently removes power from the CC/PD controller and the TPD6S300. Then the RD resistors of the TPD6S300 are exposed again, connect the power adaptor's  $V_{BUS}$  to start the cycle over. This creates an infinite loop, never or very slowly charging the mobile device.

If the CC/PD Controller is configured for DRP and has started its DRP toggle before the TPD6S300 turns on, this DRP toggle is unable to guarantee that the power adaptor does not disconnect from the port. Therefore, it is recommended if the CC/PD controller is configured for DRP, that its dead battery resistors be exposed as well, and that they remain exposed until the TPD6S300 turns on. This is typically accomplished by powering the TPD6S300 at the same time as the CC/PD controller when powering the CC/PD controller in dead battery operation.

If dead battery charging is not required in your application, connect the RPD\_G1 and RPD\_G2 pins to ground.

### 8.3.5 3-mm × 3-mm WQFN Package

The TPD6S300 comes in a small, 3-mm × 3-mm WQFN package, greatly reducing the size of implementing a similar protection solution discretely. The WQFN package allows support for a wider range of PCB designs. Additionally, the pin-out of the TPD6S300 was designed to optimize routing with the TPS6598x family of USB Type-C/PD controllers.

## 8.4 Device Functional Modes

表 1 describes all of the functional modes for the TPD6S300. The "X" in the below table are "do not care" conditions, meaning any value can be present within the absolute maximum ratings of the datasheet and maintain that functional mode. Also note the D1, D2, D3, D4 pins are not listed, because these pins have IEC ESD protection diodes that are always present, regardless of whether the device is powered and regardless of the conditions on any of the other pins.

表 1. Device Mode Table

Device Mode Table		Inputs					Outputs		
MODE		VPWR	C_CCx	C_SBUx	RPD_Gx	T <sub>J</sub>	FLT	CC FETs	SBU FETs
Normal Operating Conditions	Unpowered, no dead battery support	<UVLO	X	X	Grounded	X	High-Z	OFF	OFF
	Unpowered, dead battery support	<UVLO	X	X	Shorted to C_CCx	X	High-Z	OFF	OFF
	Powered on	>UVLO	<OVP	<OVP	X, forced OFF	<TSD	High-Z	ON	ON
Fault Conditions	Thermal shutdown	>UVLO	X	X	X, forced OFF	>TSD	Low (Fault Asserted)	OFF	OFF
	CC over voltage condition	>UVLO	>OVP	X	X, forced OFF	<TSD	Low (Fault Asserted)	OFF	OFF
	SBU over voltage condition	>UVLO	X	>OVP	X, forced OFF	<TSD	Low (Fault Asserted)	OFF	OFF

## 9 Application and Implementation

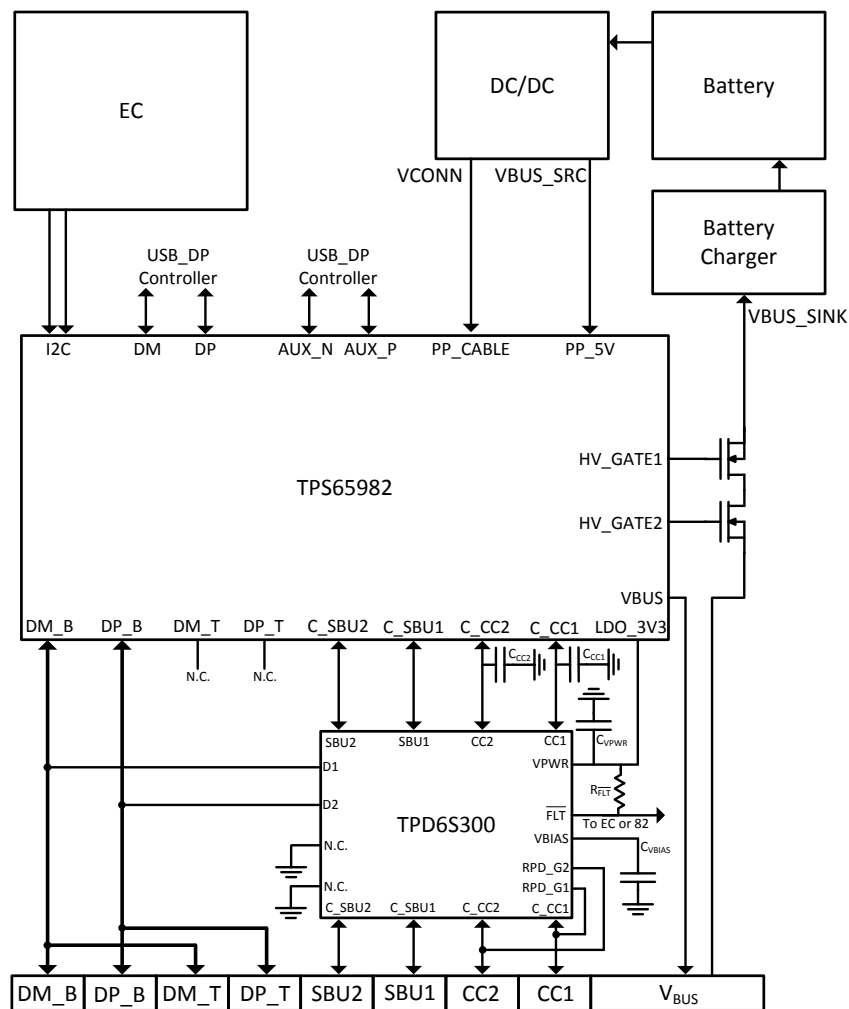
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPD6S300 provides 4-channels of Short-to-VBUS overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector, and 8-channels of IEC ESD protection for the CC1, CC2, SBU1, SBU2, DP\_T, DM\_T, DP\_B, DM\_B pins of the USB Type-C connector. Care must be taken to insure that the TPD6S300 provides adequate system protection as well as insuring that proper system operation is maintained. The following application example explains how to properly design the TPD6S300 into a USB Type-C system.

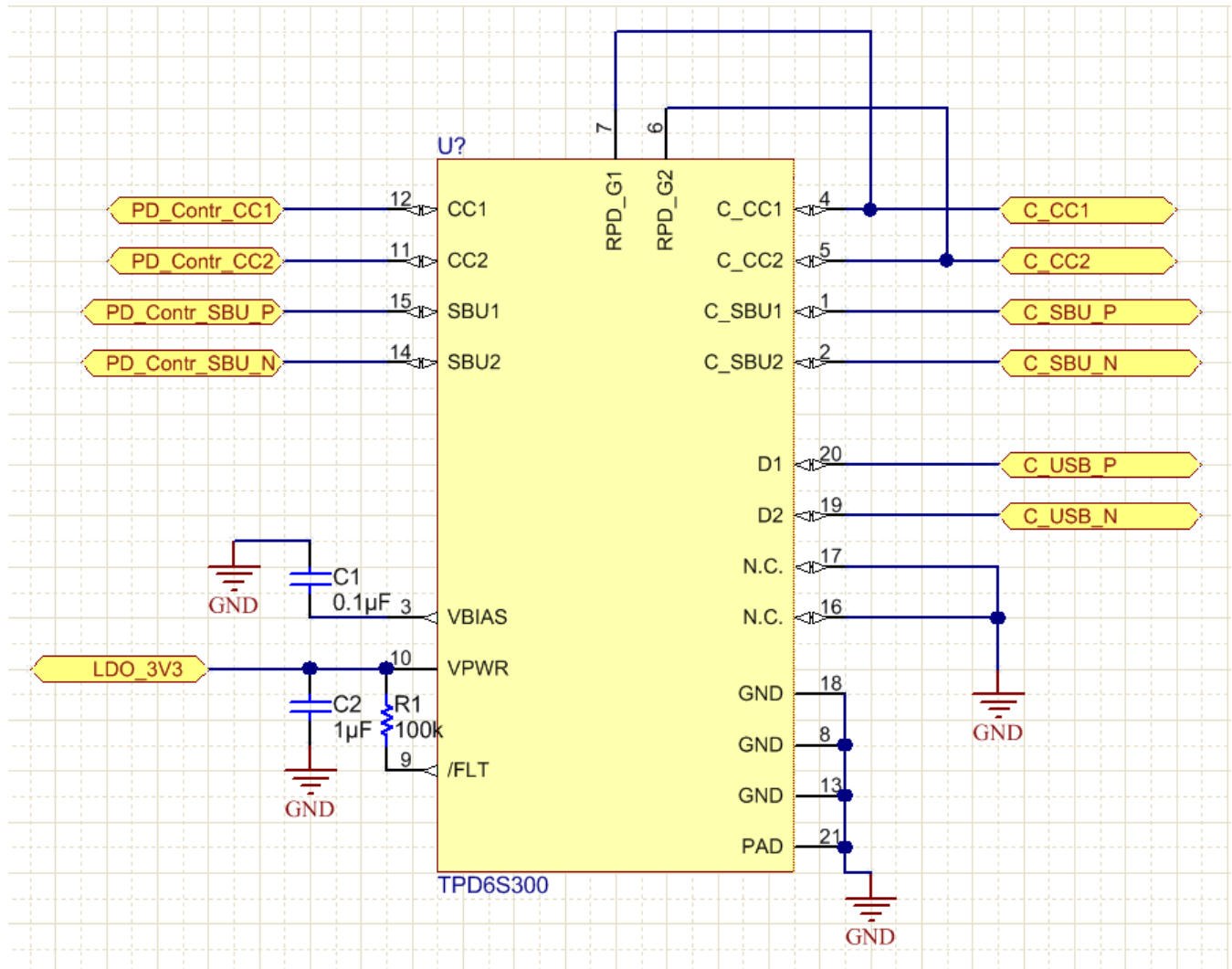
### 9.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

图 30. TPD6S300 Typical Application Diagram

Typical Application (接下页)



Copyright © 2016, Texas Instruments Incorporated

图 31. TPD6S300 Reference Schematic

9.2.1 Design Requirements

In this application example we study the protection requirements for a full-featured USB Type-C DRP Port, fully equipped with USB-PD, USB2.0, USB3.0, Display Port, and 100 W charging. The TPS65982 is used to easily enable a full-featured port with a single chip solution. In this application, all the pins of the USB Type-C connector are utilized. Both the CC and SBU pins are susceptible to shorting to the  $V_{BUS}$  pin. With 100 W charging,  $V_{BUS}$  operates at 20 V, requiring the CC and SBU pins to tolerate  $20 - V_{DC}$ . Additionally, the CC, SBU, and USB2.0 pins require IEC system level ESD protection. With these protection requirements present for the USB Type-C connector, the TPD6S300 is utilized. The TPD6S300 is a single chip solution that provides all the required protection for the low speed and USB2.0 pins in the USB Type-C connector.

表 2 lists the TPD6S300 design parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{BUS}$ nominal operating voltage	20 V
Short-to- $V_{BUS}$ tolerance for the CC and SBU pins	24 V

**表 2. Design Parameters (接下页)**

DESIGN PARAMETER	EXAMPLE VALUE
VBIAS nominal capacitance	0.1 $\mu$ F
Dead battery charging	100 W
Maximum ambient temperature requirement	85°C

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 VBIAS Capacitor Selection

As noted in the [Recommended Operating Conditions](#) table, a minimum of 35- $V_{BUS}$  rated capacitor is required for the VBIAS pin, and a 50- $V_{BUS}$  capacitor is recommended. The VBIAS capacitor is in parallel with the central IEC diode clamp integrated inside the TPD6S300. A forward biased hiding diode connects the VBIAS pin to the C\_CCx and C\_SBUx pins. Therefore, when a Short-to- $V_{BUS}$  event occurs at 20 V, 20- $V_{BUS}$  minus a forward biased diode drop is exposed to the VBIAS pin. Additionally, during the short-to- $V_{BUS}$  event, ringing can occur almost double the settling voltage of 20 V, allowing a potential 40 V to be exposed to the C\_CCx and C\_SBUx pins. However, the internal IEC clamps limit the voltage exposed to the C\_CCx and C\_SBUx pins to around 30 V. Therefore, at least 35- $V_{BUS}$  capacitor is required to insure the VBIAS capacitor does not get destroyed during Short-to- $V_{BUS}$  events.

A 50-V, X7R capacitor is recommended, however. This is to further improve the derating performance of the capacitors. When the voltage across a real capacitor is increased, its capacitance value derates. The more the capacitor derates, the greater than 2x ringing can occur in the short-to- $V_{BUS}$  RLC circuit. 50-V X7R capacitors have great derating performance, allowing for the best short-to- $V_{BUS}$  performance of the TPD6S300.

Additionally, the VBIAS capacitor helps pass IEC 61000-4-2 ESD strikes. The more capacitance present, the better the IEC performance. So the less the VBIAS capacitor derates, the better the IEC performance. [表 3](#) shows real capacitors recommended to achieve the best performance with the TPD6S300.

**表 3. Design Parameters**

CAPACITOR SIZE	PART NUMBER
0402	CC0402KRX7R9BB104
0603	GRM188R71H104KA93D

### 9.2.2.2 Dead Battery Operation

For this application, we want to support 100-W dead battery operation; when the laptop is out of battery, we still want to charge the laptop at 20 V and 5 A. This means that the USB PD Controller must receive power in dead battery mode. The TPS65982 has its own built in LDO in order to supply the TPS65982 power from  $V_{BUS}$  in a dead battery condition. The TPS65982 can also provide power to its flash during this condition through its LDO\_3V3 pin.

The TPD6S300s OVP FETs remain OFF when it is unpowered in order to insure in a dead battery situation proper protection is still provided to the PD controller in the system, in this case the TPS65982. However, when the OVP FETs are OFF, this isolates the TPS65982s dead battery resistors from the USB Type-C ports CC pins. A USB Type-C power adaptor must see the RD pull-down dead battery resistors on the CC pins or it does not provide power on  $V_{BUS}$ . Since the TPS65982s dead battery resistors are isolated from the USB Type-C connector's CC pins, the TPD6S300s built in dead battery resistors must be connected. Short the RPD\_G1 pin to the C\_CC1 pin, and short the RPD\_G2 pin to the C\_CC2 pin.

Once the power adaptor sees the TPD6S300s dead battery resistors, it applies 5 V on the  $V_{BUS}$  pin. This provides power to the TPS65982, turning the PD controller on, and allowing the battery to begin to charge. However, this application requires 100 W charging in dead battery mode, so  $V_{BUS}$  at 20 V and 5 A is required. USB PD negotiation is required to accomplish this, so the TPS65982 needs to be able to communicate on the CC pins. This means the TPD6S3000 needs to be turned on in dead battery mode as well so the TPS65982s PD controller can be exposed to the CC lines. To accomplish this, it is critical that the TPD6S300 is powered by the TPS65982s internal LDO, the LDO\_3V3 pin. This way, when the TPS65982 receives power on  $V_{BUS}$ , the TPD6S300 is turned on simultaneously.

It is critical that the TPS65982s dead battery resistors are also connected to its CC pins for dead battery operation. Short the TPS65982s RPD\_G1 pin to its C\_CC1 pin, and its RPD\_G2 pin to its C\_CC2 pin. It is critical that the TPS65982s dead battery resistors are present; once the TPD6S300 receives power, removes its dead battery resistors and turns on its OVP FETs, RD pull-down resistors must be present on the CC line in order to guarantee the power adaptor stays connected. If RD is not present and the voltage on CC changes for more than 10 ms, the power adaptor interprets this as a disconnect and remove  $V_{BUS}$ .

Also, it is important that the TPS65982s dead battery resistors are present so it properly boots up in dead battery operation with the correct voltages on its CC pins.

Once this process has occurred, the TPS65982 can start negotiating with the power adaptor through USB PD for higher power levels, allowing 100-W operation in dead battery mode.

For more information on the TPD6S300 dead battery operation, see the [CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices](#) section of the datasheet. Also, see [图 32](#) for a waveform of the CC line when the TPD6S300 is turning on and exposing the TPS65982s dead battery resistors to the USB Type-C connector.

### 9.2.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the [USB PD Specification](#) is given below in [表 4](#).

**表 4. USB PD cReceiver Specification**

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TPS65982, the TPD6S300, and any external capacitor must fall within these limits. [表 5](#) shows the analysis involved in choosing the correct external CC capacitor for this system, and shows that an external CC capacitor is required.

**表 5. CC Line Capacitor Calculation**

CC Capacitance	MIN	MAX	UNIT	COMMENT
CC line target capacitance	200	600	pF	From the <a href="#">USB PD Specification</a> section
TPS65982 capacitance	70	120	pF	From the <a href="#">TPS65982 Datasheet</a>
TPD6S300 capacitance	60	120	pF	From the table.
Proposed capacitor GRM033R71E221KA01D	110	330	pF	CAP, CERM, 220 pF, 25 V, ±10%, X7R, 0201 (For min and max, assume ±50% capacitance change with temperature and voltage derating to be overly conservative)
TPS65982 + TPD6S300 + GRM033R71E221KA01D	240	570	pF	Meets USB PD cReceiver specification

### 9.2.2.4 Additional ESD Protection on CC and SBU Lines

If additional IEC ESD protection is desired to be placed on either the CC or SBU lines, it is important that high-voltage ESD protection diodes be used. The maximum DC voltage that can be seen in USB PD is  $21-V_{BUS}$ , with 21.5 V allowed during voltage transitions. Therefore, an ESD protection diode must have a reverse stand off voltage higher than 21.5 V in order to guarantee the diode does not breakdown during a short-to- $V_{BUS}$  event and have large amounts of current flowing through it indefinitely, destroying the diode. A reverse stand off voltage of 24 V is recommended to give margin above 21.5 V in case USB Type-C power adaptors are released in the market which break the USB Type-C specification.

Furthermore, due to the fact that the Short-to- $V_{BUS}$  event applies a DC voltage to the CC and SBU pins, a deep-snap back diode cannot be used unless its minimum trigger voltage is above 42 V. During a Short-to- $V_{BUS}$  event, RLC ringing of up to 2x the settling voltage can be exposed to CC and SBU, allowing for up to 42 V to be exposed. Furthermore, if any capacitor derates on the CC or SBU line, greater than 2x ringing can occur. Since this ringing is hard to bound, it is recommended to not use deep-snap back diodes. If the diode triggers during the short-to- $V_{BUS}$  hot-plug event, it begins to operate in its conduction region. With a 20- $V_{BUS}$  source present on the CC or SBU line, this allows the diode to conduct indefinitely, destroying the diode.

### 9.2.2.5 $\overline{FLT}$ Pin Operation

The  $\overline{FLT}$  and OVP FET have specific timing parameters to allow different benefits depending on how the system designer desires the system to respond to a Short-to- $V_{BUS}$  event.

Once a Short-to- $V_{BUS}$  occurs on the  $C_{CCx}$  or  $C_{SBUx}$  pins, the  $\overline{FLT}$  pin is asserted in 20  $\mu s$  (typical) so the PD controller can be notified quickly. If  $V_{BUS}$  is being shorted to CC or SBU, it is recommended to respond to the event by forcing a detach in the USB PD controller to remove  $V_{BUS}$  from the port. Although the USB Type-C port using the TPD6S300 is not damaged, as the TPD6S300 provides protection from these events, the other device connected through the USB Type-C Cable or any active circuitry in the cable can be damaged. Although shutting the  $V_{BUS}$  off through a detach does not guarantee it stops the other device or cable from being damaged, it can mitigate any high current paths from causing further damage after the initial damage takes place. Additionally, even if the active cable or other device does have proper protection, the short-to- $V_{BUS}$  event may corrupt a configuration in an active cable or in the other PD controller, so it is best to detach and reconfigure the port.

For UFP's, the TPD6S300 automatically forces a detach, removing the need to use the  $\overline{FLT}$  pin if the only response required by your system during a short-to- $V_{BUS}$  event is forcing a detach on the port. The TPD6S300 keeps its CC OVP FET OFF for at least 21 ms after a Short-to- $V_{BUS}$  event occurs, causing the CC line voltage to change from its configuration value for more than 20 ms, forcing the PD controllers to detach. For DFPs, this operation cannot be guaranteed because of the parasitic diode in the OVP FET from  $CCx$  to  $C_{CCx}$  and from  $SBUx$  to  $C_{SBUx}$ . Therefore for DFPs, using the  $\overline{FLT}$  pin is recommended. For our application using the TPS65982 as a DRP, using the  $\overline{FLT}$  pin is recommended.

### 9.2.2.6 How to Connect Unused Pins

If either the RPD\_Gx pins or any of the Dx pins are unused in a design, they must be connected to GND.

## 9.2.3 Application Curves

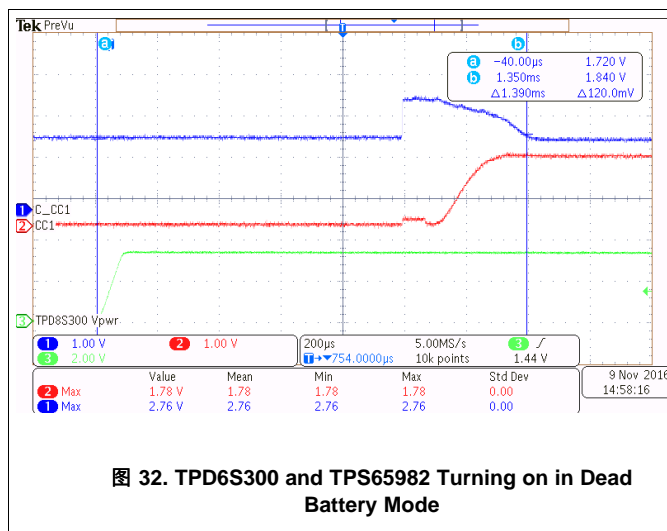


图 32. TPD6S300 and TPS65982 Turning on in Dead Battery Mode

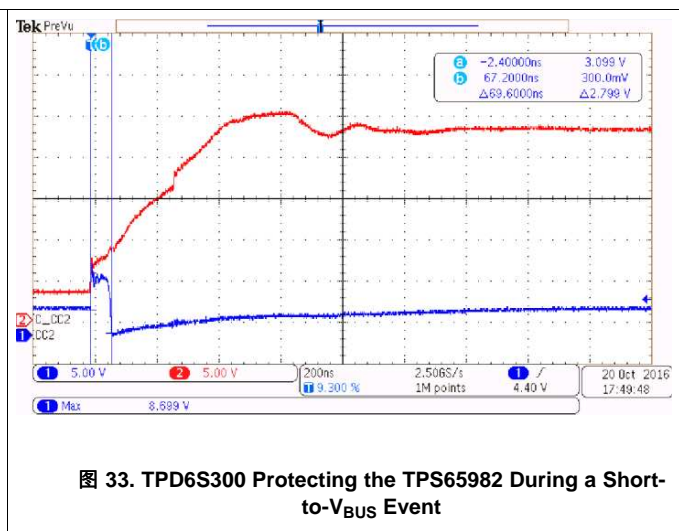


图 33. TPD6S300 Protecting the TPS65982 During a Short-to- $V_{BUS}$  Event



## 10 Power Supply Recommendations

The VPWR pin provides power to all the circuitry in the TPD6S300. It is recommended a 1- $\mu$ F decoupling capacitor is placed as close as possible to the VPWR pin. If USB PD is desired to be operated in dead battery conditions, it is critical that the TPD6S300 share the same power supply as the PD controller in dead battery boot-up (such as sharing the same dead battery LDO). See the [CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices](#) section for more details.

## 11 Layout

### 11.1 Layout Guidelines

Proper routing and placement is important to maintain the signal integrity the USB2.0, SBU, CC line signals. The following guidelines apply to the TPD6S300:

- Place the bypass capacitors as close as possible to the  $V_{PWR}$  pin, and ESD protection capacitor as close as possible to the  $V_{BIAS}$  pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to- $V_{BUS}$  and ESD strikes.
- The USB2.0 and SBU lines must be routed as straight as possible and any sharp bends must be minimized.

Standard ESD recommendations apply to the C\_CC1, C\_CC2, C\_SBU1, C\_SBU2, D1, D2, D3, and D4 pins as well:

- The optimum placement for the device is as close to the connector as possible:
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TPD6S300 and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- It is best practice to not via up to the D1, D2, D3, and D4 pins from a trace routed on another layer. Rather, it is better to via the trace to the layer with the Dx pin, and to continue that trace on that same layer. See the [ESD Protection Layout Guide](#) application report, section 1.3 for more details.

### 11.2 Layout Example

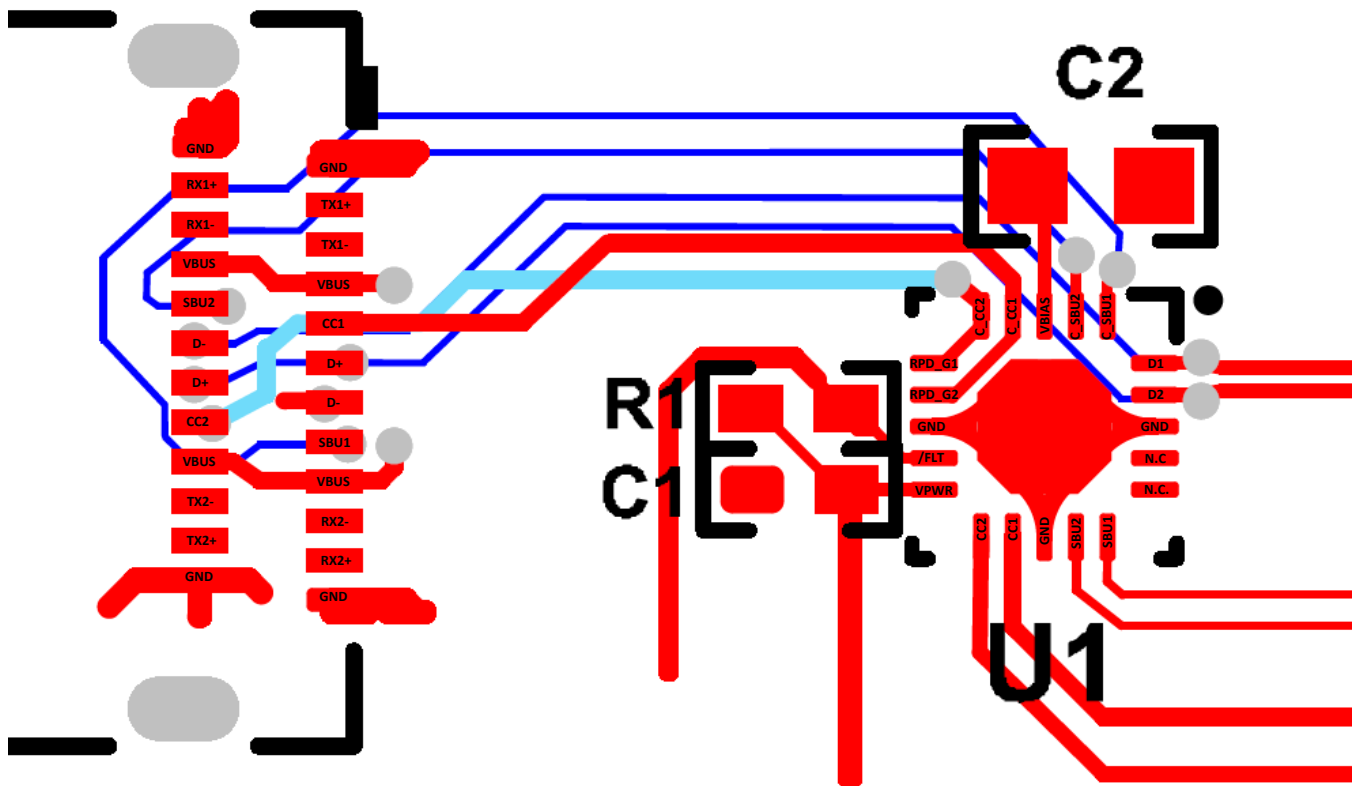


图 34. TPD6S300 Typical Layout

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档:

《TPD6S300 评估模块用户指南》

### 12.2 接收文档更新通知

如需接收文档更新通知, 请访问 [ti.com](http://ti.com) 上的器件产品文件夹。请单击右上角的通知我 进行注册, 即可收到任意产品信息更改每周摘要。有关更改的详细信息, 请查看任意已修订文档中包含的修订历史记录。

### 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

E2E is a trademark of Texas Instruments.

USB Type-C is a trademark of USB Implementers Forum.

All other trademarks are the property of their respective owners.

### 12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

## 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时, 我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本, 请参见左侧的导航栏。

### 13.1

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD6S300RUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6S30	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

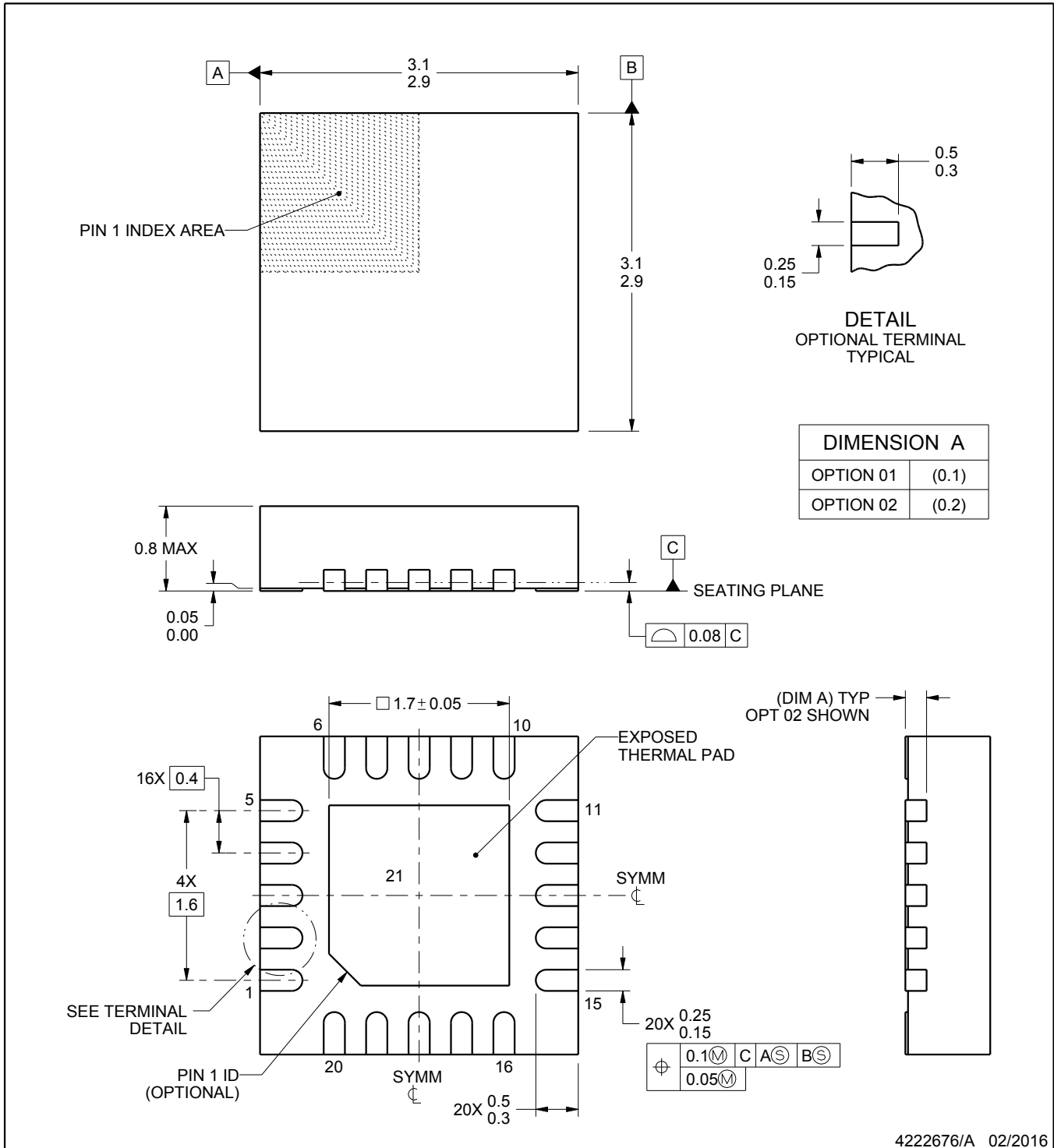
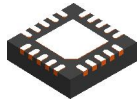

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6S300RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6S300RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0



4222676/A 02/2016

NOTES:

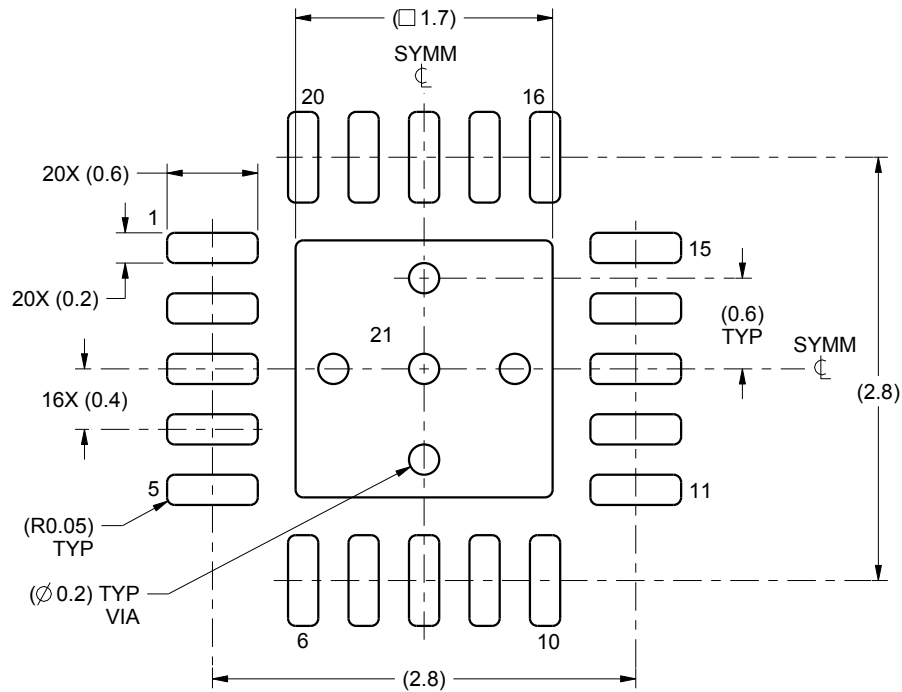
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

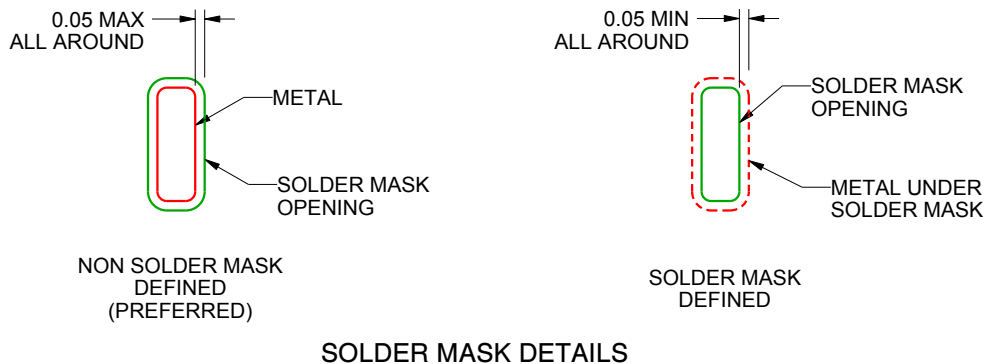
RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



4222676/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

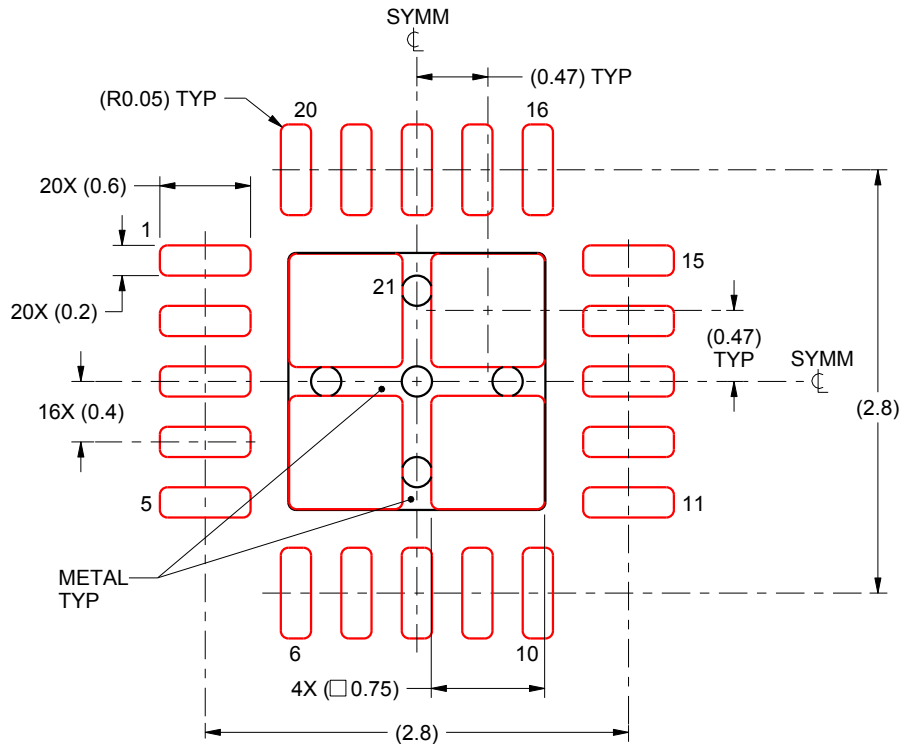


# EXAMPLE STENCIL DESIGN

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司