TXS0104E-Q1 适用于漏极开路和推挽应用的 4 位 双向电压电平转换器 转换器

1 特性

- 汽车电子 应用认证末尾新增了一段内容
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C6
- 无需方向控制信号
- 最大数据速率
  - 最大值 24Mbps（推挽）
  - 2Mbps（开漏）
- A 端口上 1.65V 至 3.6V，B 端口上 2.3V 至 5.5V ($V_{CCA} \le V_{CCB}$)
- 无需电源序列 — V_{CCA} 或 V_{CCB} 均可优先斜升
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
  - A 端口
    - 2000V 人体放电模式 (A114-B)
    - 1000V 组件充电模式 (C101)
  - B 端口
    - 15kV 人体放电模式 (A114-B)
    - 1000V 组件充电模式 (C101)
- IEC 61000-4-2 ESD（B 端口）
  - ±8kV 接触放电
  - ±10kV 空气间隙放电

2 应用范围

- 汽车用信息娱乐系统，高级驾驶员辅助系统 (ADAS)
- 主处理器和外设模块间的隔离和电平转换
- I²C 或 1 线制电压电平转换

3 说明

由于电压不匹配，TXS0104E-Q1 器件连接芯片与芯片间的非兼容逻辑通信。这款自动导向转换器可方便地用来在无需主机方向控制的情况下缩小之间的差距。在无需主机干预的情况下，每个通道可混合使用，并且可以与不同的输出类型（开漏或推挽）和混合数据流（发送或接收）相匹配。这个 4 位非反向转换器使用两个独立的可配置电源轨。A 和 B 端口被设计用来分别跟踪 V_{CCA} 和 V_{CCB}。V_{CCB} 引脚在 V_{CCA} 引脚接受 1.65V 至 3.6V 之间的任一电源电压的同时，接受 2.3V 至 5.5V 之间的任何电源电压，这样的话，V_{CCA} 小于或等于 V_{CCB}。这个跟踪功能可实现 1.8V，2.5V，3.3V 和 5V 电压节点之间的低电压双向转换。

当输出使能端 (OE) 输入为低电平时，所有输出都被置于高阻抗状态。

TXS0104E-Q1 器件被设计成 OE 输入电路由 V_{CCA} 供电。

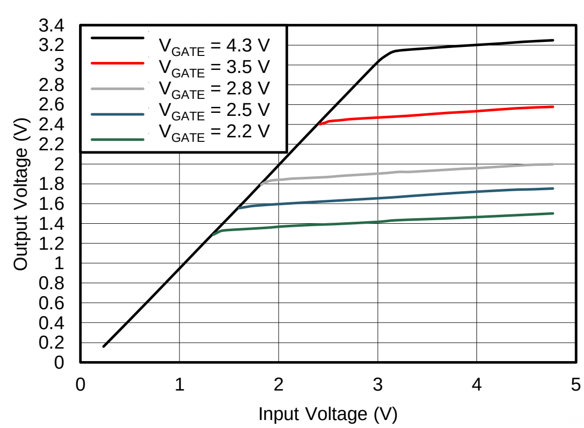
为了确保加电或断电期间的高阻抗状态，OE 引脚应该通过一个下拉电阻器接在 GND 引脚上；此电阻器的最小值由驱动器的电流供源能力决定。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TXS0104E-Q1	薄型小外形尺寸封装 (TSSOP) (14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

N 通道晶体管的传输特征



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (May 2014) to Revision C — **Page**

- Changed the type of the OE pin from output (O) to input (I) in the *Pin Functions* table ... 3
- Moved T_{stg} back to the *Absolute Maximum Ratings* table and changed the *Handling Ratings* table to *ESD Ratings* ... 4
- 已添加 *文档支持，接收文档更新通知以及社区资源部分* ... 20

Changes from Revision A (April 2014) to Revision B — **Page**

- 已更改 器件状态“*产品预览*”至“*量产数据*” ... 1

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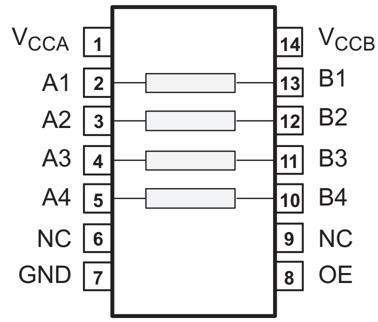
5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



NC - No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	2	I/O	Input-output 1 for the A port. This pin is referenced to V_{CCA}.
A2	3	I/O	Input-output 2 for the A port. This pin is referenced to V_{CCA}.
A3	4	I/O	Input-output 3 for the A port. This pin is referenced to V_{CCA}.
A4	5	I/O	Input-output 4 for the A port. This pin is referenced to V_{CCA}.
B1	13	I/O	Input-output 1 for the B port. This pin is referenced to V_{CCB}.
B2	12	I/O	Input-output 2 for the B port. This pin is referenced to V_{CCB}.
B3	11	I/O	Input-output 3 for the B port. This pin is referenced to V_{CCB}.
B4	10	I/O	Input-output 4 for the B port. This pin is referenced to V_{CCB}.
GND	7	—	Ground
NC	6	—	No connection
	9		
OE	8	I	Tri-state output-mode enable. Pull the OE pin low to place all outputs in tri-state mode. This pin is referenced to V_{CCA}.
V_{CCA}	1	I	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	14	I	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage	V_{CCA}		–0.5	4.6	V
	V_{CCB}		–0.5	6.5	
Input-output pin voltage, V_{IO} (2)	A1, A2, A3, A4	A port	–0.5	4.6	V
	B1, B2, B3, B4	B port	–0.5	6.5	
Output voltage, V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
Input clamp current, I_{IK}		$V_I < 0$		–50	mA
Output clamp current, I_{OK}		$V_O < 0$		–50	mA
Continuous output current, I_O				±50	mA
Continuous current through each V_{CCA}, V_{CCB}, or GND				±100	mA
Storage temperature range, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage(1)				1.65	3.6	V
V_{CCB}	Supply voltage(1)				2.3	5.5	
$V_{IH(Ax)}$	High-level input voltage	A-port I/Os	1.65 to 1.95 V	2.3 to 5.5 V	V_{CCA} – 0.2	V_{CCA}	V
			2.3 to 3.6 V		V_{CCA} – 0.4	V_{CCA}	
$V_{IH(Bx)}$	High-level input voltage	B-port I/Os	1.65 to 3.6 V	2.3 to 5.5 V	V_{CCB} – 0.4	V_{CCB}	
$V_{IH(OE)}$	High-level input voltage	OE input			V_{CCA} × 0.65	5.5	
$V_{IL(Ax)}$	Low-level input voltage	A-port I/Os	1.65 to 3.6 V	2.3 to 5.5 V	0	0.15	V
$V_{IL(Bx)}$	Low-level input voltage	B-port I/Os			0	0.15	
$V_{IL(OE)}$	Low-level input voltage	OE input			0	V_{CCA} × 0.35	
$\Delta t/\Delta v_{(Ax)}$	Input transition rise or fall rate	A-port I/Os, push-pull driving	1.65 to 3.6 V	2.3 to 5.5 V		10	ns/V
$\Delta t/\Delta v_{(Bx)}$	Input transition rise or fall rate	B-port I/Os, push-pull driving				10	
$\Delta t/\Delta v_{(OE)}$	Input transition rise or fall rate	OE input				10	
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

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6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC (1)		TXS0104E-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
$V_{OH(Ax)}$	High-level output voltage, A port	I_{OH} = –20 µA, $V_{I(Bx)} \geq V_{CCB} - 0.4$ V	1.65 to 3.6 V	2.3 to 5.5 V	$V_{CCA} \times 0.75$			V
$V_{OL(Ax)}$	Low-level output voltage, A port	I_{OL} = 1 mA, $V_{I(Bx)} \leq 0.15$ V	1.65 to 3.6 V	2.3 to 5.5 V			0.4	V
$V_{OH(Bx)}$	High-level output voltage, B port	I_{OH} = –20 µA, $V_{I(Ax)} \geq V_{CCA} - 0.2$ V	1.65 to 3.6 V	2.3 to 5.5 V	$V_{CCB} \times 0.75$			V
$V_{OL(Bx)}$	Low-level output voltage, B port	I_{OL} = 1 mA, $V_{I(Ax)} \leq 0.15$ V	1.65 to 3.6 V	2.3 to 5.5 V			0.4	V
$I_{I(OE)}$	Input current, OE	$V_I = V_{CCI}$ or GND	1.65 to 3.6 V	2.3 to 5.5 V			±2	µA
		$V_I = V_{CCI}$ or GND, T_A = 25°C					±1	
I_{OZ}	Off-state output current, A or B port	OE = V_{IL}	1.65 to 3.6 V	2.3 to 5.5 V			±3	µA
		OE = V_{IL}, T_A = 25°C					±1	
I_{CCA}	Supply current, A port	$V_I = V_O$ = Open, I_O = 0	1.65 to V_{CCB}	2.3 to 5.5 V			4	µA
			3.6 V	0			2.2	
			0	5.5 V			–1	
I_{CCB}	Supply current, B port	$V_I = V_O$ = Open, I_O = 0	1.65 to V_{CCB}	2.3 to 5.5 V			21	µA
			3.6 V	0			–1	
			0	5.5 V			5	
$I_{CCA}+I_{CCB}$	Supply current, A port plus B port supply current	$V_I = V_O$ = Open, I_O = 0	1.65 V to V_{CCB}	2.3 to 5.5 V			25	µA
$C_{I(OE)}$	Input capacitance, OE		3.3 V	3.3 V			4	pF
		T_A = 25°C				2.5		
$C_{IO(Ax)}$	Input-output capacitance, A port		3.3 V	3.3 V			6.5	pF
		T_A = 25°C				5		
$C_{IO(Bx)}$	Input-output capacitance, B port						16.5	
		T_A = 25°C				12		

(1) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

6.6 Timing Requirements—V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	Data rate	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		18	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		21	
			V_{CCB} = 5 V ± 0.5 V		23	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		2	
			V_{CCB} = 3.3 V ± 0.3 V		2	
			V_{CCB} = 5 V ± 0.5 V		2	
t_w	Pulse duration, data inputs See Figure 7	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	55		ns
			V_{CCB} = 3.3 V ± 0.3 V	47		
			V_{CCB} = 5 V ± 0.5 V	43		
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	500		
			V_{CCB} = 3.3 V ± 0.3 V	500		
			V_{CCB} = 5 V ± 0.5 V	500		

6.7 Timing Requirements—V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	Data rate	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		20	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		22	
			V_{CCB} = 5 V ± 0.5 V		24	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		2	
			V_{CCB} = 3.3 V ± 0.3 V		2	
			V_{CCB} = 5 V ± 0.5 V		2	
t_w	Pulse duration, data inputs See Figure 7	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	50		ns
			V_{CCB} = 3.3 V ± 0.3 V	45		
			V_{CCB} = 5 V ± 0.5 V	41		
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	500		
			V_{CCB} = 3.3 V ± 0.3 V	500		
			V_{CCB} = 5 V ± 0.5 V	500		

6.8 Timing Requirements—V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	Data rate	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		22	Mbps
			V_{CCB} = 5 V ± 0.5 V		24	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		2	
			V_{CCB} = 5 V ± 0.5 V		2	
t_w	Pulse duration, Data inputs See Figure 7	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	45		ns
			V_{CCB} = 5 V ± 0.5 V	41		
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	500		
			V_{CCB} = 5 V ± 0.5 V	500		

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6.9 Switching Characteristics—V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{PHL(A-B)}$	Propagation delay time (high to low), from **A** (input) to **B** (output) See Figure 8	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		6	ns
			V_{CCB} = 3.3 V ± 0.3 V		5.8	
			V_{CCB} = 5 V ± 0.5 V		5.8	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		8.8	
			V_{CCB} = 3.3 V ± 0.3 V		9.6	
			V_{CCB} = 5 V ± 0.5 V		10	
$t_{PHL(B-A)}$	Propagation delay time (high to low), from **B** (input) to **A** (output) See Figure 8	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		4.4	
			V_{CCB} = 3.3 V ± 0.3 V		4.5	
			V_{CCB} = 5 V ± 0.5 V		4.7	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		5.3	
			V_{CCB} = 3.3 V ± 0.3 V		4.4	
			V_{CCB} = 5 V ± 0.5 V		4	
$t_{PLH(A-B)}$	Propagation delay time (low to high), from **A** (input) to **B** (output) See Figure 8	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		7.7	ns
			V_{CCB} = 3.3 V ± 0.3 V		6.8	
			V_{CCB} = 5 V ± 0.5 V		7	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		50	
			V_{CCB} = 3.3 V ± 0.3 V		26	
			V_{CCB} = 5 V ± 0.5 V		33	
$t_{PLH(B-A)}$	Propagation delay time (low to high), from **B** (input) to **A** (output) See Figure 8	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		5.3	
			V_{CCB} = 3.3 V ± 0.3 V		4.5	
			V_{CCB} = 5 V ± 0.5 V		0.5	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		36	
			V_{CCB} = 3.3 V ± 0.3 V		16	
			V_{CCB} = 5 V ± 0.5 V		20	
$t_{en(OE-A)}$ $t_{en(OE-B)}$	Enable time, from **OE** (input) to **A** or **B** (output)	V_{CCB} = 2.5 V ± 0.2 V			200	ns
		V_{CCB} = 3.3 V ± 0.3 V			200	
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{dis(OE-A)}$ $t_{dis(OE-B)}$	Disable time, from **OE** (input) to **A** or **B** (output)	V_{CCB} = 2.5 V ± 0.2 V			200	ns
		V_{CCB} = 3.3 V ± 0.3 V			200	
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{r(Ax)}$	Rise time, A port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		9.5	ns
			V_{CCB} = 3.3 V ± 0.3 V		9.3	
			V_{CCB} = 5 V ± 0.5 V		15	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	38	199	
			V_{CCB} = 3.3 V ± 0.3 V	30	150	
			V_{CCB} = 5 V ± 0.5 V	22	109	
$t_{r(Bx)}$	Rise time, B port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		10.8	ns
			V_{CCB} = 3.3 V ± 0.3 V		9.1	
			V_{CCB} = 5 V ± 0.5 V		7.6	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	34	186	
			V_{CCB} = 3.3 V ± 0.3 V	23	112	
			V_{CCB} = 5 V ± 0.5 V	10	58	

Switching Characteristics—V_{CCA} = 1.8 V ± 0.15 V (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{f(Ax)}$	Fall time, A port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		5.9	ns
			V_{CCB} = 3.3 V ± 0.3 V		6	
			V_{CCB} = 5 V ± 0.5 V		13.3	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		6.9	
			V_{CCB} = 3.3 V ± 0.3 V		6.4	
			V_{CCB} = 5 V ± 0.5 V		6.1	
$t_{f(Bx)}$	Fall time, B port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		7.6	
			V_{CCB} = 3.3 V ± 0.3 V		7.5	
			V_{CCB} = 5 V ± 0.5 V		8.8	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		13.8	
			V_{CCB} = 3.3 V ± 0.3 V		16.2	
			V_{CCB} = 5 V ± 0.5 V		16.2	
t_{sk}	Channel-to-channel skew	V_{CCB} = 2.5 V ± 0.2 V			1	ns
		V_{CCB} = 3.3 V ± 0.3 V			1	
		V_{CCB} = 5 V ± 0.5 V			1	
	Maximum data rate	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		18	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		21	
			V_{CCB} = 5 V ± 0.5 V		23	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		2	
			V_{CCB} = 3.3 V ± 0.3 V		2	
			V_{CCB} = 5 V ± 0.5 V		2	

6.10 Switching Characteristics—V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{PHL(A-B)}$	Propagation delay time (high to low), from **A** (input) to **B** (output) See Figure 8	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3.2	ns
			V_{CCB} = 3.3 V ± 0.3 V		3.3	
			V_{CCB} = 5 V ± 0.5 V		3.4	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		6.3	
			V_{CCB} = 3.3 V ± 0.3 V		6	
			V_{CCB} = 5 V ± 0.5 V		5.8	
$t_{PHL(B-A)}$	Propagation delay time (high to low), from **B** (input) to **A** (output) See Figure 8	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3	
			V_{CCB} = 3.3 V ± 0.3 V		3.6	
			V_{CCB} = 5 V ± 0.5 V		4.3	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		4.7	
			V_{CCB} = 3.3 V ± 0.3 V		4.2	
			V_{CCB} = 5 V ± 0.5 V		4	
$t_{PLH(A-B)}$	Propagation delay time (low to high), from **A** (input) to **B** (output) See Figure 8	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3.5	ns
			V_{CCB} = 3.3 V ± 0.3 V		4.1	
			V_{CCB} = 5 V ± 0.5 V		4.4	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		3.5	
			V_{CCB} = 3.3 V ± 0.3 V		4.1	
			V_{CCB} = 5 V ± 0.5 V		4.4	
$t_{PLH(B-A)}$	Propagation delay time (low to high), from **B** (input) to **A** (output) See Figure 8	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		2.5	
			V_{CCB} = 3.3 V ± 0.3 V		1.6	
			V_{CCB} = 5 V ± 0.5 V		0.7	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		2.5	
			V_{CCB} = 3.3 V ± 0.3 V		1.6	
			V_{CCB} = 5 V ± 0.5 V		1	

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Switching Characteristics—V_{CCA} = 2.5 V ± 0.2 V (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{en(OE-A)}$ $t_{en(OE-B)}$	Enable time, from **OE** (input) to **A** or **B** (output)	V_{CCB} = 2.5 V ± 0.2 V			200	ns
		V_{CCB} = 3.3 V ± 0.3 V			200	
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{dis(OE-A)}$ $t_{dis(OE-B)}$	Disable time, from **OE** (input) to **A** or **B** (output)	V_{CCB} = 2.5 V ± 0.2 V			200	ns
		V_{CCB} = 3.3 V ± 0.3 V			200	
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{r(Ax)}$	Rise time, A port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		7.4	ns
			V_{CCB} = 3.3 V ± 0.3 V		6.6	
			V_{CCB} = 5 V ± 0.5 V		5.6	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	34	180	
			V_{CCB} = 3.3 V ± 0.3 V	28	150	
			V_{CCB} = 5 V ± 0.5 V	24	105	
$t_{r(Bx)}$	Rise time, B port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		8.3	ns
			V_{CCB} = 3.3 V ± 0.3 V		7.2	
			V_{CCB} = 5 V ± 0.5 V		6.1	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	35	170	
			V_{CCB} = 3.3 V ± 0.3 V	24	120	
			V_{CCB} = 5 V ± 0.5 V	12	64	
$t_{f(Ax)}$	Fall time, A port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		5.7	ns
			V_{CCB} = 3.3 V ± 0.3 V		5.5	
			V_{CCB} = 5 V ± 0.5 V		5.3	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V			
			V_{CCB} = 3.3 V ± 0.3 V			
			V_{CCB} = 5 V ± 0.5 V		5.8	
$t_{f(Bx)}$	Fall time, B port	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		7.8	ns
			V_{CCB} = 3.3 V ± 0.3 V		6.7	
			V_{CCB} = 5 V ± 0.5 V		6.6	
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V		8.8	
			V_{CCB} = 3.3 V ± 0.3 V		9.4	
			V_{CCB} = 5 V ± 0.5 V		10.4	
t_{sk}	Channel-to-channel skew	V_{CCB} = 2.5 V ± 0.2 V			1	ns
		V_{CCB} = 3.3 V ± 0.3 V			1	
		V_{CCB} = 5 V ± 0.5 V			1	
	Maximum data rate	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	20		Mbps
			V_{CCB} = 3.3 V ± 0.3 V	22		
			V_{CCB} = 5 V ± 0.5 V	24		
		Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	2		
			V_{CCB} = 3.3 V ± 0.3 V	2		
			V_{CCB} = 5 V ± 0.5 V	2		

6.11 Switching Characteristics—V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{PHL(A-B)}$	Propagation delay time (high to low), from **A** (input) to **B** (output) See Figure 8	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.4	ns
			V_{CCB} = 5 V ± 0.5 V		3.1	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		4.2	
			V_{CCB} = 5 V ± 0.5 V		4.6	
$t_{PHL(B-A)}$	Propagation delay time (high to low), from **B** (input) to **A** (output) See Figure 8	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.5	
			V_{CCB} = 5 V ± 0.5 V		3.3	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		124	
			V_{CCB} = 5 V ± 0.5 V		97	
$t_{PLH(A-B)}$	Propagation delay time (low to high), from **A** (input) to **B** (output) See Figure 8	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		4.2	ns
			V_{CCB} = 5 V ± 0.5 V		4.4	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		4.2	
			V_{CCB} = 5 V ± 0.5 V		4.4	
$t_{PLH(B-A)}$	Propagation delay time (low to high), from **B** (input) to **A** (output) See Figure 8	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.5	
			V_{CCB} = 5 V ± 0.5 V		2.6	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		2.5	
			V_{CCB} = 5 V ± 0.5 V		3.3	
$t_{en(OE-A)}$ $t_{en(OE-B)}$	Enable time, from **OE** (input) to **A** or **B** (output)	V_{CCB} = 3.3 V ± 0.3 V			200	ns
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{dis(OE-A)}$ $t_{dis(OE-B)}$	Disable time,from **OE** (input) to **A** or **B** (output)	V_{CCB} = 3.3 V ± 0.3 V			200	ns
		V_{CCB} = 5 V ± 0.5 V			200	
$t_{r(Ax)}$	Rise time, A port	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		5.6	ns
			V_{CCB} = 5 V ± 0.5 V		5	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	25	140	
			V_{CCB} = 5 V ± 0.5 V	19	102	
$t_{r(Bx)}$	Rise time, B port	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		6.4	ns
			V_{CCB} = 5 V ± 0.5 V		7.4	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	26	130	
			V_{CCB} = 5 V ± 0.5 V	14	75	
$t_{f(Ax)}$	Fall time, A port	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		5.4	ns
			V_{CCB} = 5 V ± 0.5 V		5	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		6.1	
			V_{CCB} = 5 V ± 0.5 V		5.7	
$t_{f(Bx)}$	Fall time, B port	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		7.4	ns
			V_{CCB} = 5 V ± 0.5 V		7.6	
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V		7.6	
			V_{CCB} = 5 V ± 0.5 V		8.3	
t_{sk}	Channel-to-channel skew	V_{CCB} = 3.3 V ± 0.3 V			1	ns
		V_{CCB} = 5 V ± 0.5 V			1	
	Maximum data rate	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	22		Mbps
			V_{CCB} = 5 V ± 0.5 V	24		
		Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	2		
			V_{CCB} = 5 V ± 0.5 V	2		

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6.12 Typical Characteristics

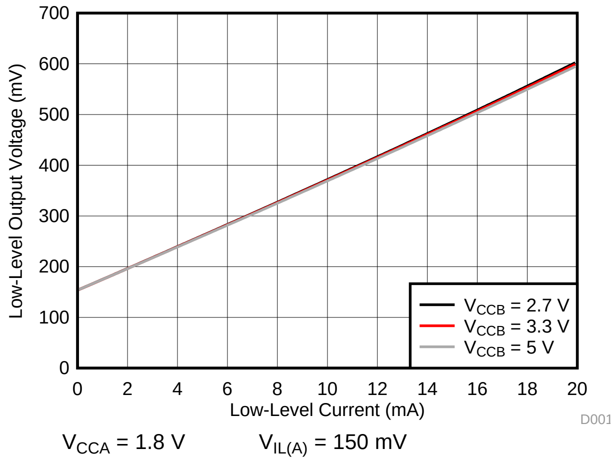


Figure 1. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

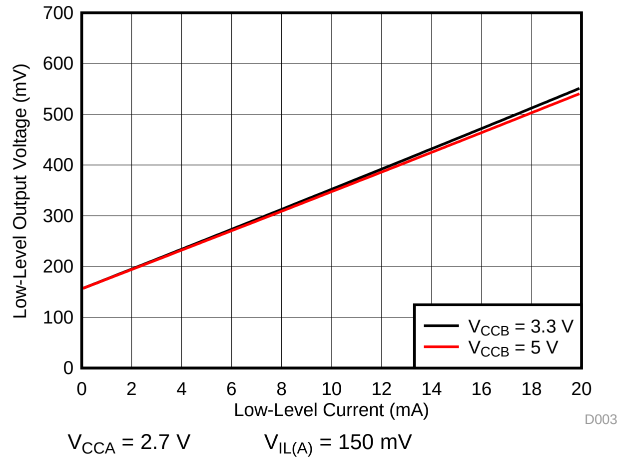


Figure 2. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

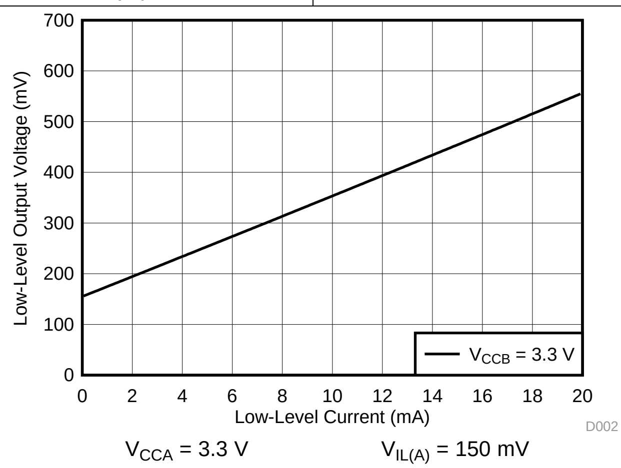


Figure 3. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

7 Parameter Measurement Information

7.1 Load Circuits

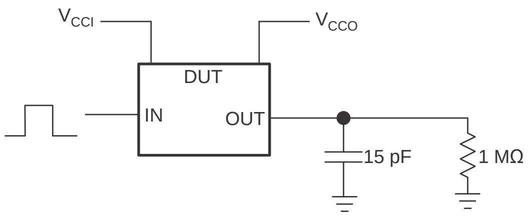


Figure 4. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

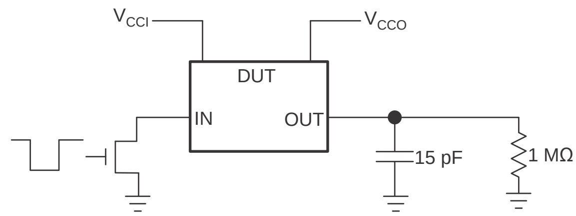
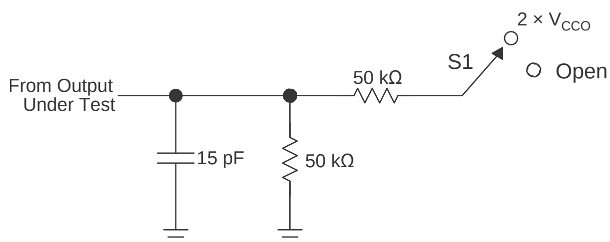


Figure 5. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL} / t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ} / t_{PZH} (t_{en})	Open

Figure 6. Load Circuit for Enable-Time and Disable-Time Measurement

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.

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7.2 Voltage Waveforms

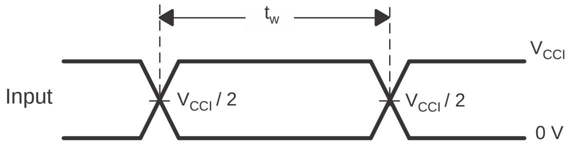

Figure 7. Pulse Duration

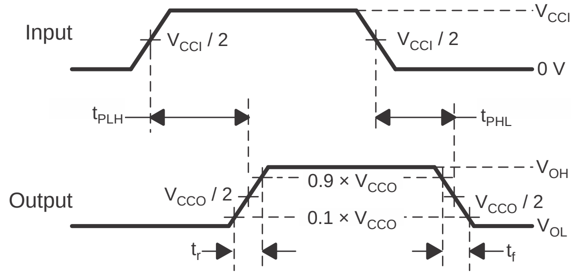

Figure 8. Propagation Delay Times

1. C_L includes probe and jig capacitance.
2. Waveform 1 in Figure 9 is for an output with internal such that the output is high, except when OE is high (see Figure 6). Waveform 2 in Figure 9 is for an output with conditions such that the output is low, except when OE is high.
3. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.

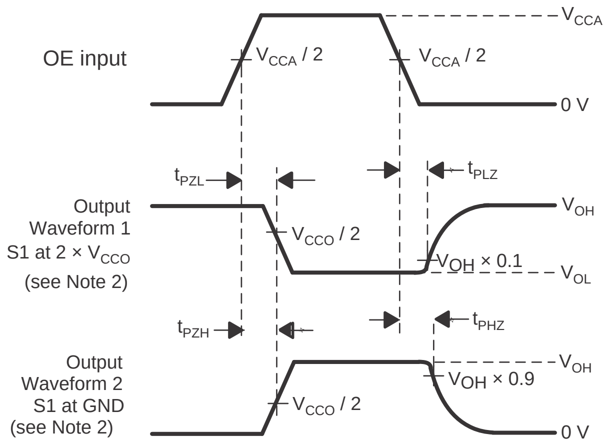

Figure 9. Enable and Disable Times

8 Detailed Description

8.1 Overview

The TXS0104E-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65 V to 3.6 V, while the B port can accept I/O voltages from 2.3 V to 5.5 V. The device is a pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. 10-kΩ pullup resistors, commonly used in open drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open drain applications, the device can also translate push-pull CMOS logic outputs.

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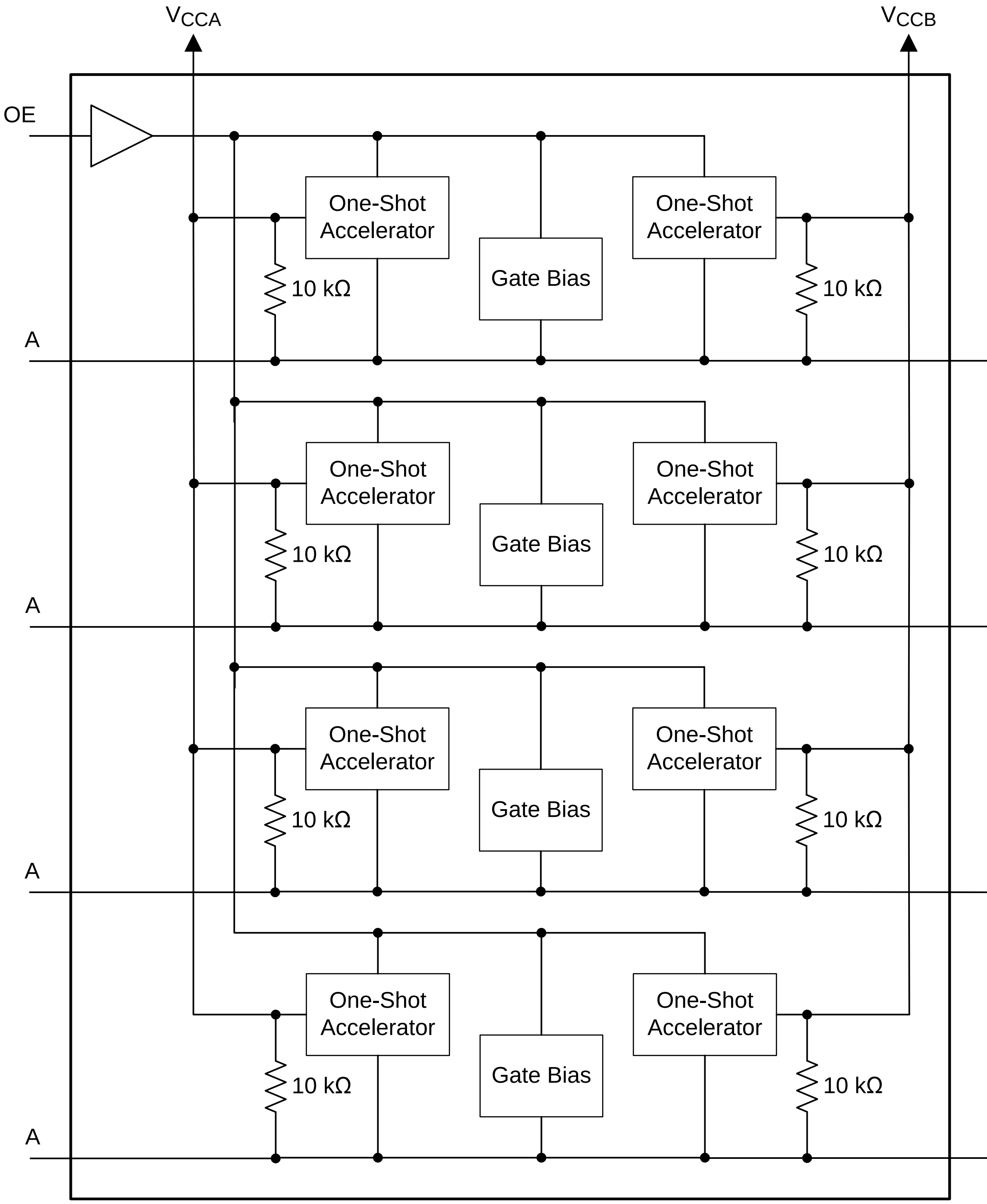
8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Architecture

The TXS0104E-Q1 architecture (see Figure 10) does not require a direction-control signal in order to control the direction of data flow from A to B or from B to A.

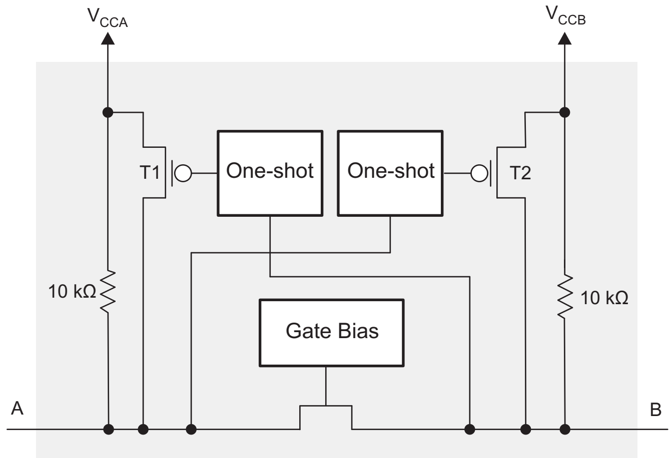

Figure 10. Architecture of a TXS01xx Cell

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T2) for a short duration which speeds up the low-to-high transition.

8.3.2 Input Driver Requirements

The fall time (t_{fA}, t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0104E-Q1 device. Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

8.3.3 Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

8.3.4 Enable and Disable

The TXS0104E-Q1 device has an OE input that disables the device by setting OE low, which places all I/Os in the high-impedance state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

8.3.5 Pullup and Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors).

8.4 Device Functional Modes

The TXS0104E-Q1 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

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9 Application and Implementation

9.1 Application Information

The TXS0104E-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0104E-Q1 device is ideal for use in applications where an open-drain driver is connected to the data I/Os. The TXS0104E-Q1 device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0104-Q1 device might be a better option for such push-pull applications.

9.2 Typical Application

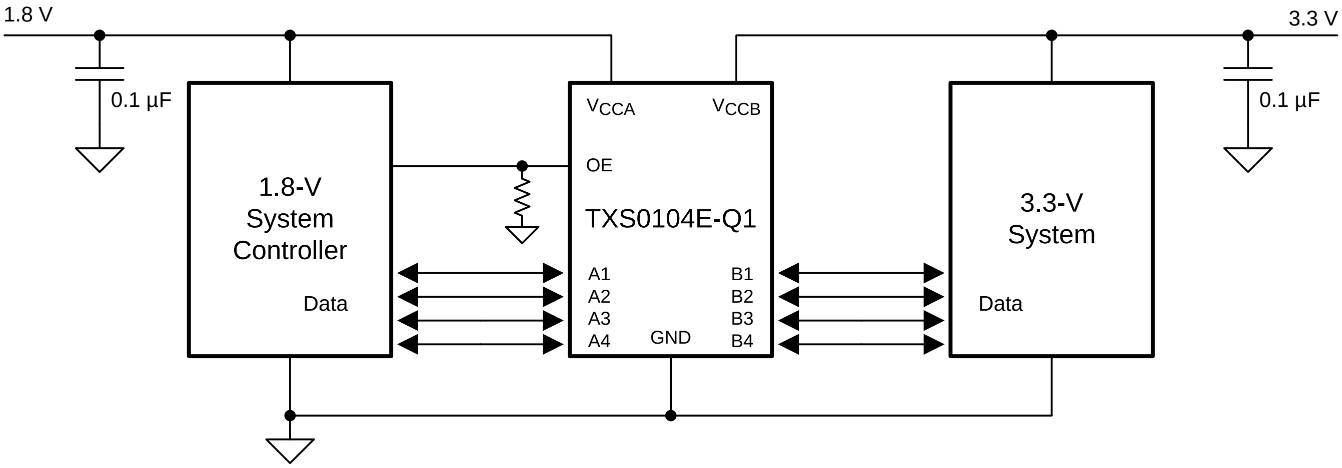

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Figure 11. Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6 V
Output voltage range	2.3 to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0104E-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXS0104E-Q1 device is driving to determine the output voltage range.
  - The TXS0104E-Q1 device has 10-kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.

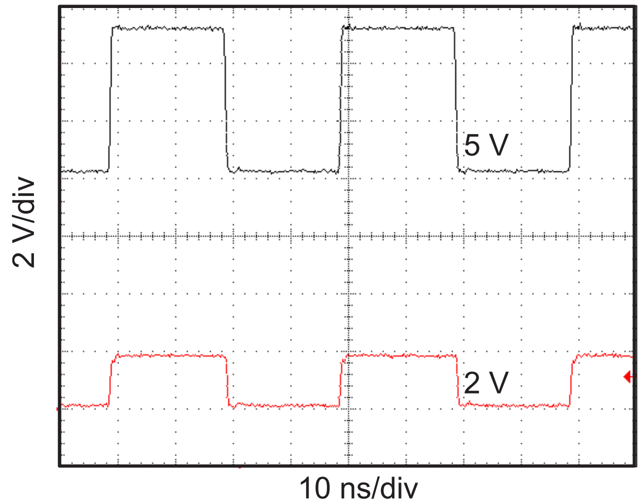
- An external pulldown resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 to calculate the V_{OH} as a result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10\ k\Omega) \tag{1}$$

where

- V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor

9.2.3 Application Curve



V_{CCA} = 1.8 V V_{CCB} = 5 V

Figure 12. Level-Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

The TXS0104E-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCB} accepts any supply voltage from 2.3 V to 5.5 V and V_{CCA} accepts any supply voltage from 1.65 V to 3.6 V as long as Vs is less than or equal to V_{CCB}. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The TXS0104E-Q1 device does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \geq V_{CCB}$) does not damage the device, but during operation, V_{CCA} must be less than or equal to V_{CCB} ($V_{CCA} \leq V_{CCB}$) at all times.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

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11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

11.2 Layout Example

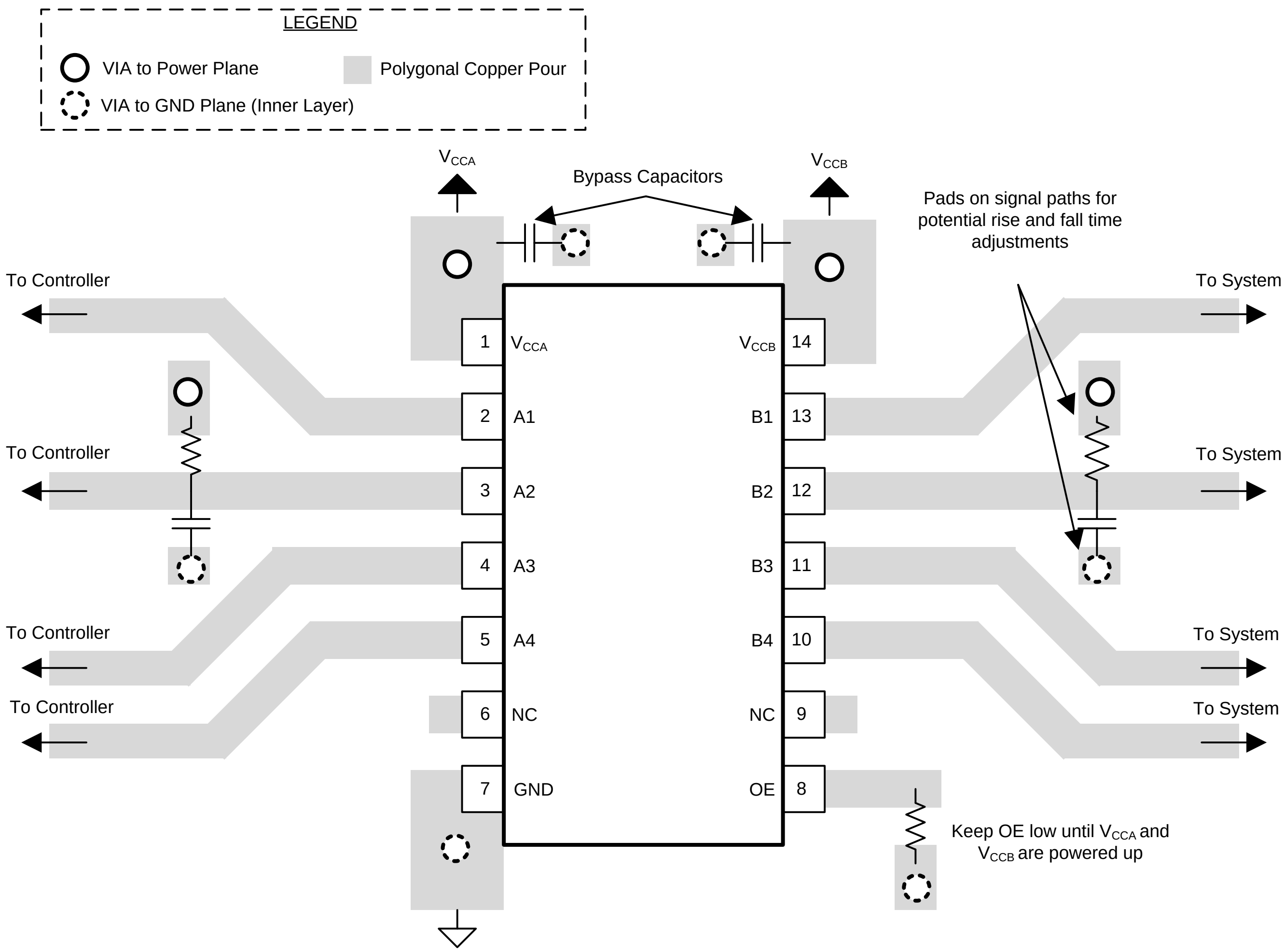

Figure 13. TXS0104E-Q1 Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

《逻辑器件简介》

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0104EQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	04EQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TXS0104E-Q1 :

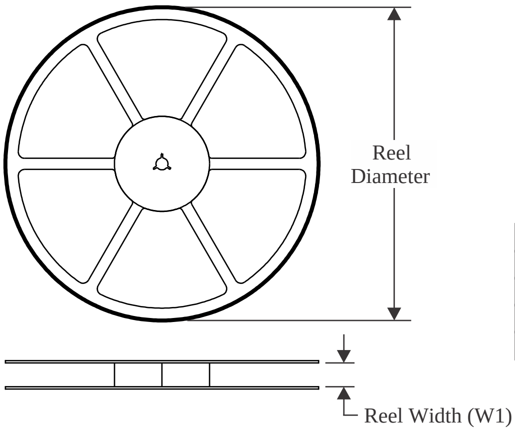
- Catalog : TXS0104E

NOTE: Qualified Version Definitions:

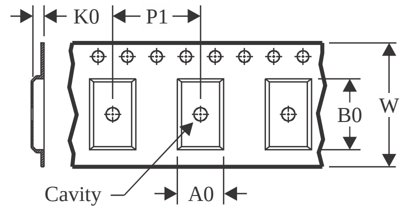
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

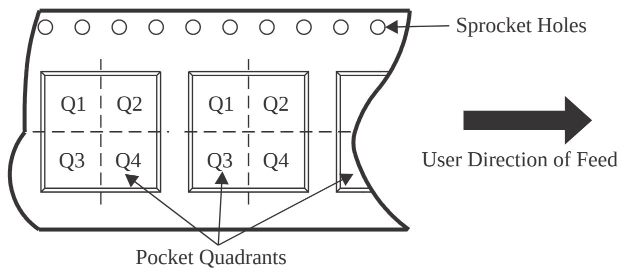


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

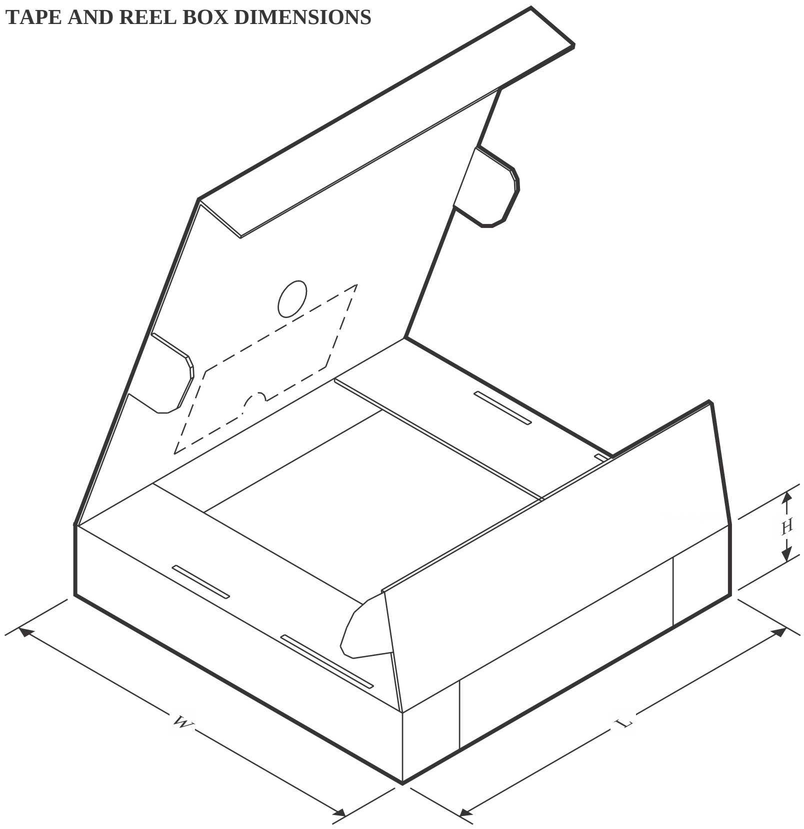
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0104EQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

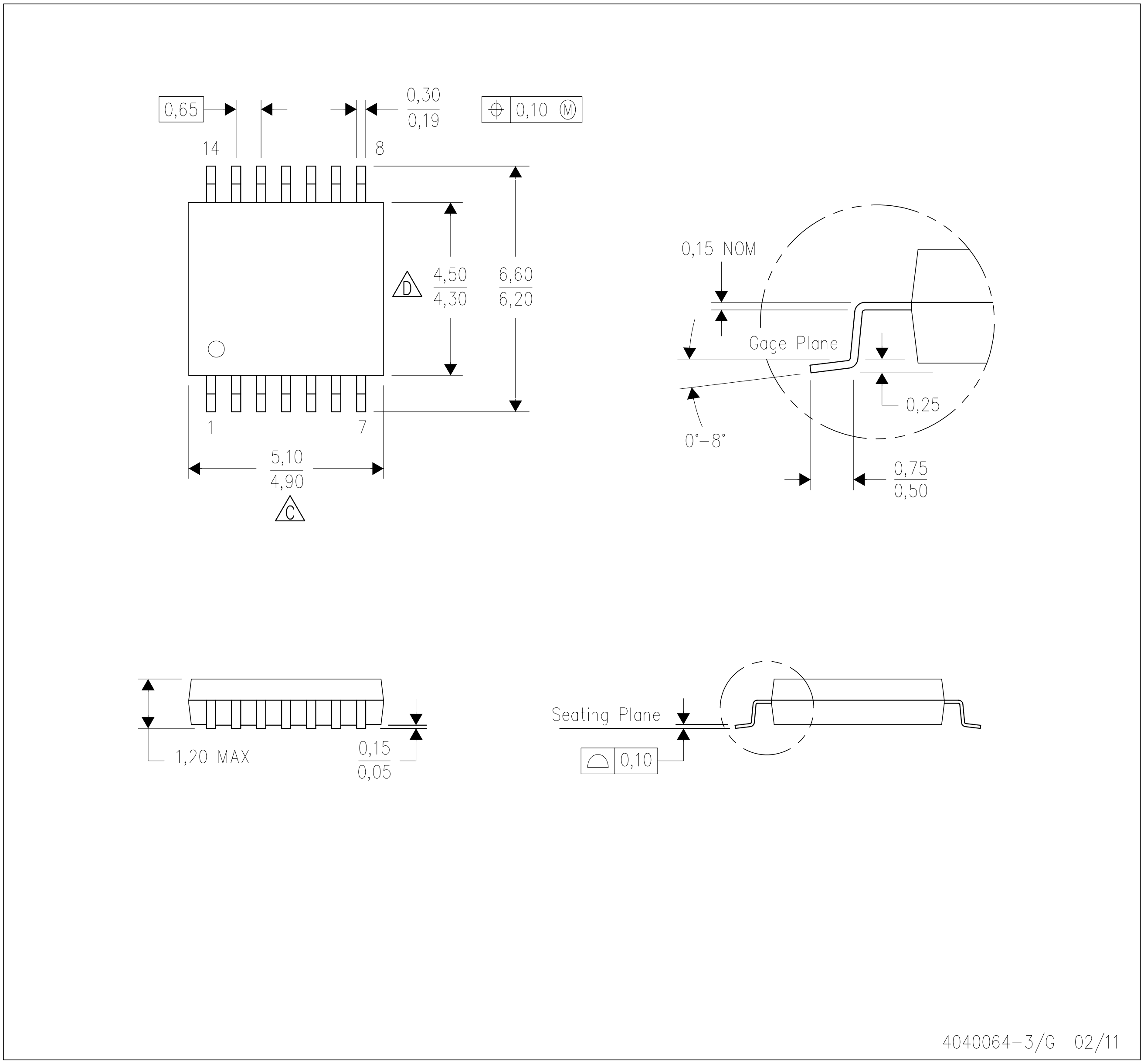
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

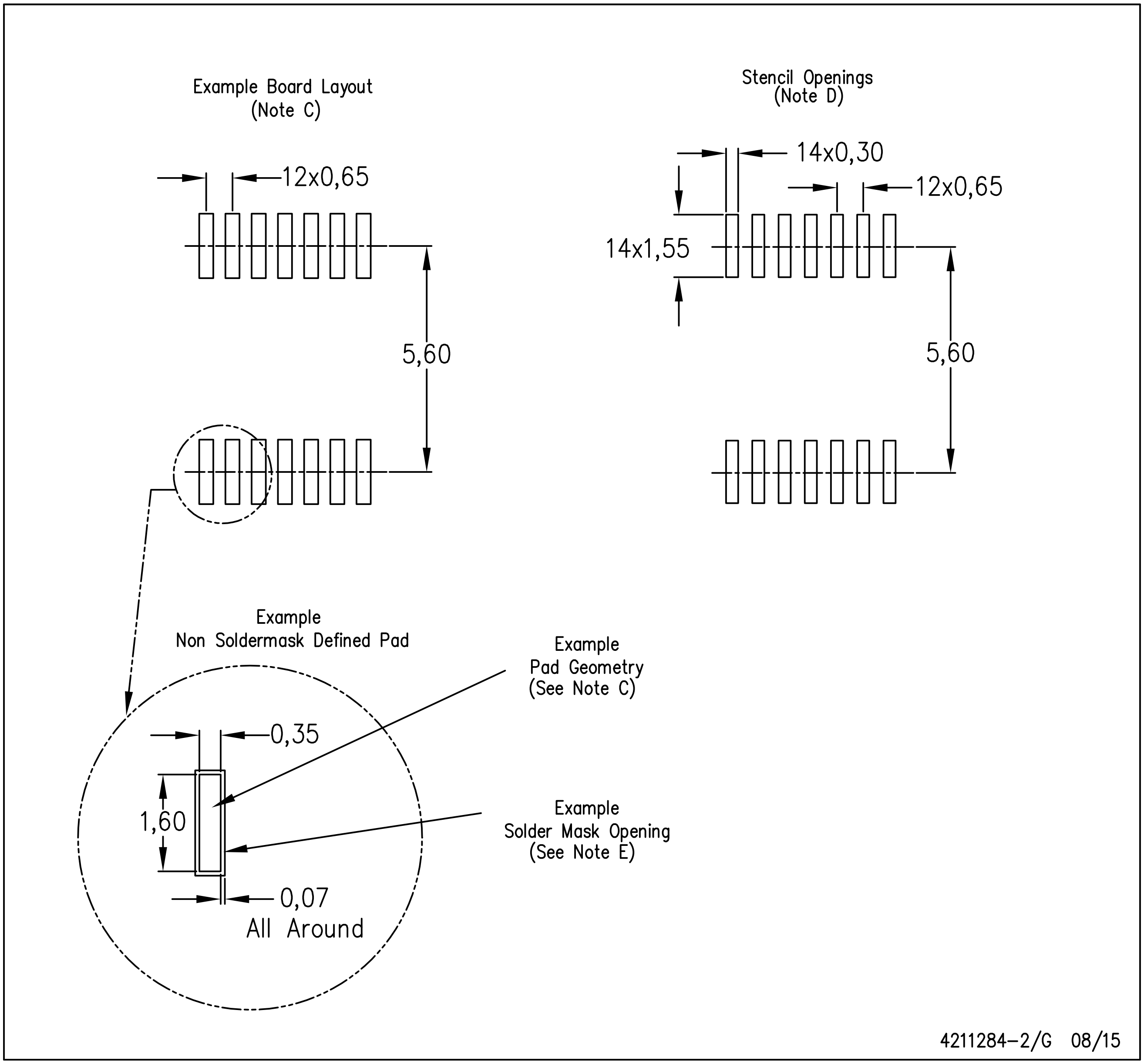
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0104EQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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