PGA970 LVDT 传感器信号调节器

1 特性

- 模拟 特性
  - 适用于 LVDT 传感器的可编程增益模拟前端
  - 激励波形发生器和放大器
  - 具有幅度和相位解调器的双通道 24 位 ADC
  - 24 位辅助 ADC
  - 片上内部温度传感器
  - 具有可编程增益的 14 位输出 DAC
  - 内置诊断
- 数字 特性
  - ARM® Cortex®-M0 微控制器
  - 16KB 铁电 RAM (FRAM) 程序存储器
  - 2KB 通用 RAM
  - 512B RAM 波形发生器查找表
  - 8MHz 片上振荡器
- 外设 特性
  - 串行外设接口 (SPI)
  - 单线接口 (OWI)
  - 比例电压输出和绝对电压输出
- 一般 特性
  - 工作电源电压范围：3.5V 至 30V
  - 环境温度范围：–40°C 至 +125°C
  - 适用于扩展级电源电压范围 (>30V) 的 DMOS 栅极控制器

2 应用

- 位置传感器信号调节
- 线性可变差动变压器 (LVDT)
- 旋转可变差动变压器 (RVDT)
- 旋转变压器
- RLC 测量

3 说明

PGA970 是一款高度集成的片上系统 LVDT 传感器信号调节器，具有先进的信号处理功能。该器件配有一个三通道、低噪声、可编程增益模拟前端，允许直接连接感测元件，后接三个独立的 24 位 Δ-Σ ADC。

此外，该器件包含的数字信号解调模块可连接到集成的 ARM-Cortex M0 MCU，从而执行器件非易失性存储器中存储的定制传感器补偿算法。该器件可使用 SPI、OWI、GPIO 或 PWM 数字接口与外部系统通信。模拟输出通过一个 14 位 DAC 和可编程增益放大器来提供支持，从而提供基准或绝对电压输出。感测元件激励通过集成的波形发生器和波形放大器来实现。波形信号数据根据用户自定义存储在指定的 RAM 存储区。

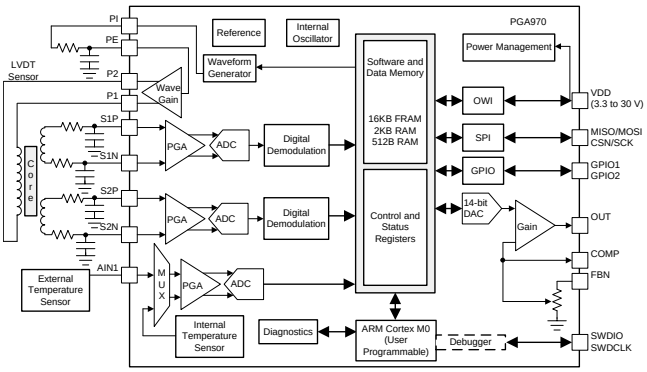
除了主要的功能组件之外，PGA970 还配有额外的支持电路。例如器件诊断、传感器诊断和集成型温度传感器。这些电路可共同为整个系统和感测元件提供保护及相关完整性信息。该器件还包含一个栅极控制器电路，可在系统电源电压超过 30V 时搭配外部耗尽型金属氧化物半导体场效应晶体管 (MOSFET) 一同调节器件电源电压。

器件信息(1)

订货编号	封装	封装尺寸（标称值）
PGA970QPHPR	HTQFP (48)	7.00mm × 7.00mm
PGA970QPHPT		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化图表



4 器件和文档支持

4.1 文档支持

4.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《PGA970 GUI 用户指南》*
- 德州仪器 (TI)，*《PGA970 软件快速入门指南》*用户指南
- 德州仪器 (TI)，*《PGA970 软件用户指南》*
- 德州仪器 (TI)，*《PGA970EVM 用户指南》*

4.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

4.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

4.4 商标

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4.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

4.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

5 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是适用于指定器件的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA970QPHPR	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	PGA970Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

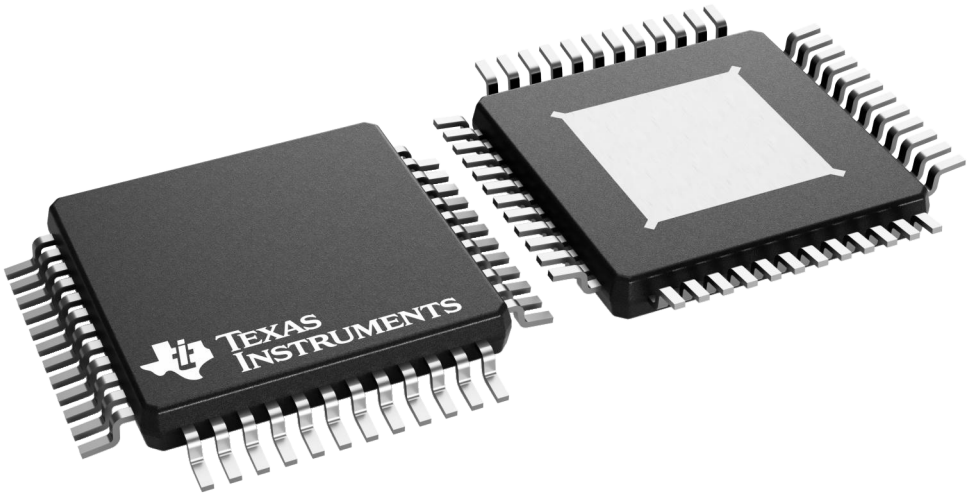
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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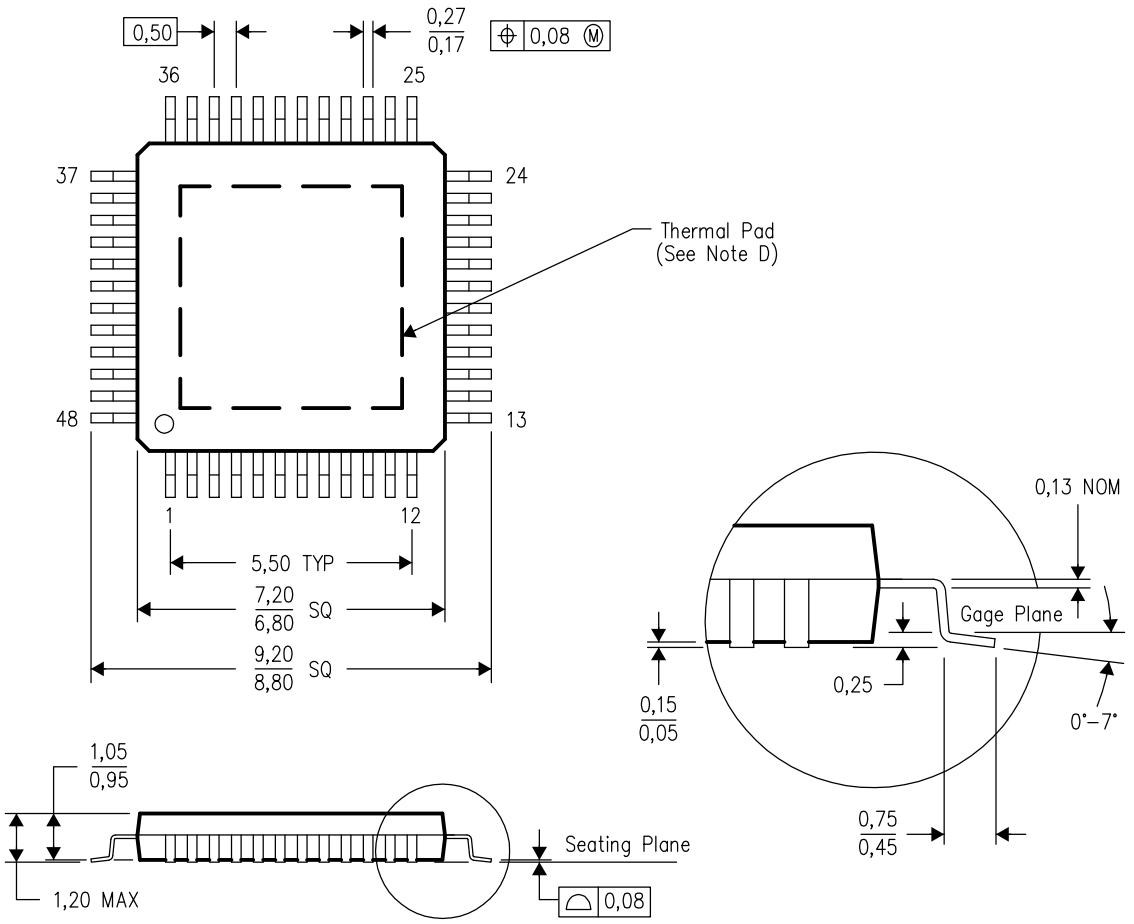
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

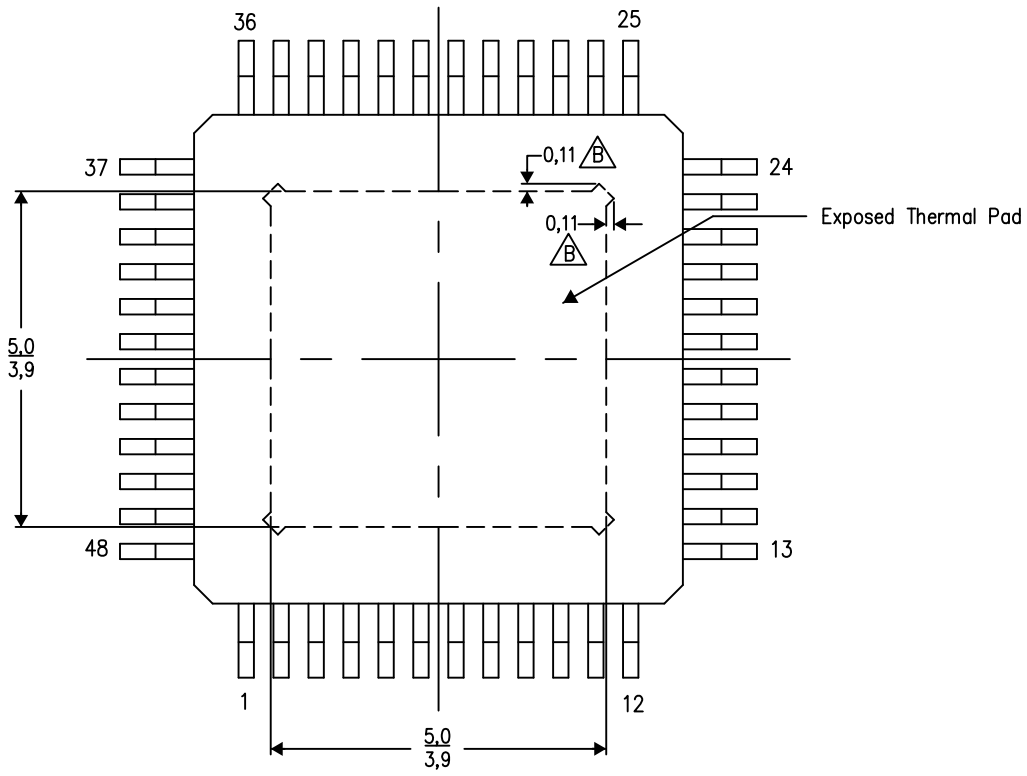
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

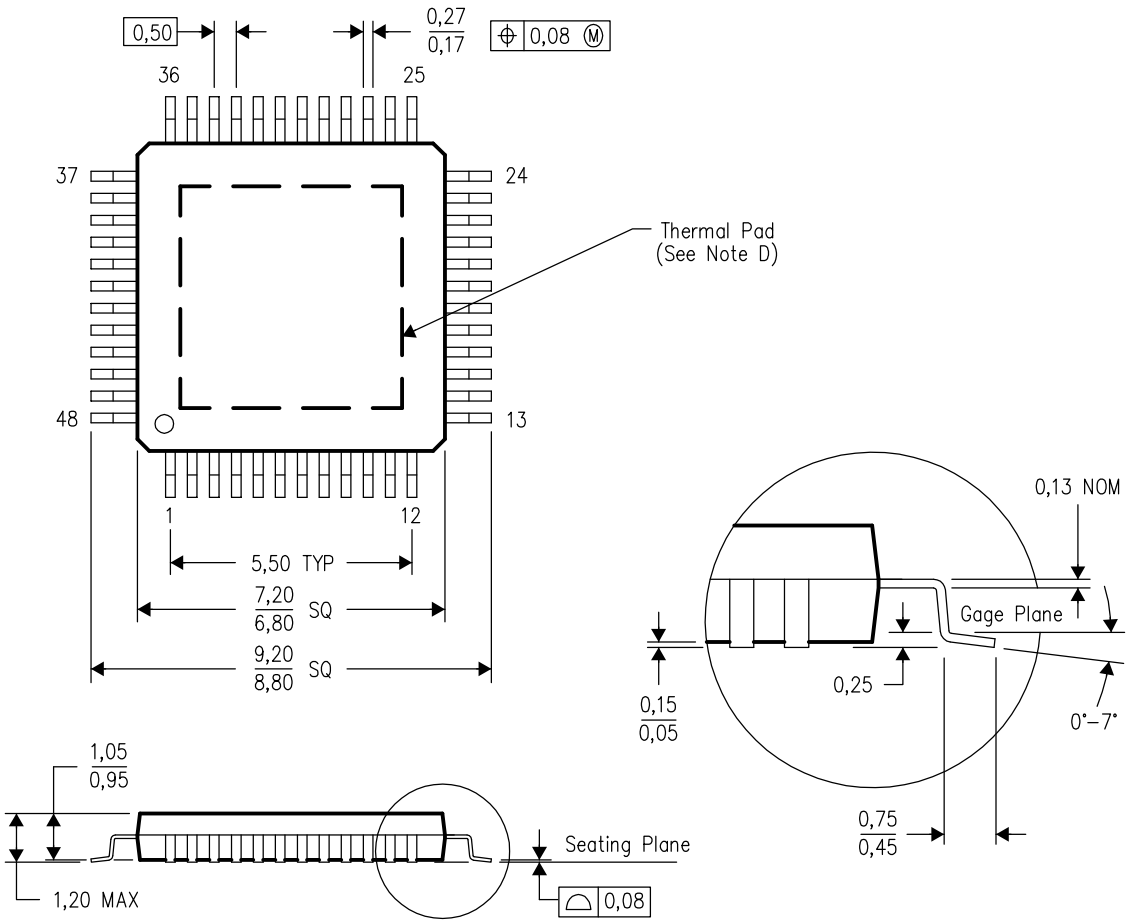
4206329–17/P 03/15

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



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PowerPAD is a trademark of Texas Instruments.

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

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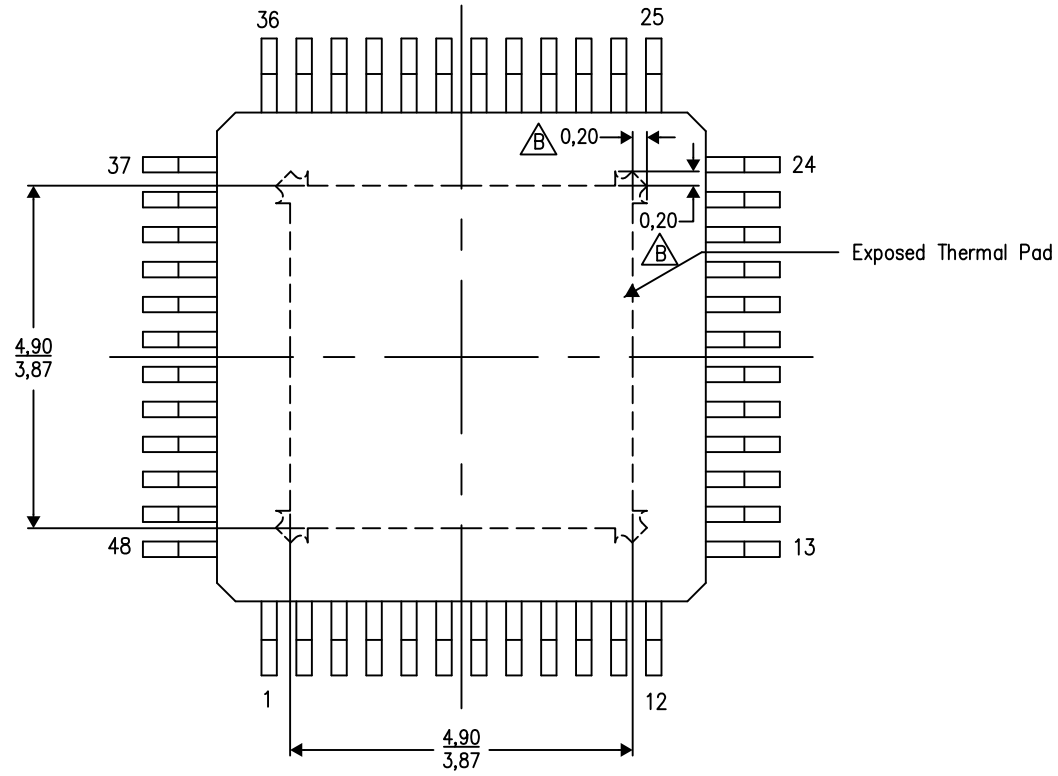


Top View

Exposed Thermal Pad Dimensions

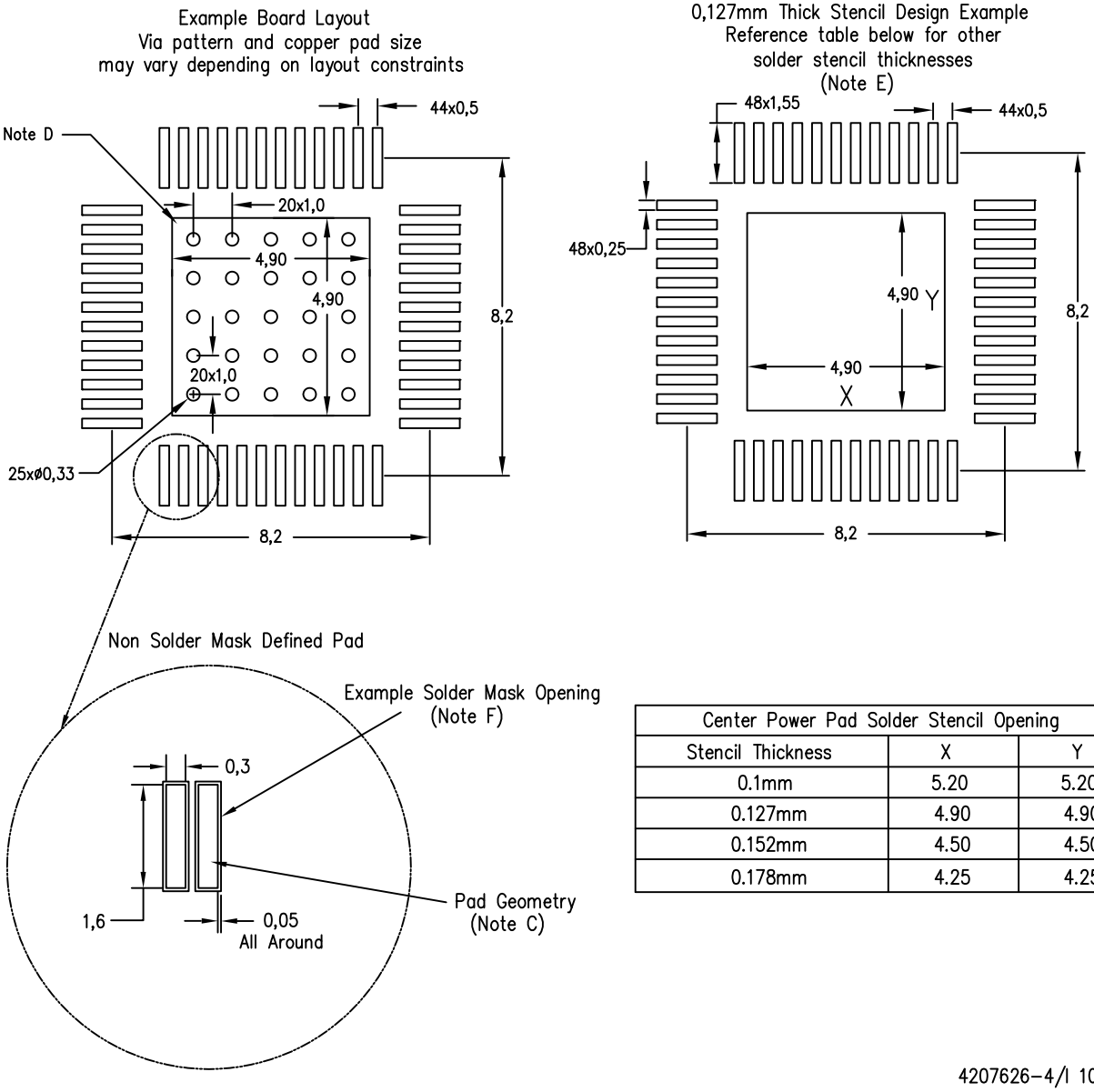
4206329–4/P 03/15

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.20	5.20
0.127mm	4.90	4.90
0.152mm	4.50	4.50
0.178mm	4.25	4.25

4207626–4/I 10/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

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