同步降压 NexFET™ 功率级

特性

- **25A** 电流下 **90%** 的系统效率
- 输入电压高达 **22V**
- 高频率工作（高达 **2MHz**）
- 整合电源块技术
- 高密度 **— SON 5** 毫米 **× 6** 毫米封装
- 低功耗：**2.8W**（在 **25A** 电流下）
- 超低电感封装
- 系统优化 **PCB** 焊脚
- 可兼容 **3.3V** 及 **5V PWM** 信号
- 三态 **PWM** 输入
- 集成型自举二极管
- 预偏置启动保护
- 贯通保护
- 符合 **RoHS** 标准——无铅型触电无卤素电镀

应用

- 同步降压转换器
- 多相同步降压型转换器
- **POL DC-DC** 转换器
- 内存卡及图形卡
- 台式电脑及服务器 **VR11.x** 和 **VR12.x V** 内核同步降压转换器

订购信息

器件	封装	介质	数量	出货
CSD97370Q5M	SON 5 毫米 × 6 毫米塑料封装	13 英寸卷带	2500	卷带包装

说明

CSD97370Q5M NexFET 功率级是一款优化型设计，适用于高功率、高密度同步降压转换器。 该产品集成了一个增强型栅极驱动器 IC 与电源块技术，以完善功率级开关功能。 这种组合形成了一个高电流、高效率、高速开关器件，并凭借其大尺寸的以地面为基础的热垫，在小型 5mm x 6mm 外形封装内提供了一个出色的热源解决方案。 此外，还对 PCB 的器件封装进行了优化，以帮助缩短设计时间并简化整个系统设计方案的完成。

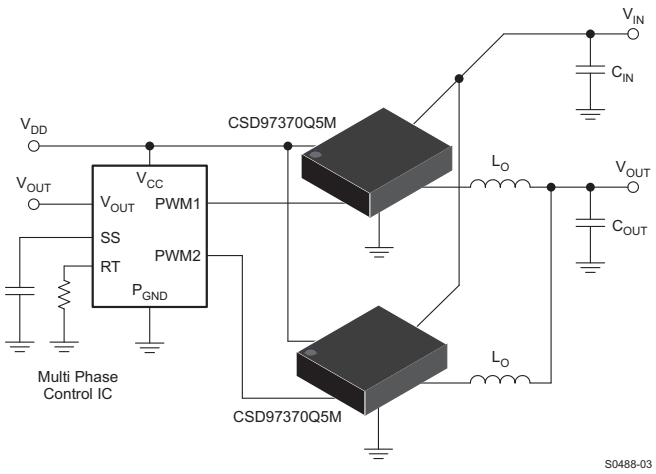


Figure 1. Application Diagram

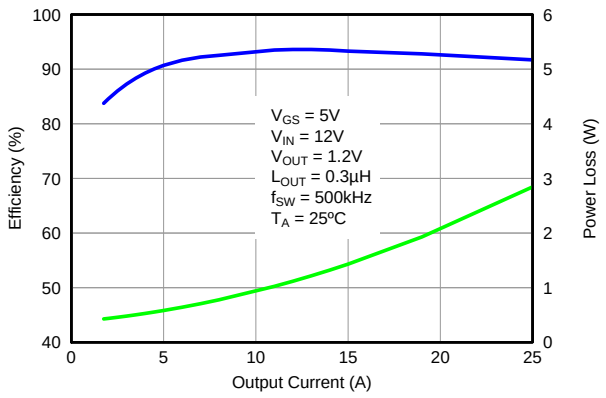


Figure 2. Efficiency and Power Loss

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

T_A = 25°C (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
V_{IN} to P_{GND} (2)			30	V
V_{SW} to P_{GND} , V_{IN} to V_{SW}		-0.8	30	V
V_{SW} to P_{GND} (10ns)		-7	32	V
V_{DD} to P_{GND}		–0.3	7	V
ENABLE to P_{GND} (3)		–0.3	V_{DD} + 0.3	V
PWM to P_{GND} (3)		–0.3	V_{DD} + 0.3	V
BOOT to BOOT_R (3)		–0.3	V_{DD} + 0.3	V
ESD Rating	Human Body Model (HBM)		2	kV
	Charged Device Model (CDM)		500	V
Power Dissipation, P_D			12	W
Operating Temperature Range, T_J		-40	150	°C
Storage Temperature Range, T_{STG}		–55	150	°C

(1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.
(2) V_{IN} to V_{SW} Max = 32V for 10ns
(3) Should not exceed 7V

RECOMMENDED OPERATING CONDITIONS

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	MAX	UNIT
Gate Drive Voltage, V_{DD}		4.5	5.5	V
Input Supply Voltage, V_{IN}		3.3	22	V
Output Voltage, V_{OUT}			5.5	V
Continuous Output Current, I_{OUT}	V_{IN} = 12V, V_{DD} = 5V, V_{OUT} = 1.2V, f_{SW} = 500kHz, L_{OUT} = 0.3µH (1)		40	A
Peak Output Current, I_{OUT-PK} (2)			60	A
Switching Frequency, f_{SW}	C_{BST} = 0.1µF (min)	200	2000	kHz
On Time Duty Cycle			85%	
Minimum PWM On Time		40		ns
Operating Temperature		–40	125	°C

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) System conditions as defined in Note 1. Peak Output Current is applied for t_p = 50µs.

THERMAL INFORMATION

T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top of package)			20	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (1)			2	°C/W

(1) $R_{\theta JB}$ value based on hottest board temperature within 1mm of the package.

ELECTRICAL CHARACTERISTICS

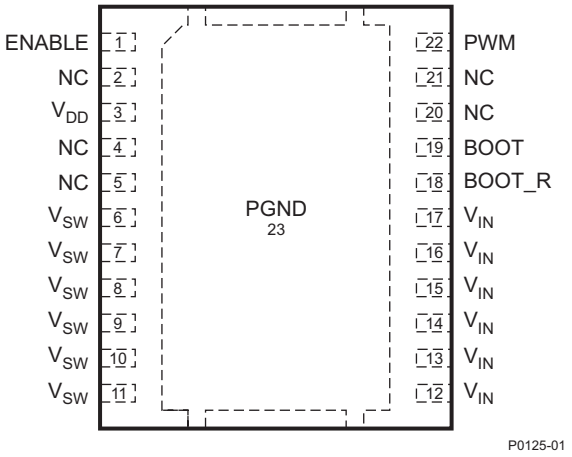
T_A = 25°C, V_{DD} = POR to 5.5V (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}					
Power Loss(1)	V_{IN} = 12V, V_{DD} = 5V, V_{OUT} = 1.2V, I_{OUT} = 25A, f_{SW} = 500kHz, L_{OUT} = 0.3µH , T_J = 25°C	–	2.8	3.3	W
Power Loss(2)	V_{IN} = 12V, V_{DD} = 5V, V_{OUT} = 1.2V, I_{OUT} = 40A, f_{SW} = 500kHz, L_{OUT} = 0.3µH , T_J = 125°C	–	8	10	W
V_{IN}					
V_{IN} Quiescent Current (I_Q)	ENABLE = 0V, V_{DD} = 5V	–	–	100	µA
V_{DD}					
Standby Supply Current (I_{DD})	ENABLE = 0V, PWM = 0V	–	1	5	µA
Operating Supply Current (I_{DD})	ENABLE = 5V, PWM = 50% Duty cycle, f_{SW} = 500kHz	–	16	20	mA
POWER-ON RESET AND UNDER VOLTAGE LOCKOUT					
Power on Reset (V_{DD} Rising)		–	3.6	3.9	V
UVLO (V_{DD} Falling)		3.4	3.5	–	V
Hysteresis		100	–	250	mV
Startup Delay(3)	ENABLE = PWM = 5V	–	600	1000	ns
ENABLE					
Logic Level Low Threshold (V_{IL})	Schmitt Trigger Input PWM = 5V (See Figure 5)	0.8	1	–	V
Logic Level High Threshold (V_{IH})		–	1.6	2.0	V
Threshold Hysteresis		–	580	–	mV
Weak Pull-down Impedance		–	100	–	kΩ
Rising Propagation Delay (t_{PDH})		–	600	–	ns
Falling Propagation Delay (t_{PDL})		–	200	–	ns
PWM					
I_{PWMH}	PWM = 5V	–	620	800	µA
I_{PWML}	PWM = 0V	–	–260	–340	µA
PWM Logic Level High (V_{PWMH})	V_{DD} = POR to 5.5V, C_{PWM} = 10pF (See Figure 6)	–	–	2.2	V
PWM Logic Level Low (V_{PWML})		0.8	–	–	V
PWM 3-State open Voltage		–	1.5	–	V
PWM to VSW propagation delay (t_{PDLH} and t_{PDHL})		–	100	–	ns
3-State Shutdown Hold-off Time (t_{3HT})		–	100	–	ns
3-State Shutdown Propagation Delay (t_{3SD})		–	650	–	ns
3-State Recovery Propagation Delay (t_{3RD})		–	75	–	ns
BOOTSTRAP SWITCH					
Forward Voltage (V_{FBOOT})	V_{DD} – V_{BOOT}, I_F = 20mA	–	180	360	mV
Reverse Leakage (I_{RBOOT})(2)	V_{BOOT} – V_{DD} = 20V	–	0.15	1	µA

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) Specified by design
(3) POR to V_{SW} rising

PIN CONFIGURATION

SON 5mm × 6mm
22-Pin Package
(Top View)



PIN DESCRIPTION

PIN		DESCRIPTION
NO.	NAME	
1	ENABLE	Enables device operation. If ENABLE=logic HIGH, turns on the device. If ENABLE=logic LOW, the device is turned off and MOSFET gates are actively pulled low. An internal 100kΩ pull down resistor will pull the ENABLE pin LOW if left floating.
2	NC	Not for electrical connection, connect to floating pad only.
3	V_{DD}	Supply Voltage to Gate Drivers and internal circuitry.
4	NC	Not for electrical connection, connect to floating pad only.
5	NC	Not for electrical connection, connect to floating pad only.
6	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
7	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
8	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
9	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
10	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
11	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
12	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
13	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
14	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
15	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
16	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
17	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
18	BOOT_R	Bootstrap capacitor connection. Connect a minimum 0.1µF 16V X5R, ceramic cap from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the Control FET. The bootstrap diode is integrated.
19	BOOT	
20	NC	Not for electrical connection, connect to floating pad only.
21	NC	Not for electrical connection, connect to floating pad only.
22	PWM	Pulse Width modulated 3-state input from external controller. Logic Low sets Control FET gate low and Sync FET gate high. Logic High sets Control FET gate high and Sync FET gate Low. Open or High Z sets both MOSFET gates low if greater than the 3-State Shutdown Hold-off Time (t_{3HT})
23	P_{GND}	Power Ground

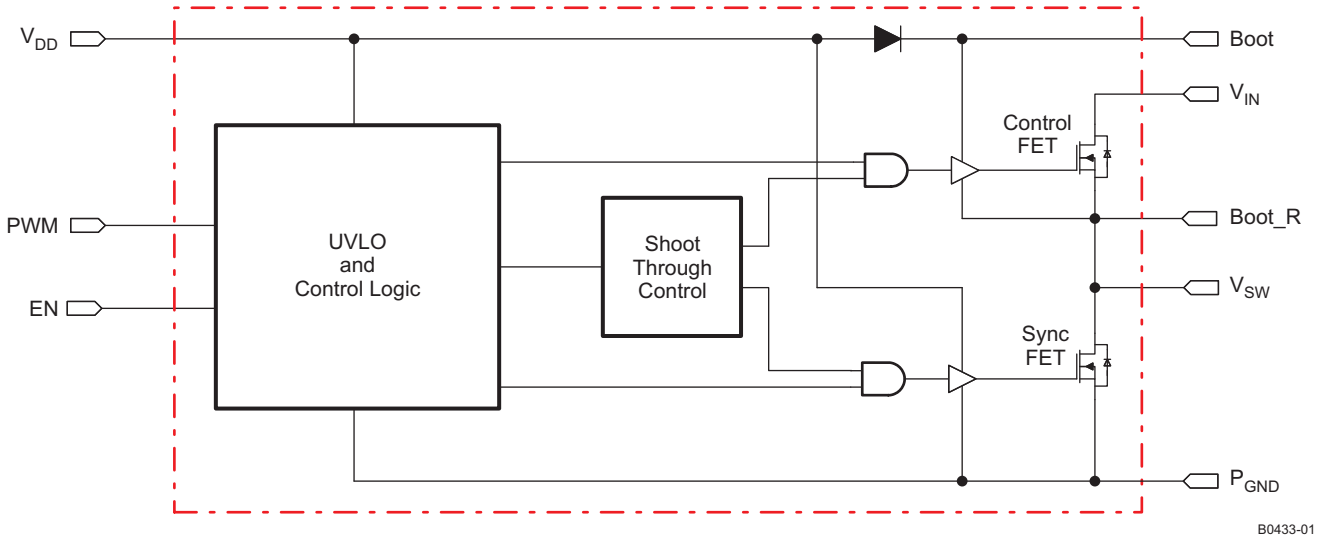


Figure 3. Functional Block Diagram

FUNCTIONAL DESCRIPTION

POWERING CSD97370Q5M AND GATE DRIVERS

An external V_{DD} voltage is required to supply the integrated gate driver IC and provide the necessary gate drive power for the MOSFETS. The gate driver IC is capable of supplying in excess of 4 Amps peak current into the MOSFET gates to achieve fast switching. A 1uF 10V X5R or higher ceramic capacitor is recommended to bypass V_{DD} pin to PGND. A bootstrap circuit to provide gate drive power for the Control FET is also included. The bootstrap supply to drive the Control FET is generated by connecting a 100nF 16V X5R ceramic capacitor between BOOT and BOOT_R pins. An optional R_{BOOT} resistor which can be used to slow down the turn on speed of the Control FET and reduce voltage spikes on the Vsw node. A typical 1Ω to 4.7Ω value is a compromise between switching loss and V_{SW} spike amplitude.

UVLO (Under Voltage Lock Out)

The V_{DD} supply is monitored for UVLO conditions and both Control FET and Sync FET gates are held low until adequate supply is available. An internal comparator evaluates the V_{DD} voltage level and if V_{DD} is greater than the Power On Reset threshold (V_{POR}) the gate driver becomes active. If V_{DD} is less than the UVLO threshold, the gate driver is disabled and the internal MOSFET gates are actively driven low. At the rising edge of the V_{DD} voltage, both Control FET and Sync FET gates will be actively held low during V_{DD} transitions between 1.0V to V_{POR}. This region is referred to the Gate Drive Latch Zone (see Figure 4). In addition, at the falling edge of the V_{DD} voltage, both Control FET and Sync FET gates are actively held low during the UVLO to 1.0V transition.

The Power Stage CSD97370Q5M device must be powered up and Enabled before the PWM signal is applied.

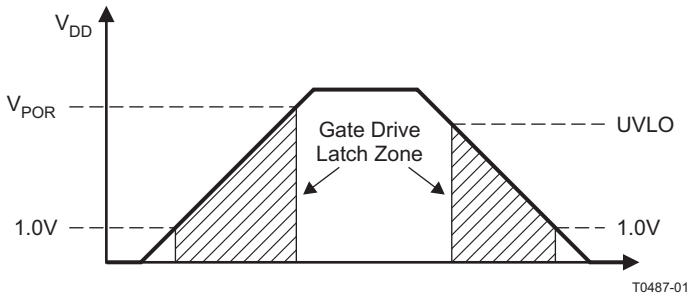


Figure 4. POR and UVLO

ENABLE

The ENABLE pin is TTL compatible. The logic level thresholds are sustained under all V_{DD} operating conditions between V_{POR} to V_{DD}. In addition, if this pin is left floating, a weak internal pull down resistor of 100kΩ will pull the ENABLE pin below the logic level low threshold. The operational functions of this pin should follow the timing diagram outlined in Figure 5. A logic level low will actively hold both Control FET and Sync FET gates low and V_{DD} pin should typically draw less than 5μA.

POWER UP SEQUENCING

If the ENABLE signal is used, it is necessary to ensure proper co-ordination with the ENABLE and soft-start features of the external PWM controller in the system. If the CSD97370Q5M was disabled through ENABLE without sequencing with the PWM IC controller, the buck converter output will have no voltage or fall below regulation set point voltage. As a result, the PWM controller IC delivers Max duty cycle on the PWM line. If the Power Stage CSD97370Q5M is re-enabled by driving the ENABLE pin high, there will be an extremely large input inrush current when the output voltage builds back up again. The input inrush current might have undesirable consequences such as inductor saturation, driving the input power supply into current limit or even catastrophic failure of the CSD97370Q5M device. Disabling the PWM controller is recommended when the CSD97370Q5M is disabled. The PWM controller should always be re-enabled by going through soft-start routine to control and minimize the input inrush current and reduce current and voltage stress on all buck converter components. It is recommended that the external PWM controller be disabled when CSD97370Q5M is disabled or nonoperational because of UVLO.

PWM

The input PWM pin incorporates a 3-State function. The Control FET and Sync FET gates are forced low if the PWM pin is left floating for more than the 3-State Hold off time (t_{3HT}), typically 100ns. This requires the source impedance of the driving PWM signal to be a minimum of 250kΩ when in 3-State mode. Operation in and out of 3-State mode should follow the timing diagram outlined in Figure 6. Both V_{PWML} and V_{PWMH} threshold levels are set to accommodate both 3.3V and 5V logic controllers. During normal operation, the PWM signal should be driven to logic levels Low and High with a maximum of 220Ω/320Ω sink/source impedance respectively.

GATE DRIVERS

The CSD97370Q5M has an internal high-performance gate driver IC that ensures minimum MOSFET dead-time while eliminating potential shoot-through currents. Propagation delays between the Control FET and Sync FET gates are kept to a minimum to minimize body diode conduction and improve efficiency. The gate driver IC incorporates an adaptive shoot through protection scheme which ensures that neither MOSFET is turned on while the other one is still conducting at the same time, preventing cross conduction. See Table 1.

Table 1. Truth Table

ENABLE	PWM	CONTROL FET GATE	SYNC FET GATE	V_{SW}
L	X	L	L	3-State
H	<Min ON time	L	L	3-State
H	L	L	H	P_{GND}
H	3-State	L	L	3-State
H	H	H	L	V_{IN}
L = Logic Low; H = Logic High; X = Don't care; minimum on time = 40ns				

START UP IN PRE-BIASED OUTPUT VOLTAGE

The CSD97370Q5M incorporates a simple pre-bias feature to protect against the discharging of a prebiased output voltage and inducing large negative inductor currents. After the Power On Reset threshold is crossed and the ENABLE pin is set to logic level high, both internal MOSFETs are actively held low until the PWM pin receives a signal that crosses logic level high threshold and meets the minimum on time criteria (see the *Electrical Characteristics Table*). This allows the PWM control IC to provide a soft start routine that creates a monotonic startup of the output voltage. The pre-bias feature is enabled for a single event and subsequent PWM signals creates normal switching of the internal MOSFETs (see Table 1). To reactivate the pre-bias feature, the ENABLE pin needs to be pulled below logic level low or the V_{DD} supply voltage needs to cross UVLO.

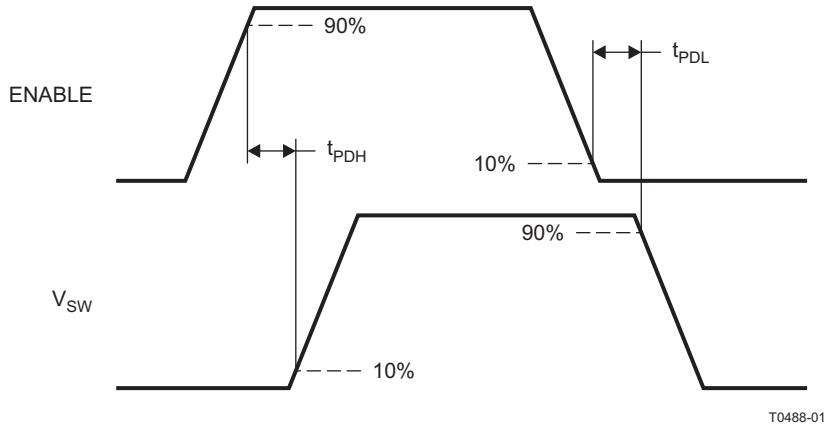


Figure 5. CSD97370Q5M ENABLE Timing Diagram (V_{DD} = PWM = 5V)

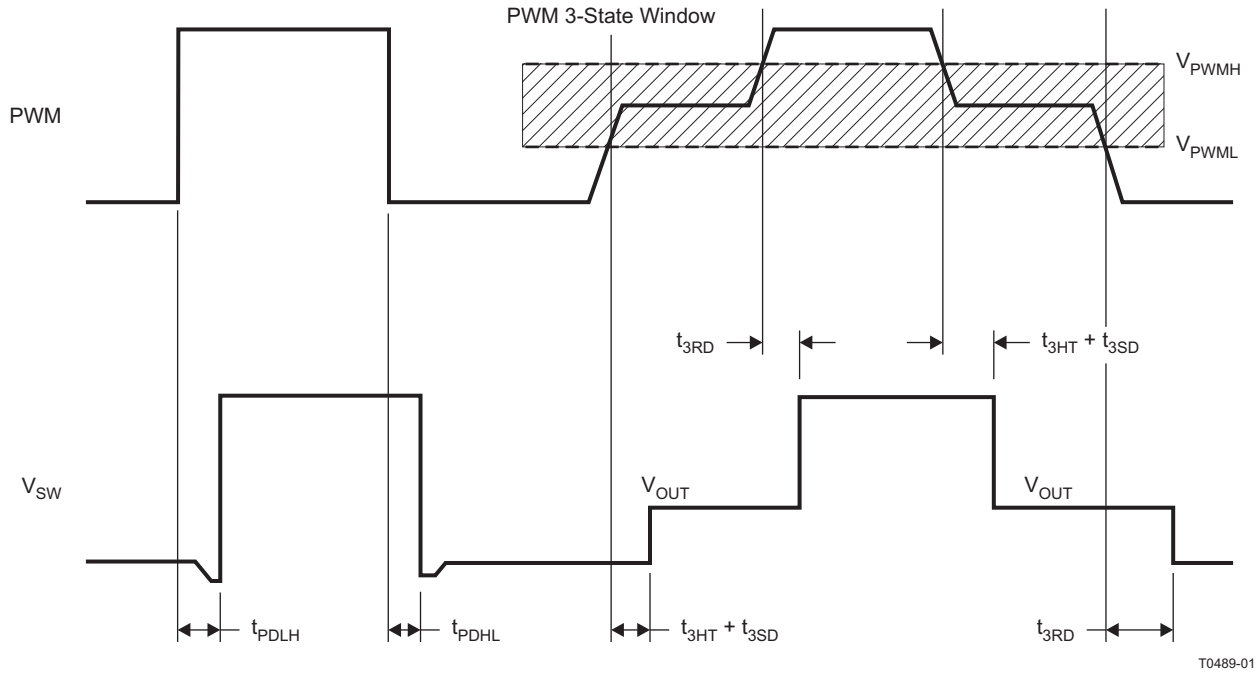


Figure 6. CSD97370Q5M PWM Timing Diagram

TYPICAL CHARACTERISTICS

Test conditions: V_{IN} = 12V, V_{DD} = 5V, f_{SW}= 500kHz, V_{OUT} = 1.2V, L_{OUT} = 0.3µH, DCR = 0.54mΩ, T_J = 125°C

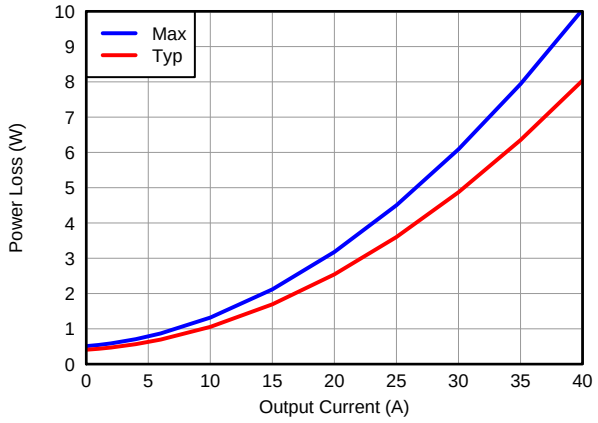


Figure 7. Power Loss vs Output Current

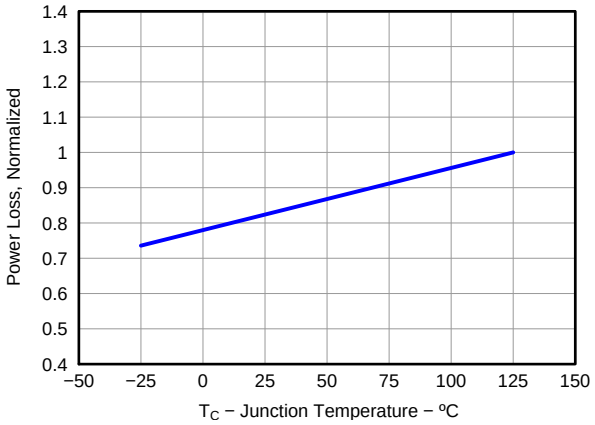


Figure 8. Power Loss vs Temperature

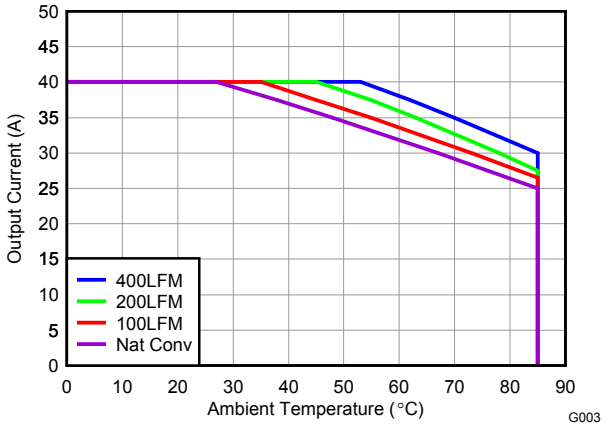


Figure 9. Safe Operating Area – PCB Vertical Mount (1)

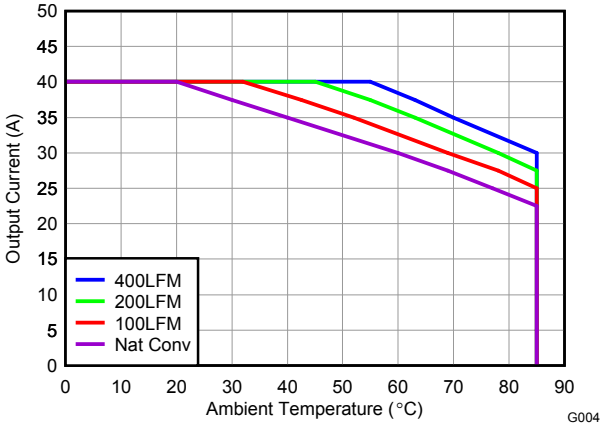


Figure 10. Safe Operating Area – PCB Horizontal Mount (1)

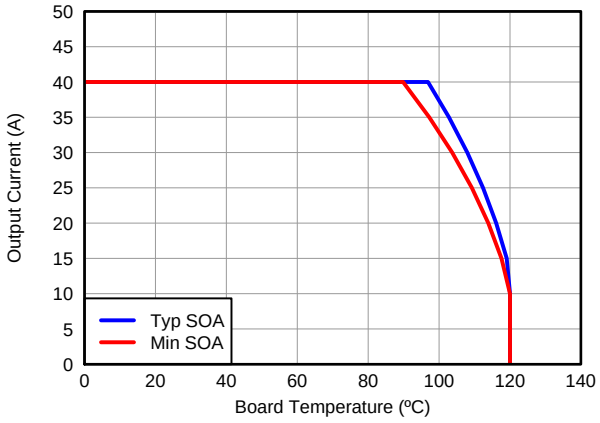


Figure 11. Typical and Min Safe Operating Area (1)

1. The Typical CSD97370Q5M System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness. See the *Application section*

TYPICAL CHARACTERISTICS (continued)

Test conditions: V_{IN} = 12V, V_{DD} = 5V, f_{SW}= 500kHz, V_{OUT} = 1.2V, L_{OUT} = 0.3µH, DCR = 0.54mΩ, T_J = 125°C

for detailed explanation.

TYPICAL CHARACTERISTICS

Test conditions: V_{IN} = 12V, V_{DD} = 5V, f_{SW}= 500kHz, V_{OUT} = 1.2V, L_{OUT} = 0.3µH, DCR = 0.54mΩ, T_J = 125°C

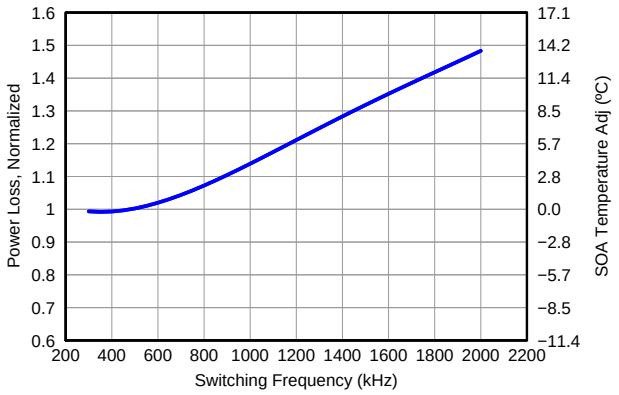


Figure 12. Normalized Power Loss vs Frequency

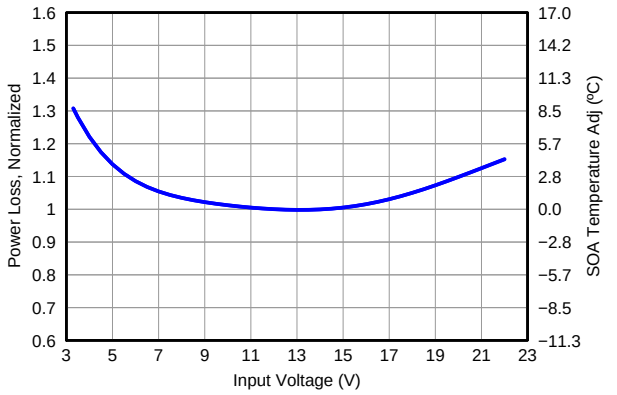


Figure 13. Normalized Power Loss vs Input Voltage

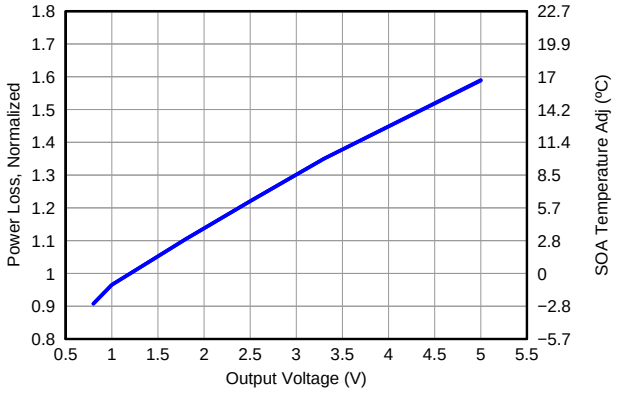


Figure 14. Normalized Power Loss vs Output Voltage

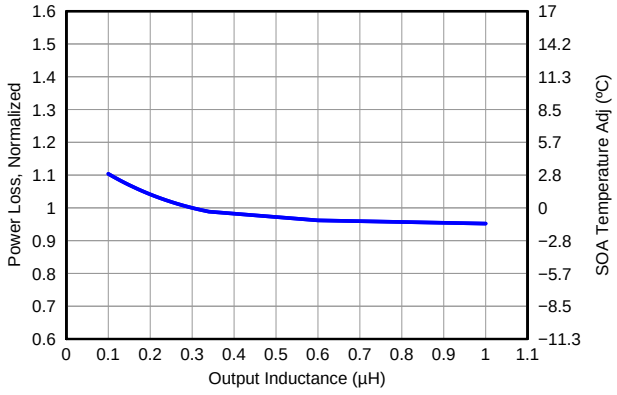


Figure 15. Normalized Power Loss vs Output Inductance

TYPICAL CHARACTERISTICS (continued)

Test conditions: V_{IN} = 12V, V_{DD} = 5V, f_{SW}= 500kHz, V_{OUT} = 1.2V, L_{OUT} = 0.3µH, DCR = 0.54mΩ, T_J = 125°C

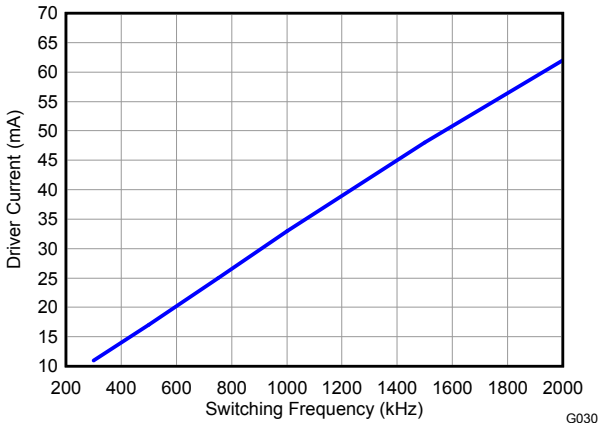


Figure 16. Driver Current vs Frequency

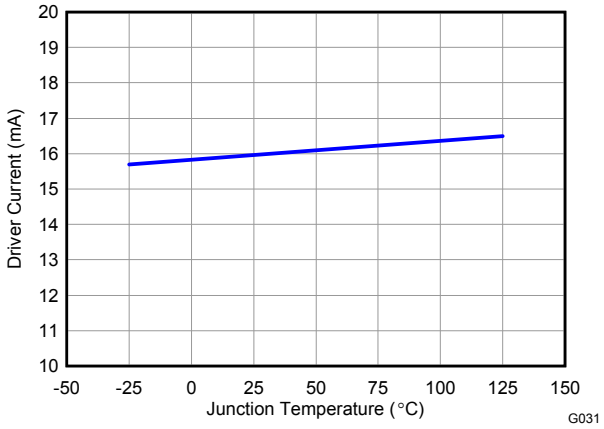


Figure 17. Driver Current vs Temperature

APPLICATION INFORMATION

The Power Stage CSD97370Q5M is a highly optimized design for synchronous buck applications using NexFET devices with a 5V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems centric environment. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System level performance curves such as Power Loss, Safe Operating Area and normalized graphs allow engineers to predict the product performance in the actual application.

Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 7 plots the power loss of the CSD97370Q5M as a function of load current. This curve is measured by configuring and running the CSD97370Q5M as it would be in the final application (see Figure 18). The measured power loss is the CSD97370Q5M device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\textbf{Power Loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 7 is measured at the maximum recommended junction temperature of T_J = 125°C under isothermal test conditions.

Safe Operating Curves (SOA)

The SOA curves in the CSD97370Q5M datasheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 9, Figure 10, and Figure 11 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness.

Normalized Curves

The normalized curves in the CSD97370Q5M data sheet give engineers guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

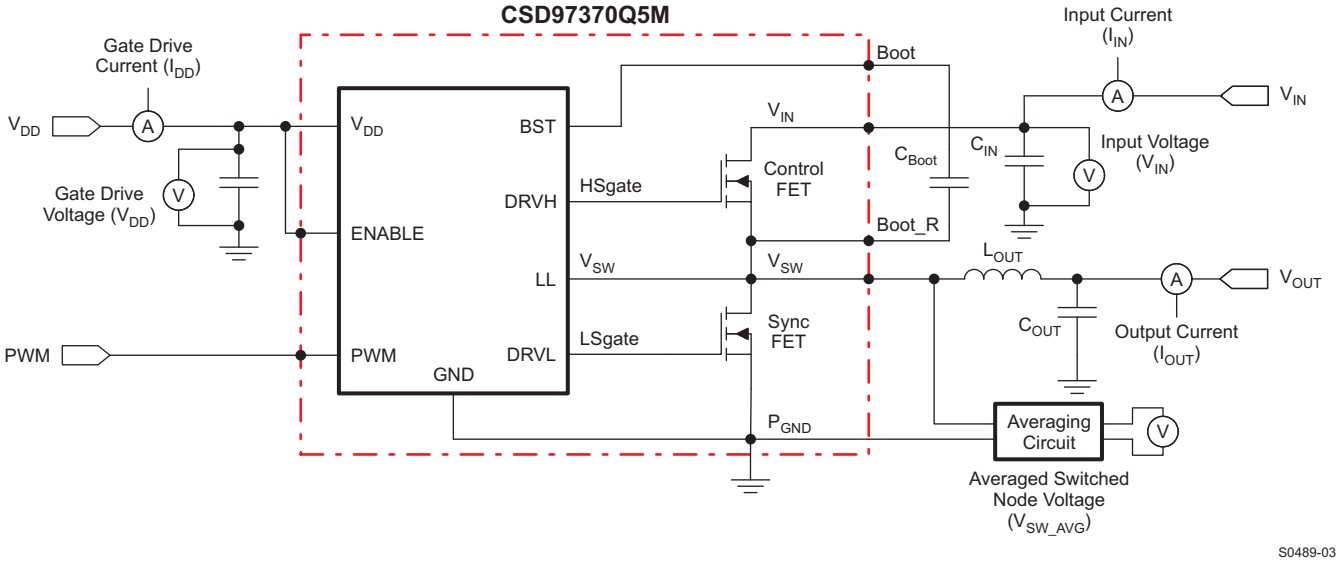


Figure 18. Power Loss Test Circuit

Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see the Design Example). Though the Power Loss and SOA curves in this datasheet are taken for a specific set of test conditions, the following procedure will outline the steps engineers should take to predict product performance for any set of system conditions.

Design Example

Operating Conditions: Output Current (I_{OUT}) = 25A, Input Voltage (V_{IN}) = 7V, Output Voltage (V_{OUT}) = 1V, Switching Frequency (f_{SW}) = 800kHz, Output Inductor (L_{OUT}) = 0.2µH

Calculating Power Loss

- Typical Power Loss at 25A = 3.5W (Figure 7)
- Normalized Power Loss for switching frequency ≈ 1.08 (Figure 12)
- Normalized Power Loss for input voltage ≈ 1.05 (Figure 13)
- Normalized Power Loss for output voltage ≈ 0.7 (Figure 14)
- Normalized Power Loss for output inductor ≈ 1.04 (Figure 15)
- **Final calculated Power Loss = 3.5W × 1.08 × 1.05 × 0.7 × 1.04 ≈ 2.89W**

Calculating SOA Adjustments

- SOA adjustment for switching frequency ≈ 2.6°C (Figure 12)
- SOA adjustment for input voltage ≈ 1.4°C (Figure 13)
- SOA adjustment for output voltage ≈ –1.0°C (Figure 14)
- SOA adjustment for output inductor ≈ 1.3°C (Figure 15)
- **Final calculated SOA adjustment = 2.6 + 1.4 + (–1.0) + 1.3 ≈ 4.3°C**

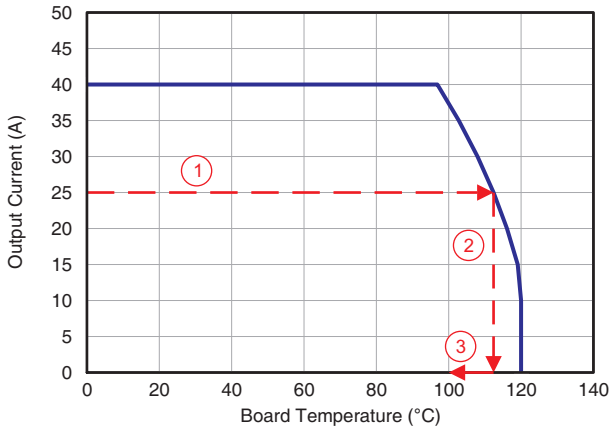


Figure 19. Power Stage CSD97370Q5M SOA

In the design example above, the estimated power loss of the CSD97370Q5M would increase to 2.89W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 4.3°C. Figure 19 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 4.3°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

RECOMMENDED PCB DESIGN OVERVIEW

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. Below is a brief description on how to address each parameter.

Electrical Performance

The CSD97370Q5M has the ability to switch at voltages rates greater than 10kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor and output capacitors.

- The placement of the input capacitors relative to V_{IN} and P_{GND} pins of CSD97370Q5M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the V_{IN} and P_{GND} pins (see Figure 20). The example in Figure 20 uses 6 x 10µF 1206 25V ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C5, C8 and C7, C19 should follow in order.
- The bootstrap cap C_{BOOT} 0.1µF 0603 16V ceramic capacitor should be closely connected between BOOT and BOOT_R pins
- The switching node of the output inductor should be placed relatively close to the Power Stage CSD97370Q5M V_{SW} pins. Minimizing the V_{SW} node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.(1)

Thermal Performance

The CSD97370Q5M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 20 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

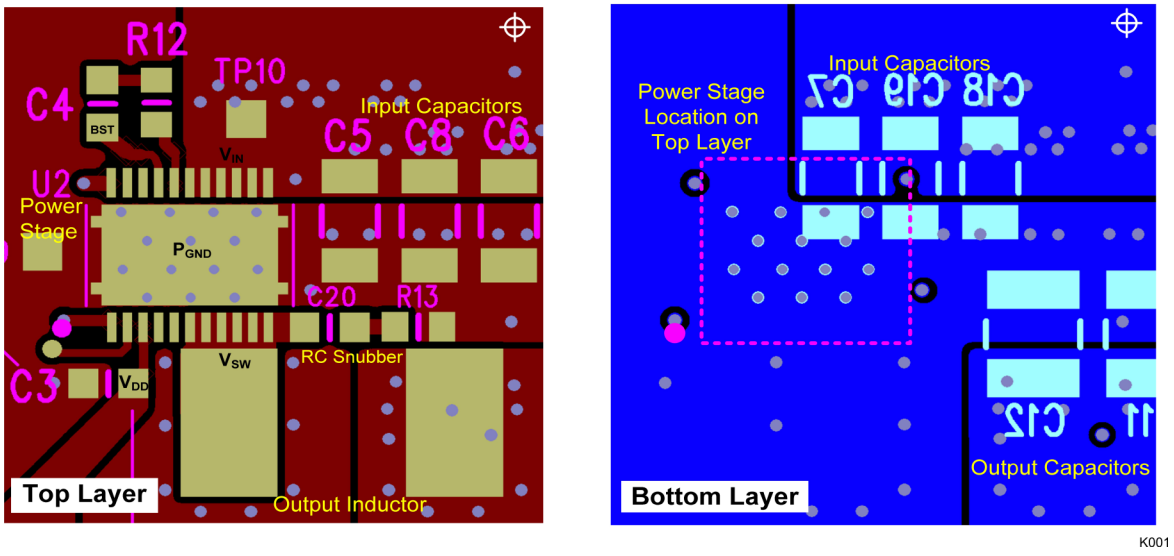
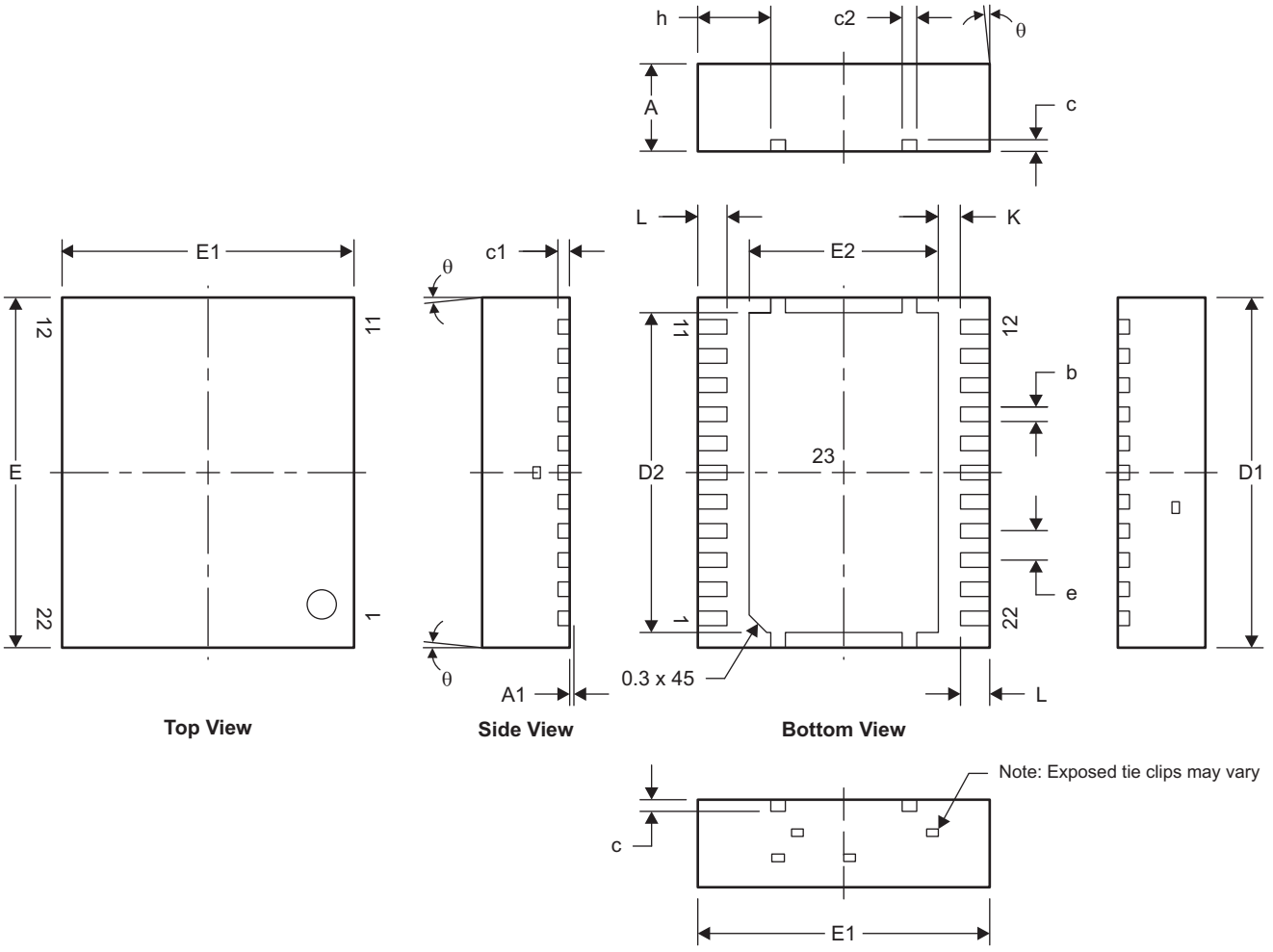


Figure 20. Recommended PCB Layout (Top Down View)

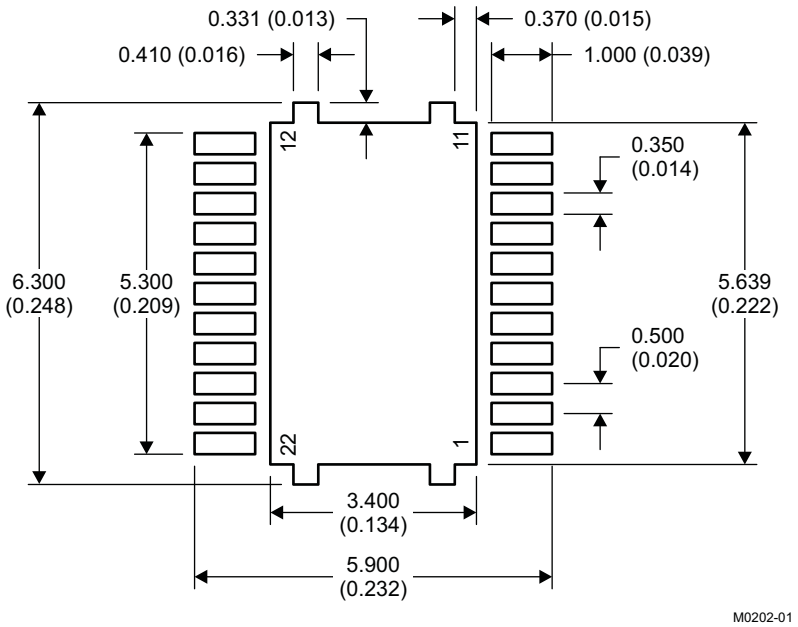
(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

MECHANICAL DATA



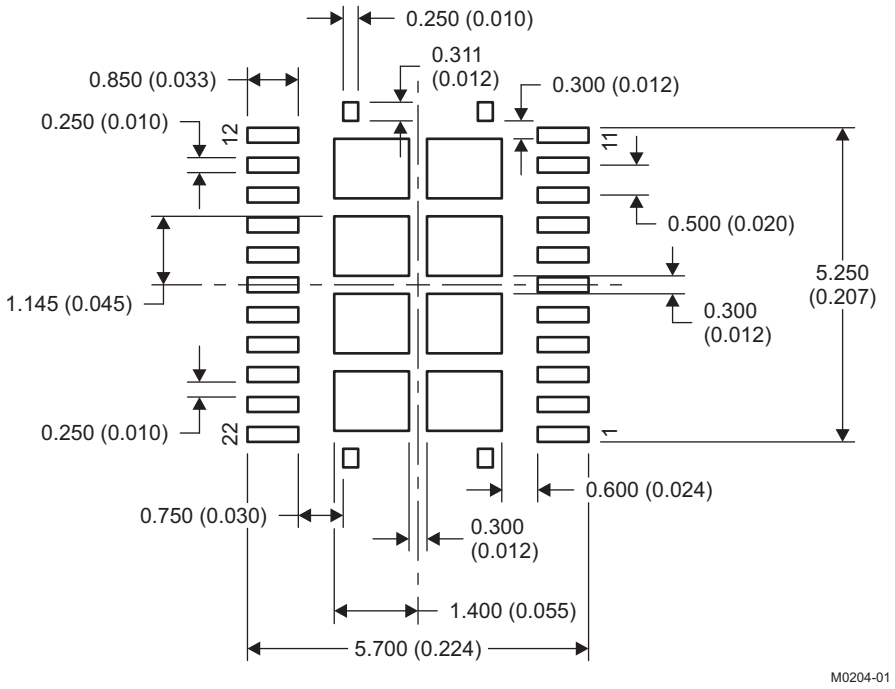
DIM	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.400	1.450	1.500	0.055	0.057	0.059
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.350	0.008	0.010	0.014
c	0.150	0.200	0.250	0.006	0.008	0.010
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.200	0.250	0.300	0.008	0.010	0.012
D1	5.900	6.000	6.100	0.232	0.236	0.240
D2	5.379	5.479	5.579	0.212	0.216	0.220
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.140	3.240	3.340	0.124	0.128	0.132
e		0.500 TYP			0.020 TYP	
h	1.150	1.250	1.350	0.045	0.049	0.053
K		0.380 TYP			0.015 TYP	
L	0.400	0.500	0.600	0.016	0.020	0.024
θ	0.00	—	—	0.00	—	—

Land Pattern Recommendation



NOTE: Dimensions are in mm (inches).

Stencil Recommendation



NOTE: Dimensions are in mm (inches).

REVISION HISTORY

Changes from Original (June 2011) to Revision A **Page**

- Added Features List item: "Input Voltages up to 22V" 1

Changes from Revision A (June 2011) to Revision B **Page**

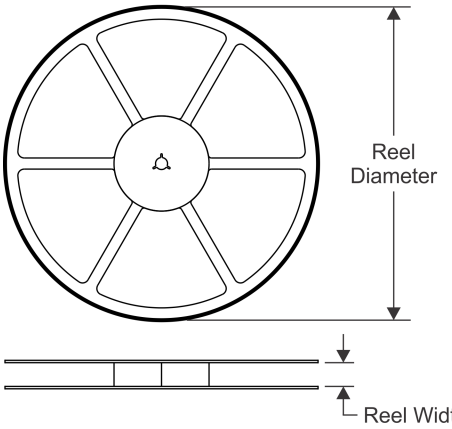
- Changed DIM A Min/Nom/Max values 14
- Changed DIM b Max Millimeters From: 0.300 To 0.350 and Max inches From: 0.013 To: 0.014 14
- Changed lead width From: 0.300(0.012) To: 0.350(0.014) 15

Changes from Revision B (October 2011) to Revision C **Page**

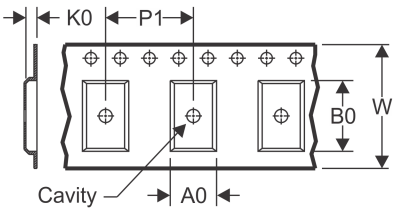
- Changed the max value of V_{DD} to P_{GND} From: 6 V To: 7 V in the Abs Max Table 2

TAPE AND REEL INFORMATION

REEL DIMENSIONS

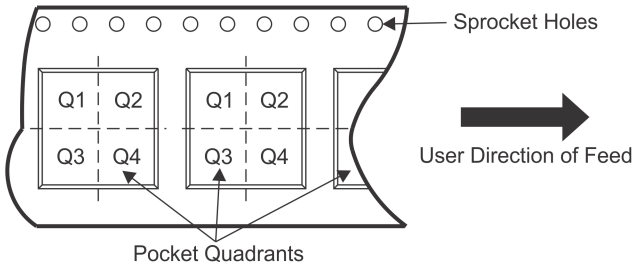


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

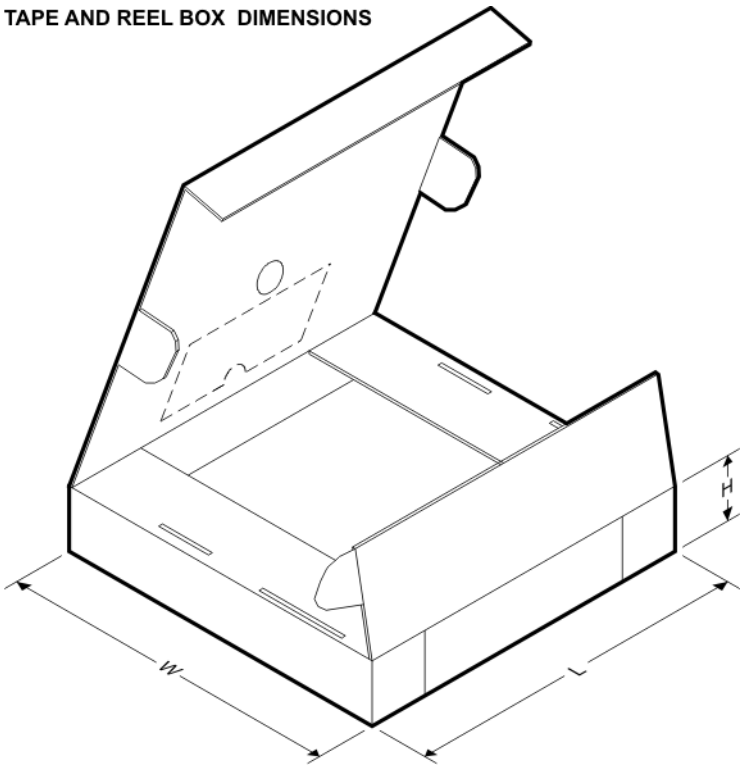
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD97370Q5M	LSON-CLIP	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD97370Q5M	LSON-CLIP	DQP	22	2500	367.0	367.0	35.0

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122