ADS7x51 12 位，2MSPS 和 14 位，1.5MSPS，双路，差分输入，同步采样模数转换器，具有内部基准

1 特性

- 12 和 14 位引脚兼容系列
- 两个通道同时采样
- 支持全差分模拟输入
- 独立内部基准（每个 ADC 一个）
- 高速：
  - 使用 ADS7251（12 位）时高达 2MSPS
  - 使用 ADS7851（14 位）时高达 1.5MSPS
- 出色的性能：
  - ADS7251：
    - 信噪比 (SNR)：73dB
    - 积分非线性 (INL)：±1 最低有效位 (LSB)
  - ADS7851：
    - 信噪比 (SNR)：83.5dB
    - 积分非线性 (INL)：±2LSB
- 在 -40°C 至 +125°C 的扩展工业用温度范围内完全额定运行
- 小型封装：超薄四方扁平无引线 (WQFN)-16 (3mm x 3mm)

2 应用范围

- 电机控制：与 SinCos 编码器的直接对接
- 光网络互连：掺铒光纤放大器 (EDFA) 增益控制环路
- 保护中继器
- 电源质量测量
- 三相电源控制
- 可编程逻辑控制器
- 工业自动化

3 说明

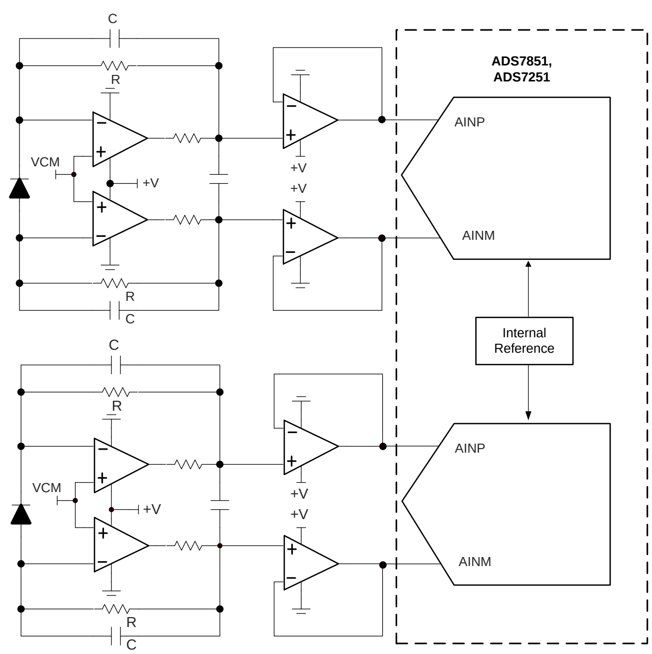
ADS7251 和 ADS7851 属于引脚兼容、双路、高速、同步采样模数转换器 (ADC) 产品系列，此系列产品支持全差分模拟输入，并且特有 2 个单独的内部电压基准。 ADS7251 提供 12 位分辨率以及高达 2MSPS 的采样速度。 ADS7851 提供 14 位分辨率以及高达 1.5MSPS 的采样速度。

此器件支持宽数字电源电压范围，从而通过一个简单串口轻松实现与多种数字主机控制器的通信。 两个器件都在扩展工业用温度范围（-40°C 至 +125°C）内完全额定运行，并且采用引脚兼容、节省空间的 WQFN-16 (3mm x 3mm) 封装。

器件信息

订货编号	封装	封装尺寸
ADS7251RTE	WQFN (16)	3mm x 3mm
ADS7851RTE	WQFN (16)	3mm x 3mm

典型应用图



目录

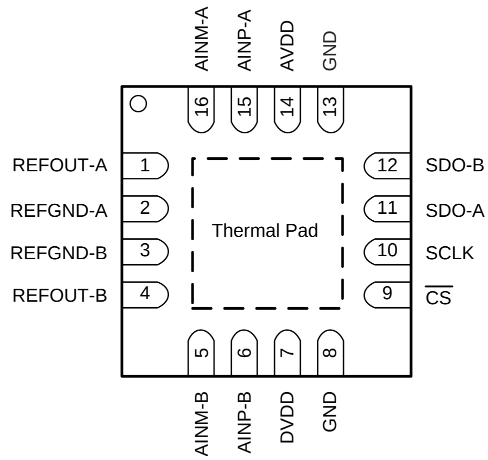
4 修订历史记录

Changes from Original (January 2014) to Revision A **Page**

- 已将格式更改为最新的数据表标准；已添加 *电路板布局* 部分，已移动现有部分 1
- Deleted Ordering Information table 3
- Changed Supply Current, I_{DVDD} parameter typical specification in Electrical Characteristics: ADS7251 table 5
- Changed Supply Current, I_{DVDD} parameter typical specification in Electrical Characteristics: ADS7851 table 6
- Changed *Input Voltage* column in Table 1 20

5 Terminal Configuration and Functions

RTE Package
WQFN-16
(Top View)



Terminal Descriptions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AINM-A	16	Analog input	Negative analog input, channel A
AINP-A	15	Analog input	Positive analog input, channel A
AINM-B	5	Analog input	Negative analog input, channel B
AINP-B	6	Analog input	Positive analog input, channel B
AVDD	14	Supply	ADC supply voltage
$\overline{CS}$	9	Digital input	Chip-select signal; active low
DVDD	7	Supply	Digital I/O supply
GND	8, 13	Supply	Digital ground
REFGND-A	2	Supply	Reference ground potential, channel A
REFGND-B	3	Supply	Reference ground potential, channel B
REFOUT-A	1	Analog output	Reference voltage output, REF_A
REFOUT-B	4	Analog output	Reference voltage output, REF_B
SCLK	10	Digital input	Serial communication clock
SDO-A	11	Digital output	Data output for serial communication, channel A
SDO-B	12	Digital output	Data output for serial communication, channel B
Thermal pad		Supply	Exposed thermal pad. TI recommends connecting this pin to the printed circuit board (PCB) ground.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	AVDD to GND	–0.3	+7	V
	DVDD to GND	–0.3	+7	V
Analog input voltage	AINP_x to REFGND_x	REFGND_x – 0.3	AVDD + 0.3	V
	AINM_x to REFGND_x	REFGND_x – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, SCLK to GND	GND – 0.3	DVDD + 0.3	V
Ground voltage difference	| REFGND_x – GND |		0.3	V
Input current	Any pin except supply pins		±10	mA
Maximum virtual junction temperature, T_J			+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	+150	°C
V_{ESD} (1), all pins	Human body model (HBM) ESD stress voltage(2), JEDEC standard 22, test method A114-C.01		±2000	V
	Charged device model (CDM) ESD stress voltage(3), JEDEC standard 22, test method C101		±500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that ±2000-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that ±500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage		5		V
DVDD	Digital supply voltage		3.3		V

6.4 Thermal Information

THERMAL METRIC(1)		ADS7251, ADS7851 RTE (WQFN) 16 TERMINALS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: ADS7251

All minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 5 V, V_{REF_A} = V_{REF_B} = 2.5 V, and f_{DATA} = 2 MSPS, unless otherwise noted. Typical values are at T_A = +25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution		12			Bits
SAMPLING DYNAMICS						
t_{CONV}	Conversion time				t_{SU_CSCK} + 12 t_{CLK}	ns
t_{ACQ}	Acquisition time		75			ns
f_{DATA}	Data rate				2	MSPS
f_{CLK}	Clock frequency				32	MHz
DC ACCURACY						
NMC	No missing codes		12			Bits
DNL	Differential nonlinearity		–0.99	±0.3	1	LSB
INL	Integral nonlinearity		–1	±0.5	1	LSB
V_{OS}	Input offset error		–1	±0.2	1	mV
	V_{OS} match	ADC_A to ADC_B	–1	±0.2	1	mV
dV_{OS}/dT	Input offset thermal drift			4		µV/°C
G_E	Gain error	Referenced to the voltage at REFOUT_x	–0.1%	±0.05%	0.1%	
	G_{ERR} match	ADC_A to ADC_B	–0.1%	±0.05%	0.1%	
G_E/dT	Gain error thermal drift	Referenced to the voltage at REFOUT_x		1		ppm/°C
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		72		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	For 20-kHz input frequency, at –0.5 dBFS	72.7	72.9		dB
SNR	Signal-to-noise ratio		72.8	73		dB
THD	Total harmonic distortion			–90		dB
SFDR	Spurious-free dynamic range			90		dB
	Isolation between ADC_A and ADC_B	f_{IN} = 15 kHz, f_{NOISE} = 25 kHz		–105		dB
SUPPLY CURRENT						
$I_{AVDD-DYNAMIC}$	Supply current: Analog, during conversion	Throughput = 2 MSPS, AVDD = 5 V		11	12	mA
$I_{AVDD-STATIC}$	Supply current: Analog, static			5.5		mA
I_{DVDD}	Supply current: Digital, for code 800			0.15		mA
POWER DISSIPATION						
$P_{D-ACTIVE}$	Power dissipation: During conversion	Throughput = 2 MSPS, AVDD = 5 V		55	60	mW
$P_{D-STATIC}$	Power dissipation: Static mode			27.5		mW

6.6 Electrical Characteristics: ADS7851

All minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 5 V, V_{REF_A} = V_{REF_B} = 2.5 V, and f_{DATA} = 1.5 MSPS, unless otherwise noted. Typical values are at T_A = +25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION							
	Resolution			14			Bits
SAMPLING DYNAMICS							
t_{CONV}	Conversion time					t_{SU_CSCK} + 14 t_{CLK}	ns
t_{ACQ}	Acquisition time			90			ns
f_{DATA}	Data rate					1500	kSPS
f_{CLK}	Clock frequency					27	MHz
DC ACCURACY							
NMC	No missing codes			13			Bits
DNL	Differential nonlinearity			–1	±0.75	2	LSB
INL	Integral nonlinearity			–2	±1	2	LSB
V_{OS}	Input offset error			–1	±0.2	1	mV
	V_{OS} match		ADC_A to ADC_B	–1	±0.2	1	mV
dV_{OS}/dT	Input offset thermal drift				1		µV/°C
G_E	Gain error		Referenced to the voltage at REFOUT_x	–0.1%	±0.05%	0.1%	
	G_{ERR} match		ADC_A to ADC_B	–0.1%	±0.05%	0.1%	
G_E/dT	Gain error thermal drift		Referenced to the voltage at REFOUT_x		1		ppm/°C
CMRR	Common-mode rejection ratio		Both ADCs, dc to 20 kHz		72		dB
AC ACCURACY							
SINAD	Signal-to-noise + distortion		For 20-kHz input frequency, at –0.5 dBFS	81.4	82.6		dB
SNR	Signal-to-noise ratio		For 20-kHz input frequency, at –0.5 dBFS	82	83.5		dB
THD	Total harmonic distortion		For 20-kHz input frequency, at –0.5 dBFS		–90		dB
SFDR	Spurious-free dynamic range		For 20-kHz input frequency, at –0.5 dBFS		90		dB
	Isolation between ADC_A and ADC_B		f_{IN} = 15 kHz, f_{NOISE} = 25 kHz		–120		dB
SUPPLY CURRENT							
$I_{AVDD-DYNAMIC}$	Supply current	Analog, during conversion	Throughput = 1.5 MSPS, AVDD = 5 V		10	12	mA
$I_{AVDD-STATIC}$	Supply current	Analog, static			5.5		mA
I_{DVDD}	Supply current	Digital, for code 2000			0.15		mA
POWER DISSIPATION							
$P_{D-ACTIVE}$	Power dissipation	During conversion	Throughput = 1.5 MSPS, AVDD = 5 V		50	60	mW
$P_{D-STATIC}$	Power dissipation	Static mode			27.5		mW

6.7 Electrical Characteristics: Common

All minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 5 V, V_{REF_A} = V_{REF_B} = 2.5 V, and f_{DATA} = 2 MSPS, unless otherwise noted. Typical values are at T_A = +25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
FSR	Full-scale input range (AINP_x – AINM_x)		For AVDD ≥ 5 V	–2 V_{REF}		2 V_{REF}	V
			For AVDD < 5 V	–AVDD		AVDD	V
V_{IN}	Absolute input voltage (AINP_x or AIM_x to REFGND_x)		For AVDD ≥ 5 V	0		2 V_{REF}	V
			For AVDD < 5 V	0		AVDD	V
V_{CM}	Input common-mode voltage range		V_{REF_A} = V_{REF_B} = V_{REF}	V_{REF} – 0.1	V_{REF}	V_{REF} + 0.1	V
C_{IN}	Input capacitance		In sample mode		40		pF
			In hold mode		4		pF
SAMPLING DYNAMICS							
t_A	Aperture delay				8		ns
	t_A match		ADC_A to ADC_B		40		ps
BW	Full-power bandwidth	At 3 dB			25		MHz
		At 0.1 dB			5		MHz
INTERNAL VOLTAGE REFERENCE							
V_{REFOUT}	Internal reference output voltage		At +25°C	2.495	2.500	2.505	V
$V_{REFOUT\text{-}match}$	V_{REFOUT} matching		| REFOUT_A – REFOUT_B |		±1		mV
dV_{REFOUT}/dt	Long-term voltage drift		1000 hours		150		ppm
dV_{REFOUT}/dT	Reference voltage drift with temperature				±10		ppm/°C
R_O	Internal reference output impedance				1		Ω
C_{OUT}	External output capacitor				22		µF
	Internal reference output settling time		C_{OUT} = 22 µF		10		ms
DIGITAL INPUTS(1)							
V_{IH}	Input voltage, high			0.7 DVDD		DVDD + 0.3	V
V_{IL}	Input voltage, low			–0.3		0.3 DVDD	V
C_{IN}	Input capacitance				5		pF
I_{IN}	Input leakage current		0 ≤ $V_{digital\text{-}input}$ ≤ DVDD		±0.1	1	µA
DIGITAL OUTPUTS(1)							
V_{OH}	Output voltage, high		I_{OH} = 500-µA source	0.8 DVDD		DVDD	V
V_{OL}	Output voltage, low		I_{OH} = 500-µA sink	0		0.2 DVDD	V
POWER SUPPLY							
AVDD	Supply voltage	Analog (AVDD to GND)		4.75(2)	5.0	5.25	V
DVDD		Digital (DVDD to GND)	Operational range	1.65	3.3	5.25	V
			For specified performance	1.65	3	3.6	V
TEMPERATURE RANGE							
T_A	Operating free-air temperature			–40		+125	°C

(1) Specified by design; not production tested.
(2) The AVDD supply voltage defines the permissible voltage swing on the analog input pins. Refer to the *Power Supply Recommendations* section for more details.

6.8 ADS7251 Timing Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{THROUGHPUT}$	Throughput		f_{CLK} = max			2000	kSPS
f_{CLK}	CLOCK frequency		$f_{THROUGHPUT}$ = max			32	MHz
t_{CLK}	CLOCK period		$f_{THROUGHPUT}$ = max	31.25			ns
t_{PH_CK}	CLOCK high time			0.45		0.55	t_{CLK}
t_{PL_CK}	CLOCK low time			0.45		0.55	t_{CLK}
t_{CONV}	Conversion time					t_{SU_CSCK} + 12 t_{CLK}	ns
t_{ACQ}	Acquisition time		f_{CLK} = max	75			ns
t_{PH_CS}	$\overline{CS}$ high time			30			ns
t_{D_CKDO}	Delay time	SCLK rising edge to (next) data valid				15	ns
t_{DV_CSDO}		$\overline{CS}$ falling to data enable				10	ns
t_{D_CKCS}		Last SCLK rising to $\overline{CS}$ rising		5			ns
t_{DZ_CSDO}		$\overline{CS}$ rising to DOUT going to 3-state				10	ns
t_{SU_CSCK}	Setup time	$\overline{CS}$ falling to SCLK falling		15			ns

Figure 1 shows the details of the serial interface between the ADS7251 and the digital host controller.

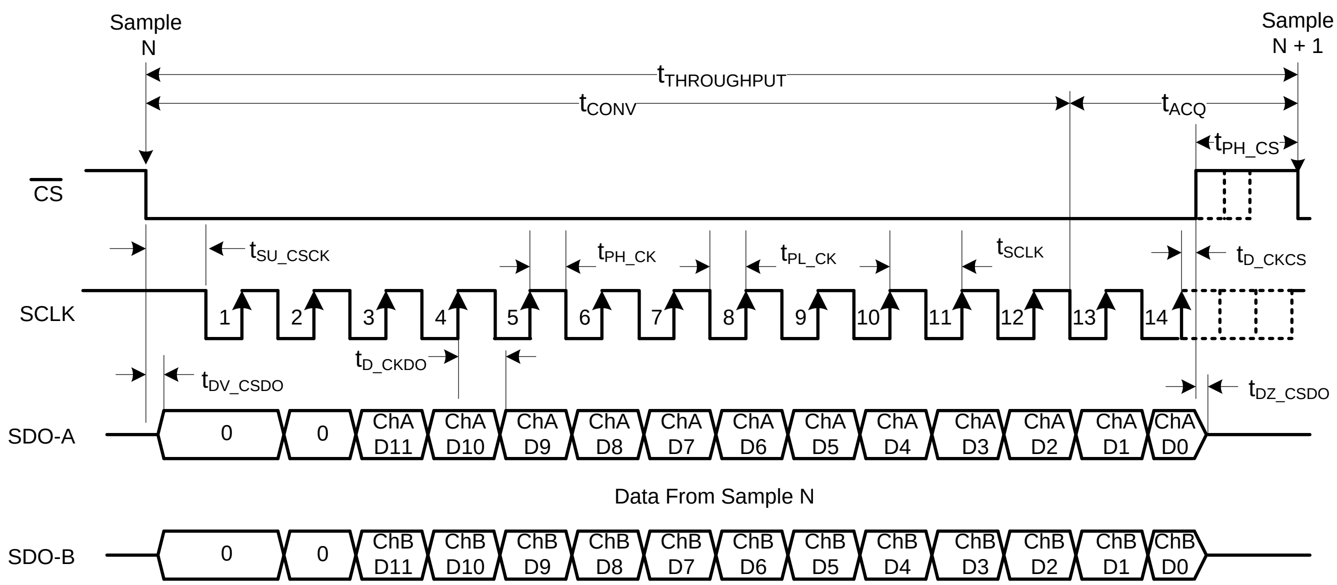


Figure 1. ADS7251 Serial Interface Timing Diagram

6.9 ADS7851 Timing Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{THROUGHPUT}$	Sample taken to data read		f_{CLK} = max			1500	kSPS
f_{CLK}	CLOCK frequency		$f_{THROUGHPUT}$ = max			27	MHz
t_{CLK}	CLOCK period		$f_{THROUGHPUT}$ = max	37			ns
t_{PH_CK}	CLOCK high time			0.45		0.55	t_{CLK}
t_{PL_CK}	CLOCK low time			0.45		0.55	t_{CLK}
t_{CONV}	Conversion time					t_{SU_CSCK} + 14 t_{CLK}	ns
t_{ACQ}	Acquisition time		f_{CLK} = max	90			ns
t_{PH_CS}	$\overline{CS}$ high time			30			ns
t_{D_CKDO}	Delay time	SCLK rising edge to (next) data valid				15	ns
t_{DV_CSDO}	Delay time	$\overline{CS}$ falling to data enable				10	ns
t_{D_CKCS}	Delay time	Last SCLK rising to $\overline{CS}$ rising		5			ns
t_{DZ_CSDO}	Delay time	$\overline{CS}$ rising to DOUT going to 3-state				10	ns
t_{SU_CSCK}	Setup time	$\overline{CS}$ falling to SCLK falling		15			ns

Figure 2 shows the details of the serial interface between the ADS7851 and the digital host controller.

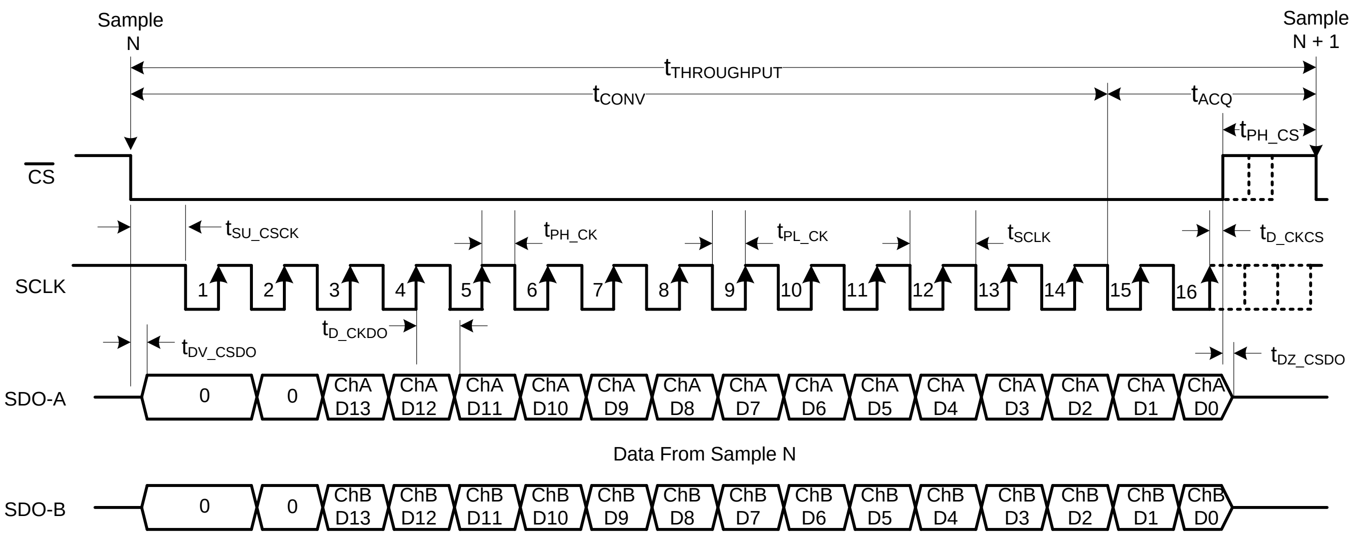
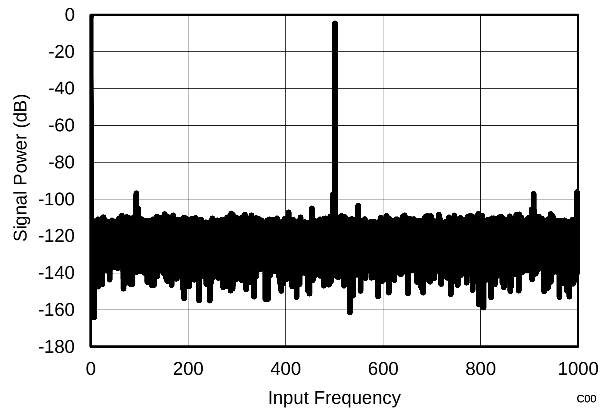


Figure 2. ADS7851 Serial Interface Timing Diagram

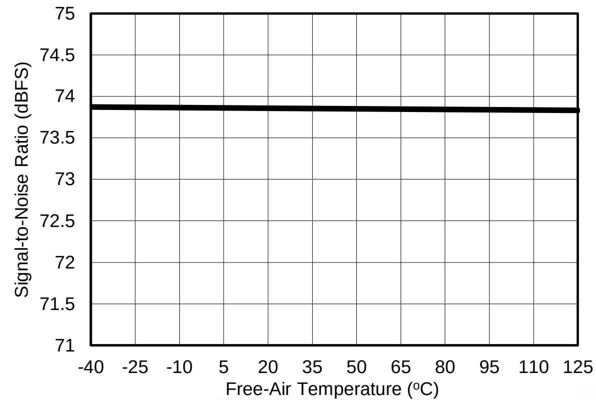
6.10 Typical Characteristics: ADS7251

At T_A = +25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1 MSPS, unless otherwise noted.



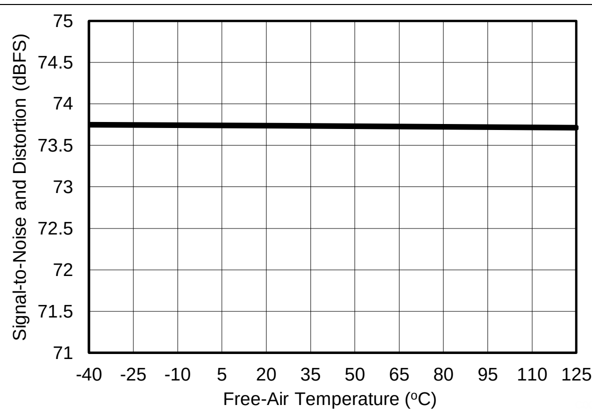
f_{IN} = 500 kHz

Figure 3. Typical FFT for 500-kHz Input



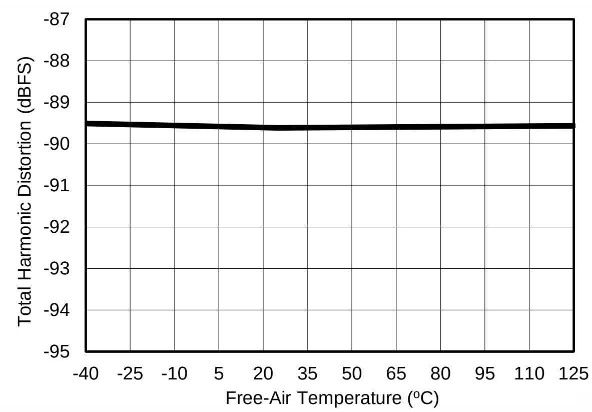
f_{IN} = 10 kHz

Figure 4. SNR vs Device Temperature



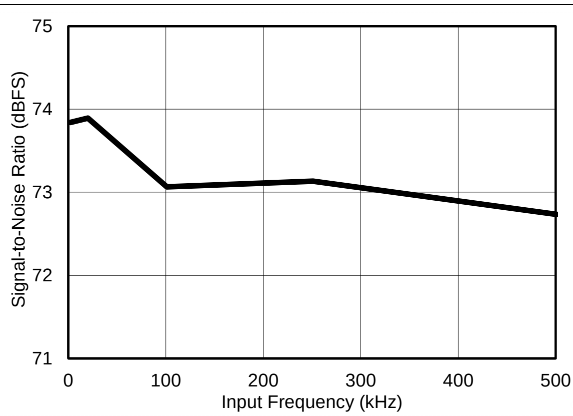
f_{IN} = 10 kHz

Figure 5. SINAD vs Device Temperature



f_{IN} = 10 kHz

Figure 6. THD vs Device Temperature



f_{IN} = 10 kHz

Figure 7. SNR vs Input Frequency

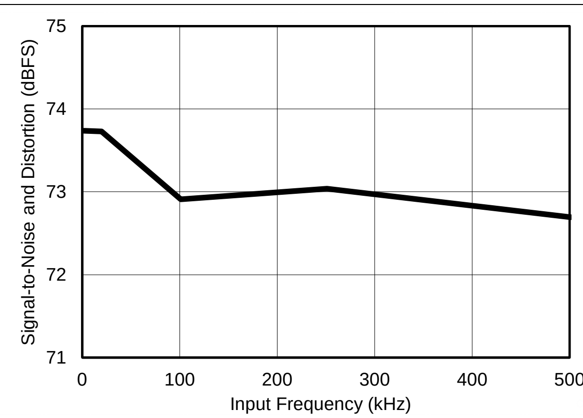


Figure 8. SINAD vs Input Frequency

Typical Characteristics: ADS7251 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1 MSPS, unless otherwise noted.

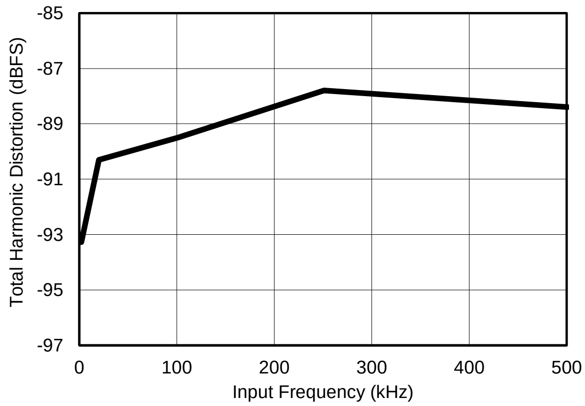


Figure 9. THD vs Input Frequency

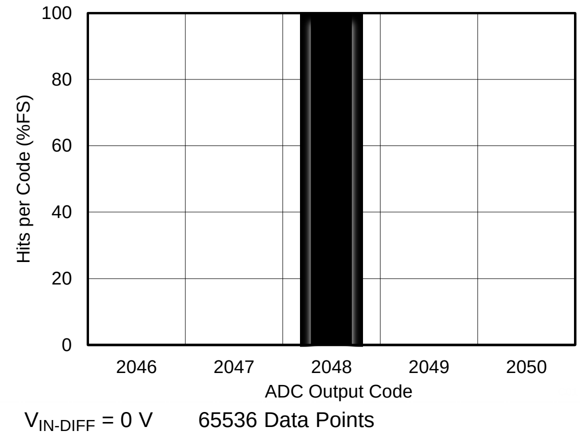


Figure 10. DC Histogram

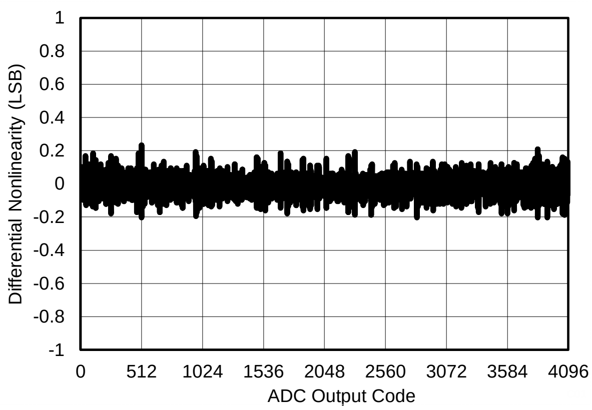


Figure 11. Typical DNL

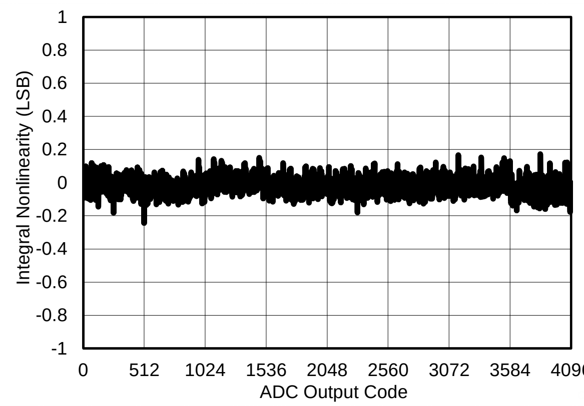


Figure 12. Typical INL

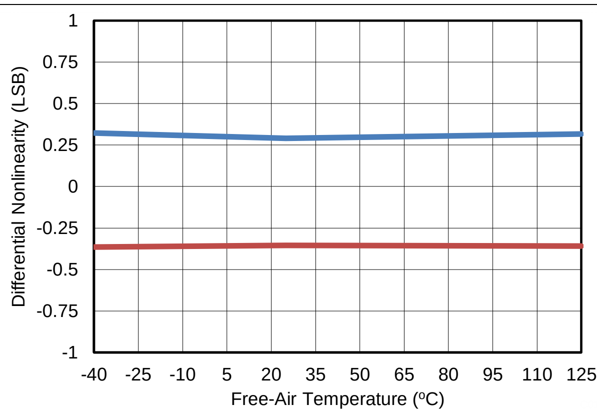


Figure 13. DNL vs Device Temperature

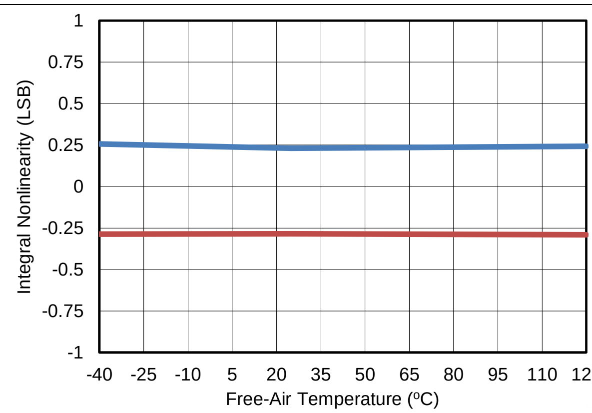


Figure 14. INL vs Device Temperature

Typical Characteristics: ADS7251 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1 MSPS, unless otherwise noted.

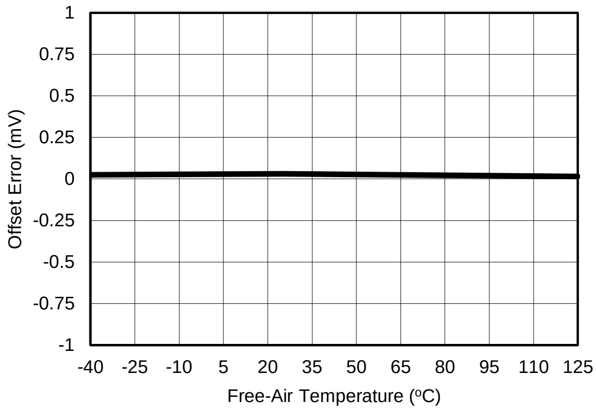


Figure 15. Offset Error vs Device Temperature

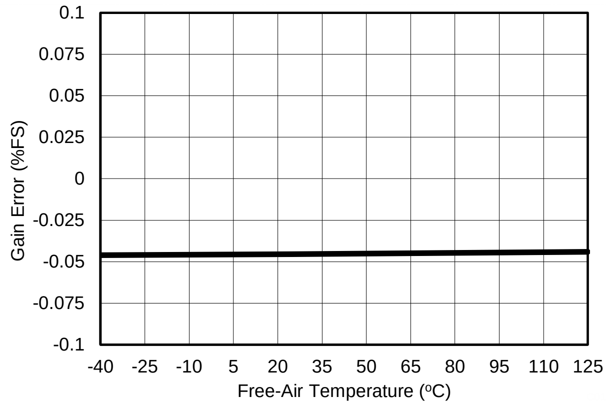


Figure 16. Gain Error vs Device Temperature

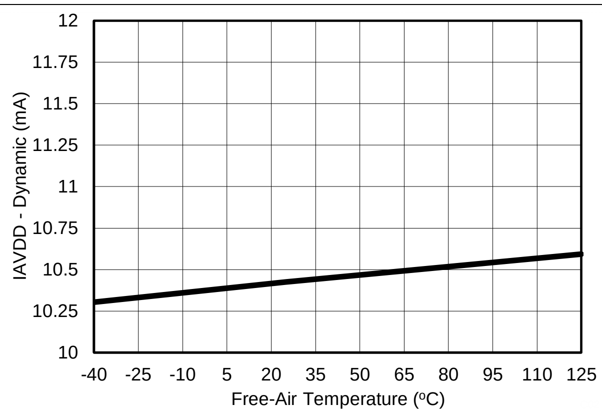


Figure 17. I_{AVDD} vs Device Temperature

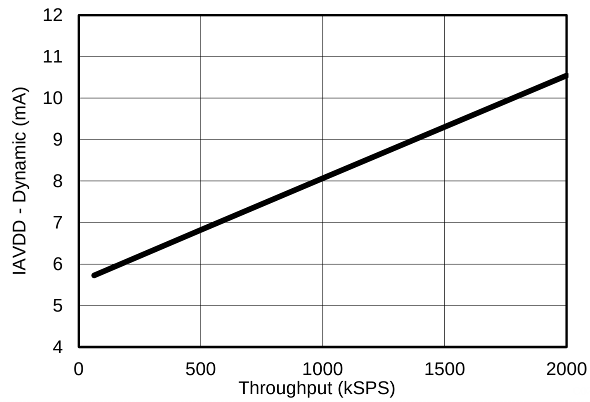
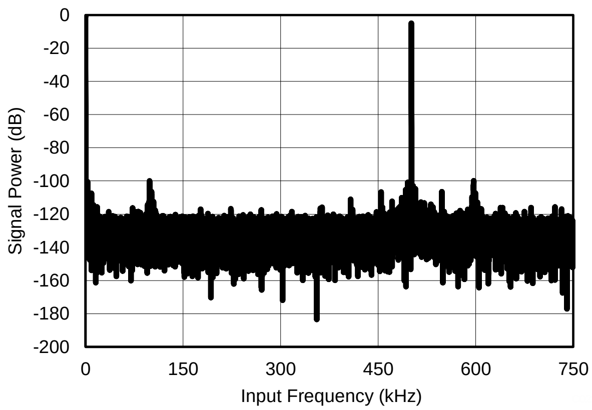


Figure 18. I_{AVDD} vs Throughput

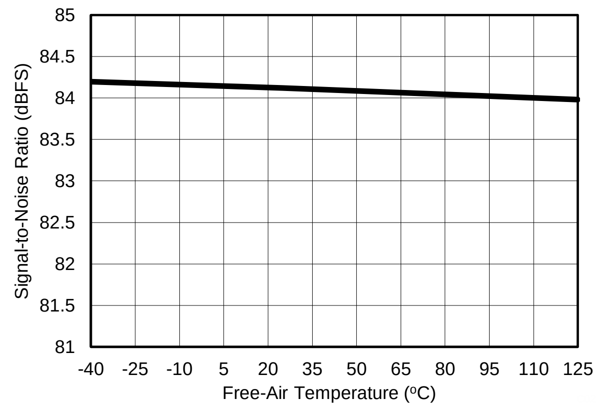
6.11 Typical Characteristics: ADS7851

At T_A = +25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1 MSPS, unless otherwise noted.



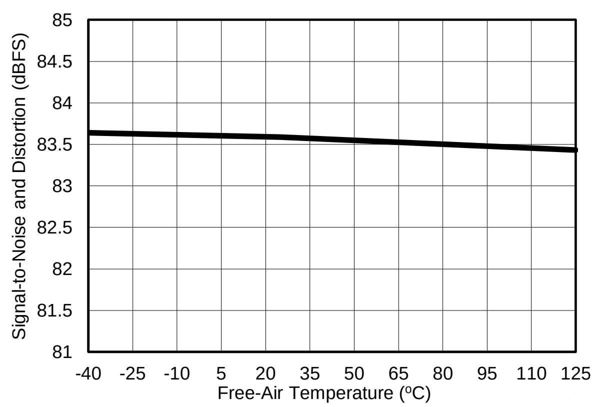
f_{IN} = 500 kHz

Figure 19. Typical FFT for 500-kHz Input



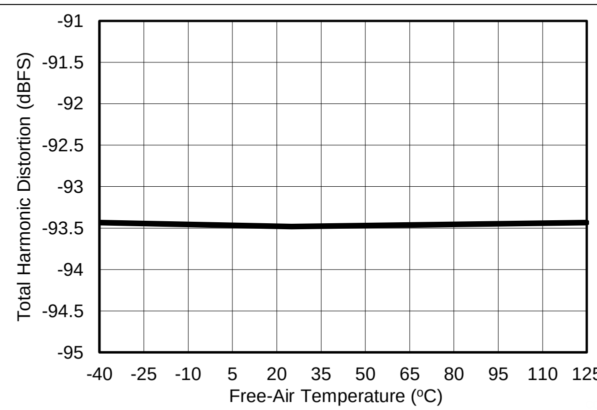
f_{IN} = 10 kHz

Figure 20. SNR vs Device Temperature



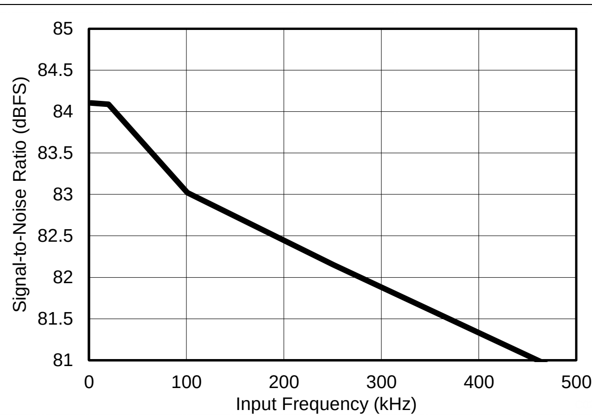
f_{IN} = 10 kHz

Figure 21. SINAD vs Device Temperature



f_{IN} = 10 kHz

Figure 22. THD vs Device Temperature



f_{IN} = 10 kHz

Figure 23. SNR vs Input Frequency

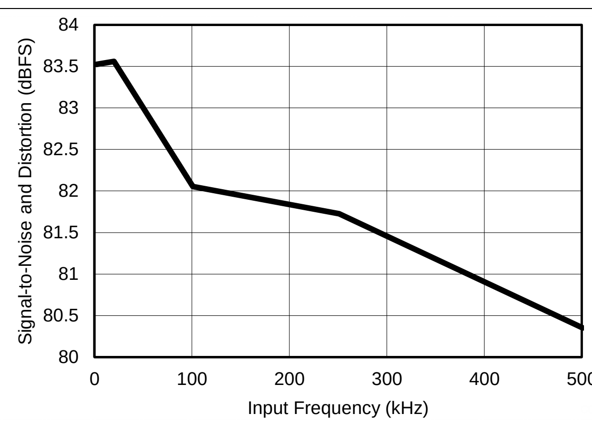


Figure 24. SINAD vs Input Frequency

Typical Characteristics: ADS7851 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1 MSPS, unless otherwise noted.

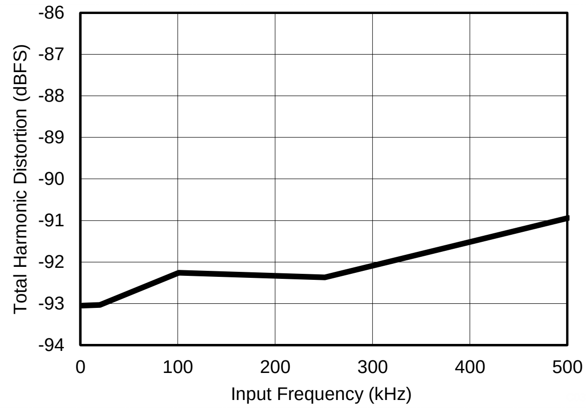


Figure 25. THD vs Input Frequency

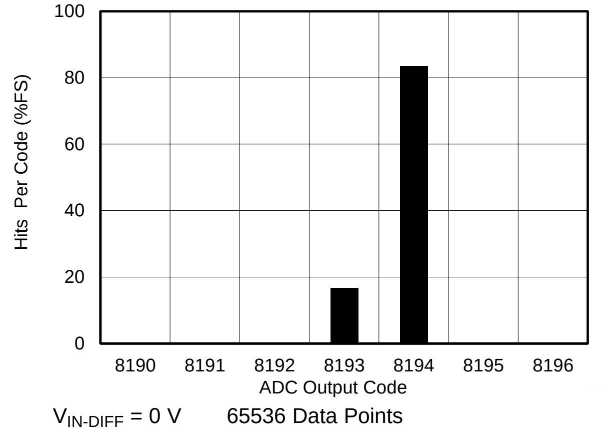


Figure 26. DC Histogram

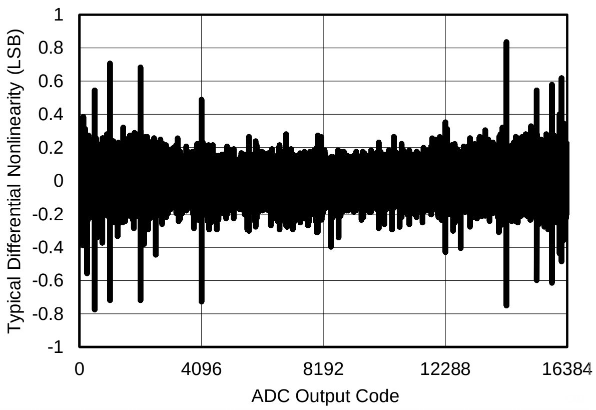


Figure 27. Typical DNL

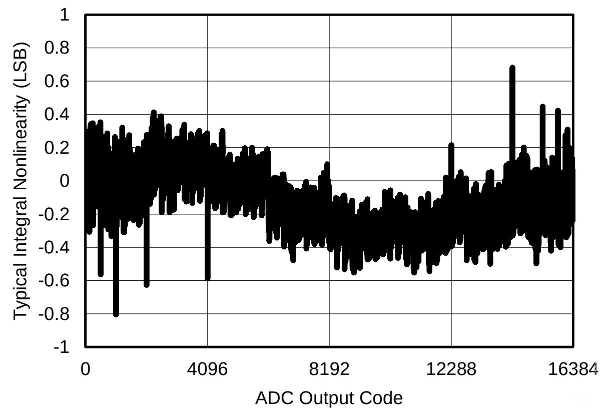


Figure 28. Typical INL

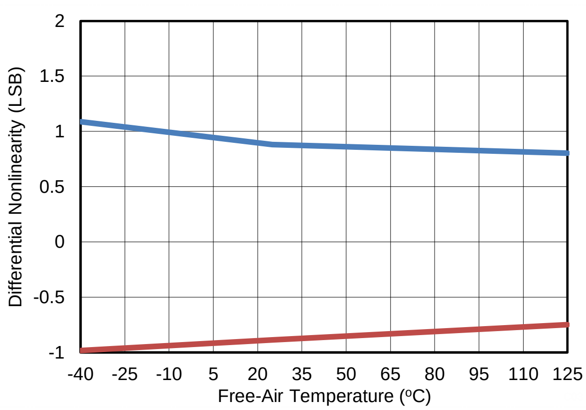


Figure 29. DNL vs Device Temperature

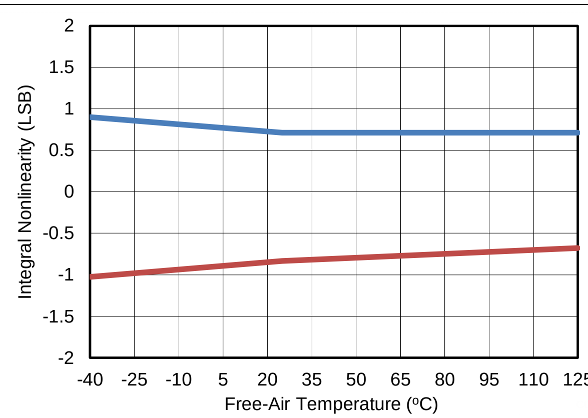


Figure 30. INL vs Device Temperature

Typical Characteristics: ADS7851 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1 MSPS, unless otherwise noted.

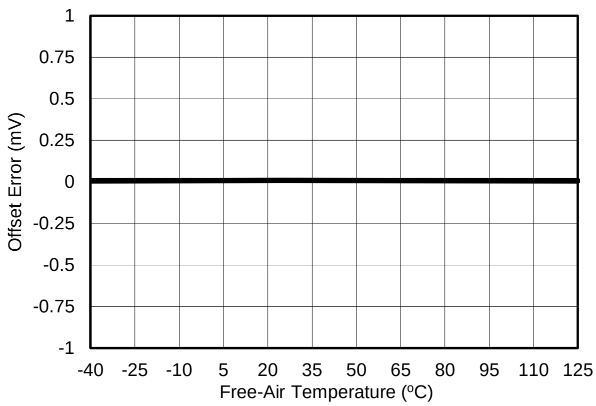


Figure 31. Offset Error vs Device Temperature

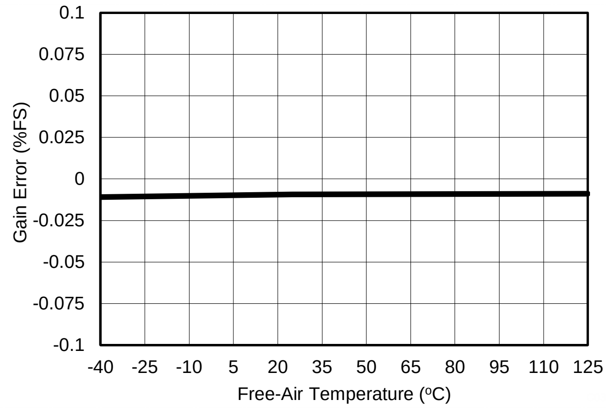


Figure 32. Gain Error vs Device Temperature

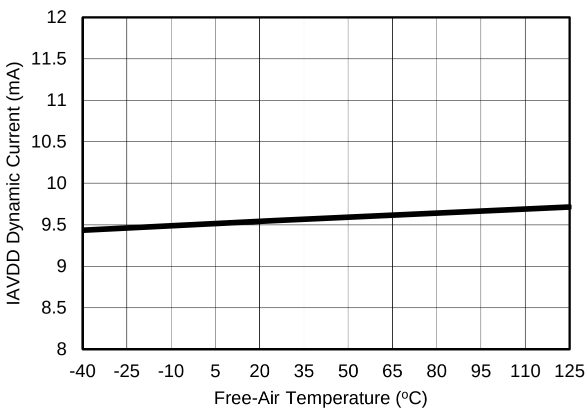


Figure 33. I_{AVDD} vs Device Temperature

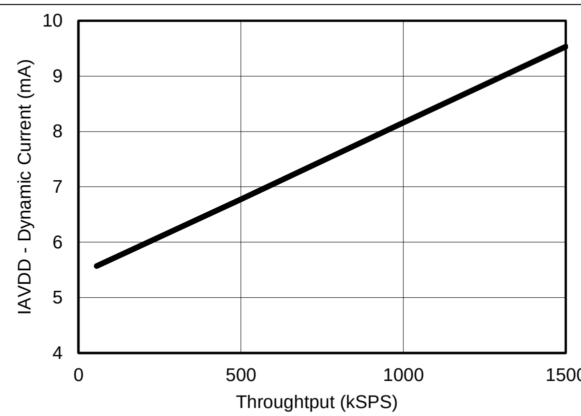


Figure 34. I_{AVDD} vs Throughput

6.12 Typical Characteristics: Common

At T_A = +25°C, AVDD = 5 V, DVDD = 3.3 V, and V_{REF} = 2.5 V (internal), unless otherwise noted.

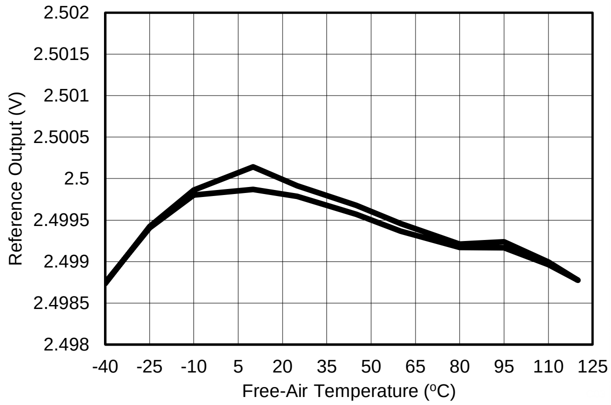
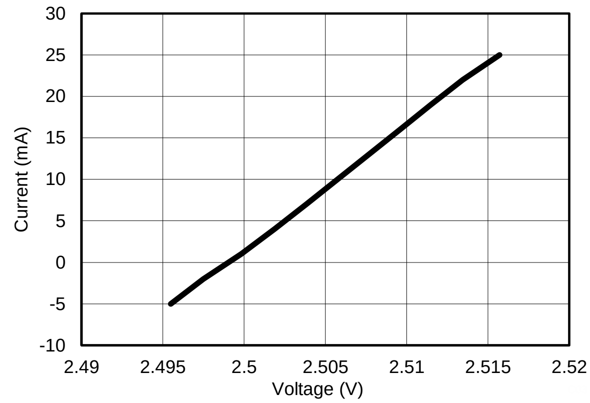


Figure 35. Reference Output vs Device Temperature



R_{out} = 0.75 Ω Typ

Figure 36. Internal Reference: Output Current vs Output Voltage

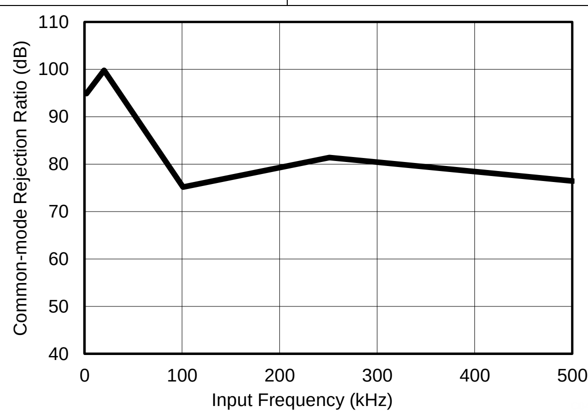


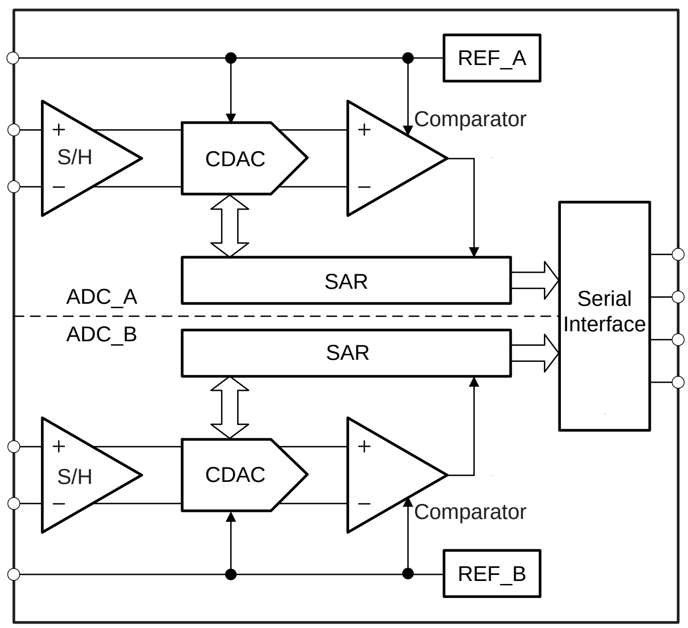
Figure 37. CMRR vs Input Frequency

7 Detailed Description

7.1 Overview

The ADS7251 and ADS7851 are pin-compatible, dual, simultaneous-sampling, analog-to-digital converters (ADCs). Each device features two independent internal voltage references and supports fully-differential input signals with the input common-mode on each input pin equal to the reference voltage. The full-scale input signal on each input pin is equal to twice the reference voltage. The devices provide a simple, serial interface to the host controller and operate over a wide range of digital power supplies.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference

The device has two simultaneous sampling ADCs (ADC_A and ADC_B) and two independent internal reference sources (INTREF_A and INTREF_B). INTREF_A outputs voltage V_{REF_A} on pin REFOUT_A and INTREF_B outputs voltage V_{REF_B} on pin REFOUT_B. As shown in Figure 38, the REFOUT_A and REFOUT_B pins must be decoupled with the REFGND_A and REFGND_B pins, respectively, with individual 22-µF decoupling capacitors. ADC_A operates with reference voltage V_{REF_A} and ADC_B operates with reference voltage V_{REF_B}.

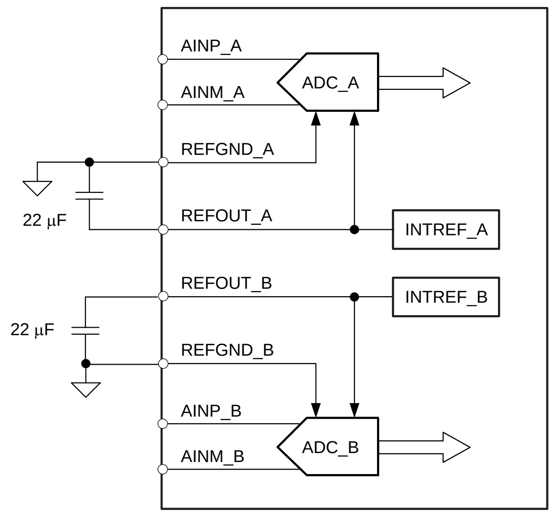


Figure 38. Reference Block Diagram

Feature Description (continued)

7.3.2 Analog Input

The devices support fully-differential analog input signals. These inputs are sampled and converted simultaneously by the two ADCs, ADC_A and ADC_B. Figure 39a and Figure 39b show equivalent circuits for the ADC_A and ADC_B analog input pins, respectively.

Series resistance (R_S) represents the on-state sampling switch resistance (typically 50 Ω) and C_{SAMPLE} is the device sampling capacitor (typically 40 pF). ADC_A samples V_{AINP_A} and V_{AINM_A} and converts for the difference voltage (V_{AINP_A} – V_{AINM_A}). ADC_B samples V_{AINP_B} and V_{AINM_B} and converts for the difference voltage (V_{AINP_B} – V_{AINM_B}).

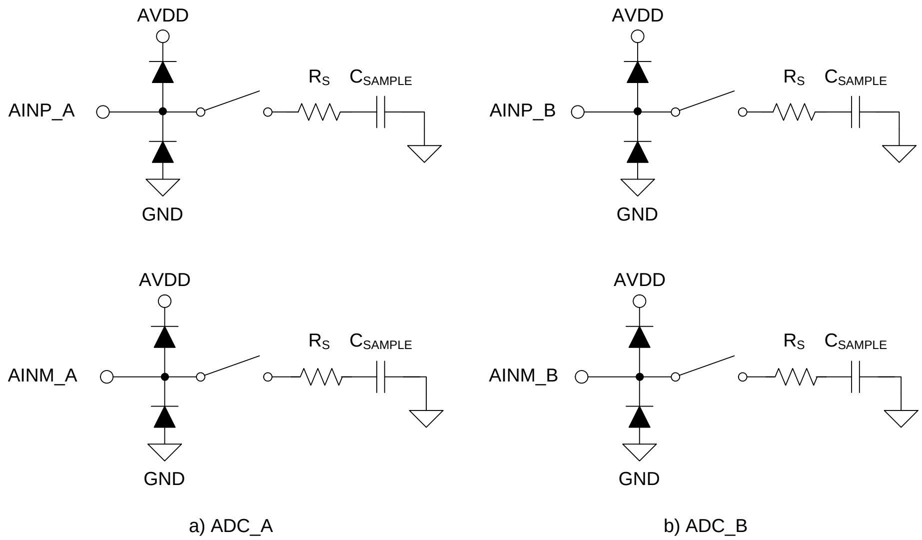


Figure 39. Equivalent Circuit for the Analog Input Pins

7.3.2.1 Analog Input Full-Scale Range

The analog input full-scale range (FSR) for ADC_A and ADC_B is twice the reference voltage provided to the particular ADC. Therefore, the FSR for ADC_A and ADC_B can be determined by Equation 1 and Equation 2, respectively:

$$FSR\_ADC\_A = 2 \times V_{REF\_A},\quad V_{AINP\_A} \text{ and } V_{AINM\_A} = 0 \text{ to } 2 \times V_{REF\_A}, \tag{1}$$

$$FSR\_ADC\_B = 2 \times V_{REF\_B},\quad V_{AINP\_B} \text{ and } V_{AINM\_B} = 0 \text{ to } 2 \times V_{REFIN\_B} \tag{2}$$

To use the full dynamic input range on the analog input pins, AVDD must be as shown in Equation 3, Equation 4, and Equation 5:

$$AVDD \geq 2 \times V_{REF\_A} \tag{3}$$

$$AVDD \geq 2 \times V_{REF\_B} \tag{4}$$

$$4.5\text{ V} \leq AVDD \leq 5.5\text{ V} \tag{5}$$

7.3.2.2 Common-Mode Voltage Range

For the analog input, the devices support a common-mode voltage equal to the reference voltage provided to the ADC. Therefore, the common-mode voltage for the ADC_A and ADC_B must be as shown in Equation 6 and Equation 7, respectively.

$$V_{CM\_A} = V_{REF\_A} \tag{6}$$

$$V_{CM\_B} = V_{REF\_B} \tag{7}$$

Feature Description (continued)

7.3.3 ADC Transfer Function

The device output is in twos compliment format. Device resolution for the fully-differential input can be computed by Equation 8:

$$1\ LSB = (4 \times V_{REF}) / (2^N) \quad (8)$$

where:

- $V_{REF} = V_{REF\_A} = V_{REF\_B}$, and
- N = 12 (ADS7251), or 14 (ADS7851).

Table 1 shows the different input voltages and the corresponding device output codes. Figure 40 shows the ideal transfer characteristics for the device.

Table 1. Transfer Characteristics

INPUT VOLTAGE (AINP_x – AINM_x)	OUTPUT CODE (Hex)		
	CODE	ADS7251	ADS7851
$< -2 \times V_{REF}$	NFSC	800	2000
$-2 \times V_{REF}$ + 1 LSB	NFSC + 1	801	2001
–1 LSB	MC	FFF	3FFF
0	PLC	000	0000
$> 2 \times V_{REF}$ – 1 LSB	PFSC	7FF	1FFF

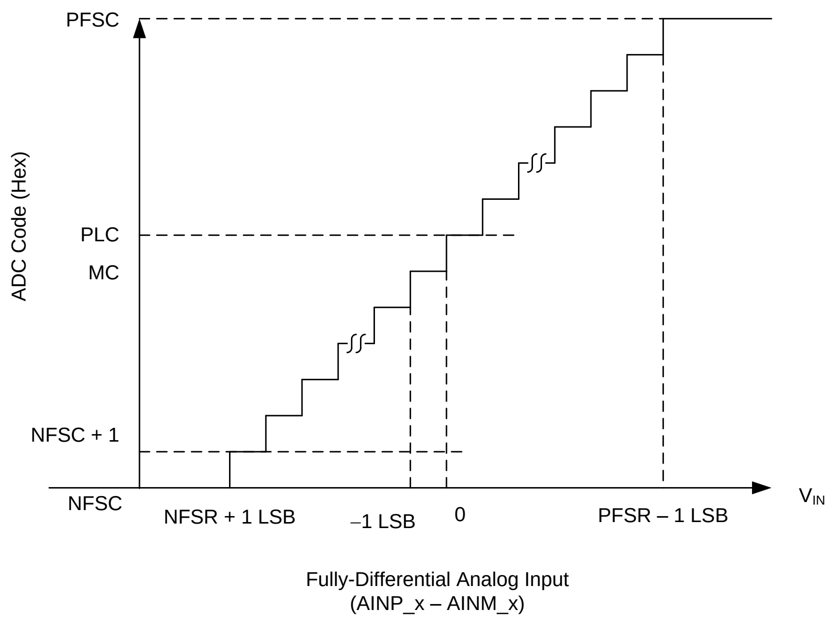


Figure 40. Ideal Transfer Characteristics

7.4 Device Functional Modes

7.4.1 Serial Interface

The devices support a simple, SPI-compatible interface to the external digital host. The CS signal defines one conversion and serial transfer frame. A frame starts with a CS falling edge and ends with a CS rising edge. The SDO_A and SDO_B pins output the ADC_A and ADC_B conversion results, respectively. Figure 41 shows a detailed timing diagram for the ADS7251.

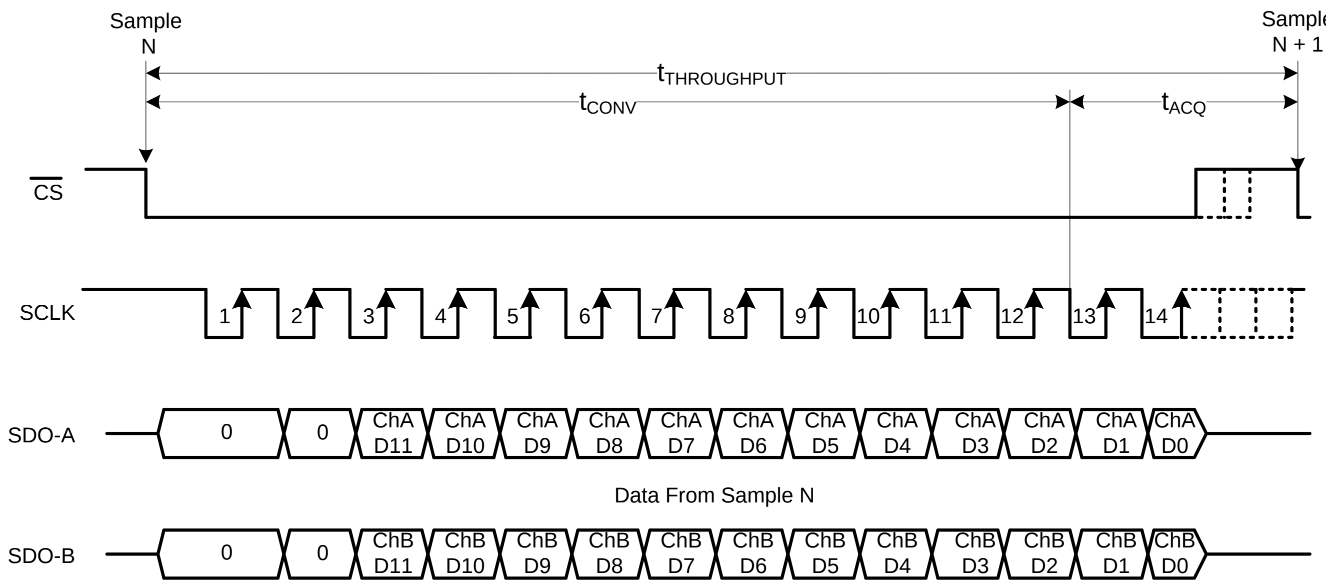


Figure 41. ADS7251 Serial Interface Timing Diagram

Figure 42 shows a detailed timing diagram for the ADS7851.

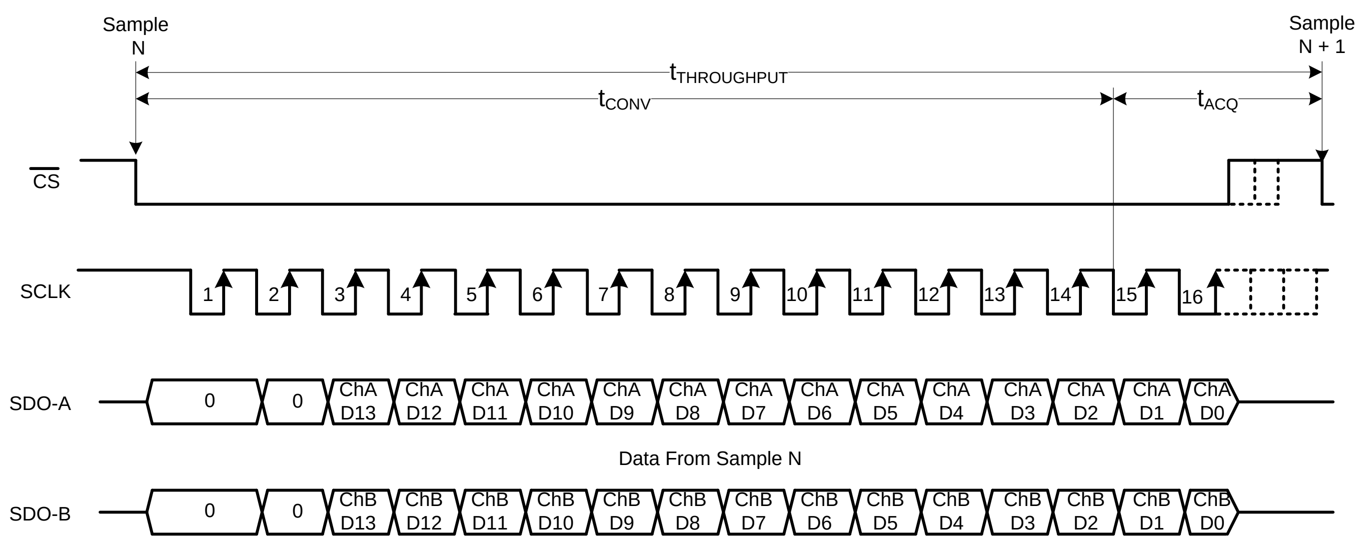


Figure 42. ADS7851 Serial Interface Timing Diagram

Device Functional Modes (continued)

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs '0' on the SDO_A and SDO_B pins. A minimum delay of t_{SU_CSCK} must elapse between the $\overline{CS}$ falling edge and the first SCLK falling edge. The subsequent clock edges are used to shift out the conversion result using the serial interface, as shown in Table 2. The sample-and-hold circuit returns to sample mode as soon as the conversion process is over. Any extra clock edges output a '0' on the SDO pins. A $\overline{CS}$ rising edge ends the frame and brings the serial data bus to 3-state.

Table 2. Data Launch Edge

DEVICE	PIN	LAUNCH EDGE									
			SCLK								$\overline{CS}$↑
		$\overline{CS}$↓	↓1	↓2	…	↓13	↓14	↓15	↓16	…	
ADS7851	SDO-A	0	0	D13_A	…	D2_A	D1_A	D0_A	0	…	Hi-Z
	SDO-B	0	0	D13_B	…	D2_B	D1_B	D0_B	0	…	Hi-Z
ADS7251	SDO-A	0	0	D11_A	…	D0_A	0	0	0	…	Hi-Z
	SDO-B	0	0	D11_B	…	D0_B	0	0	0	…	Hi-Z

7.4.2 Short-Cycling Feature

For the ADS7851, a minimum of 16 SCLK rising edges must be provided between the beginning and end of the frame to complete the 14-bit data transfer. For the ADS7251, a minimum of 14 SCLK rising edges must be provided between the beginning and end of the frame to complete the 12-bit data transfer. As shown in Figure 43, if $\overline{CS}$ is brought high before the expected number of SCLK rising edges are provided, the current frame is aborted and the device starts sampling the new analog input signal. However, the output data bits latched into the digital host before this $\overline{CS}$ rising edge are still valid data corresponding to sample *N*.

After aborting the current frame, $\overline{CS}$ must be kept high for t_{ACQ} to ensure minimum acquisition time is provided for the next conversion.

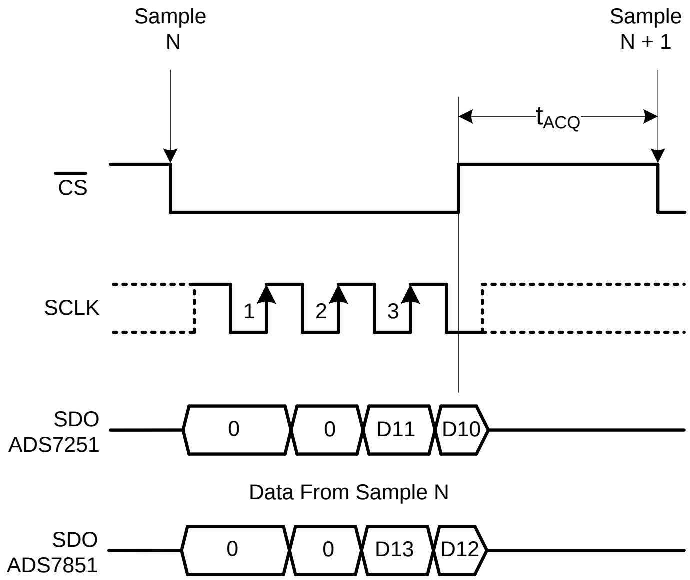


Figure 43. Short-Cycling Feature

8 Application and Implementation

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. The ADS7851 and ADS7251 feature an internal reference designed to support device requirements. This section details some general principles for designing the input driver circuit and provides some application circuits designed using these devices.

8.2 Typical Application

The application circuit shown in Figure 44 is optimized for using the ADS7251 at a 2-MSPS throughput to achieve lowest distortion and lowest noise for input signal frequencies up to 100 kHz.

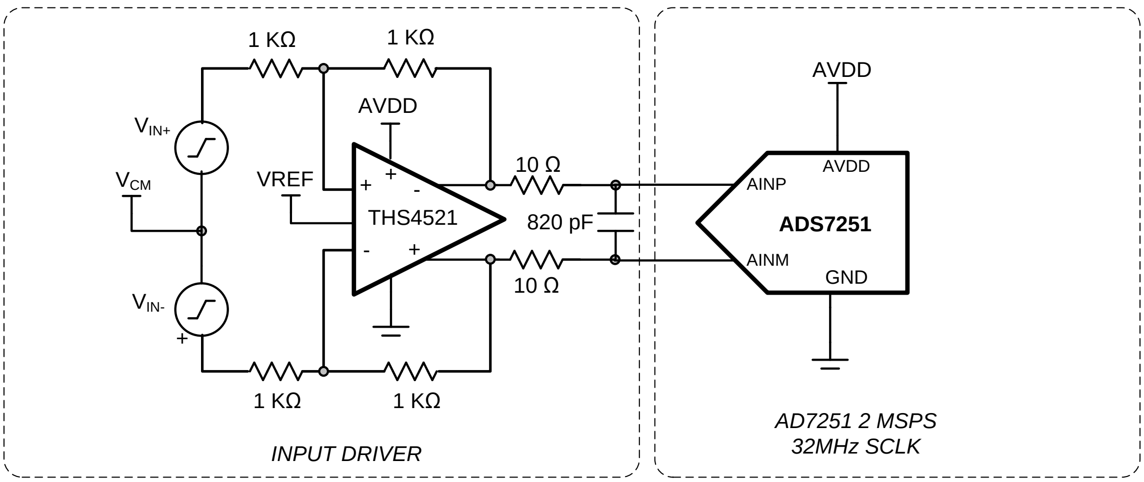


Figure 44. ADS7251 DAQ Circuit: Maximum SINAD for Input Signal Frequencies up to 100 kHz

The application circuit shown in Figure 45 is optimized for using the ADS7851 at a 1.5-MSPS throughput to achieve lowest distortion and lowest noise for input signal frequencies up to 100 kHz.

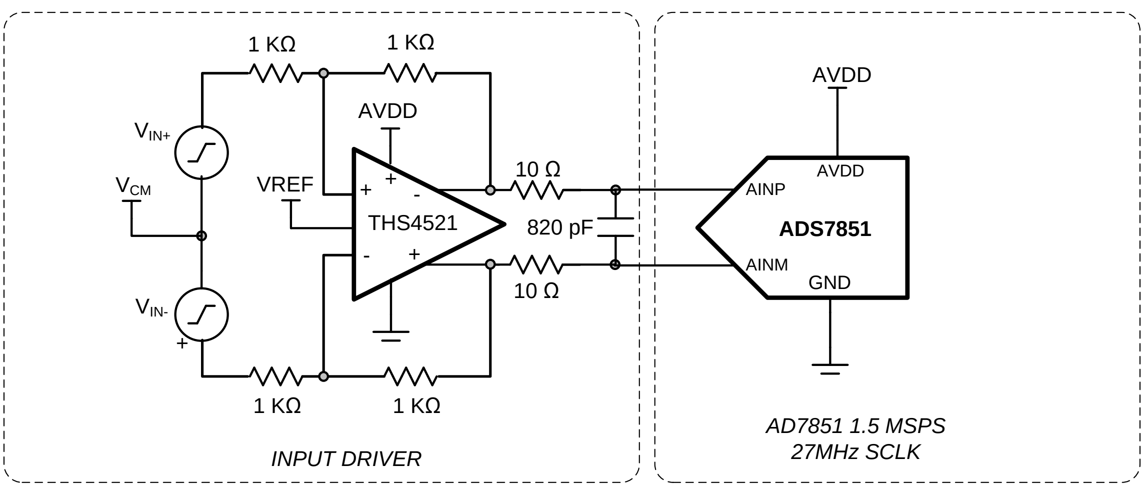


Figure 45. ADS7851 DAQ Circuit: Maximum SINAD for Input Signal Frequencies up to 100 kHz

Typical Application (continued)

8.2.1 Design Requirements

For the ADS7251, design an input driver and reference driver circuit to achieve > 71-dB SNR and < –90-dB THD at input frequencies of 10 kHz and 100 kHz.

For the ADS7851, design an input driver and reference driver circuit to achieve > 81-dB SNR and < –90-dB THD at input frequencies of 10 kHz and 100 kHz.

8.2.2 Detailed Design Procedure

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and an antialiasing filter. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

8.2.2.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in Equation 9:

$$\text{Unity} - \text{Gain Bandwidth} \geq 4 \times \left(\frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \tag{9}$$

- *Noise.* Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is bandlimited by designing a low cutoff frequency RC filter, as explained in Equation 10.

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20} \right)}$$

where:

- V_{1/f_AMP_PP} is the peak-to-peak flicker noise in μV_{RMS},
- e_{n_RMS} is the amplifier broadband noise density in nV/√Hz,
- f_{-3dB} is the 3-dB bandwidth of the RC filter, and
- N_G is the noise gain of the front-end circuit, which is equal to '1' in a buffer configuration. (10)

- *Distortion.* Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10 dB lower than the distortion of the ADC, as shown in Equation 11.

$$THD_{AMP} \leq THD_{ADC} - 10\ (dB) \tag{11}$$

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, the settling behavior of the input driver should always be verified by TINA™-SPICE simulations before selecting the amplifier.

Typical Application (continued)

The distortion resulting from variation in the common-mode signal is eliminated by using a fully-differential amplifier (FDA) in an inverting gain configuration that establishes a fixed common-mode level at the ADC input. This configuration also eliminates the requirement of rail-to-rail swing at the amplifier input. The low-power THS4521, used as an input driver, provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications. The device REFOUT_x pin can be directly connected to the V_{OCM} pin of the THS4521 to set the output common-mode voltage to 2.5 V, as required by the ADC.

8.2.2.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements (as shown in Figure 46). For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system.

Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected across the ADC inputs. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of C_{FLT} should be greater than 400 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For these devices, TI recommends limiting the value of R_{FLT} to a maximum of 22 Ω in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

$$f_{-3dB} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}}$$

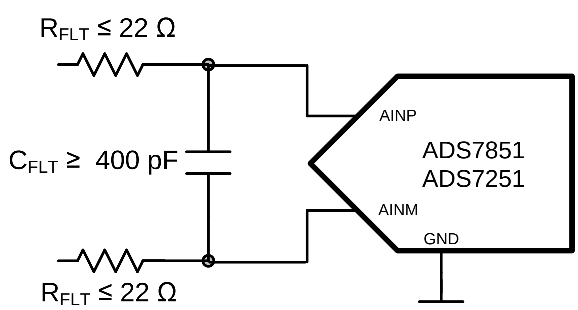


Figure 46. Antialiasing Filter

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22-Ω resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

Typical Application (continued)

8.2.3 Application Curves

Figure 47 shows an FFT plot for the ADS7251 with the circuit shown in Figure 44 and an input frequency of 10 kHz. Figure 48 shows an FFT plot for the ADS7251 with the same circuit configuration but for an input frequency of 100 kHz.

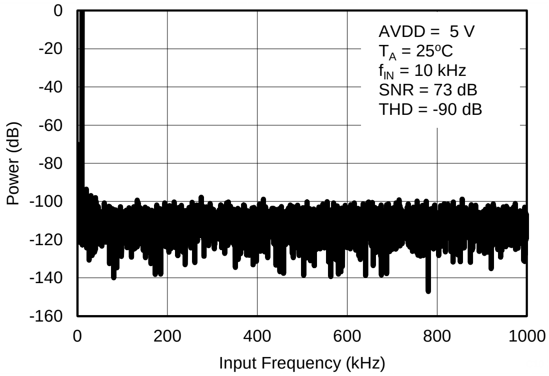


Figure 47. Test Results for ADS7251 with a 10-kHz Input

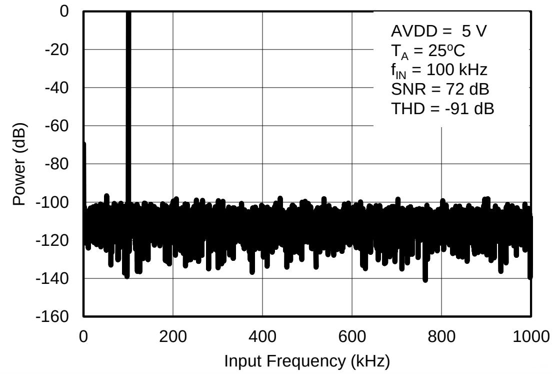


Figure 48. Test Results for ADS7251 with a 100-kHz Input

Figure 49 shows an FFT plot for the ADS7851 with the circuit shown in Figure 45 and an input frequency of 10 kHz. Figure 50 shows an FFT plot for the ADS7251 with the same circuit configuration but for an input frequency of 100 kHz.

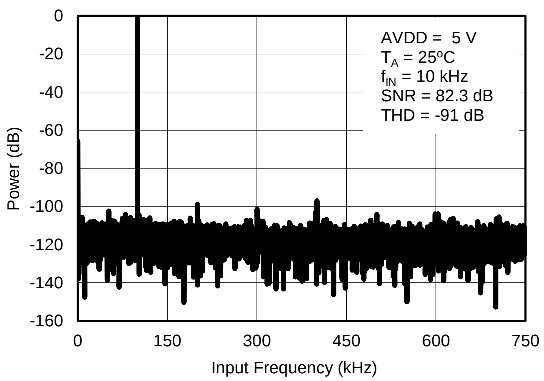


Figure 49. Test Results with a 10-kHz Input

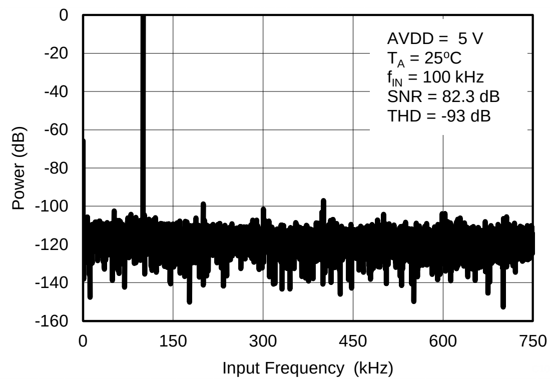


Figure 50. Test Results with a 100-kHz Input

9 Power Supply Recommendations

The devices have two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges.

The AVDD supply voltage value defines the permissible voltage swing on the analog input pins. To avoid saturation of output codes, and to use the full dynamic range on the analog input pins, AVDD must be set as shown in Equation 12, Equation 13, and Equation 14:

$$AVDD \geq 2 \times V_{REF\_A} \quad (12)$$

$$AVDD \geq 2 \times V_{REF\_B} \quad (13)$$

$$4.75\ V \leq AVDD \leq 5.25\ V \quad (14)$$

Decouple the AVDD and DVDD pins with the GND pin using individual 10-µF decoupling capacitors, as shown in Figure 51.

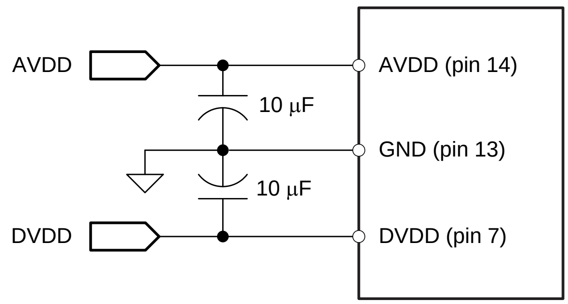


Figure 51. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

Figure 52 shows a board layout example for the ADS7251 and ADS7851. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 52, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the device must be clean and well-bypassed. Use 10-µF, ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths.

The REFOUT-A and REFOUT-B reference outputs are bypassed with 10-µF, X7R-grade ceramic capacitors (C_{REF-x}). Place the reference bypass capacitors as close as possible to the reference REFOUT-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFOUT-x pins and the bypass capacitors. Small 0.1-Ω to 0.2-Ω resistors (R_{REF-x}) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Figure 52 shows C_{IN-A} and C_{IN-B} filter capacitors placed across the analog input pins of the device.

10.2 Layout Example

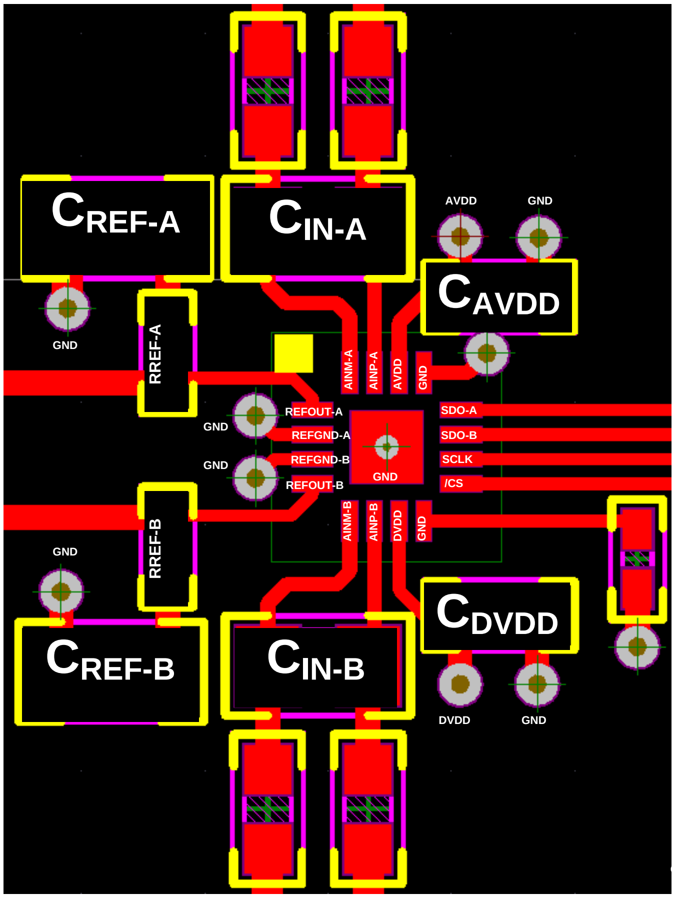


Figure 52. Example Layout for the ADS7251 and ADS7851

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- THS4521 数据表，SBOS458

11.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，以及样片与购买的快速访问。

Table 3. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ADS7251	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS7851	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 Trademarks

TINA is a trademark of Texas Instruments Inc..
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7251IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7251	Samples
ADS7251IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7251	Samples
ADS7851IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7851	Samples
ADS7851IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7851	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

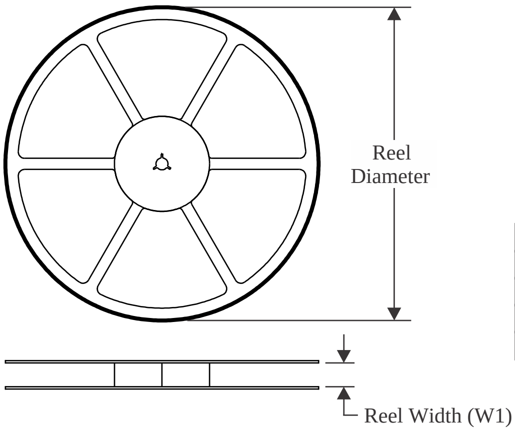
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

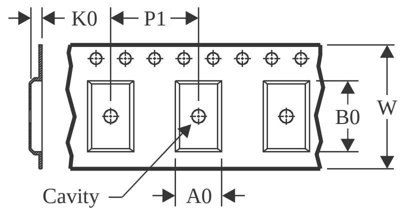
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

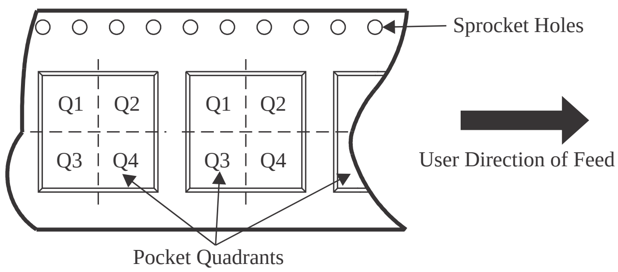


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

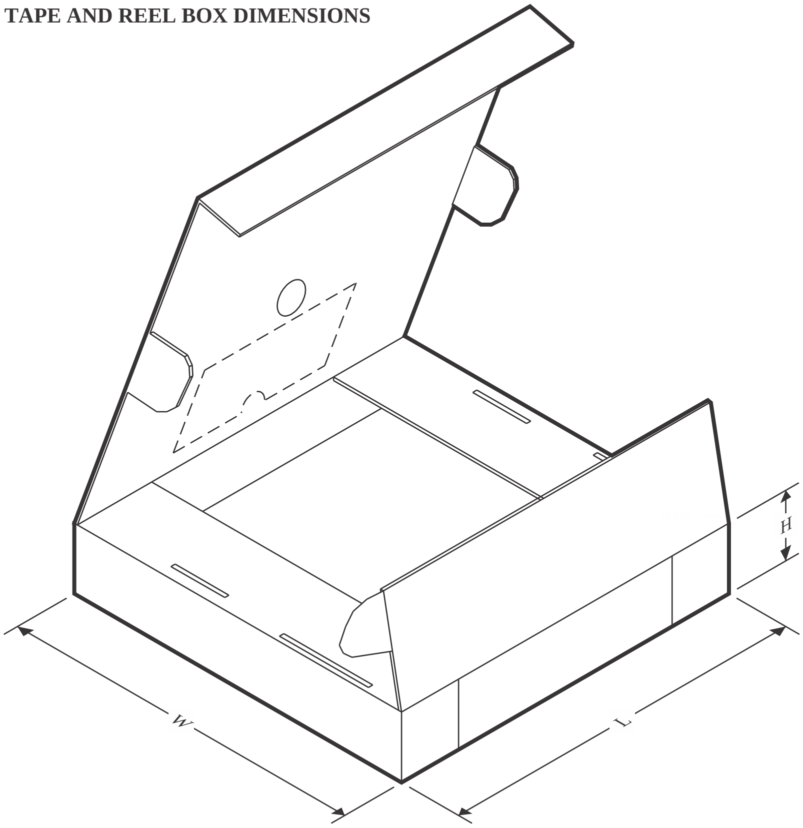
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7251IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7851IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7851IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7251IRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7851IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7851IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

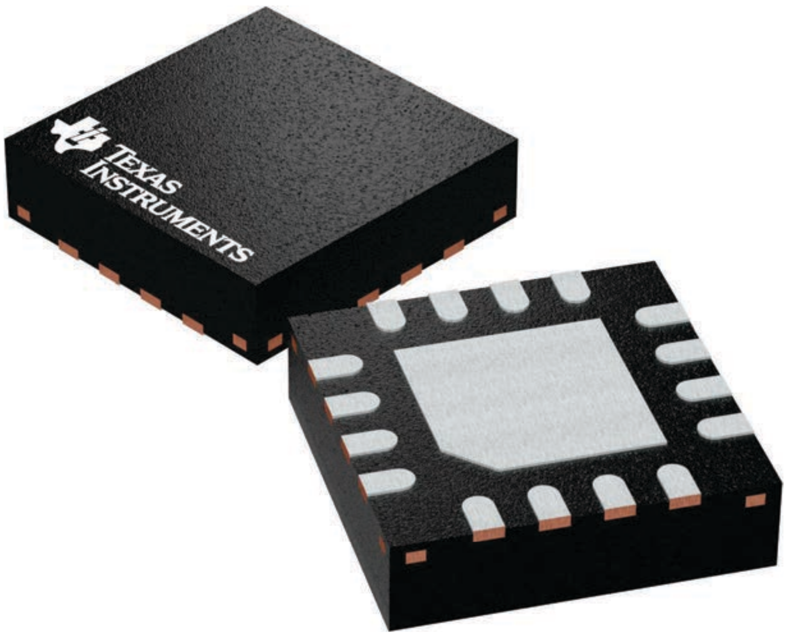
RTE 16

WQFN - 0.8 mm max height

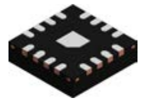
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



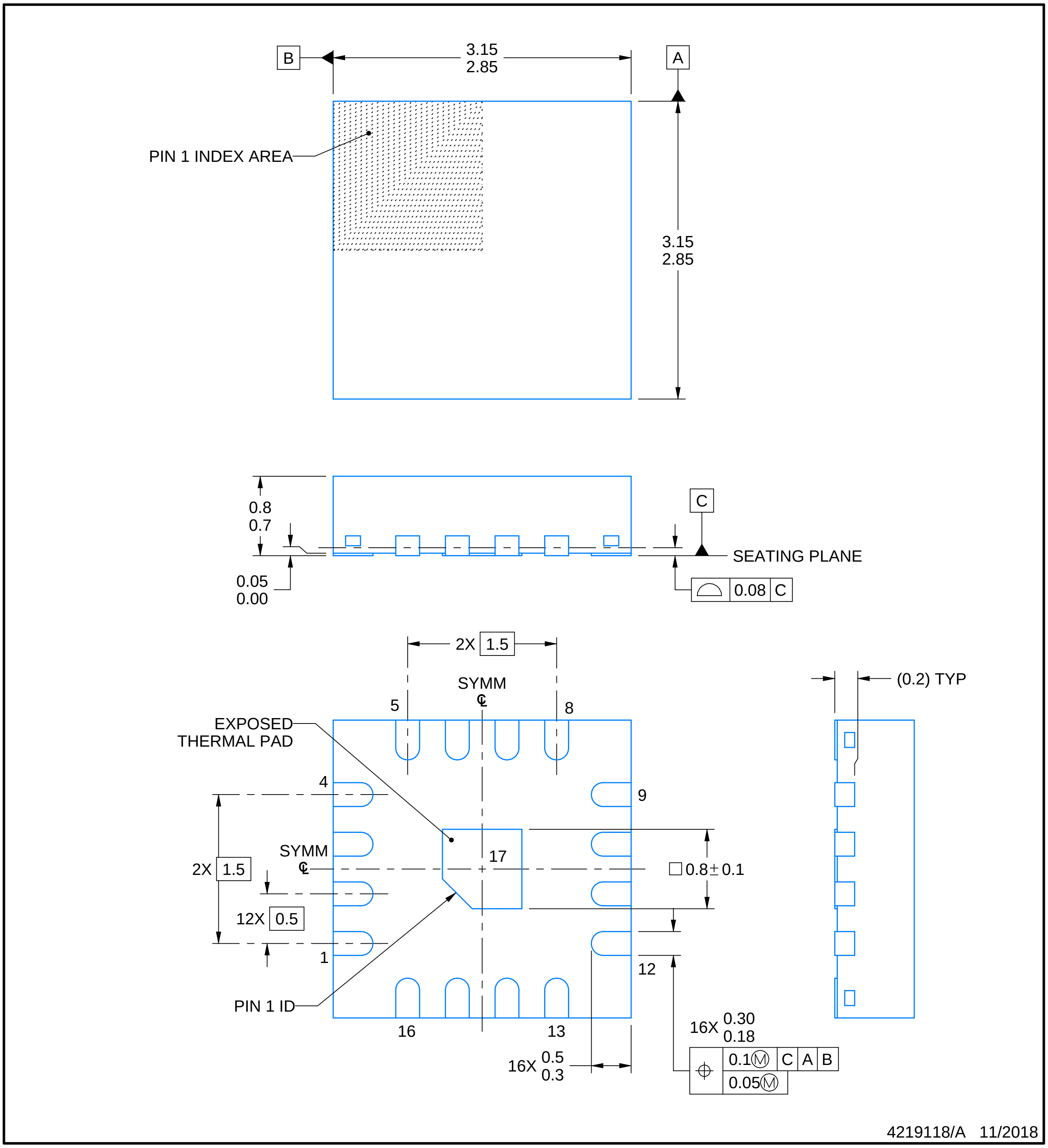
4225944/A



PACKAGE OUTLINE

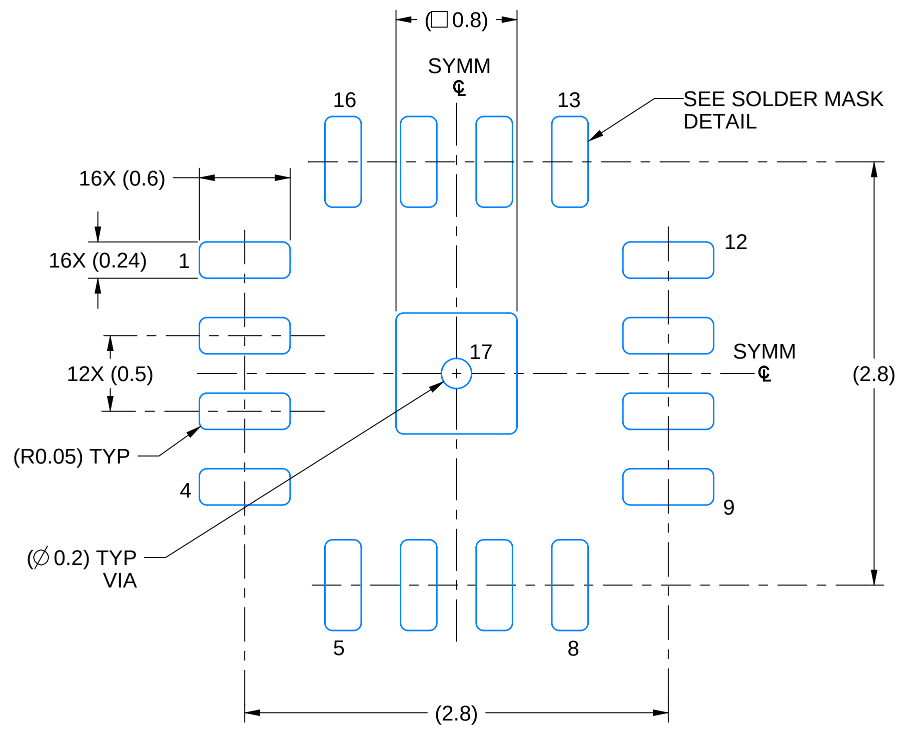
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

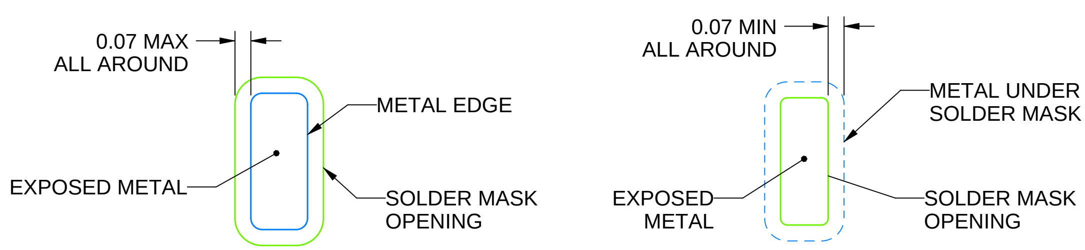


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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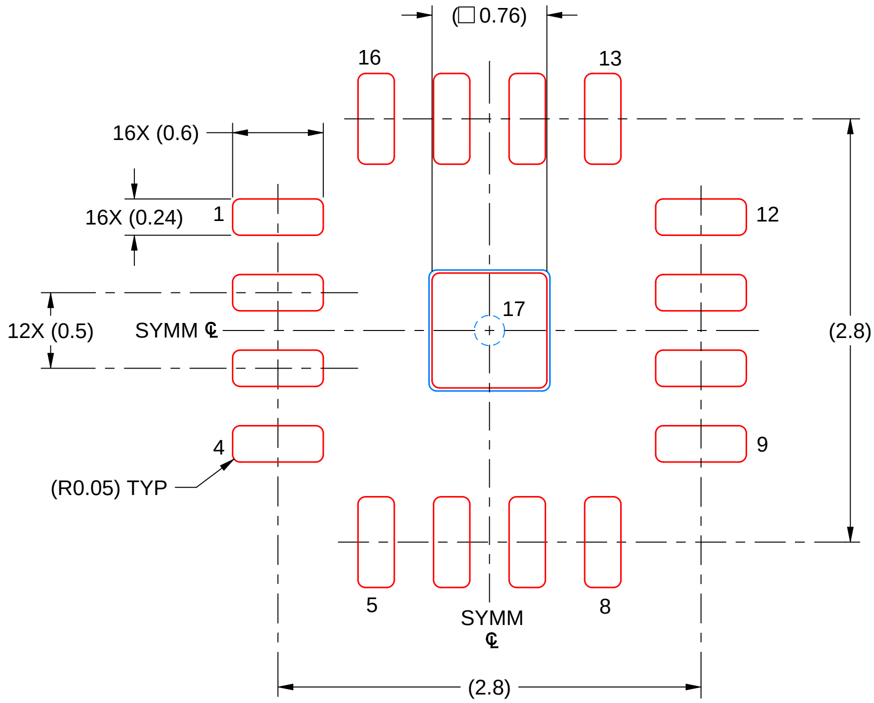
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219118/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.