TEXAS INSTRUMENTS

ADCS7476, ADCS7477, ADCS7478

SNAS192G – APRIL 2003 – REVISED MAY 2016

ADCS747x 1-MSPS, 12-Bit, 10-Bit, and 8-Bit A/D Converters

1 Features

- Variable Power Management
- Packaged in 6-Pin SOT-23
- Power Supply Used as Reference
- Single 2.7-V to 5.25-V Supply Operation
- Compatible With SPI™, QSPI™, MICROWIRE™, and DSP
- Key Specifications
  - Resolution With No Missing Codes (12-Bit, 10-Bit, and 8-Bit)
  - Conversion Rate: 1 MSPS
  - DNL: 0.5, –0.3 LSB (Typical)
  - INL: ±0.4 LSB (Typical)
  - Power Consumption:
    - 3-V Supply: 2 mW (Typical)
    - 5-V Supply: 10 mW (Typical)

2 Applications

- Automotive Navigation
- FA or ATM Equipment
- Portable Systems
- Medical Instruments
- Mobile Communications
- Instrumentation and Control Systems

3 Description

The ADCS7476, ADCS7477, and ADCS7478 devices are low power, monolithic CMOS 12-, 10-, and 8-bit analog-to-digital converters that operate at 1 MSPS. The ADCS747x devices are a drop-in replacement for Analog Device's AD747x. Each device is based on a successive approximation register architecture with internal track-and-hold. The serial interface is compatible with several standards, such as SPI, QSPI, MICROWIRE, and many common DSP serial interfaces.
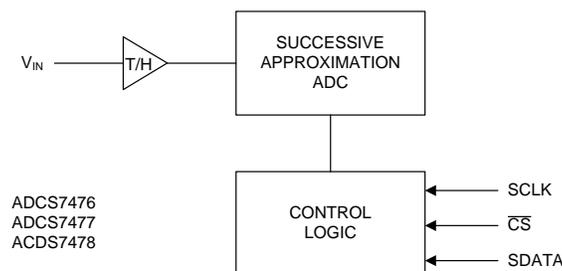
The ADCS747x uses the supply voltage as a reference, enabling the device to operate with a full-scale input range of 0 to V_{DD}. The conversion rate is determined from the serial clock (SCLK) speed. These converters offer a shutdown mode, which can be used to trade throughput for power consumption. The ADCS747x is operated with a single supply that can range from 2.7 V to 5.25 V. Normal power consumption during continuous conversion, using a 3-V or 5-V supply, is 2 mW or 10 mW respectively. The power-down feature, which is enabled by a chip select ($\overline{CS}$) pin, reduces the power consumption to under 5 µW using a 5-V supply. All three converters are available in a 6-pin SOT-23 package, which provides an extremely small footprint for applications where space is a critical consideration. These products are designed for operation over the automotive and extended industrial temperature range of −40°C to 125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADCS7476 ADCS7477 ADCS7478	SOT-23 (6)	1.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

ADCS7476
ADCS7477
ACDS7478

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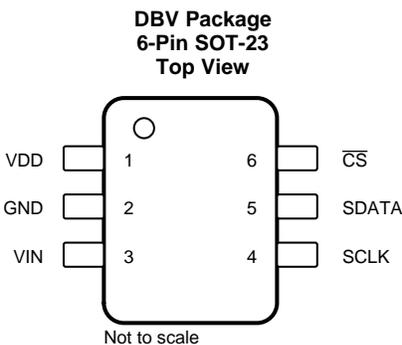
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G   **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Moved V_{DD} from the *Electrical Characteristics* tables to the *Recommended Operating Conditions* table 5

Changes from Revision E (March 2013) to Revision F   **Page**

- Changed layout of National Data Sheet to TI format 1

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View

```
        ○
VDD  ┌─ 1      6 ─┐  CS̄
GND  ┌─ 2      5 ─┐  SDATA
VIN  ┌─ 3      4 ─┐  SCLK
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Not to scale

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	V_{DD}	P	Positive supply pin. These pins must be connected to a quiet 2.7-V to 5.25-V source and bypassed to GND with 0.1-µF and 1-µF monolithic capacitors placed within 1 cm of the power pin. ADCS747x uses this power supply as a reference, so it must be thoroughly bypassed.
2	GND	G	The ground return for the supply.
3	V_{IN}	I	Analog input. This signal can range from 0 V to V_{DD}.
4	SCLK	I	Digital clock input. The range of frequencies for this input is 10 kHz to 20 MHz, with ensured performance at 20 MHz. This clock directly controls the conversion and readout processes.
5	SDATA	O	Digital data output. The output words are clocked out of this pin by the SCLK pin.
6	$\overline{CS}$	I	Chip select. A conversion process begins on the falling edge of $\overline{CS}$.

(1)　G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
Supply voltage, V_{DD}	−0.3	6.5	V
Voltage on any analog pin to GND	−0.3	V_{DD} + 0.3	V
Voltage on any digital pin to GND	−0.3	6.5	V
Input current at any pin (except power supply pins)		±10	mA
Soldering temperature, infrared (10 sec)		215	°C
Operating temperature, T_A		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.7	5.25	V
	Digital input pins voltage (independent of supply voltage)	2.7	5.25	V
T_A	Operating temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		ADCS7476, ADCS7477, ADCS7478	UNIT
		DBV (SOT-23)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics – ADCS7476

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS							
	Resolution with no missing codes	V_{DD} = 2.7 V to 3.6 V, −40°C ≤ T_A ≤ 125°C				12	Bits
INL	Integral non-linearity	V_{DD} = 2.7 V to 3.6 V	T_A = 25°C		±0.4		LSB
			−40°C ≤ T_A ≤ 85°C			±1	
		V_{DD} = 2.7 V to 3.6 V, T_A = 125°C		−1.1		1	LSB
DNL	Differential non-linearity	V_{DD} = 2.7 V to 3.6 V	T_A = 25°C	−0.3	0.5		LSB
			−40°C ≤ T_A ≤ 85°C	−0.9		1	
		V_{DD} = 2.7 V to 3.6 V, T_A = 125°C				±1	LSB
V_{OFF}	Offset error	V_{DD} = 2.7 V to 3.6 V	T_A = 25°C		±0.1		LSB
			−40°C ≤ T_A ≤ 125°C			±1.2	
GE	Gain error	V_{DD} = 2.7 V to 3.6 V	T_A = 25°C		±0.2		LSB
			−40°C ≤ T_A ≤ 125°C			±1.2	
DYNAMIC CONVERTER CHARACTERISTICS							
SINAD	Signal-to-noise plus distortion ratio	f_{IN} = 100 kHz	T_A = 25°C		72		dB
			−40°C ≤ T_A ≤ 125°C	70			
SNR	Signal-to-noise ratio	f_{IN} = 100 kHz	T_A = 25°C		72.5		dB
			−40°C ≤ T_A ≤ 85°C	70.8			
		f_{IN} = 100 kHz, T_A = 125°C		70.6			dB
THD	Total harmonic distortion	f_{IN} = 100 kHz			−80		dB
SFDR	Spurious-free dynamic range	f_{IN} = 100 kHz			82		dB
IMD	Intermodulation distortion, second order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			−78		dB
	Intermodulation distortion, third order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			−78		dB
FPBW	−3-dB full power bandwidth	5-V supply			11		MHz
		3-V supply			8		MHz
POWER SUPPLY CHARACTERISTICS							
I_{DD}	Normal mode (static)	V_{DD} = 4.75 V to 5.25 V, SCLK On or Off			2		mA
		V_{DD} = 2.7 V to 3.6 V, SCLK On or Off			1		mA
	Normal mode (operational)	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mA
			−40°C ≤ T_A ≤ 85°C			3.5	
		V_{DD} = 2.7 V to 3.6 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		0.6		mA
			−40°C ≤ T_A ≤ 85°C			1.6	
	Shutdown mode	V_{DD} = 5 V, SCLK Off			0.5		μA
		V_{DD} = 5 V, SCLK On			60		μA
P_D	Power consumption, normal mode (operational)	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		10		mW
			−40°C ≤ T_A ≤ 85°C			17.5	
		V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mW
			−40°C ≤ T_A ≤ 85°C			4.8	
	Power consumption, shutdown mode	V_{DD} = 5 V, SCLK Off			2.5		μW
		V_{DD} = 3 V, SCLK Off			1.5		μW
ANALOG INPUT CHARACTERISTICS							
V_{IN}	Input range				0 to V_{DD}		V
I_{DCL}	DC leakage current	−40°C ≤ T_A ≤ 85°C				±1	μA
C_{INA}	Analog input capacitance				30		pF
DIGITAL INPUT CHARACTERISTICS							

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

Electrical Characteristics – ADCS7476 (continued)

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage	−40°C ≤ T_A ≤ 85°C		2.4			V
V_{IL}	Input low voltage	V_{DD} = 5 V, −40°C ≤ T_A ≤ 85°C				0.8	V
		V_{DD} = 3 V, −40°C ≤ T_A ≤ 85°C				0.4	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DD}	T_A = 25°C			±10	nA
			−40°C ≤ T_A ≤ 85°C			±1	μA
C_{IND}	Digital input capacitance	T_A = 25°C				2	pF
		−40°C ≤ T_A ≤ 85°C				4	
DIGITAL OUTPUT CHARACTERISTICS							
V_{OH}	Output high voltage	I_{SOURCE} = 200 μA, V_{DD} = 2.7 V to 5.25 V, −40°C ≤ T_A ≤ 85°C		V_{DD} − 0.2			V
V_{OL}	Output low voltage	I_{SINK} = 200 μA, −40°C ≤ T_A ≤ 85°C				0.4	V
I_{OL}	TRI-STATE leakage current	−40°C ≤ T_A ≤ 85°C				±10	μA
C_{OUT}	TRI-STATE output capacitance	T_A = 25°C				2	pF
		−40°C ≤ T_A ≤ 85°C				4	
	Output coding				Straight (natural) binary		
AC ELECTRICAL CHARACTERISTICS							
f_{SCLK}	Clock frequency	−40°C ≤ T_A ≤ 125°C				20	MHz
DC	SCLK duty cycle	−40°C ≤ T_A ≤ 85°C		40%		60%	
t_{TH}	Track or hold acquisition time	−40°C ≤ T_A ≤ 85°C				400	ns
f_{RATE}	Throughput rate	−40°C ≤ T_A ≤ 85°C				1	MSPS
t_{AD}	Aperture delay				3		ns
t_{AJ}	Aperture jitter				30		ps

6.6 Electrical Characteristics – ADCS7477

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS							
	Resolution with no missing codes	−40°C ≤ T_A ≤ 85°C				10	Bits
INL	Integral non-linearity	T_A = 25°C			±0.2		LSB
		−40°C ≤ T_A ≤ 85°C				±0.7	
DNL	Differential non-linearity	T_A = 25°C		−0.2		0.3	LSB
		T−40°C ≤ T_A ≤ 85°C		±0.7		±0.7	
V_{OFF}	Offset error	T_A = 25°C			±0.1		LSB
		−40°C ≤ T_A ≤ 85°C				±0.7	
GE	Gain error	T_A = 25°C			±0.2		LSB
		−40°C ≤ T_A ≤ 85°C				±1	
DYNAMIC CONVERTER CHARACTERISTICS							
SINAD	Signal-to-noise plus distortion ratio	f_{IN} = 100 kHz	T_A = 25°C		61.7		dBFS
			−40°C ≤ T_A ≤ 85°C	61			
SNR	Signal-to-noise ratio	f_{IN} = 100 kHz			62		dB
THD	Total harmonic distortion	f_{IN} = 100 kHz	T_A = 25°C		−77		dB
			−40°C ≤ T_A ≤ 85°C			−73	
SFDR	Spurious-free dynamic range	f_{IN} = 100 kHz	T_A = 25°C		78		dB
			−40°C ≤ T_A ≤ 85°C	74			

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

Electrical Characteristics – ADCS7477 (continued)

$T_A = 25°C$, $V_{DD} = 2.7$ V to 5.25 V, $f_{SCLK} = 20$ MHz, and $f_{SAMPLE} = 1$ MSPS (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
IMD	Intermodulation distortion, second order terms	$f_a = 103.5$ kHz, $f_b = 113.5$ kHz			−78		dB
	Intermodulation distortion, third order terms	$f_a = 103.5$ kHz, $f_b = 113.5$ kHz			−78		dB
FPBW	−3-dB full power bandwidth	5-V supply			11		MHz
		3-V supply			8		MHz
POWER SUPPLY CHARACTERISTICS							
I_{DD}	Normal mode (static)	$V_{DD} = 4.75$ V to 5.25 V, SCLK On or Off			2		mA
		$V_{DD} = 2.7$ V to 3.6 V, SCLK On or Off			1		mA
	Normal mode (operational)	$V_{DD} = 4.75$ V to 5.25 V, $f_{SAMPLE} = 1$ MSPS	$T_A = 25°C$		2		mA
			−40°C ≤ T_A ≤ 85°C			3.5	
		$V_{DD} = 2.7$ V to 3.6 V, $f_{SAMPLE} = 1$ MSPS	$T_A = 25°C$		0.6		mA
			−40°C ≤ T_A ≤ 85°C			1.6	
	Shutdown mode	$V_{DD} = 5$ V, SCLK Off			0.5		µA
		$V_{DD} = 5$ V, SCLK On			60		
P_D	Power consumption, normal mode (operational)	$V_{DD} = 5$ V, $f_{SAMPLE} = 1$ MSPS	$T_A = 25°C$		10		mW
			−40°C ≤ T_A ≤ 85°C			17.5	
		$V_{DD} = 3$ V, $f_{SAMPLE} = 1$ MSPS	$T_A = 25°C$		2		mW
			−40°C ≤ T_A ≤ 85°C			4.8	
	Power consumption, shutdown mode	$V_{DD} = 5$ V, SCLK Off			2.5		µW
		$V_{DD} = 3$ V, SCLK Off			1.5		
ANALOG INPUT CHARACTERISTICS							
V_{IN}	Input range				0 to V_{DD}		V
I_{DCL}	DC leakage current	$T_A = −40°C$ to 85°C				±1	µA
C_{INA}	Analog input capacitance				30		pF
DIGITAL INPUT CHARACTERISTICS							
V_{IH}	Input high voltage	$T_A = −40°C$ to 85°C		2.4			V
V_{IL}	Input low voltage	$V_{DD} = 5$ V, −40°C ≤ T_A ≤ 85°C				0.8	V
		$V_{DD} = 3$ V, −40°C ≤ T_A ≤ 85°C				0.4	V
I_{IN}	Input current	$V_{IN} = 0$ V or V_{DD}	$T_A = 25°C$			±10	nA
			−40°C ≤ T_A ≤ 85°C			±1	µA
C_{IND}	Digital input capacitance	$T_A = 25°C$			2		pF
		−40°C ≤ T_A ≤ 85°C				4	
DIGITAL OUTPUT CHARACTERISTICS							
V_{OH}	Output high voltage	$I_{SOURCE} = 200$ µA, $V_{DD} = 2.7$ V to 5.25 V, −40°C ≤ T_A ≤ 85°C		$V_{DD} − 0.2$			V
V_{OL}	Output low voltage	$I_{SINK} = 200$ µA, −40°C ≤ T_A ≤ 85°C				0.4	V
I_{OL}	TRI-STATE leakage current	−40°C ≤ T_A ≤ 85°C				±10	µA
C_{OUT}	TRI-STATE output capacitance	$T_A = 25°C$			2		pF
		−40°C ≤ T_A ≤ 85°C				4	
	Output coding				Straight (natural) binary		
AC ELECTRICAL CHARACTERISTICS							
f_{SCLK}	Clock frequency	−40°C ≤ T_A ≤ 85°C				20	MHz
DC	SCLK duty cycle	−40°C ≤ T_A ≤ 85°C		40%		60%	
t_{TH}	Track or hold acquisition time	−40°C ≤ T_A ≤ 85°C				400	ns
f_{RATE}	Throughput rate	−40°C ≤ T_A ≤ 85°C				1	MSPS
t_{AD}	Aperture delay				3		ns

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

Electrical Characteristics – ADCS7477 (continued)

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{AJ}	Aperture jitter			30		ps

6.7 Electrical Characteristics – ADCS7478

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS							
	Resolution with no missing codes	−40°C ≤ T_A ≤ 85°C				8	Bits
INL	Integral non-linearity	T_A = 25°C			±0.05		LSB
		−40°C ≤ T_A ≤ 85°C				±0.3	
DNL	Differential non-linearity	T_A = 25°C			±0.07		LSB
		−40°C ≤ T_A ≤ 85°C				±0.3	
V_{OFF}	Offset error	T_A = 25°C			±0.03		LSB
		−40°C ≤ T_A ≤ 85°C				±0.3	
GE	Gain error	T_A = 25°C			±0.08		LSB
		−40°C ≤ T_A ≤ 85°C				±0.4	
	Total unadjusted error	T_A = 25°C			±0.07		LSB
		−40°C ≤ T_A ≤ 85°C				±0.3	
DYNAMIC CONVERTER CHARACTERISTICS							
SINAD	Signal-to-noise plus distortion ratio	f_{IN} = 100 kHz	T_A = 25°C		49.7		dB
			−40°C ≤ T_A ≤ 85°C	49			
SNR	Signal-to-noise ratio	f_{IN} = 100 kHz			49.7		dB
THD	Total harmonic distortion	f_{IN} = 100 kHz	T_A = 25°C		−77		dB
			−40°C ≤ T_A ≤ 85°C			−65	
SFDR	Spurious-free dynamic range	f_{IN} = 100 kHz	T_A = 25°C		69		dB
			−40°C ≤ T_A ≤ 85°C	65			
IMD	Intermodulation distortion, second order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			−68		dB
	Intermodulation distortion, third order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			−68		dB
FPBW	−3-dB full power bandwidth	5-V supply			11		MHz
		3-V supply			8		MHz
POWER SUPPLY CHARACTERISTICS							
I_{DD}	Normal mode (static)	V_{DD} = 4.75 V to 5.25 V, SCLK On or Off			2		mA
		V_{DD} = 2.7 V to 3.6 V, SCLK On or Off			1		mA
	Normal mode (operational)	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mA
			−40°C ≤ T_A ≤ 85°C			3.5	
		V_{DD} = 2.7 V to 3.6 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		0.6		mA
			−40°C ≤ T_A ≤ 85°C			1.6	
	Shutdown mode	V_{DD} = 5 V, SCLK Off			0.5		µA
		V_{DD} = 5 V, SCLK On			60		

(1) Data sheet min/max specification limits are ensured by design, test, or statistical analysis.

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

Electrical Characteristics – ADCS7478 (continued)

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_D	Power consumption, normal mode (operational)	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		10		mW
			−40°C ≤ T_A ≤ 85°C			17.5	
		V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mW
			−40°C ≤ T_A ≤ 85°C			4.8	
	Power consumption, shutdown mode	V_{DD} = 5 V, SCLK Off			2.5		µW
		V_{DD} = 3 V, SCLK Off			1.5		
ANALOG INPUT CHARACTERISTICS							
V_{IN}	Input range				0 to V_{DD}		V
I_{DCL}	DC leakage current	−40°C ≤ T_A ≤ 85°C				±1	µA
C_{INA}	Analog input capacitance				30		pF
DIGITAL INPUT CHARACTERISTICS							
V_{IH}	Input high voltage	−40°C ≤ T_A ≤ 85°C		2.4			V
V_{IL}	Input low voltage	V_{DD} = 5 V, −40°C ≤ T_A ≤ 85°C				0.8	V
		V_{DD} = 3 V, −40°C ≤ T_A ≤ 85°C				0.4	V
I_{IN}	Digital input current	V_{IN} = 0 V or V_{DD}	T_A = 25°C		±10		nA
			−40°C ≤ T_A ≤ 85°C			±1	µA
C_{IND}	Input capacitance	T_A = 25°C			2		p
		−40°C ≤ T_A ≤ 85°C				4	
DIGITAL OUTPUT CHARACTERISTICS							
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5.25 V, −40°C ≤ T_A ≤ 85°C		V_{DD} − 0.2			V
V_{OL}	Output low voltage	I_{SINK} = 200 µA, −40°C ≤ T_A ≤ 85°C				0.4	V
I_{OL}	TRI-STATE leakage current	−40°C ≤ T_A ≤ 85°C				±10	µA
C_{OUT}	TRI-STATE output capacitance				2	4	pF
	Output coding				Straight (natural) binary		
AC ELECTRICAL CHARACTERISTICS							
f_{SCLK}	Clock frequency	−40°C ≤ T_A ≤ 85°C				20	MHz
DC	SCLK duty cycle	−40°C ≤ T_A ≤ 85°C		40%		60%	
t_{TH}	Track or hold acquisition time	−40°C ≤ T_A ≤ 85°C				400	ns
f_{RATE}	Throughput rate	−40°C ≤ T_A ≤ 85°C (see *Application Information*)		1			MSPS
t_{AD}	Aperture delay				3		ns
t_{AJ}	Aperture jitter				30		ps

6.8 Timing Requirements

−40°C ≤ T_A ≤ 85°C, V_{DD} = 2.7 V to 5.25 V, and f_{SCLK} = 20 MHz (unless otherwise noted)[1]

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CONVERT}$		T_A = 25°C		$16 \times t_{SCLK}$		
t_{QUIET}	Quiet time [2]		50			ns
t_1	Minimum $\overline{CS}$ pulse width		10			ns
t_2	$\overline{CS}$ to SCLK setup time		10			ns
t_3	Delay from $\overline{CS}$ until SDATA TRI-STATE disabled [3]				20	ns

(1) All input signals are specified as $t_r = t_f$ = 5 ns (10% to 90% V_{DD}) and timed from 1.6 V.
(2) Minimum quiet time required between bus relinquish and start of next conversion.
(3) Measured with the load circuit (Figure 1), and defined as the time taken by the output to cross 1 V.

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

Timing Requirements (continued)

$-40°C \leq T_A \leq 85°C$, V_{DD} = 2.7 V to 5.25 V, and f_{SCLK} = 20 MHz (unless otherwise noted)[1]

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_4	Data access time after SCLK falling edge[4]	V_{DD} = 2.7 V to 3.6 V			40	ns
		V_{DD} = 4.75 V to 5.25 V			20	ns
t_5	SCLK low pulse width		$0.4 \times t_{SCLK}$			ns
t_6	SCLK high pulse width		$0.4 \times t_{SCLK}$			ns
t_7	SCLK to data valid hold time	V_{DD} = 2.7 V to 3.6 V	7			ns
		V_{DD} = 4.75 V to 5.25 V	5			ns
t_8	SCLK falling edge to SDATA high impedance [5]	V_{DD} = 2.7 V to 3.6 V	6		25	ns
		V_{DD} = 4.75 V to 5.25 V	5		25	ns
$t_{POWER-UP}$	Power-up time from full power down	T_A = 25°C		1		µs

(4) Measured with the load circuit (Figure 1), and defined as the time taken by the output to cross 1 V or 2 V.
(5) t_8 is derived from the time taken by the outputs to change by 0.5 V with the loading circuit (Figure 1). The measured number is then adjusted to remove the effects of charging or discharging the 25-pF capacitor. This means t_8 is the true bus relinquish time, independent of the bus loading.
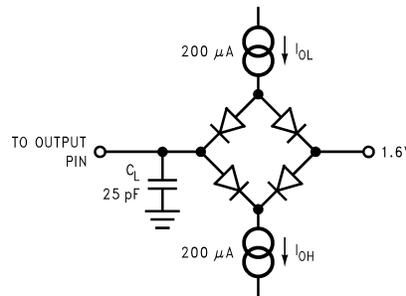
Figure 1. Timing Test Circuit
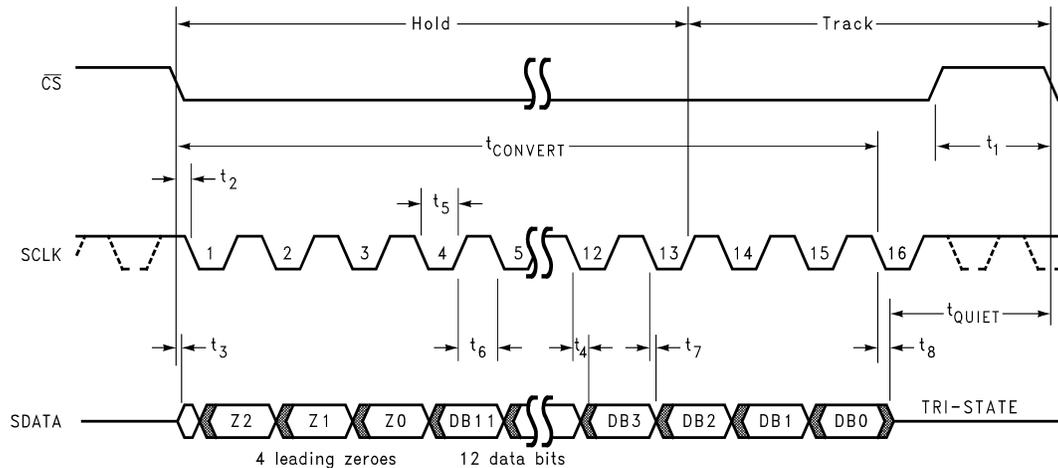
Figure 2. ADCS7476 Serial Interface Timing Diagram

Product Folder Links: _ADCS7476 ADCS7477 ADCS7478_
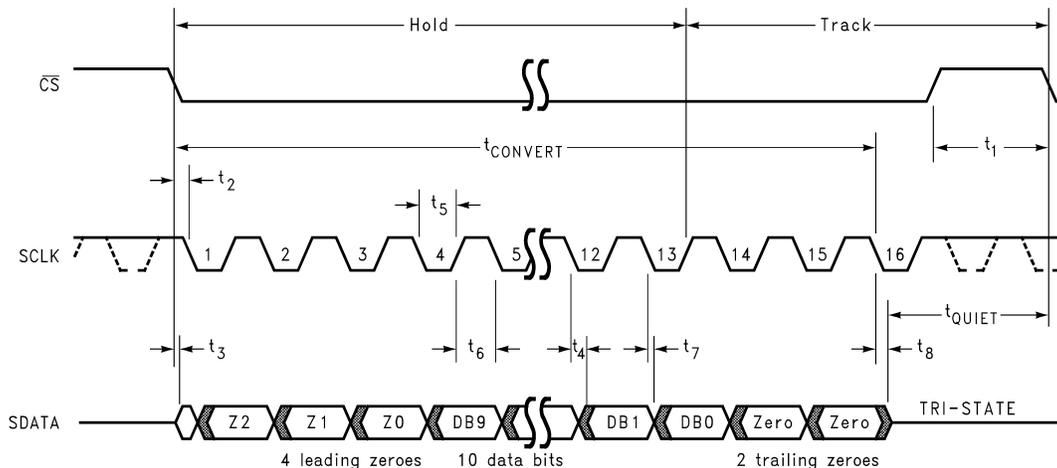
Figure 3. ADCS7477 Serial Interface Timing Diagram
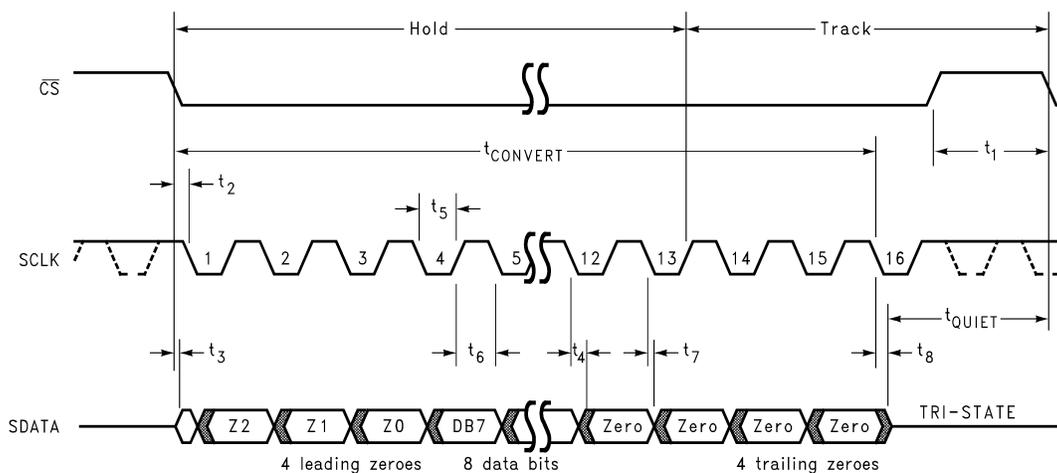
Figure 4. ADCS7478 Serial Interface Timing Diagram

6.9 Typical Characteristics

T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwise noted)
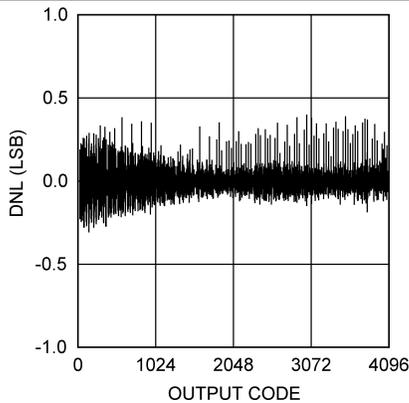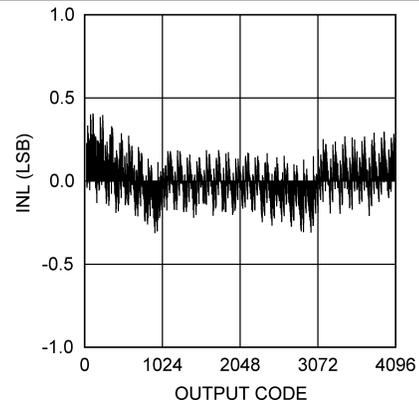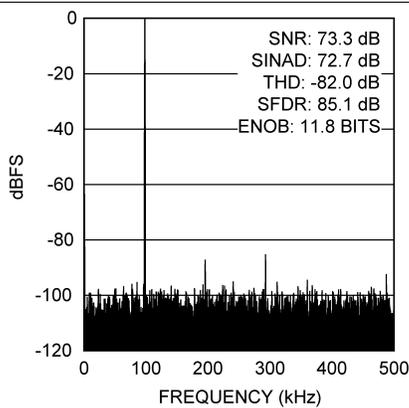

Figure 5. ADCS7476 DNL

Figure 6. ADCS7476 INL

Figure 7. ADCS7476 Spectral Response at 100-kHz Input
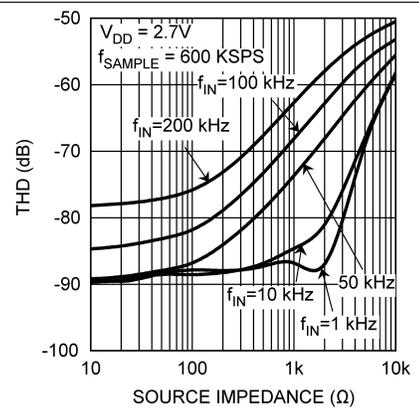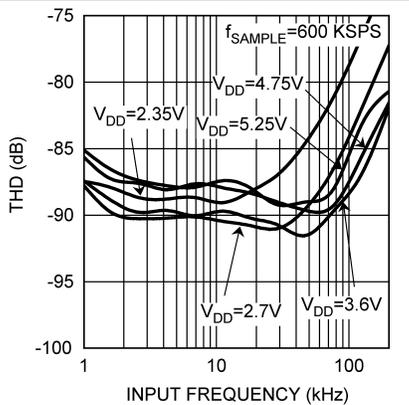

Figure 8. ADCS7476 THD vs Source Impedance
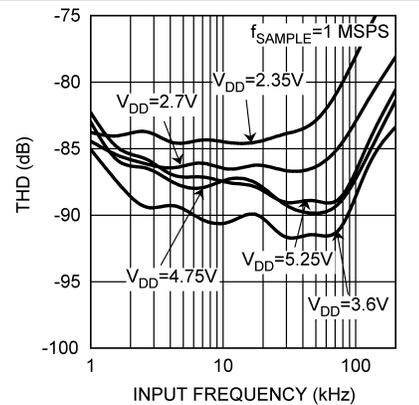

Figure 9. ADCS7476 THD vs Input Frequency, 600 KSPS

Figure 10. ADCS7476 THD vs Input Frequency, 1 MSPS

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwise noted)
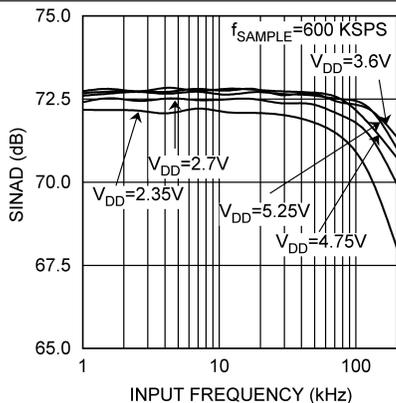
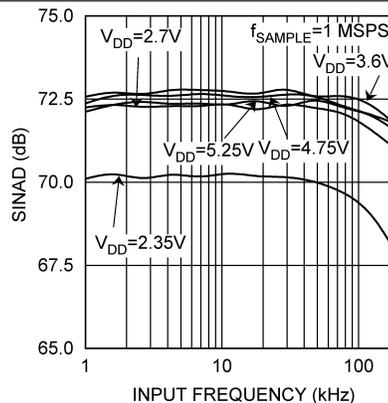**Figure 11. ADCS7476 SINAD vs Input Frequency, 600 KSPS**
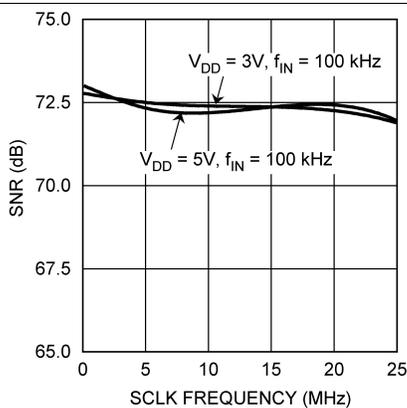
Figure 12. ADCS7476 SINAD vs Input Frequency, 1 MSPS
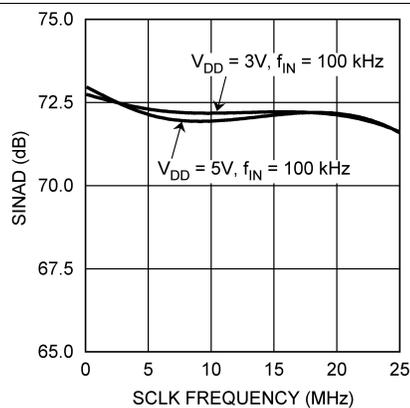
Figure 13. ADCS7476 SNR vs f_{SCLK}
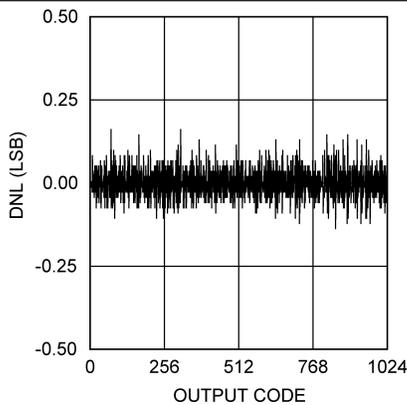
Figure 14. ADCS7476 SINAD vs f_{SCLK}

Figure 15. ADCS7477 DNL
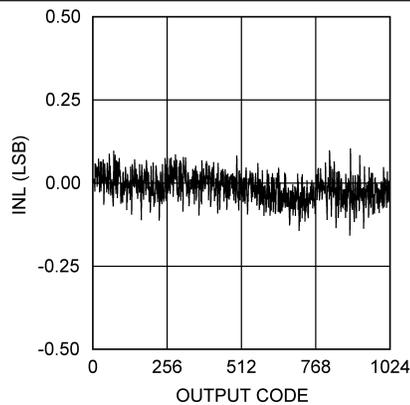
Figure 16. ADCS7477 INL

Product Folder Links: ADCS7476 ADCS7477 ADCS7478

Typical Characteristics (continued)

$T_A = 25°C$, $V_{DD} = 3$ V, $f_{SAMPLE} = 1$ MSPS, $f_{SCLK} = 20$ MHz, and $f_{IN} = 100$ kHz (unless otherwise noted)

SINAD: 61.9
SNR: 61.9
THD: -81.0
SFDR: 84.4
ENOB: 9.987
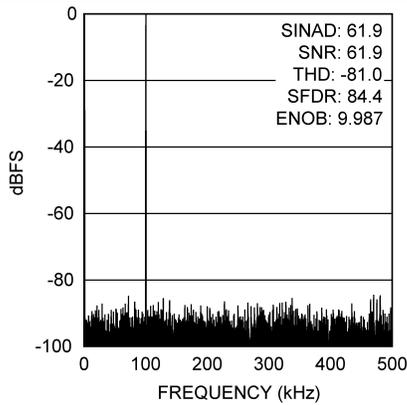
Figure 17. ADCS7477 Spectral Response at 100-kHz Input

$V_{DD} = 3V$

$V_{DD} = 5V$
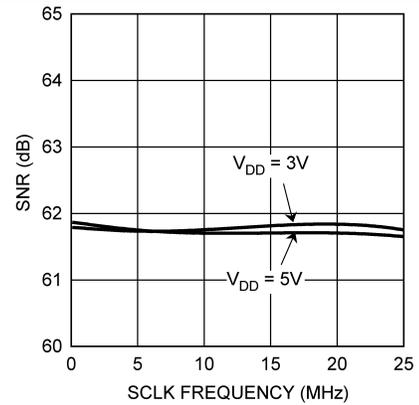
Figure 18. ADCS7477 SNR vs f_{SCLK}

$V_{DD} = 3V$

$V_{DD} = 5V$

Figure 19. ADCS7477 SINAD vs f_{SCLK}
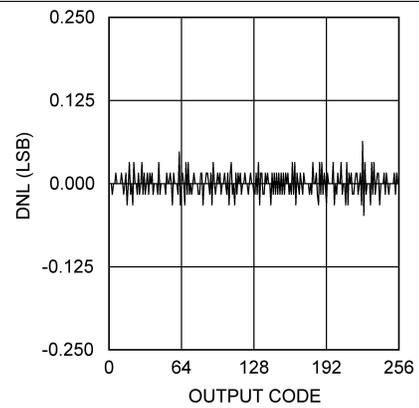
Figure 20. ADCS7478 DNL

Figure 21. ADCS7478 INL

SINAD: 49.8
SNR: 49.8
THD: -70.9
SFDR: 68.9
ENOB: 7.977
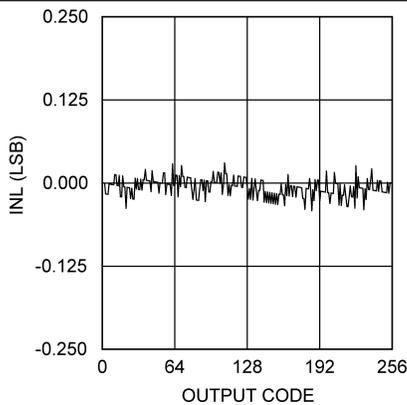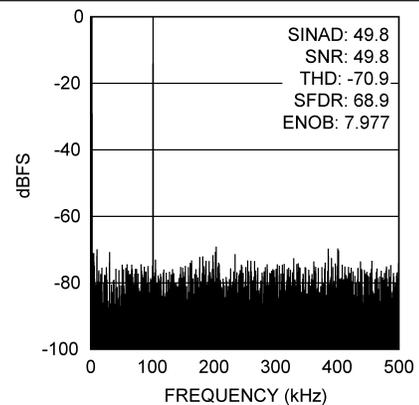
Figure 22. ADCS7478 Spectral Response at 100-kHz Input

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

Typical Characteristics (continued)

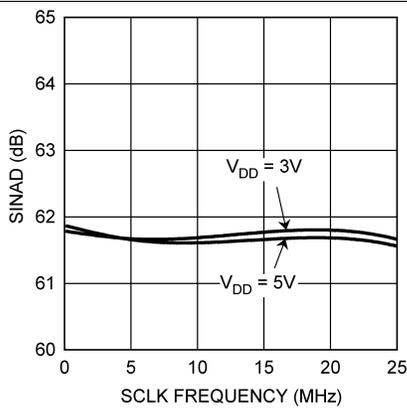T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwise noted)

Figure 23. ADCS7478 SNR vs f_{SCLK}

Figure 24. ADCS7478 SINAD vs f_{SCLK}

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Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*
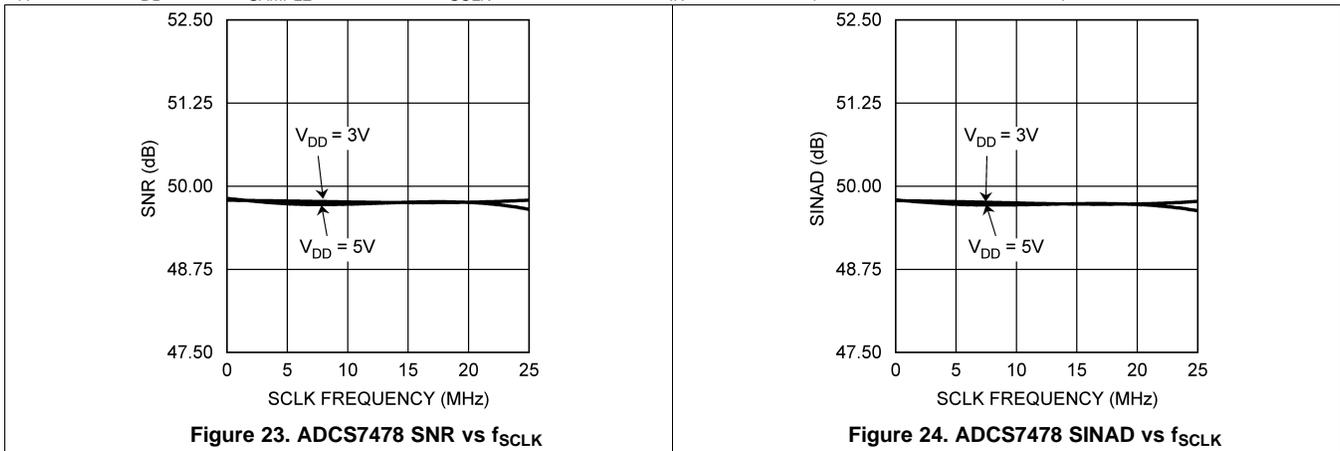
7 Detailed Description

7.1 Overview

The ADCS747x devices are successive-approximation analog-to-digital converters designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the ADCS747x in both track and hold operation are shown in Figure 25 and Figure 26. In Figure 26, the device is in track mode where the switch SW1 connects the sampling capacitor to the input, and SW2 balances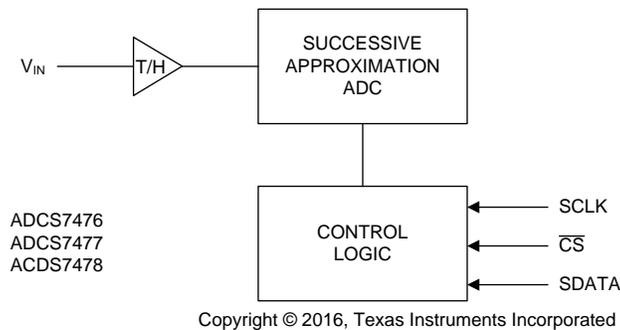 the comparator inputs. The device is in this state until $\overline{CS}$ is brought low, at which point the device moves to hold mode.

7.2 Functional Block Diagram

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7.3 Feature Description

Serial interface timing diagrams for the ADCS747x are shown in Figure 2, Figure 3, and Figure 4. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found.

Basic operation of the ADCS747x begins with $\overline{CS}$ going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK will be labeled with reference to the falling edge of $\overline{CS}$; for example, *the third falling edge of SCLK* shall refer to the third falling edge of SCLK after $\overline{CS}$ goes low.

At the fall of $\overline{CS}$, the SDATA pin comes out of TRI-STATE, and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion at the falling edge of $\overline{CS}$. The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see Figure 2, Figure 3, or Figure 4). The SDATA pin is placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of $\overline{CS}$, whichever occurs first. After a conversion is completed, the quiet time t_{QUIET} must be satisfied before bringing $\overline{CS}$ low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the ADCS747x. The sample bits (including any leading or trailing zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent falling edges of SCLK. ADCS747x produces four leading zeroes on SDATA, followed by twelve, ten, or eight data bits (the most significant first). After the data bits, the ADCS7477 clocks out two trailing zeros, and the ADCS7478 clocks out four trailing zeros. The ADCS7476 does not clock out any trailing zeros; the least significant data bit is valid on the 16th falling edge of SCLK.

Depending upon the application, the first edge on SCLK after $\overline{CS}$ goes low may be either a falling edge or a rising edge. If the first SCLK edge after $\overline{CS}$ goes low is a rising edge, all four leading zeroes are valid on the first four falling edges of SCLK. If instead the first SCLK edge after $\overline{CS}$ goes low is a falling edge, the first leading zero may not be set up in time for a microprocessor or DSP to read it correctly. The remaining data bits are still clocked out on the falling edges of SCLK.

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

7.4 Device Functional Modes

Figure 25 shows the device in hold mode where the switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode (Figure 26) on the 13th rising edge of SCLK.
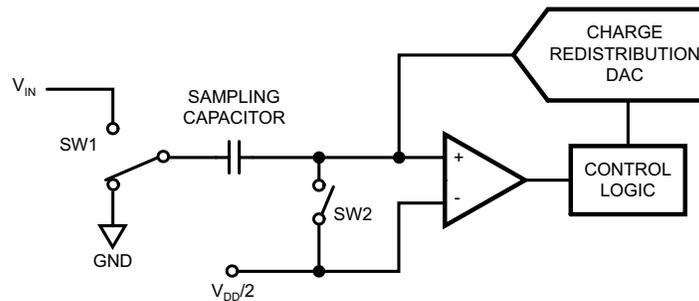
Figure 25. ADCS747x in Hold Mode
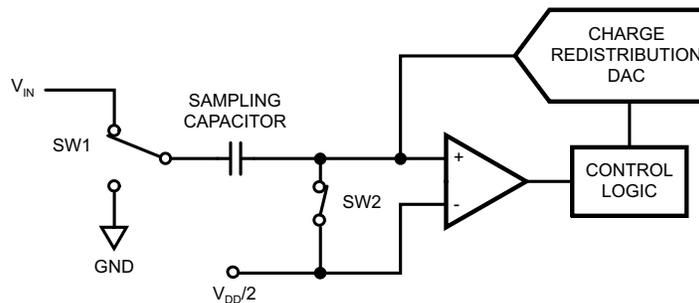
Figure 26. ADCS747x in Track Mode

7.4.1 Transfer Function

The output format of ADCS747x is straight binary. Code transitions occur midway between successive integer LSB values. The LSB widths for the ADCS7476 is V_{DD} / 4096; for the ADCS7477 the LSB width is V_{DD} / 1024; for the ADCS7478, the LSB width is V_{DD} / 256. The ideal transfer characteristic for the ADCS7476 and ADCS7477 is shown in Figure 27, while the ideal transfer characteristic for the ADCS7478 is shown in Figure 28.

Device Functional Modes (continued)

1LSB = $V_{DD}/4096$ (ADCS7476)

1LSB = $V_{DD}/1024$ (ADCS7477)
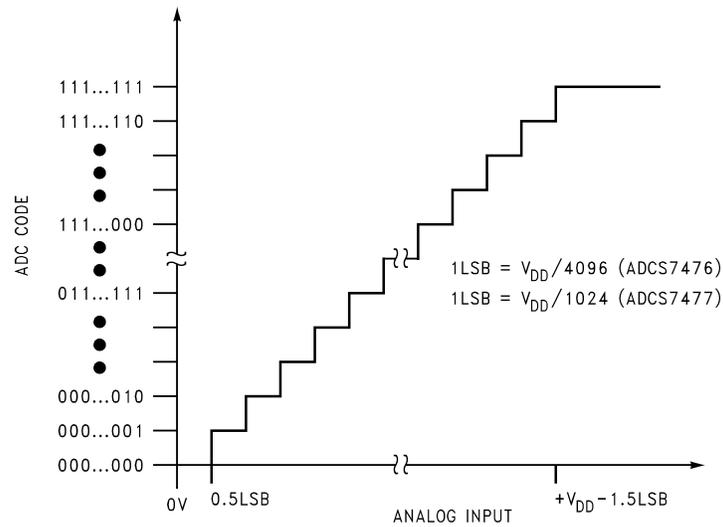
Figure 27. ADCS7476/77 Ideal Transfer Characteristic

1LSB = $V_{DD}/256$ (ADCS7478)
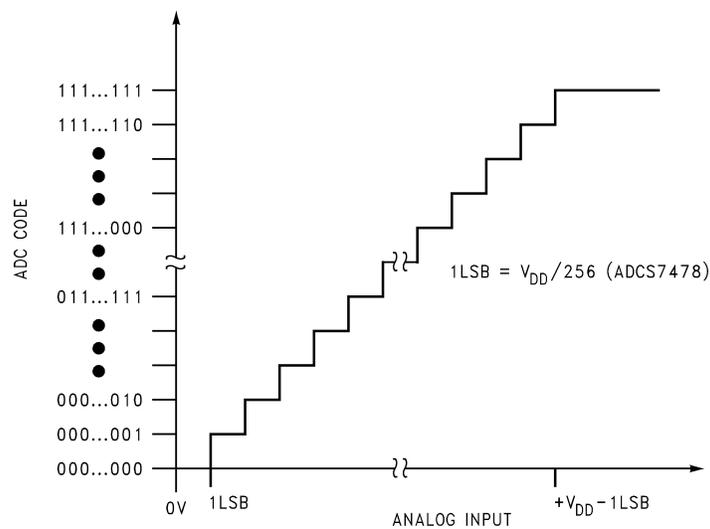
Figure 28. ADCS7478 Ideal Transfer Characteristic

7.4.2 Power-Up Timing

The ADCS747x typically requires 1 µs to power up, either after first applying V_{DD}, or after returning to normal mode from shutdown mode. This corresponds to one *dummy* conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the ADCS747x performs conversions properly.

> **NOTE**
> The t_{QUIET} time must still be included between the first dummy conversion and the second valid conversion.

Device Functional Modes (continued)

7.4.3 Modes of Operation

The ADCS747x has two possible modes of operation: *Normal Mode* and *Shutdown Mode*. ADCS747x enters normal mode (and a conversion process is begun) when $\overline{CS}$ is pulled low. The device enters shutdown mode if $\overline{CS}$ is pulled high before the tenth falling edge of SCLK after $\overline{CS}$ is pulled low, or stays in normal mode if $\overline{CS}$ remains low. Once in shutdown mode, the device stays there until $\overline{CS}$ is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade off throughput for power consumption.

7.4.3.1 Normal Mode

The best possible throughput is obtained by leaving the ADCS747x in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

If $\overline{CS}$ is brought high after the 10th falling edge, but before the 16th falling edge, the device remains in normal mode, but the current conversion is aborted, and SDATA returns to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed, $\overline{CS}$ may be idled either high or low until the next conversion. If $\overline{CS}$ is idled low, it must be brought high again before the start of the next conversion, which begins when $\overline{CS}$ is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after t_{QUIET} has elapsed, by bringing $\overline{CS}$ low again.

7.4.3.2 Start-Up Mode

When the V_{DD} supply is first applied, the ADCS747x may power up in either of the two modes: normal or shutdown. As such, one dummy conversion should be performed after start-up, exactly as described in *Power-Up Timing*. The part may then be placed into either normal mode or the shutdown mode, as described in *Normal Mode* and *Shutdown Mode*.

7.4.3.3 Shutdown Mode

Shutdown mode is appropriate for applications that either do not sample continuously, or are willing to trade throughput for power consumption. When the ADCS747x is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing $\overline{CS}$ back high anytime between the second and tenth falling edges of SCLK, as shown in Figure 29. Once $\overline{CS}$ has been brought high in this manner, the device enters shutdown mode; the current conversion is aborted and SDATA enters TRI-STATE. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the device does not change mode; this is to avoid accidentally changing mode as a result of noise on the $\overline{CS}$ line.
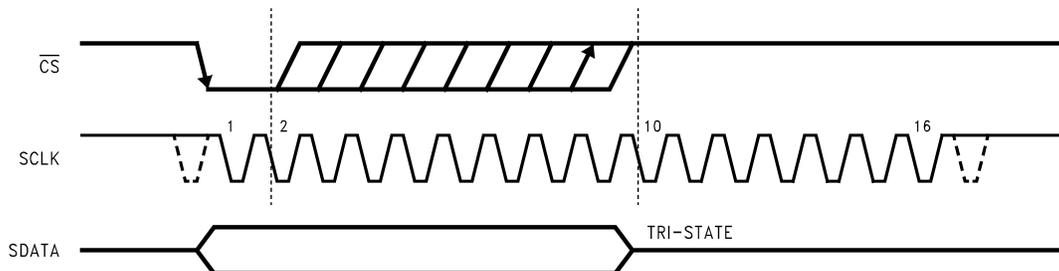

Figure 29. Entering Shutdown Mode

Device Functional Modes (continued)
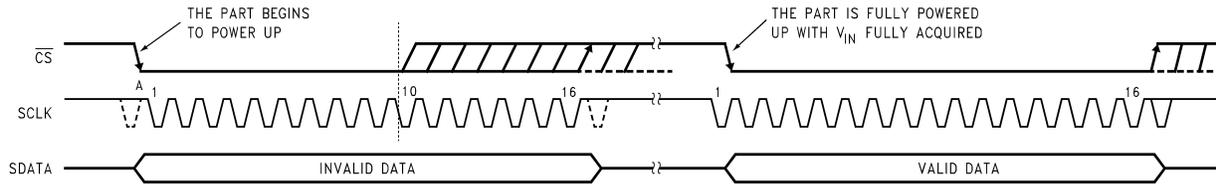
Figure 30. Entering Normal Mode

To exit shutdown mode, bring $\overline{CS}$ back low. Upon bringing $\overline{CS}$ low, the ADCS747x begins powering up. Power up typically takes 1 µs. This microsecond of power-up delay results in the first conversion result being unusable. The second conversion performed after power-up, however, is valid, as shown in Figure 30.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device returns to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit shutdown mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK. The ADCS747x is fully powered up after 16 SCLK cycles.

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

8 Application and Implementation

> **NOTE**
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A typical application of ADCS747x is shown in Figure 32. The combined analog and digital supplies are provided in this example by the TI LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The supply is bypassed with a capacitor network located close to the device. The three-wire interface is also shown connected to a microprocessor or DSP.

8.1.1 Analog Inputs

An equivalent circuit for the ADCS747x input channel is shown in Figure 31. The diodes D1 and D2 provide ESD protection for the analog inputs. At no time should an analog input exceed V_{DD} + 300 mV or GND – 300 mV, as these ESD diodes begin conducting current into the substrate or supply line and affect ADC operation.

The capacitor C1 in Figure 31 typically has a value of 4 pF, and is mainly due to pin capacitance. The resistor R1 represents the ON resistance of the multiplexer and track or hold switch, and is typically 100 Ω. The capacitor C2 is the ADCS747x sampling capacitor, and is typically 26 pF.

The sampling nature of the analog input causes input current pulses that result in voltage spikes at the input. ADCS747x delivers best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. In some applications where dynamic performance is critical, the input must be driven with a low output-impedance amplifier. In addition, when using ADCS747x to sample AC signals, a band-pass or low-pass filter reduces harmonics and noise and thus improve THD and SNR.
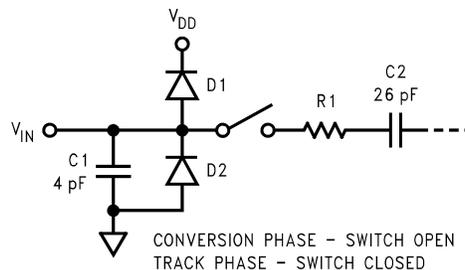
Figure 31. Equivalent Input Circuit

8.1.2 Digital Inputs and Outputs

The ADCS747x digital inputs (SCLK and $\overline{CS}$) are not limited by the same absolute maximum ratings as the analog inputs. The digital input pins are instead limited to 6.5 V with respect to GND, regardless of V_{DD}, the supply voltage. This allows ADCS747x to be interfaced with a wide range of logic levels, independent of the supply voltage.

> **NOTE**
> Even though the digital inputs are tolerant of up to 6.5 V above GND, the digital outputs are only capable of driving V_{DD} out.

In addition, the digital input pins are not prone to latch-up; SCLK and $\overline{CS}$ may be asserted before V_{DD} without any risk.

8.2 Typical Application

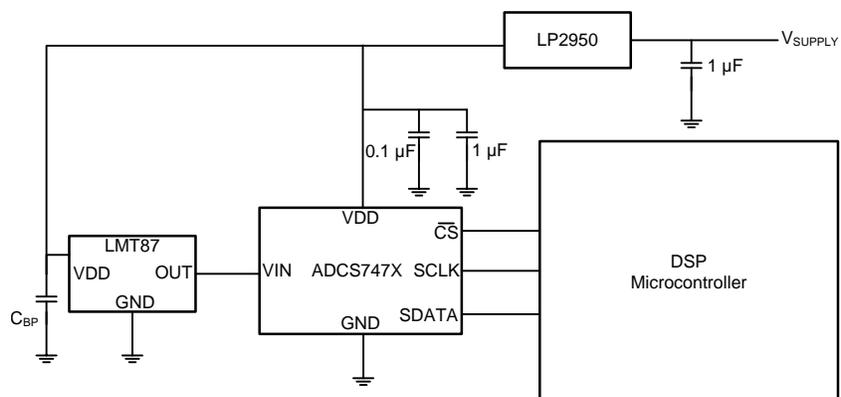The ADCS747x are monolithic CMOS 12-, 10-, and 8-bit ADCs that use the supply voltage as a reference, enabling the devices to operate with a full-scale input range of 0 to V_{DD}. An example low-power application with the LMT87, which is a wide range ±0.3°C accurate temperature sensor, is shown in Figure 32.

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Figure 32. Typical Application Circuit

8.2.1 Design Requirements

A successful ADCS747x and LMT87 design is constrained by the following factors:

- V_{IN} range must be 0 V to V_{DD} where V_{DD} can range from 2.7 V to 5.25 V.

8.2.2 Detailed Design Procedure

Designing for an accurate measurement requires careful attention to the timing requirements for the ADCS747x parts.

Because the ADC747x parts use the supply voltage as a reference, ensuring that the supply voltage is settled to its final level before exiting the shutdown mode and beginning a conversion is important. After the supply voltage has settled, the $\overline{CS}$ is brought to a low level (ideally 0 V) to start a conversion.

Ensuring that any noise on the power supply is less than ½ LSB in amplitude is also important. The supply voltage must be regarded as a precise voltage reference.

After the $\overline{CS}$ has been brought low, the user must wait for one complete conversion cycle (approximately 1 μs) for meaningful data. The dummy conversion cycle is the start-up time of the ADCS747x. The ADCS747x digital output can then be correlated to the LMT87 output level to get an accurate temperature reading. At V_{DD} = 3.3 V, 1 LSB of ADCS7476 is 0.805 mV.

Typical Application (continued)

8.2.3 Application Curves

Figure 33. ADCS7476/77 Ideal Transfer Characteristic

Figure 34. ADCS7478 Ideal Transfer Characteristic
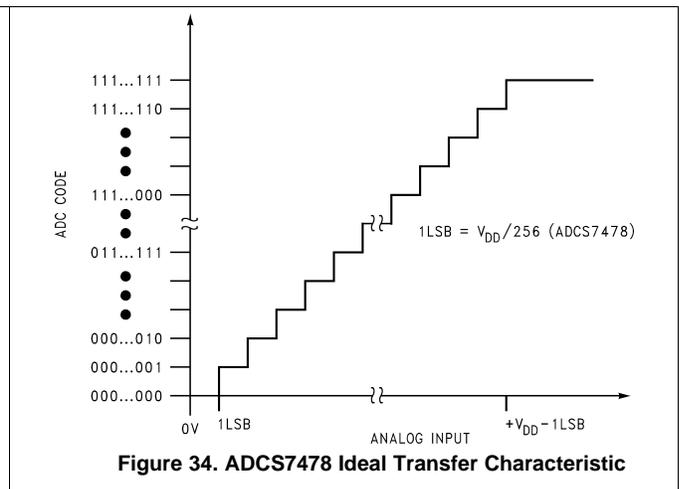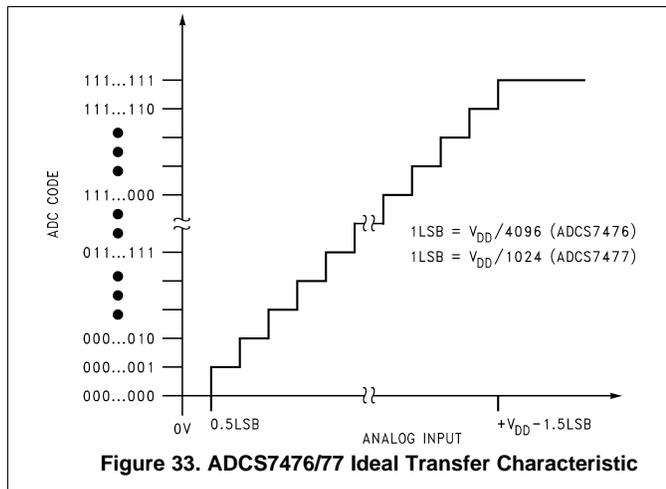
9 Power Supply Recommendations

There are three concerns relating to the power supply of these products: the effects of *Power Supply Noise* upon the conversion process, the *Digital Output Effect Upon Noise* upon the conversion process, and *Power Management* of the product.

9.1 Power Supply Noise

Because the supply voltage of the ADCS747x is the reference voltage, any noise greater than 1/2 LSB in amplitude has some effect upon the converter noise performance. This effect is proportional to the input voltage level. The power supply must receive all the considerations of a reference voltage as far as stability and noise is concerned. Using the same supply voltage for these devices as is used for digital components leads to degraded noise performance.

9.2 Digital Output Effect Upon Noise

The charging of any output load capacitance requires current from the digital supply, V_{DD}. The current pulses required from the supply to charge the output capacitance causes voltage variations at the ADC supply line. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate, causing *ground bounce* noise in the substrate that degrades noise performance if that current is large enough. The larger the output capacitance, the more current flows through the device power supply line and die substrate and the greater is the noise coupled into the analog path.

The first solution to keeping digital noise out of the power supply is to decouple the supply from any other components or use a separate supply for the ADC. To keep noise out of the supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100-Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This limits the charge and discharge current of the output capacitance and improve noise performance. Because the series resistor and the load capacitance form a low frequency pole, verify signal integrity when the series resistor is added.

9.3 Power Management

When ADCS747x is operated continuously in normal mode, throughput up to 1 MSPS can be achieved. The user may trade throughput for power consumption by simply performing fewer conversions per unit time and putting the ADCS747x into shutdown mode between conversions. This method is not advantageous beyond 350-kSPS throughput.

Power Management (continued)

A plot of maximum power consumption versus throughput is shown in Figure 35. To calculate the power consumption for a given throughput, remember that each time the part exits shutdown mode and enters normal mode, one dummy conversion is required. Generally, the user puts the part into normal mode, execute one dummy conversion followed by one valid conversion, and then put the part back into shutdown mode. When this is done, the fraction of time spent in normal mode may be calculated by multiplying the throughput (in samples per second) by 2 µs, the time taken to perform one dummy and one valid conversion. The power consumption can then be found by multiplying the fraction of time spent in normal mode by the normal mode power consumption figure. The power dissipated while the part is in shutdown mode is negligible.

For example, to calculate the power consumption at 300 kSPS with V_{DD} = 5 V, begin by calculating the fraction of time spent in normal mode: 300,000 samples/second x 2 µs = 0.6, or 60%. The power consumption at 300 kSPS is then 60% of 17.5 mW (the maximum power consumption at V_{DD} = 5 V) or 10.5 mW.

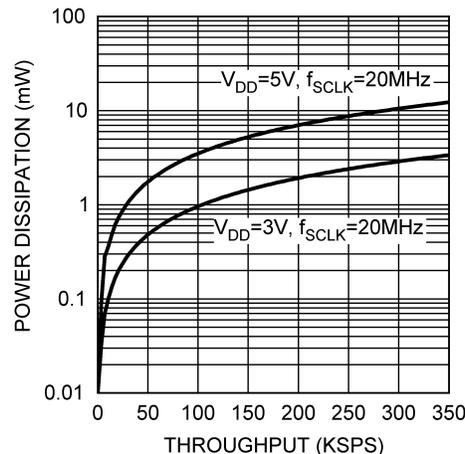**Figure 35. Maximum Power Consumption vs Throughput**

10 Layout

10.1 Layout Guidelines

Capacitive coupling between noisy digital circuitry and sensitive analog circuitry can lead to poor performance. The solution is to keep the analog and digital circuitry separated from each other and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. This digital noise could have significant impact upon system noise performance. To avoid performance degradation of the ADCS747x due to supply noise, do not use the same supply for the ADCS747x that is used for digital logic.

Generally, analog and digital lines must cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line must also be treated as a transmission line and be properly terminated.

The analog input must be isolated from noisy signal lines to avoid coupling of spurious signals into the input. Any external component (that is, a filter capacitor) connected between the input pins and ground of the converter or to the reference input pin and ground must be connected to a very clean point in the ground plane.

TI recommends the use of a single, uniform ground plane and the use of split power planes. The power planes must be placed within the same board layer. All analog circuitry (input amplifiers, filters, reference components, and so on) must be placed over the analog power plane. All digital circuitry and I/O lines must be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground must be connected together with short traces and enter the analog ground plane at a single, quiet point.
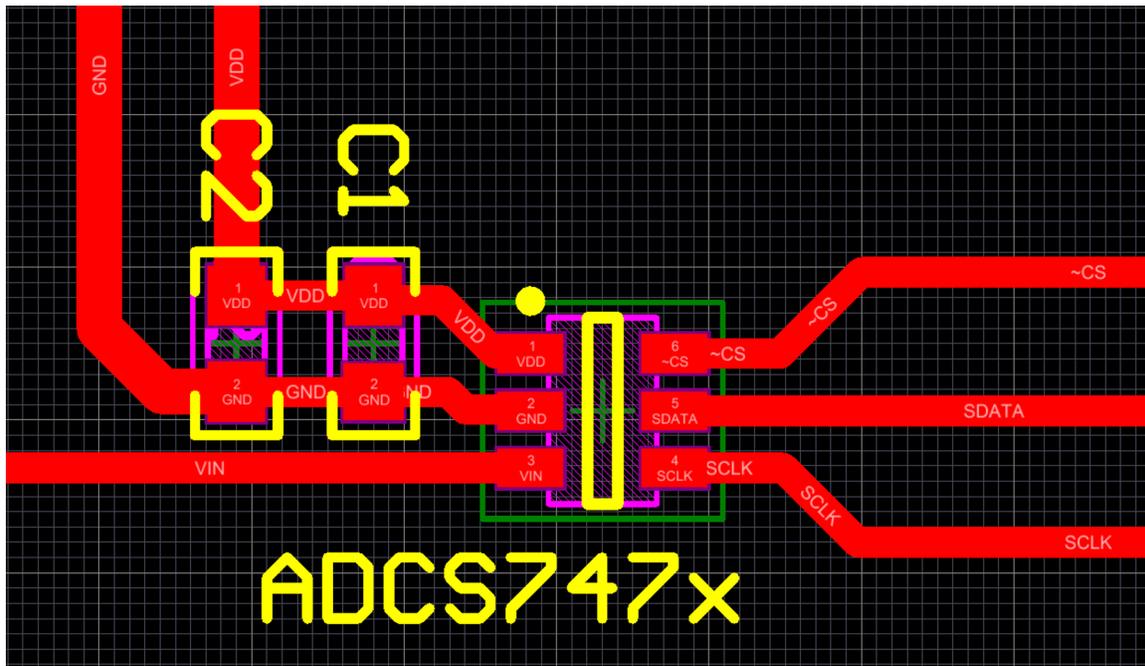
Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

10.2 Layout Example

Figure 36. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

APERTURE DELAY is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} − 1.5 LSB for ADCS7476 and ADCS7477, V_{REF} − 1 LSB for ADCS7478), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the either the two second order or all four third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that never appear at the ADC outputs. ADCS747x is ensured not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (that is, GND + 0.5 LSB for the ADCS7476 and ADCS7477, and GND + 1 LSB for the ADCS7478).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first five harmonic levels at the output to the level of the fundamental at the output. THD is calculated as:

$$THD = 20 \times \log \sqrt{\frac{f_2{}^2 + \ldots + f_6{}^2}{f_1{}^2}}$$

where
- f_1 is the RMS power of the fundamental (output) frequency
- f_2 through f_6 are the RMS power in the first 5 harmonic frequencies (1)

Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

Device Support (continued)

TOTAL UNADJUSTED ERROR is the worst deviation found from the ideal transfer function. As such, it is a comprehensive specification which includes full scale error, linearity error, and offset error.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

SPI, QSPI, MICROWIRE, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Product Folder Links: *ADCS7476 ADCS7477 ADCS7478*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADCS7476AIMF	NRND	SOT-23	DBV	6	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	X01A	
ADCS7476AIMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	X01A	Samples
ADCS7476AIMFE/NOPB	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	X01A	Samples
ADCS7476AIMFX	NRND	SOT-23	DBV	6	3000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	X01A	
ADCS7476AIMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	X01A	Samples
ADCS7477AIMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	X02A	Samples
ADCS7477AIMFE/NOPB	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	X02A	Samples
ADCS7477AIMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	X02A	Samples
ADCS7478AIMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	X03A	Samples
ADCS7478AIMFE/NOPB	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	X03A	Samples
ADCS7478AIMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	X03A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
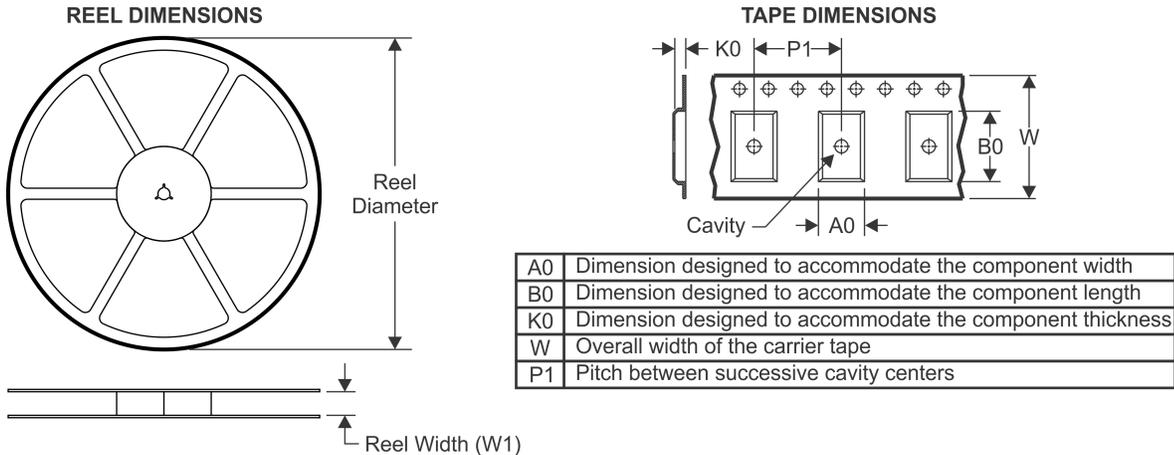
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
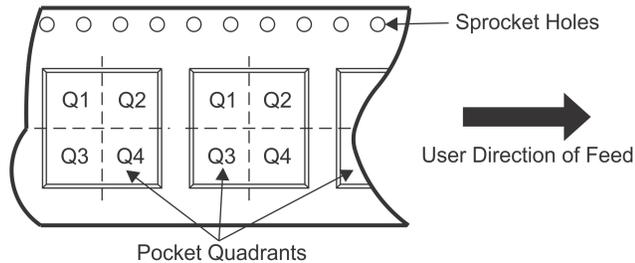
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADCS7476AIMF	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7476AIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7476AIMFE/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7476AIMFX	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7476AIMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7477AIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7477AIMFE/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7477AIMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7478AIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7478AIMFE/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7478AIMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS
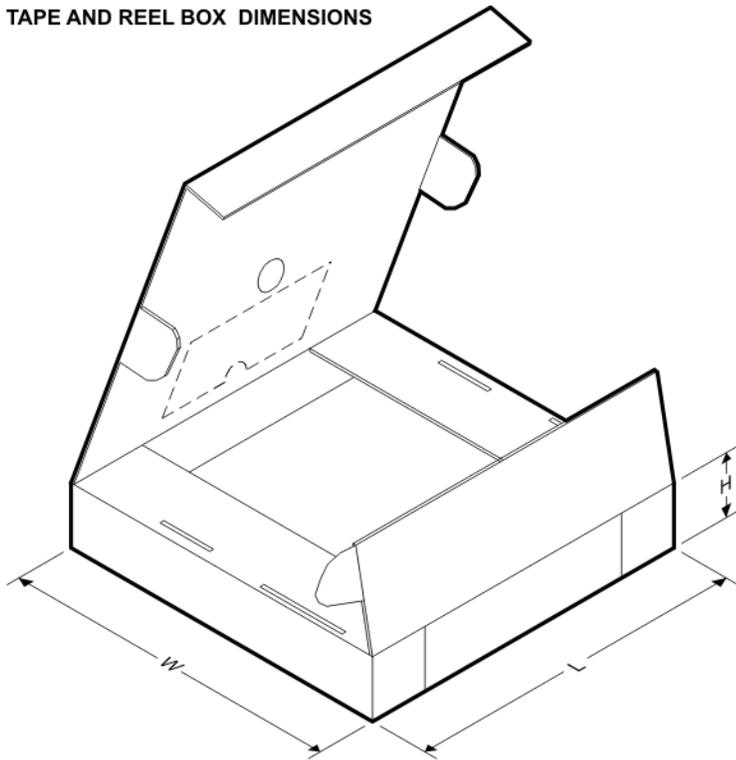
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADCS7476AIMF	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADCS7476AIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADCS7476AIMFE/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
ADCS7476AIMFX	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADCS7476AIMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADCS7477AIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADCS7477AIMFE/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
ADCS7477AIMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADCS7478AIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADCS7478AIMFE/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
ADCS7478AIMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
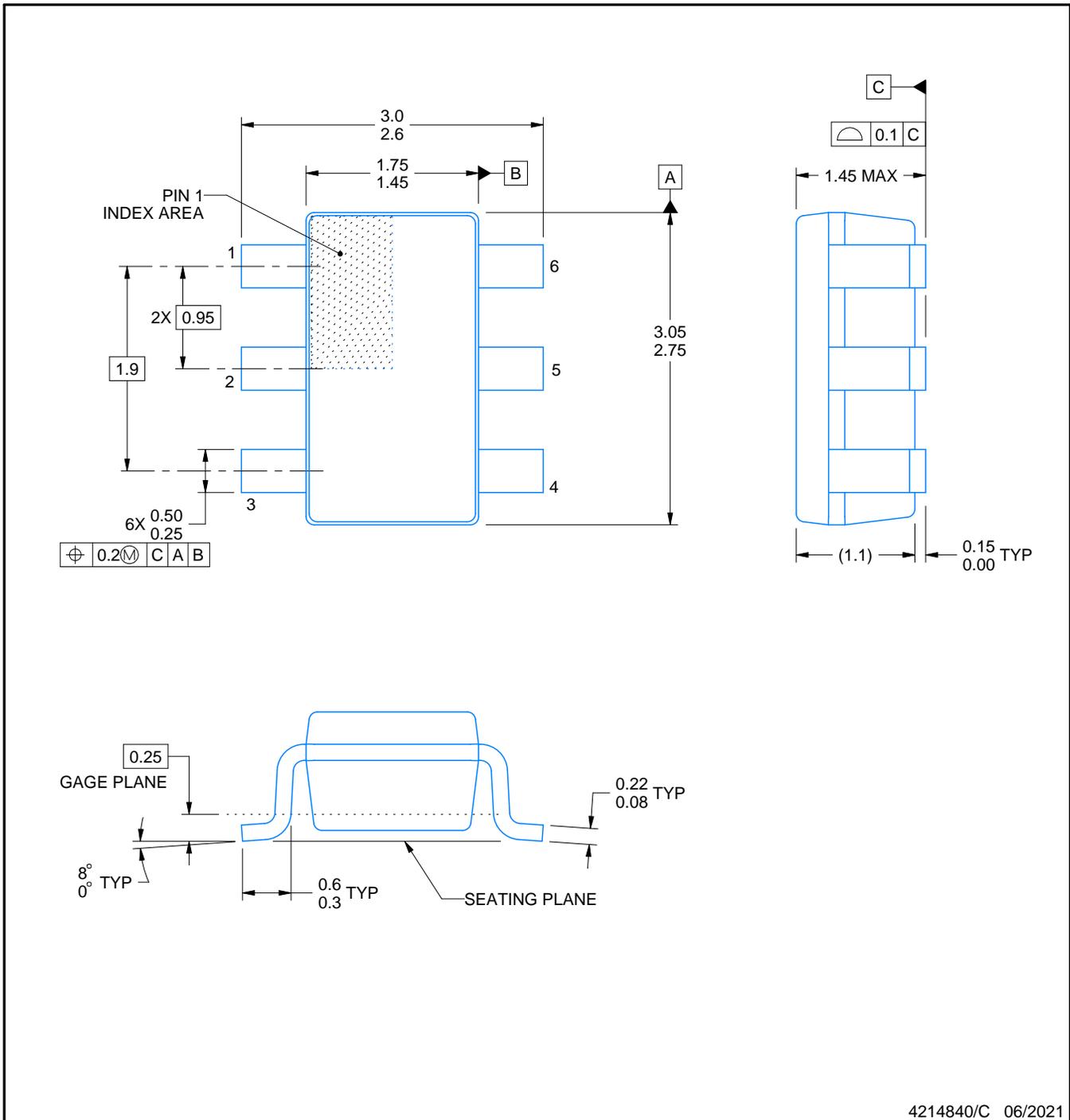
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

PKG ℄

6X (1.1)

1

6X (0.6)

6

2

SYMM ℄

5

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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INSTRUMENTS
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PKG
$\mathbb{C}$

6X (1.1)

1

6X (0.6)

2

SYMM
$\mathbb{C}$

5

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C   06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.