SN65HVDA540-Q1, SN65HVDA541-Q1
SN65HVDA542-Q1, SN65HVDA540-5-Q1
SN65HVDA541-5-Q1, SN65HVDA542-5-Q1

SLLS804D – MARCH 2009 – REVISED AUGUST 2016

SN65HVDA54x-Q1, SN65HVDA54x-5-Q1 5-V Can Transceiver With I/O Level Adapting and Low-Power Mode Supply Optimization

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
  - Device MM ESD Classification Level M4
- Meets or Exceeds the Requirements of ISO 11898-2 and ISO 11898-5
- GIFT/ICT Compliant
- ESD Protection up to ±12 kV (Human-Body Model) on Bus Pins
- I/O Voltage Level Adapting
  - SN65HVDA54x: Adaptable I/O Voltage Range (V_{IO}) From 3 V to 5.33 V
  - SN65HVDA54x-5: 5 V V_{CC} Device Version
- Operating Modes:
  - Normal Mode: All Devices
  - Low Power Standby Mode (V_{CC} Not Required, Only V_{IO} Supply Needed Saving System Power)
    - SN65HVDA540: No Wake Up
    - SN65HVDA541: RXD Wake Up Request
  - Silent (Receive Only) Mode: HVDA542
- High Electromagnetic Compliance (EMC)
- Protection
  - Undervoltage Protection on V_{IO} and V_{CC}
  - Bus-Fault Protection of –27 V to 40 V
  - TXD Dominant State Time Out
  - RXD Wake Up Request Lock Out on CAN Bus Stuck Dominant Fault (HVDA541)
  - Thermal Shutdown Protection
  - Power-Up/Down Glitch-Free Bus I/O
  - High Bus Input Impedance When Unpowered (No Bus Load)

2 Applications

- SAE J2284 High-Speed CAN for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- GMW3122 Dual-Wire CAN Physical Layer
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface

3 Description

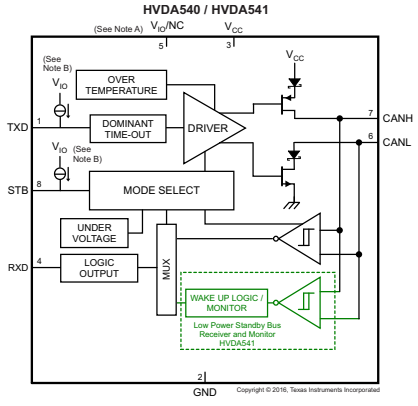
The SN65HVDA54x-Q1 and SN65HVDA54x-5-Q1 devices, known as the HVDA54x and HVDA54x-5 respectively, are designed and qualified for use in automotive applications and meets or exceeds the specifications of the ISO 11898 High Speed CAN (Controller Area Network) Physical Layer standard (transceiver).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVDA54x-Q1, SN65HVDA54x-5-Q1	SOIC (8)	4.90 mm × 3.91 mm

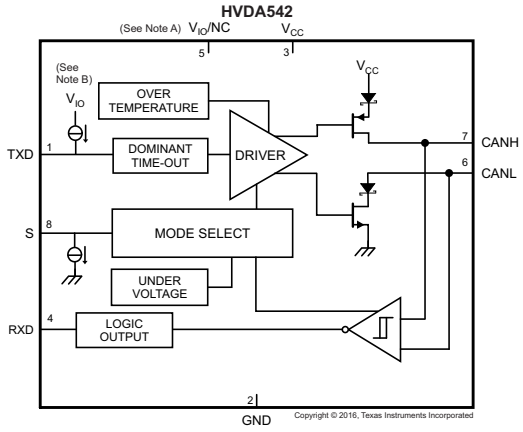
(1) For all available packages, see the orderable addendum at the end of the data sheet.

HVDA54x Functional Block Diagram



HVDA54x devices pin 5 is V_{IO}. HVDA54x-5 devices pin 5 is NC and V_{IO} is internally connected to V_{CC}.

HVDA54x-5 Functional Block Diagram



HVDA54x-5 devices: V_{IO} is internally connected to V_{CC}

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2012) to Revision D **Page**

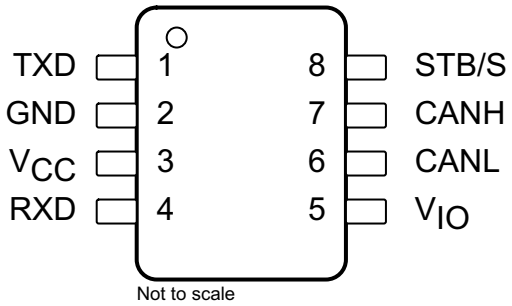
- Changed device numbers From: SN65HVD54x-Q1 To: HVD54x-Q1 ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed *Ordering Information* table, see POA at the end of the data sheet ... 4

Changes from Revision B (September 2010) to Revision C **Page**

- Deleted DSJ package info ... 1
- Deleted DSJ package info ... 3
- Added note in line 4.5 Test Conditions, "T_A = –40°C, 25°C, 125°C" ... 5
- Deleted DSJ package info ... 8
- Deleted DSJ (VSON) package info ... 17

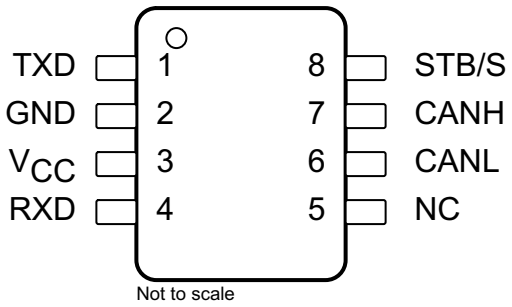
5 Pin Configuration and Functions

HVDA54x D Package
8-Pin SOIC
Top View



Not to scale

HVDA54x-5 D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	HVDA54x	HVDA54x-5		
CANH	7	7	I/O	High level CAN bus line
CANL	6	6	I/O	Low level CAN bus line
GND	2	2	GND	Ground connection
NC	—	5	Supply	HVDA54x: Transceiver logic level (IO) supply voltage HVDA54x-5: No connect
RXD	4	4	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
STB/S	8	8	I	Mode select: STB, Standby mode (HVDA540/541) select pin (active high) S, Silent mode (HVDA542) select pin (active high)
TXD	1	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
V_{CC}	3	3	Supply	Transceiver 5V supply voltage
V_{IO}	5	—	Supply	HVDA54x: Transceiver logic level (IO) supply voltage HVDA54x-5: No connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	6	V
V_{IO}	I/O supply voltage		–0.3	6	V
	Voltage at bus terminals (CANH, CANL)		–27	40	V
I_O	Receiver output current (RXD)			20	mA
V_I	Voltage input (TXD, STB, S)	HVDA54x	–0.3	6 V and $V_I \le V_{IO} + 0.3$	V
		HVDA54x-5	–0.3	6	V
T_J	Operating virtual-junction temperature		–40	150	°C
T_{LEAD}	Lead temperature (soldering, 10 seconds)			260	°C
T_{stg}	Storage temperature				°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except 6 and 7	±4000	V
			Pins 6 and 7(2)	±12000	
		Charged-device model (CDM), per AEC Q100-011		±1000	
		Machine model		±7000	
		IEC 61000-4-2 contact discharge(3)	Pins 6 and 7 to pin 2	±7000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) HBM test method based on AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
(3) IEC 61000-4-2 is a system level ESD test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations will lead to different results.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.68	5.33	V
V_{IO}	I/O supply voltage		3	5.33	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, STB, S (for HVD54x-5: $V_{IO} = V_{CC}$)	0.7 × V_{IO}	V_{IO}	V
V_{IL}	Low-level input voltage	TXD, STB, S (for HVD54x-5: $V_{IO} = V_{CC}$)	0	0.3 × V_{IO}	V
V_{ID}	Differential input voltage, bus	Between CANH and CANL	–6	6	V
I_{OH}	High-level output current	RXD	–2		mA
I_{OL}	Low-level output current	RXD		2	mA
T_A	Operating ambient free-air temperature	See *Thermal Information* and *Power Dissipation Ratings*	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]			HVDA54x, HVDA54x-5-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K thermal resistance	140	°C/W
		High-K thermal resistance	112	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		50	°C/W
ψ_{JT}	Junction-to-top characterization parameter		13	°C/W
ψ_{JB}	Junction-to-board characterization parameter		55	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA54x-5 devices $V_{IO} = V_{CC}$

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
SUPPLY CHARACTERISTICS (HVDA54x)							
I_{CC}	5-V supply current	Standby mode (HVDA540/541 Only)	STB at V_{IO}, V_{CC} = 5.33 V, V_{IO} = 3 V, TXD at V_{IO} [2]			5	µA
		Normal mode (Dominant)	TXD at 0 V, 60-Ω load, STB / S at 0 V		50	70	mA
		Normal mode (Recessive)	TXD at V_{IO}, No load, STB / S at 0 V or S at V_{IO}		5.5	10	
		Silent Mode (HVDA542 only)	TXD at V_{IO}, No load, STB / S at 0 V or S at V_{IO}		5.5	10	
I_{IO}	I/O supply current	Standby mode (HVDA540/541 Only)	STB at V_{IO} , V_{CC} = 5.33 V or 0 V, RXD floating, TXD at V_{IO} T_A = –40°C, 25°C, 125°C[3]		7	15	µA
		Normal mode (recessive or dominant) and Silent Mode (HVDA542 Only)	V_{CC} = 5.33 V, RXD floating, TXD at 0 V or V_{IO}. Normal Mode: STB or S at 0 V. Silent Mode (HVDA542): S at V_{IO}.		75	300	
UV_{VCC}	Undervoltage detection on V_{CC} for forced standby mode			3.2	3.6	4	V
$V_{HYS(UVVCC)}$	Hysteresis voltage for undervoltage detection on UV_{VCC} for standby mode				200		mV
UV_{VIO}	Undervoltage detection on V_{IO} for forced standby mode			1.9	2.45	2.95	V
$V_{HYS(UVVIO)}$	Hysteresis voltage for undervoltage detection on UV_{VIO} for forced standby mode				130		mV

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 3.3 V.
(2) The V_{CC} supply is not needed during standby mode so in the application I_{CC} in standby mode may be zero. If the V_{CC} supply remains, then I_{CC} is per specification with V_{CC}.
(3) See *SN65HVDA54x-Q1 Errata* .

Electrical Characteristics (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA54x-5 devices $V_{IO} = V_{CC}$

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
SUPPLY CHARACTERISTICS (HVDA54x-5)							
I_{CC}	5-V supply current	Standby mode (HVDA540-5/541-5 Only)	STB at V_{CC}, V_{CC} = 5.33 V, TXD at V_{CC} (2)			20	µA
		Normal mode (Dominant)	TXD at 0 V, 60-Ω load, STB / S at 0 V		50	70	mA
		Normal mode (Recessive)	TXD at V_{IO}, No load, STB / S at 0 V or S at V_{IO}		5.5	10	
		Silent Mode (HVDA542 only)	TXD at V_{IO}, No load, STB / S at 0 V or S at V_{IO}		5.5	10	
UV_{VCC}	Undervoltage detection on V_{CC} for forced standby mode			3.2	3.6	4	V
$V_{HYS(UVVCC)}$	Hysteresis voltage for undervoltage detection on UV_{VCC} for standby mode				240		mV
DEVICE SWITCHING CHARACTERISTICS: PROPAGATION TIME (LOOP TIME TXD TO RXD)							
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant		Figure 9, STB at 0 V	70		230	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			70		230	
DRIVER ELECTRICAL CHARACTERISTICS							
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB / S at 0 V, R_L = 60 Ω, See Figure 2 and Figure 15	2.9		4.5	V
		CANL		0.8		1.75	
$V_{O(R)}$	Bus output voltage (recessive)		$V_I = V_{IO}$, V_{IO} = 3 V, STB at 0 V or S at X(4), R_L = 60 Ω, See Figure 2 and Figure 15	2	2.5	3	V
$V_{O(STBY)}$	Bus output voltage, standby mode (HVDA540, HVDA541 only)		STB / S at V_{IO}, R_L = 60 Ω, See Figure 2 and Figure 15	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB / S at 0 V, See Figure 2, Figure 15, and Figure 3	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB / S at 0 V, See Figure 2, Figure 15, and Figure 3	1.4		3	
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB / S at 0 V, R_L = 60 Ω, See Figure 2 and Figure 15	–0.012		0.012	V
			V_I = 3 V, STB / S at 0 V, No load	–0.5		0.05	
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)} + V_{O(CANL)}$)		STB / S at 0 V, R_L = 60 Ω, See Figure 12	0.9 V_{CC}	V_{CC}	1.1 V_{CC}	V
$V_{OC(SS)}$	Steady-state common-mode output voltage		STB / S at 0 V, R_L = 60 Ω, See Figure 8	2	2.5	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		STB / S at 0 V, R_L = 60 Ω, See Figure 8		40		mV
$I_{OS(SS)\_DOM}$	Short-circuit steady-state output current, Dominant		V_{CANH} = 0 V, CANL open, TXD = low, See Figure 11	–100			mA
			V_{CANL} = 32 V, CANH open, TXD = low, See Figure 11			100	

(4) For the HVDA542 device the bus output voltage (recessive) will be the same if the device is in normal mode with S pin at 0 V or if the device is in silent mode with the S pin at HIGH.

Electrical Characteristics (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA54x-5 devices $V_{IO} = V_{CC}$

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{OS(SS)\_REC}$	Short-circuit steady-state output current, Recessive	–20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, See Figure 11	–10		10	mA
		–20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, See Figure 11	–10		10	
C_O	Output capacitance	See receiver input capacitance				
DRIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high level output	STB / S at 0 V, See Figure 4		65		ns
t_{PHL}	Propagation delay time, high-to-low level output	STB / S at 0 V, See Figure 4		50		ns
t_R	Differential output signal rise time	STB / S at 0 V, See Figure 4		25		ns
t_F	Differential output signal fall time	STB / S at 0 V, See Figure 4		55		ns
t_{EN}	Enable time from standby or silent mode to normal mode dominant	See Figure 7			20	µs
$t_{(DOM)}$ (5)	Dominant time out	See Figure 10	300	400	700	µs
RECEIVER ELECTRICAL CHARACTERISTICS						
V_{IT+}	Positive-going input threshold voltage, normal mode	STB / S at 0 V, See Table 1		800	900	mV
$V_{IT–}$	Negative-going input threshold voltage, normal mode	STB / S at 0 V, See Table 1	500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)		100	125		mV
$V_{IT(STBY)}$	Input threshold voltage, standby mode (HVDA541 only)	STB at V_{IO}	400		1150	mV
$I_{I(OFF\_LKG)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5 V, V_{CC} at 0 V, V_{IO} at 0 V, TXD at 0 V			3	µA
C_I	Input capacitance to ground (CANH or CANL)	HVDA54x: TXD at V_{IO}, V_{IO} at 3.3 V. HVDA54x-5: TXD at V_{CC} V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C_{ID}	Differential input capacitance	HVDA54x: TXD at V_{IO}, V_{IO} at 3.3 V. HVDA54x-5: TXD at V_{CC} V_I = 0.4 sin(4E6πt)		5		pF
R_{ID}	Differential input resistance	HVDA54x: TXD at V_{IO}, V_{IO} = 3.3 V, STB at 0 V HVDA54x-5: TXD at V_{CC}, STB at 0 V	29		80	kΩ
R_{IN}	Input resistance (CANH or CANL)		14.5	25	40	kΩ
$R_{I(M)}$	Input resistance matching [1 – ®$_{IN(CANH)}$/$R_{IN(CANL)}$)] × 100%	$V_{(CANH)} = V_{(CANL)}$	–3	0	3	%
RECEIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high-level output	STB / S at 0 V , See Figure 6		95		ns
t_{PHL}	Propagation delay time, high-to-low-level output	STB / S at 0 V , See Figure 6		60		ns
t_R	Output signal rise time	STB / S at 0 V , See Figure 6		13		ns
t_F	Output signal fall time	STB / S at 0 V , See Figure 6		10		ns

(5) The TXD dominant time out ($t_{(DOM)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(DOM)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(DOM)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ $t_{(DOM)}$ = 11 bits / 300 µs = 37 kbps

Electrical Characteristics (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA54x-5 devices $V_{IO} = V_{CC}$

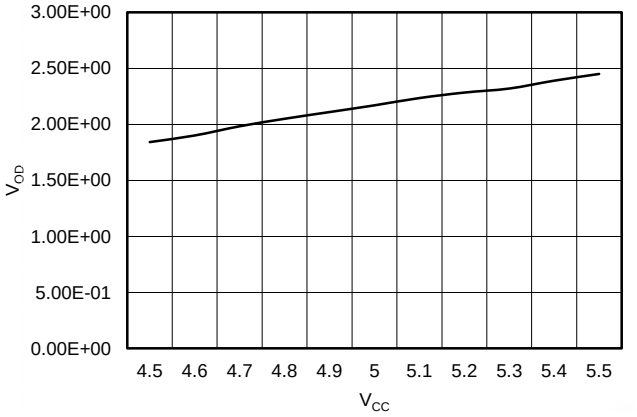
PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{BUS}	Dominant time required on bus for wake-up from standby (HVDA541 only)	STB at V_{IO}, See Figure 17 and Figure 18	1.5		5	µs
t_{CLEAR}	Recessive time on the bus to clear the standby mode receiver output (RXD) if standby mode is entered while bus is dominant (HVDA541 only)		1.5		5	µs
TXD PIN CHARACTERISTICS						
V_{IH}	High-level input voltage	HVD54x-5: $V_{IO} = V_{CC}$	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	HVD54x-5: $V_{IO} = V_{CC}$			0.3 × V_{IO}	V
I_{IH}	High-level input current	HVDA54x: TXD at V_{IO} HVDA54x-5: TXD at V_{CC}	–2		2	µA
I_{IL}	Low-level input current	TXD at 0 V	–100		–7	µA
RXD PIN CHARACTERISTICS						
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 6 HVD54x-5: $V_{IO} = V_{CC}$	0.8 × V_{IO}			V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 6 HVD54x-5: $V_{IO} = V_{CC}$			0.2 × V_{IO}	V
STB PIN CHARACTERISTICS (HVDA540 AND HVDA541 ONLY)						
V_{IH}	High-level input voltage	HVD54x-5: $V_{IO} = V_{CC}$	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	HVD54x-5: $V_{IO} = V_{CC}$			0.3 × V_{IO}	V
I_{IH}	High-level input current	HVDA54x: STB at V_{IO} HVDA54x-5: STB at V_{CC}	–2		2	µA
I_{IL}	Low-level input current	STB at 0 V	–20			µA
S PIN CHARACTERISTICS (HVDA542 ONLY)						
V_{IH}	High-level input voltage	HVD54x-5: $V_{IO} = V_{CC}$	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	HVD54x-5: $V_{IO} = V_{CC}$			0.3 × V_{IO}	V
I_{IH}	High-level input current	HVDA54x: S at V_{IO} HVDA54x-5: S at V_{CC}			30	µA
I_{IL}	Low-level input current	S at 0 V	–2		2	µA
	Thermal shutdown temperature			185		°C

6.6 Power Dissipation Ratings

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA54x-5 devices $V_{IO} = V_{CC}$

			MIN	TYP	MAX	UNIT
P_D	Average power dissipation	V_{CC} = 5 V, $V_{IO} = V_{CC}$, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		140		mW
		V_{CC} = 5.33 V, $V_{IO} = V_{CC}$, T_J = 130°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			215	

6.7 Typical Characteristics



STB = 0 V RL= 60 Ω CL= Open Rcm= open
Temp = 25°C

Figure 1. HVDA540 V_{CC} vs V_{OD} from 4.5 V to 5.5 V

7 Parameter Measurement Information

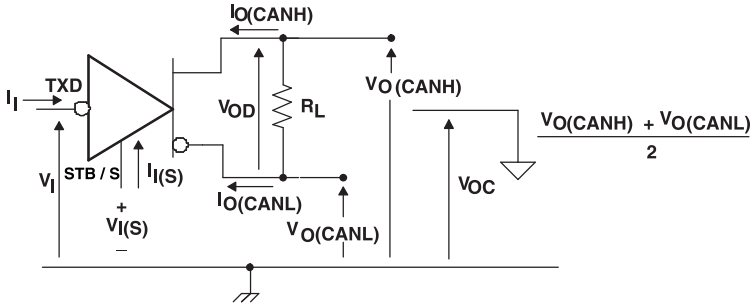


Figure 2. Driver Voltage, Current, and Test Definition

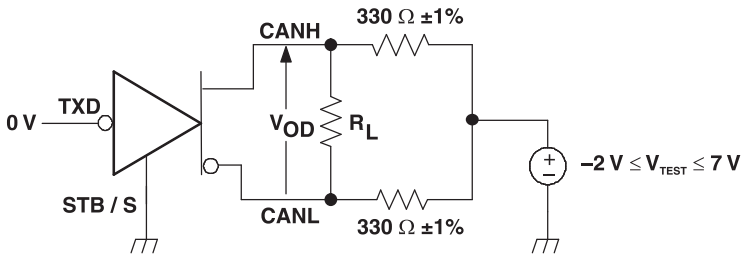
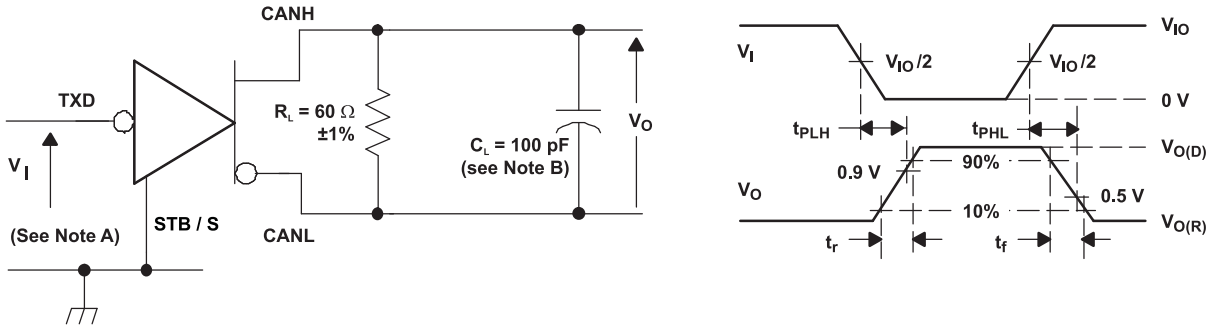


Figure 3. Driver V_{OD} Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

C. For HVDA54x-5 device versions, $V_{IO} = V_{CC}$.

Figure 4. Driver Test Circuit and Voltage Waveforms

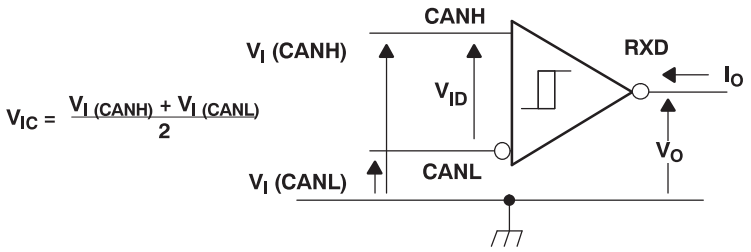
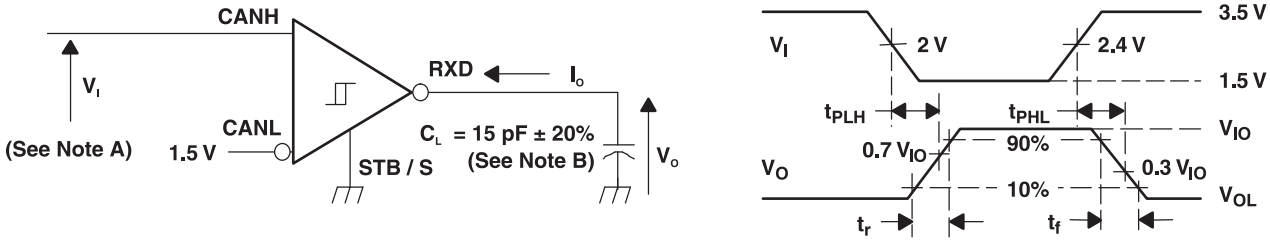


Figure 5. Receiver Voltage and Current Definitions

Parameter Measurement Information (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

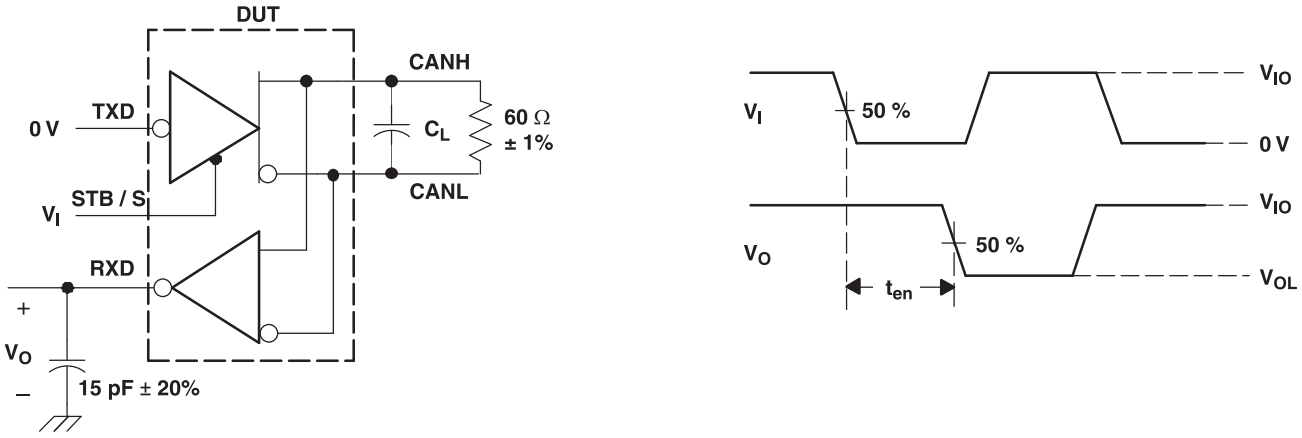
B. C_L includes instrumentation and fixture capacitance within ±20%.

C. C. For HVDA54x-5 device versions $V_{IO} = V_{CC}$.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

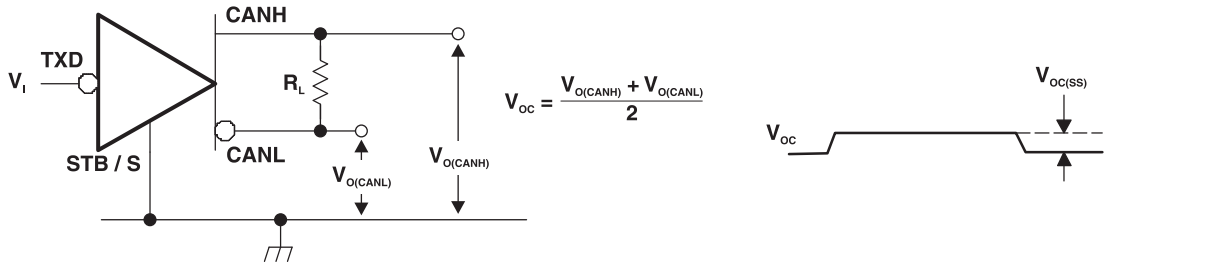


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 25 kHz, 50% duty cycle.

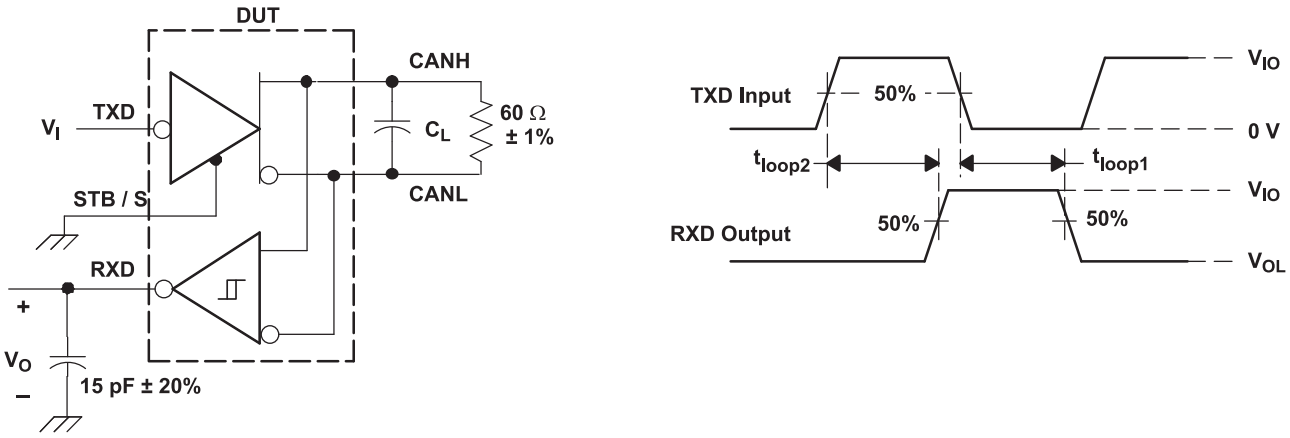
C. C. For HVDA54x-5 device versions $V_{IO} = V_{CC}$.

Figure 7. t_{EN} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Common-Mode Output Voltage Test and Waveforms

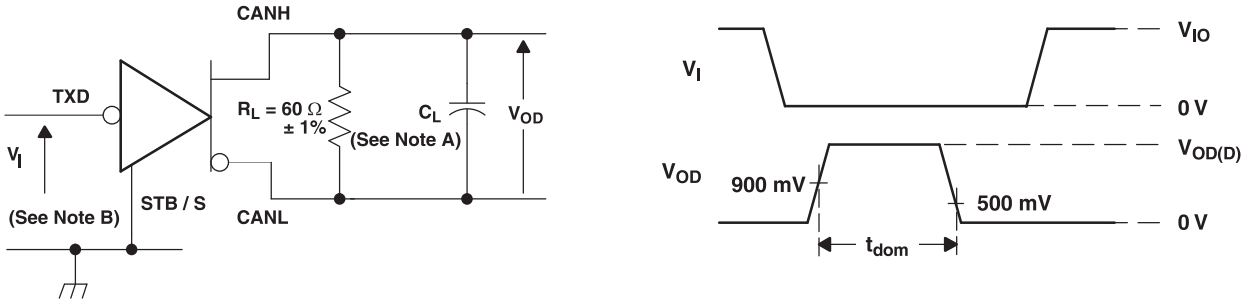


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

C. For HVDA54x-5 device versions, $V_{IO} = V_{CC}$.

Figure 9. $t_{PROP(LOOP)}$ Test Circuit and Waveform

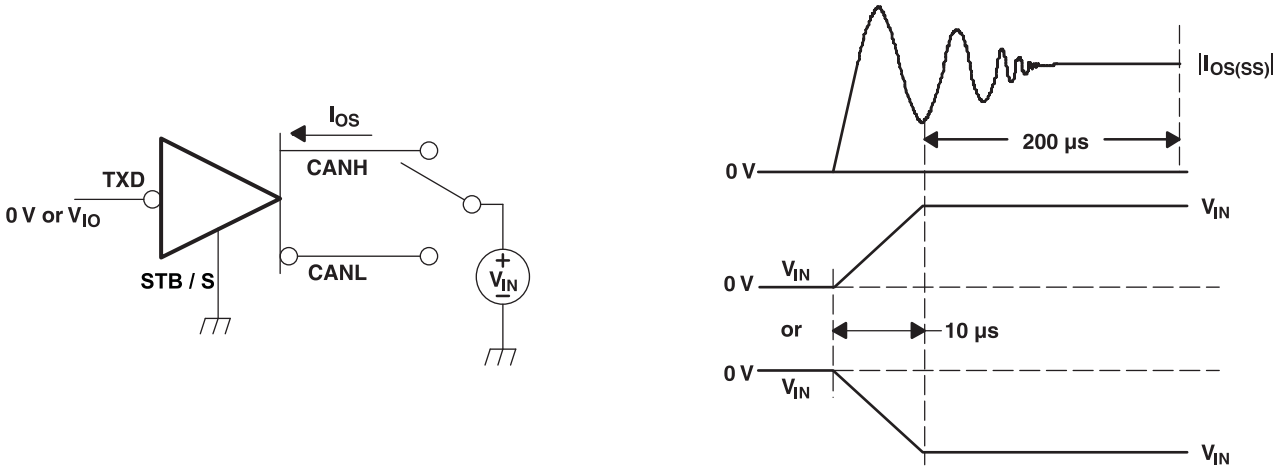


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

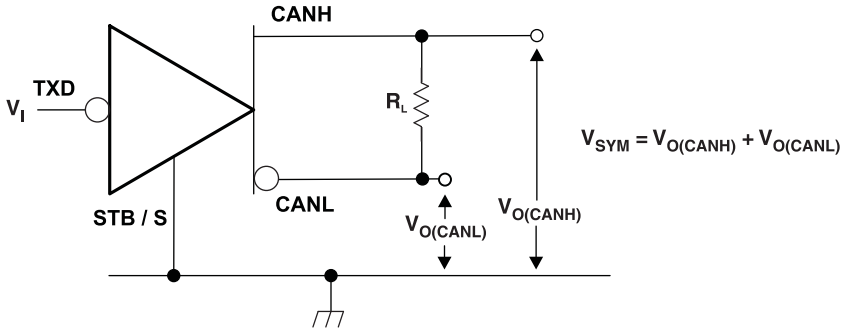
C. For HVDA54x-5 device versions, $V_{IO} = V_{CC}$.

Figure 10. TXD Dominant Time Out Test Circuit and Waveforms



A. For HVDA54x-5 device versions $V_{IO} = V_{CC}$.

Figure 11. Driver Short-Circuit Current Test and Waveforms



A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: $t_r/t_f \leq 6$ ns, Pulse Repetition Rate (PRR) = 250 kHz, 50% duty cycle.

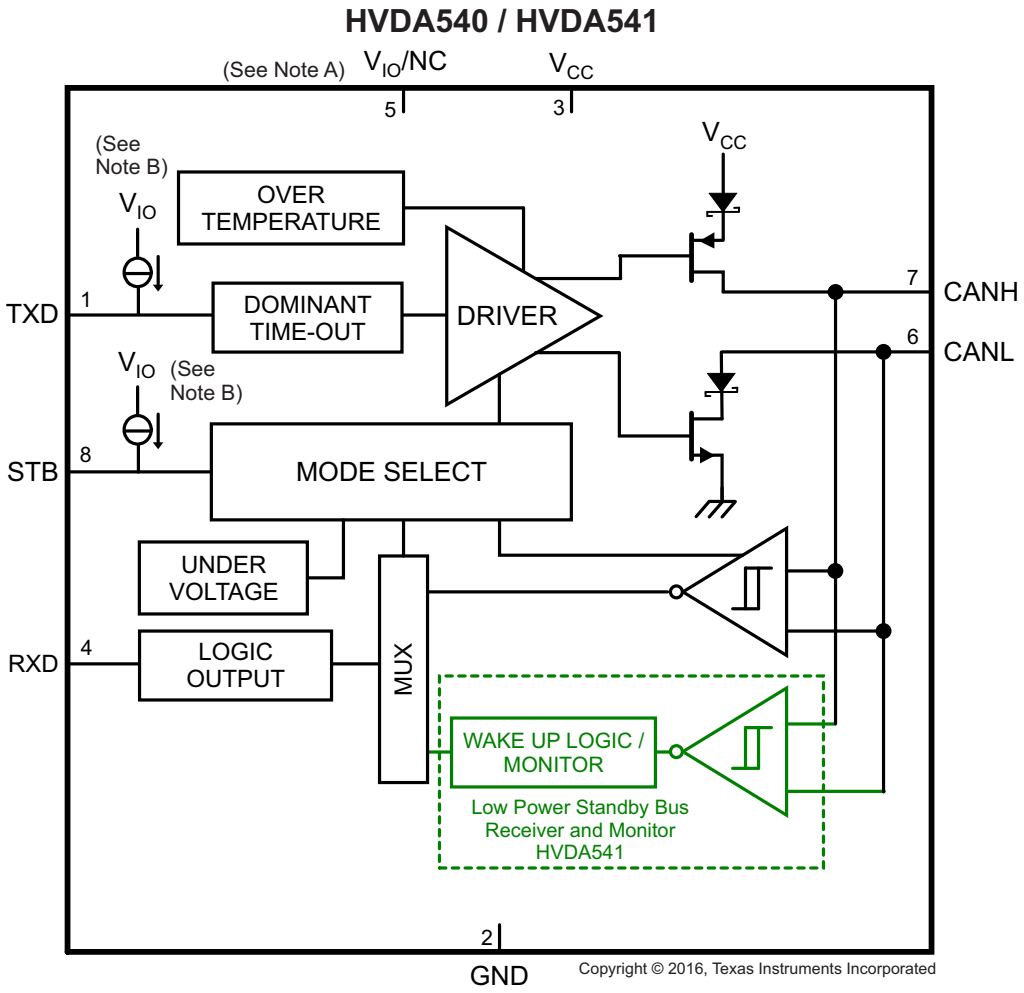
Figure 12. Driver Output Symmetry Test Circuit

8 Detailed Description

8.1 Overview

The device meets or exceeds the specifications of the ISO 11898 High Speed CAN (Controller Area Network) Physical Layer standard (transceiver). This device provides CAN transceiver functions: differential transmit capability to the bus and differential receive capability at data rates up to 1 megabit per second (Mbps). The device includes many protection features providing device and CAN network robustness.

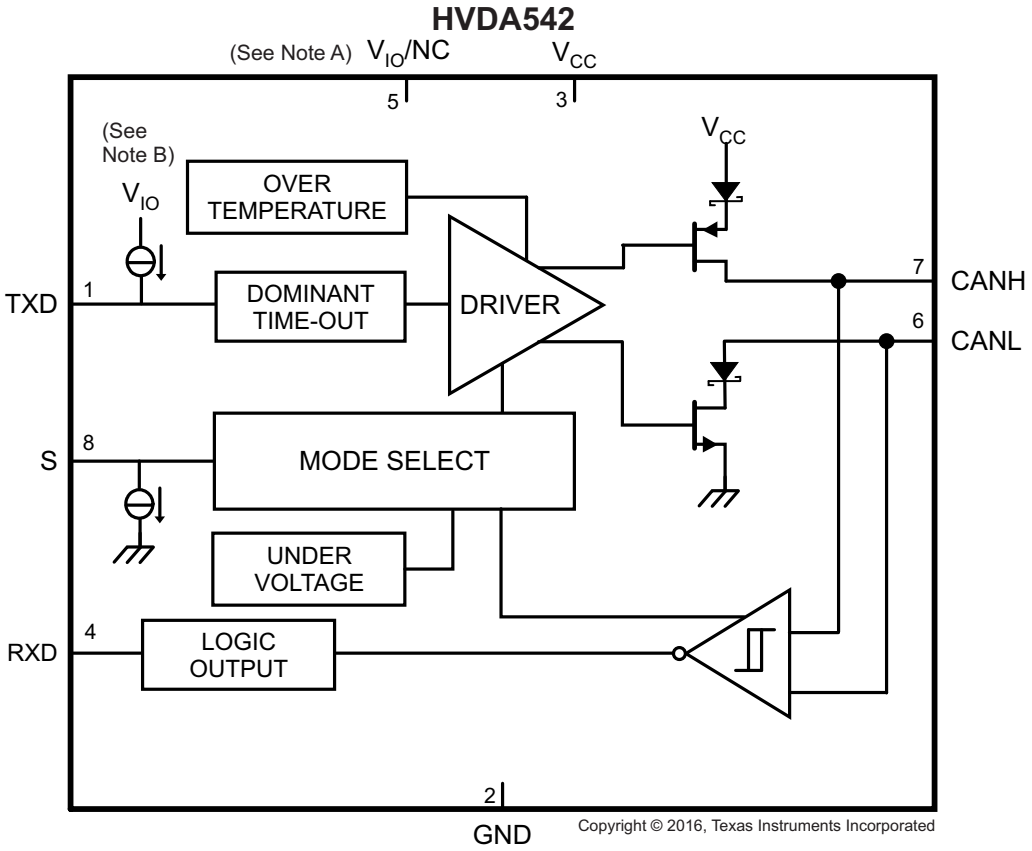
8.2 Functional Block Diagrams



HVDA54x devices pin 5 is V_{IO}. HVDA54x-5 devices pin 5 is NC and V_{IO} is internally connected to V_{CC}.

Figure 13. HVDA54x Functional Block Diagram

Functional Block Diagrams (continued)



HVDA54x-5 devices: V_{IO} is internally connected to V_{CC}

Figure 14. HVDA54x-5 Functional Block Diagram

8.3 Feature Description

8.3.1 Digital Inputs and Outputs

The HVDA54x devices have an I/O supply voltage input pin (V_{IO}) to ratiometrically level shift the digital logic input and output levels with respect to V_{IO} for compatibility with protocol controllers having I/O supply voltages between 3 V and 5.33 V.

The HVDA54x-5 devices have a single V_{CC} supply (5 V). The digital logic input and output levels for these devices are with respect to V_{CC} for compatibility with protocol controllers having I/O supply voltages between 4.68 V and 5.33 V.

8.3.2 TXD Dominant State Time Out

During normal mode, the only mode where the CAN driver is active, the TXD dominant time out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period $t_{(DOM)}$. The dominant time out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit expires ($t_{(DOM)}$) the CAN bus driver is disabled freeing the bus for communication between other network nodes. The CAN driver is reactivated when a recessive signal is seen on TXD pin, thus clearing the dominant state time out. The CAN bus pins is biased to recessive level during a TXD dominant state time out.

Feature Description (continued)

NOTE

The maximum dominant TXD time allowed by the TXD Dominant state time out limits the minimum possible data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(DOM)}$ minimum, limits the minimum bit rate.

The minimum bit rate may be calculated in Equation 1:

$$\text{Minimum Bit Rate} = 11/t_{(DOM)} \quad (1)$$

8.3.3 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device will turn off the CAN driver circuits. This condition is cleared once the temperature drops below the thermal shut down temperature of the device. The CAN bus pins will be biased to recessive level during a thermal shutdown.

8.3.4 Undervoltage Lockout and Unpowered Device

Both of the supply pins have undervoltage detection which place the device in forced standby mode to protect the bus during an undervoltage event on either the V_{CC} or V_{IO} supply pins. If V_{IO} is undervoltage the RXD pin is tri-stated and the device does not pass any wake-up signals from the bus to the RXD pin. Since the device is placed into forced standby mode the CAN bus pins have a common mode bias to ground protecting the CAN network, see Figure 15 and Figure 16.

The device is designed to be an *ideal passive* load to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered so they will not load down the bus but rather be *no load*. This is critical, especially if some nodes of the network will be unpowered while the rest of the network remains in operation.

NOTE

Once an undervoltage condition is cleared and the V_{CC} and V_{IO} have returned to valid levels the device will typically need 300 µs to transition to normal operation.

Table 2. Undervoltage Protection

DEVICE	V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD
HVDA540	Bad	Good	Forced Standby Mode	Common mode bias to GND(1)	HIGH (Recessive)
HVDA541			Forced Standby Mode	Common mode bias to GND(1)	Mirrors bus state via wake-up filter(2)
HVDA542			Forced Standby Mode	Common mode bias to GND(1)	HIGH (Recessive)
HVDA54x	Good	Bad	Forced Standby Mode(3)	Common mode bias to GND(1)	tri-state
HVDA54x-5	Bad	N/A	Forced Standby Mode	Common mode bias to GND(1)	HIGH (Recessive) or tri-state
All Devices	Unpowered		Unpowered	No Load	High Z

(1) See Figure 15 and Figure 16 for common mode bias information.
(2) See Figure 17 and Figure 18 for operation of the low power wake up receiver and bus monitor for RXD Wake Up Request behavior and Table 5 for the wake up receiver threshold levels.
(3) When V_{IO} is undervoltage, the device is forced into standby mode with respect to the CAN bus since there is not a valid digital reference to determine the digital I/O states or power the wake-up receiver.

8.3.5 Floating Pins

The device has integrated pullup and pulldowns on critical pins to place the device into known states if the pins float. The TXD pin is pulled up to V_{IO} to force a recessive input level if the pin floats. The STB is pulled up to the IO supply pin, V_{IO}(HVDA540 and HVDA541), or V_{CC} (HVDA540-5 and HVDA541-5) to force the device in standby mode (low power) if the pin floats. The S pin is pulled down to GND to force the device into normal mode if the pin floats (HVDA542 and HVDA542-5).

8.3.6 CAN Bus Short-Circuit Current Limiting

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive) and TXD dominant state time out to prevent continuously driving dominant. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in termination resistance and common mode choke ratings the average short circuit current should be used. The device has TXD dominant state time out which prevents permanently having the higher short circuit current of dominant state. The CAN protocol also has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

NOTE

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents.

The average short circuit current may be calculated by Equation 2:

$$I_{OS(AVG)} = \%Transmit * [(\%REC\_Bits * I_{OS(SS)\_REC}) + (\%DOM\_Bits * I_{OS(SS)\_DOM})] + [\%Receive * I_{OS(SS)\_REC}] \quad (2)$$

where

- $I_{OS(AVG)}$ is the average short circuit current,
- %Transmit is the percentage the node is transmitting CAN messages,
- %Receive is the percentage the node is receiving CAN messages,
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages,
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages,
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- and $I_{OS(SS)\_DOM}$ is the dominant steady-state short circuit current.

8.4 Device Functional Modes

The device has two main operating modes: normal mode (all devices) and standby mode (HVDA540 / 541) or silent mode (HVDA542). Operating mode selection is made through the STB (HVDA540 / 541) or the S (HVDA542) input pin.

Table 3. Operating Modes

DEVICE	STB / S	MODE	DRIVER	RECEIVER	RXD Pin
All Devices	LOW	Normal Mode	Enabled (On)	Enabled (On)	Mirrors bus state(1)
HVDA540	HIGH	Standby Mode (No Wake Up)	Disabled (Off)	Disabled (Off)	Recessive (HIGH)
HVDA541	HIGH	Standby Mode (RXD Wake Up Request)	Disabled (Off)	Low power wake-up receiver and bus monitor enabled	Mirrors bus state via wake-up filter(2)
HVDA542	HIGH	Silent Mode	Disabled (Off)	Enabled (On)	Mirrors bus state(1)

(1) Mirrors bus state: LOW if CAN bus is dominant, HIGH if CAN bus is recessive.
(2) See Figure 17 and Figure 18 for operation of the low power wake up receiver and bus monitor for RXD Wake Up Request behavior and Table 5 for the wake up receiver threshold levels.

8.4.1 Bus States by Mode

The CAN bus has three valid states during powered operation depending on the mode of the device. In normal mode the bus may be dominant (logic LOW) where the bus lines are driven differentially apart or recessive (logic HIGH) where the bus lines are biased to $V_{CC}/2$ via the high-ohmic internal input resistors R_{IN} of the receiver. The third state is low power standby mode where the bus lines will be biased to GND via the high-ohmic internal input resistors R_{IN} of the receiver.

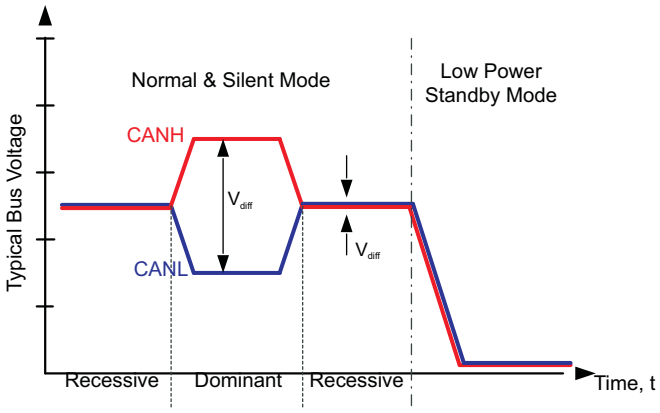


Figure 15. Bus States (Physical Bit Representation)

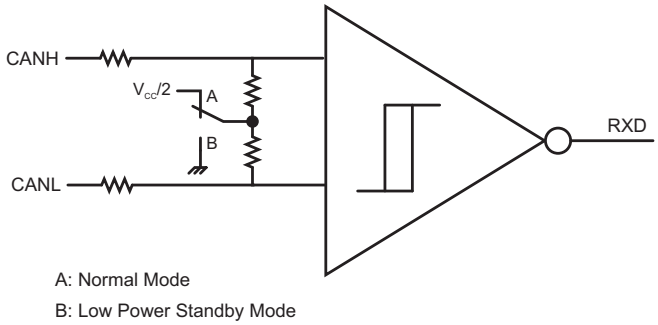


Figure 16. Simplified Common Mode Bias and Receiver Implementation

8.4.2 Normal Mode

This is the normal operating mode of the device. It is selected by setting STB or S low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state the CAN bus pins (CANH and CANL) are biased to $0.5 \times V_{CC}$. In dominant state the bus pins are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

8.4.3 Standby Mode (HVDA540)

This is the low power mode of the device. It is selected by setting STB high. The CAN driver and receiver are turned off and bidirectional CAN communication is not possible. There is no wake up capability in the HVDA540, the RXD pin will remain recessive (high) while the device is in standby mode. This state is supplied via the V_{IO} supply, thus the V_{CC} (5V) supply may be turned off for additional power savings at the system level. The local protocol controller (MCU) should reactivate the device to normal mode to enable communication via the CAN bus. The 5 V (V_{CC}) supply needs to be reactivated by the local protocol controller to resume normal mode if it has been turned off for low-power standby operation. The CAN bus pins are weakly pulled to GND, see Figure 15 and Figure 16.

8.4.4 Standby Mode With RXD Wake Up-Request (HVDA541)

This is the low power mode of the device. It is selected by setting STB high. The CAN driver and main receiver are turned off and bidirectional CAN communication is not possible. The low power receiver and bus monitor, both supplied via the V_{IO} supply, are enabled to allow for RXD wake up requests via the CAN bus. The V_{CC} (5V) supply may be turned off for additional power savings at the system level. A wake up request will be output to RXD (driven low) for any dominant bus transmissions longer than the filter time t_{BUS}. The local protocol controller (MCU) should monitor RXD for transitions and then reactivate the device to normal mode based on the wake up request. The 5 V (V_{CC}) supply needs to be reactivated by the local protocol controller to resume normal mode if it has been turned off for low-power standby operation. The CAN bus pins are weakly pulled to GND, see Figure 15 and Figure 16.

8.4.4.1 RXD Wake Up Request Lock Out for Bus Stuck Dominant Fault (HVDA541)

If the bus has a fault condition where it is stuck dominant while the HVDA541 is placed into standby mode via the STB pin, the device locks out the RXD wake up request until the fault has been removed to prevent false wake up signals in the system.

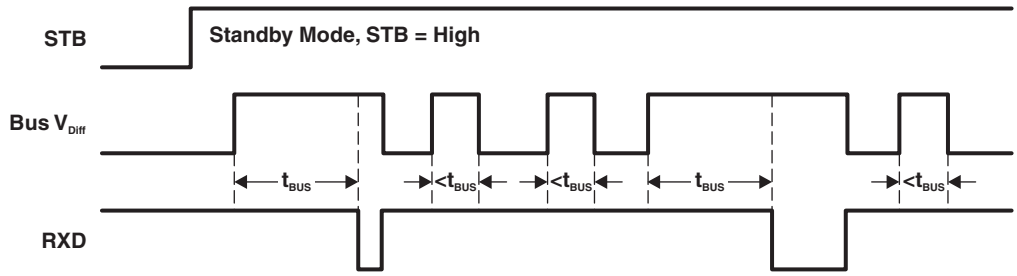


Figure 17. HVDA541 RXD Wake Up Request With No Bus Fault Condition

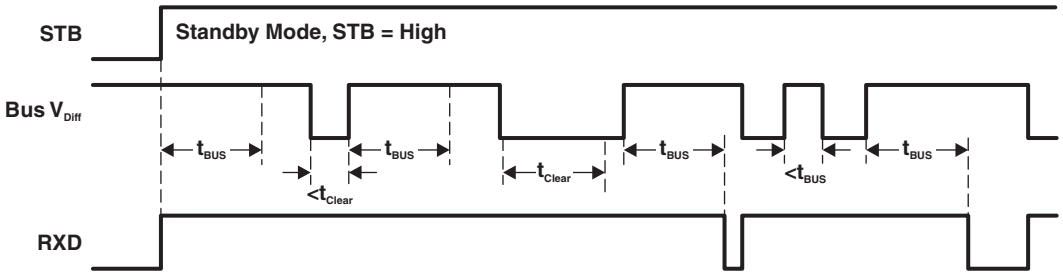


Figure 18. HVDA541 RXD Wake Up Request Lock Out When Bus Dominant Fault Condition

8.4.5 Silent (Receive Only) Mode (HVDA542)

This is the silent (receive only) mode of the device. It is selected by setting S high. The CAN driver is turned off while the receiver remains active and RXD will output the received bus state. There is no low power mode in the HVDA542 except for V_{CC} and V_{IO} supply undervoltage conditions (see *Undervoltage Lockout and Unpowered Device*).

8.4.6 Driver and Receiver Function Tables

Table 4. Driver Function Table

	INPUTS		OUTPUTS		DRIVEN BUS STATE
DEVICE	STB / S(1)	TXD(1)	CANH(1)	CANL(1)	
All Devices	L	L	H	L	Dominant
	L	H	Z	Z	Recessive
	L	Open	Z	Z	Recessive
HVDA540/541(2)	H	X	Y	Y	Recessive
HVDA542(3)	H	X	Z	Z	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = common mode bias to GND, Z = common mode bias to V_{CC}/2. See Figure 15 and Figure 16 for common mode bias information.
(2) HVDA540/541 have internal pull up to V_{IO} on STB pin. If STB pin is open the pin will be pulled high and the device will be in standby mode.
(3) HVDA542 has internal pulldown to GND on S pin. If S pin is open the pin will be pulled low and the device will be in normal mode.

Table 5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	BUS STATE	RXD PIN(1)
STANDBY (HVDA540)(2)	X	X	H
STANDBY WITH RXD WAKE UP REQUEST (HVDA541)(3)	$V_{ID} \geq 1.15$ V	DOMINANT	L
	0.4 V < V_{ID} < 1.15 V	?	?
	$V_{ID} \leq 0.4$ V	RECESSIVE	H
NORMAL OR SILENT	$V_{ID} \geq 0.9$ V	DOMINANT	L
	0.5 V < V_{ID} < 0.9 V	?	?
	$V_{ID} \leq 0.5$ V	RECESSIVE	H
ANY	Open	N/A	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate.
(2) While STB is high (standby mode) the RXD output of the HVDA540 is always high (recessive) because it has no wake-up receiver.
(3) While STB is high (standby mode) the RXD output of the HVDA541 functions according to the levels above and the wake-up conditions shown in Figure 17 and Figure 18.

9 Application and Implementation

NOTE

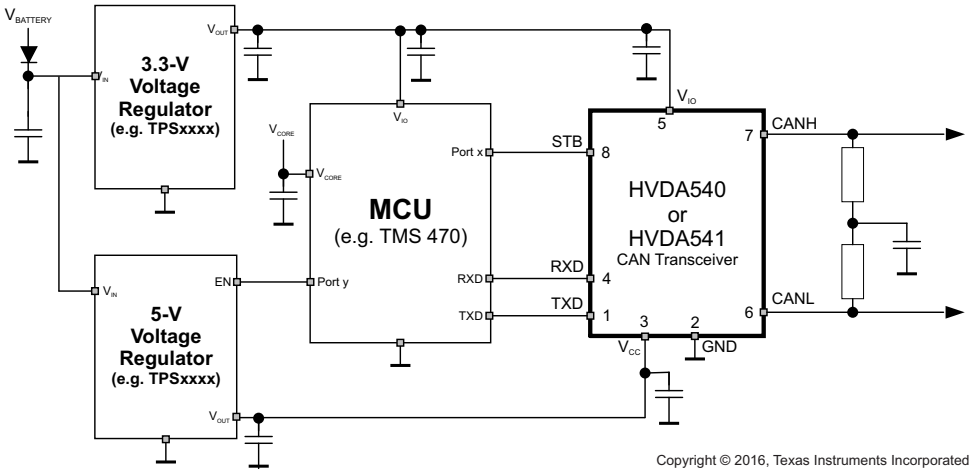
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Below are typical application configurations for both 5-V and 3.3-V microprocessor applications. The bus termination is shown for illustrative purposes.

9.2 Typical Applications

9.2.1 3.3-V I/O Voltage Level and Normal Mode



5-V V_{CC}, Not Needed in Low-Power Mode

Figure 19. Typical Application Using 3.3-V I/O Voltage Level and Low-Power Mode

9.2.1.1 Design Requirements

The ISO 11898-2 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the HVDA54x family of transceivers.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2. They have made system-level tradeoffs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet, and NMEA2000.

Typical Applications (continued)

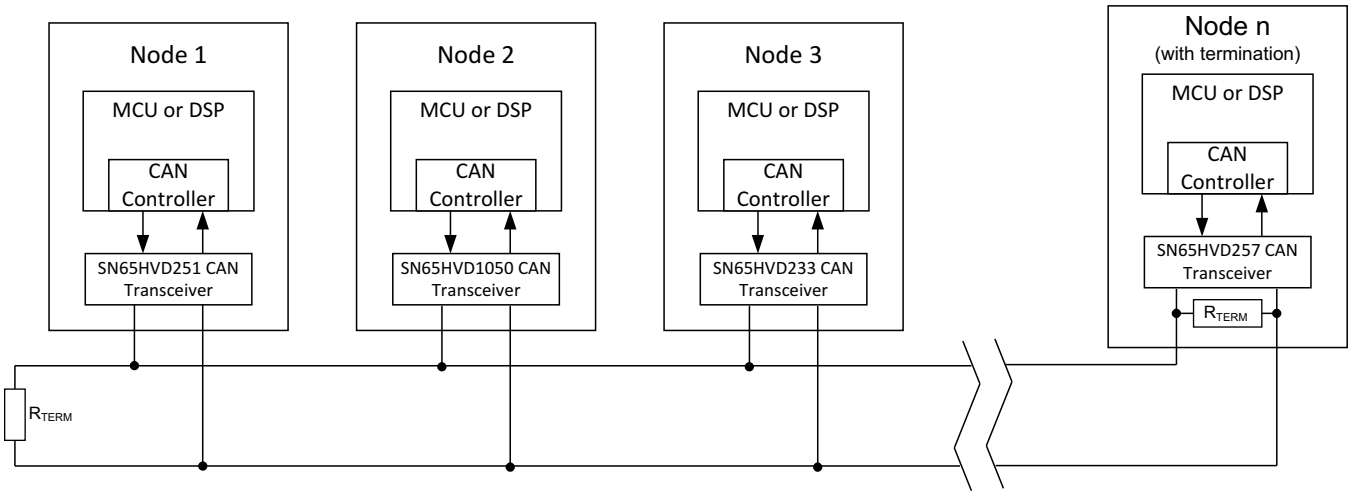


Figure 20. Typical CAN Bus

9.2.1.2 Detailed Design Procedure

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network. Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 21). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

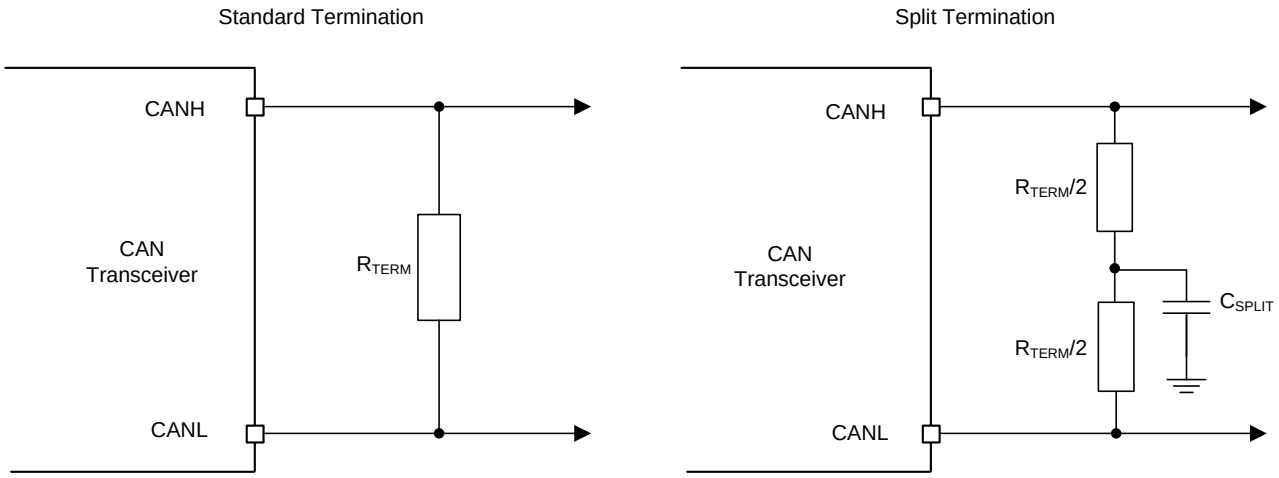


Figure 21. CAN Bus Termination Concepts

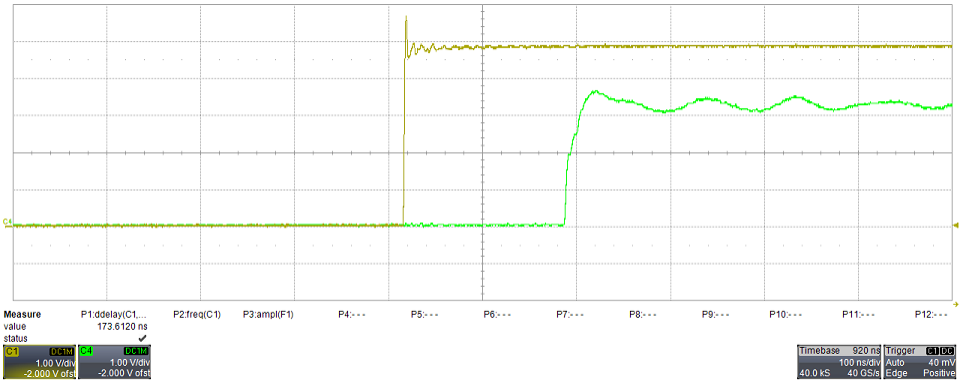
The family of transceivers have variants for both 5-V only applications and applications where level shifting is needed for a 3.3-V micrcontroller.

Typical Applications (continued)

9.2.1.2.1 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay and consists of the delay from driver input (TXD pin) to differential outputs (CANH and CANL), plus the delay from the receiver inputs (CANH and CANL) to the output pin RXD.

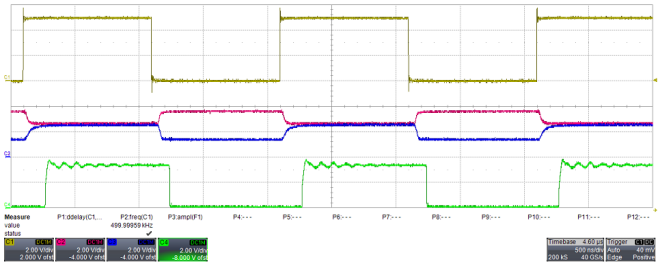
In Figure 22 is displayed the loop delay at 1 Mbps with Vio equal to 3.3 V



Data rate = 1 Mbps, Temp = 25°C, V_{CC} = 5 V, Load = 60 Ω, STB = 0, V_{IO} = 3.3 V.

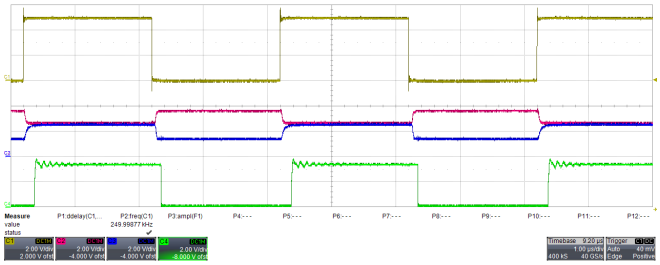
Figure 22. t_LOOP Delay

9.2.1.3 Application Curves



Data rate = 1 Mbps, Temp = 25°C, V_{CC} = 5 V, Load = 60 Ω, STB = 0, V_{IO} = 3.3 V.

Figure 23. HVDA540 TXD, CANH, CANL and RXD Waveforms at 1 Mbps



Data rate = 500 Kbps, Temp = 25°C, V_{CC} = 5 V, Load = 60 Ω, STB = 0, V_{IO} = 3.3 V.

Figure 24. HVDA540 TXD, CANH, CANL and RXD Waveforms at 500 Kbps

9.3 System Examples

Figure 25, Figure 26, and Figure 27 show three different example applications using the HVDA54x family of transceivers. Different devices and configurations can be used depending on the I/O voltage levels supported by the MCU and different operating modes required by the end application.

System Examples (continued)

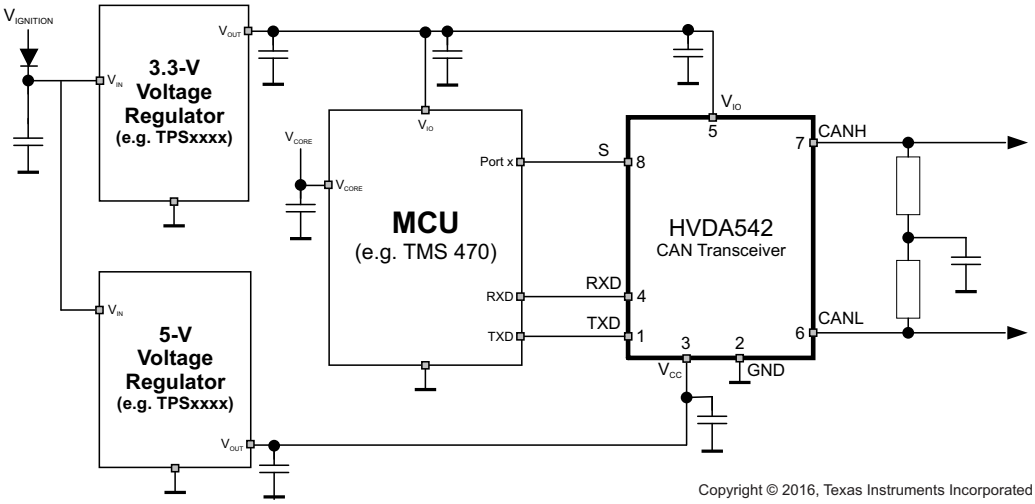


Figure 25. Typical Application Using 3.3-V I/O Voltage Level and No Low-Power Mode

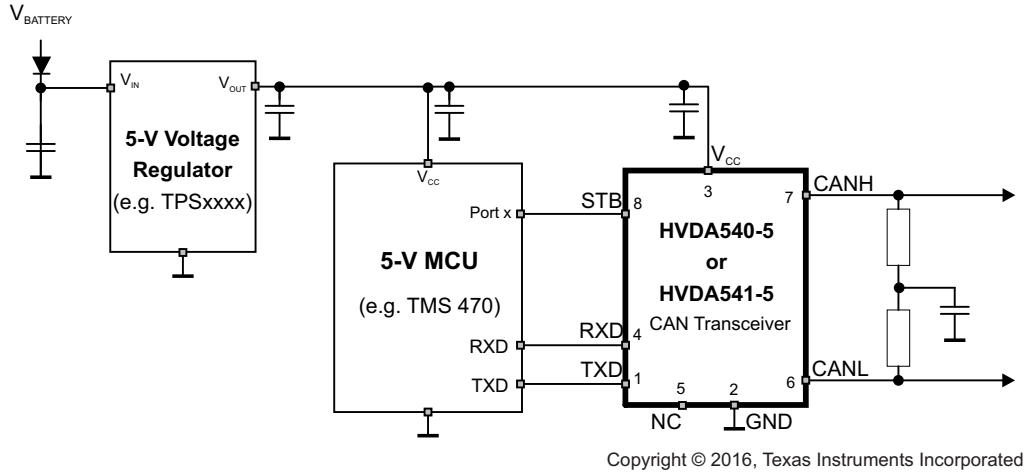


Figure 26. Typical Application Using 5-V MCU and Low-Power Mode

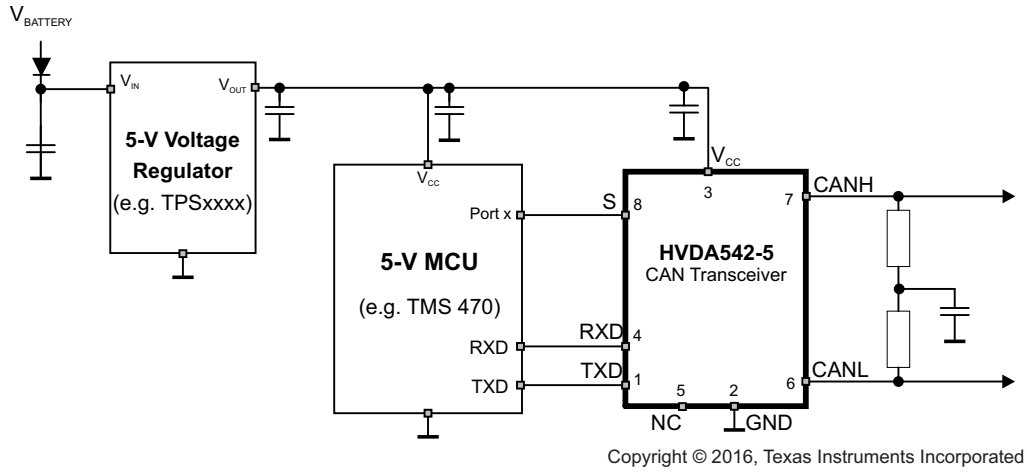


Figure 27. Typical Application Using 5-V MCU and No Low-Power Mode

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the V_{CC} supply pins as possible. Either a linear regulator or switched-mode power supply may be used. Power and ground nets should be routed on the PCB using planes or wide traces so that series resistance and inductance are minimized.

11 Layout

11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection device to protect against EFT and surge transients that may occur in industrial enviroments. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The HVDA54x-Q1 and HVDA54x-5-Q1 families come with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the onboard connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

- Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example a transient voltage suppression (TVS) device, D1, has been used for added protection. The production solution can be either bidirectional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C4 and C5. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the transceiver U1 and connector J1.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance.

NOTE

High-frequency currents follows the path of least impedance and not the path of least resistance.

- Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1, C2 on the V_{CC} supply and C6 and C7 on the V_{IO} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, take additional care to ensure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).
- To limit current of digital lines, serial resistors may be used. Examples are R2, R3, and R4. These are not required.
- Terminal 1: R1 is shown optionally for the TXD input of the device. If an open drain host processor is used, this is mandatory to ensure the bit timing into the device is met.
- Terminal 5: For devices with a VIO input, bypass capacitors should be placed as close to the pin as possible (example C6 and C7). In devices without a VIO input, this pin is not internally connected and can be left floating or tied to any existing net (for example, a split pin connection).
- Terminal 8: is shown assuming the mode terminal, STB, will be used. If the device is only used in normal mode, R4 is not needed and R5 could be used for the pulldown resistor to GND.

11.2 Layout Examples

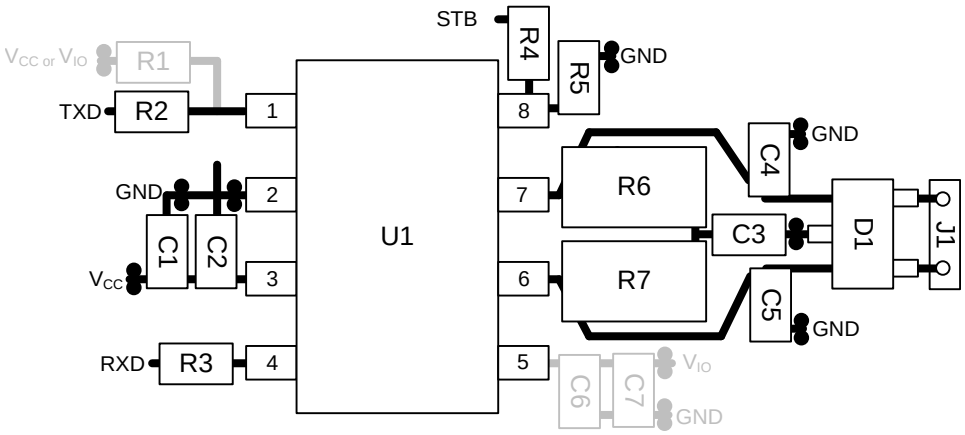


Figure 28. HVDA540/HVDA541 Layout Example

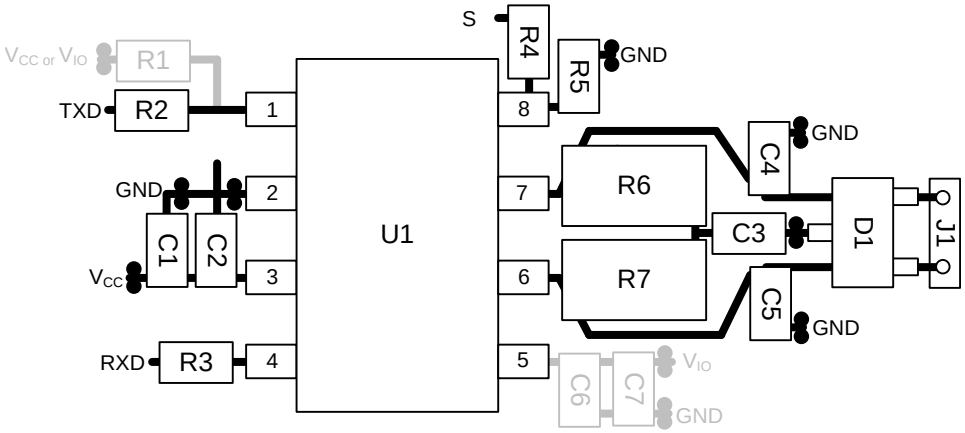


Figure 29. HVDA542 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

SN65HVDA54x-Q1 Errata (SLLZ073)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVDA540-Q1	Click here	Click here	Click here	Click here	Click here
SN65HVDA541-Q1	Click here	Click here	Click here	Click here	Click here
SN65HVDA542-Q1	Click here	Click here	Click here	Click here	Click here
SN65HVDA540-5-Q1	Click here	Click here	Click here	Click here	Click here
SN65HVDA541-5-Q1	Click here	Click here	Click here	Click here	Click here
SN65HVDA542-5-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HVDA5405QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H5405Q	Samples
HVDA540QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H540Q	Samples
HVDA5415QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H5415Q	Samples
HVDA541QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H541Q	Samples
HVDA5425QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H5425Q	Samples
HVDA542QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H542Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN65HVDA540-5-Q1, SN65HVDA540-Q1, SN65HVDA541-5-Q1, SN65HVDA542-5-Q1, SN65HVDA542-Q1 :

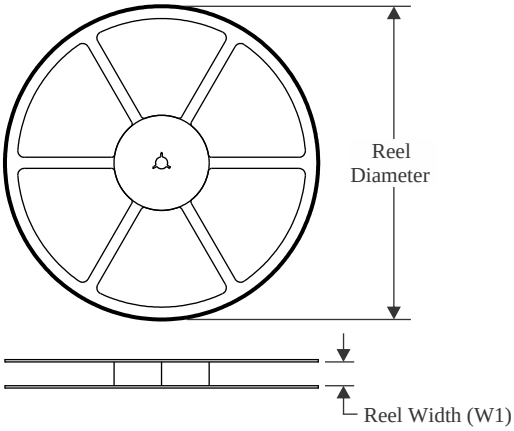
- Catalog: SN65HVDA540, SN65HVDA542-5-Q1
- Automotive: SN65HVDA540-Q1, SN65HVDA541-Q1, SN65HVDA542-Q1

NOTE: Qualified Version Definitions:

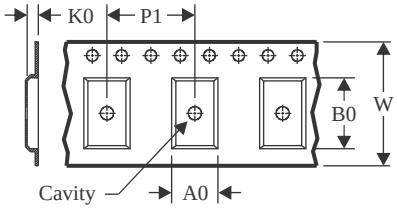
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

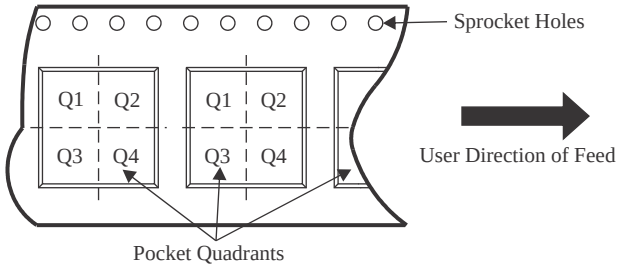


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

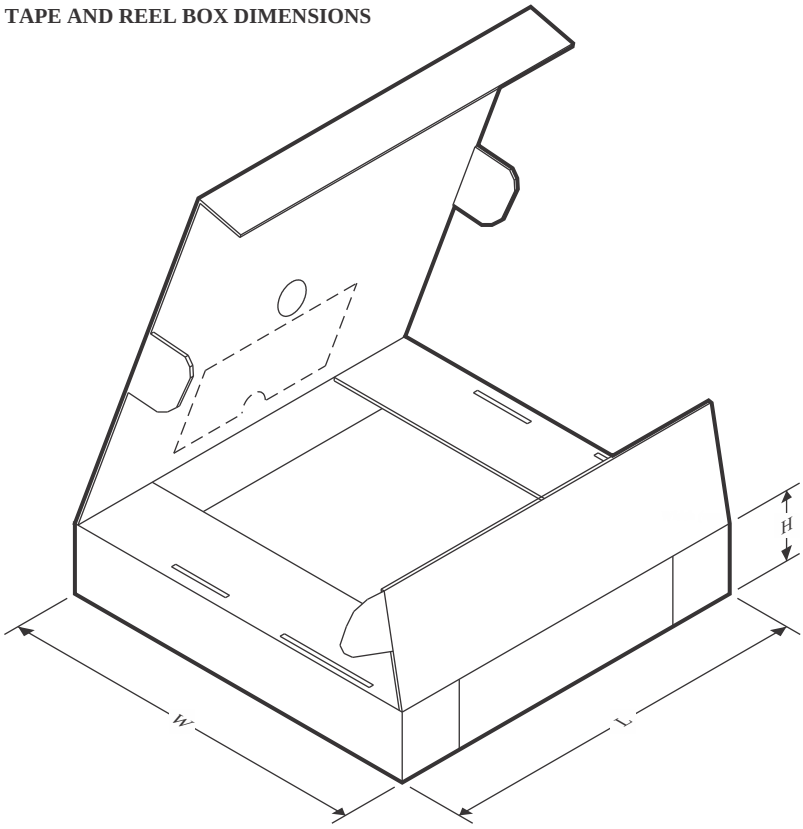
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

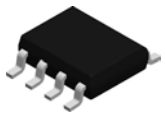
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HVDA5405QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA540QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA5415QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA541QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA5425QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA542QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HVDA5405QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
HVDA540QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
HVDA5415QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA541QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
HVDA5425QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA542QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

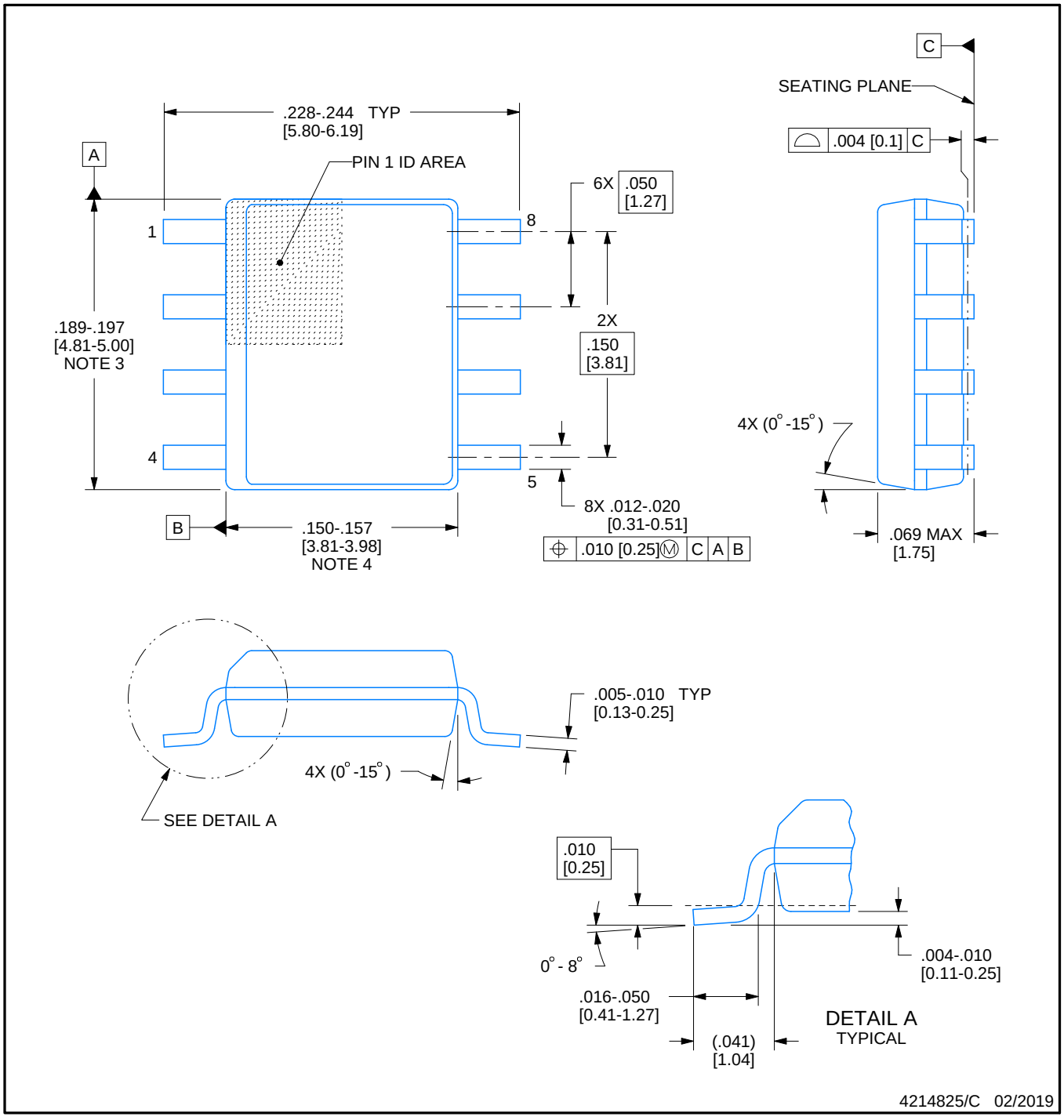


PACKAGE OUTLINE

D0008A

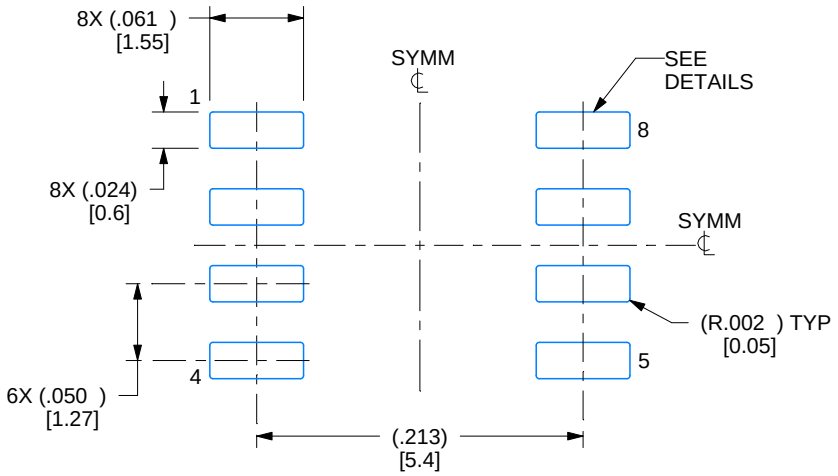
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

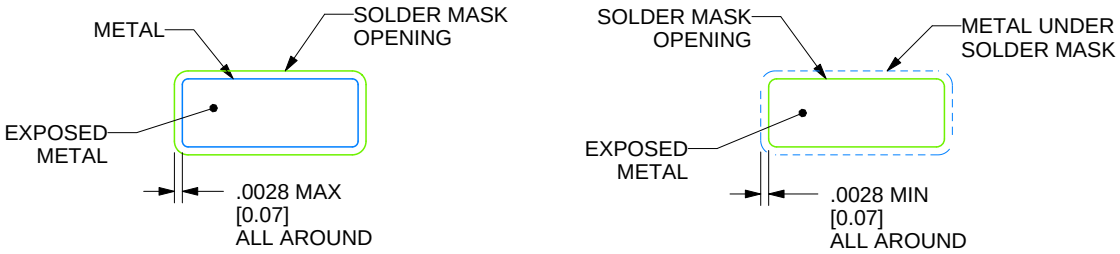


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

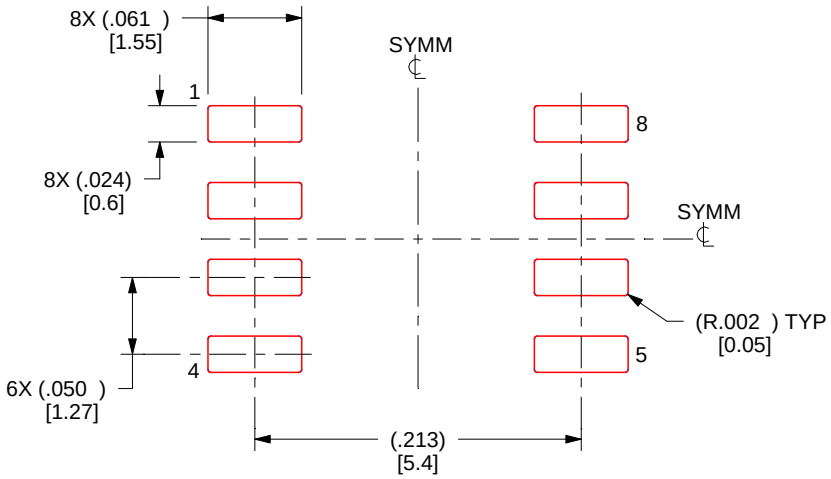
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265