

TS5MP646 4 数据通道 2:1 MIPI 开关 (10 通道, 2:1 模拟开关)

1 特性

- 电源电压范围 1.65V 至 5.5V
- 10 通道 2:1 开关
- 关断保护：
V_{DD} = 0V 时，I/O 类型为 Hi-Z
- 较低的 R_{ON}，典型值 4.2Ω
- 3GHz 带宽
- -40dB 超低串扰
- 低功耗禁用模式
- 1.8V 兼容型逻辑输入
- ESD 保护性能超出 JESD 22 标准
 - 2000V 人体放电模型 (HBM)

2 应用

- 移动电话
- 平板电脑
- 台式机/笔记本电脑
- 虚拟现实和增强现实
- 无人机
- 基于摄像头的条形码扫描仪
- 医疗
- IP 网络摄像机

3 说明

TS5MP646 是一款四数据通道 MIPI 开关。此器件是一款经优化的 10 通道（包含 5 个差分通道）单极双投开关，适用于高速应用。TS5MP646 可方便地将多个符合 MIPI 标准的器件与单个 CSI/DSI、C-PHY/D-PHY 模块相连接。

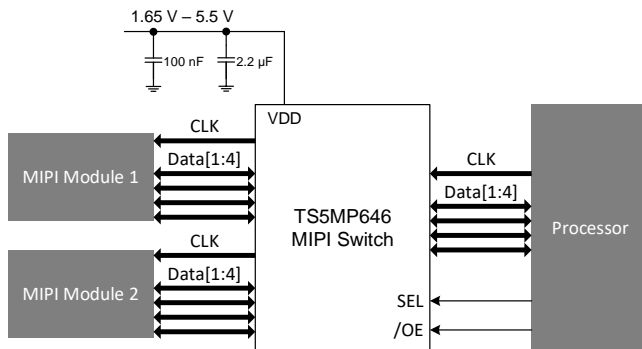
此器件具有 3GHz 带宽、不会造成信号恶化的低通道间偏差以及可补偿布局损失的宽余量。此器件的低电流消耗可满足低功率应用的需求包括移动电话和其他个人电子产品。

器件信息(1)

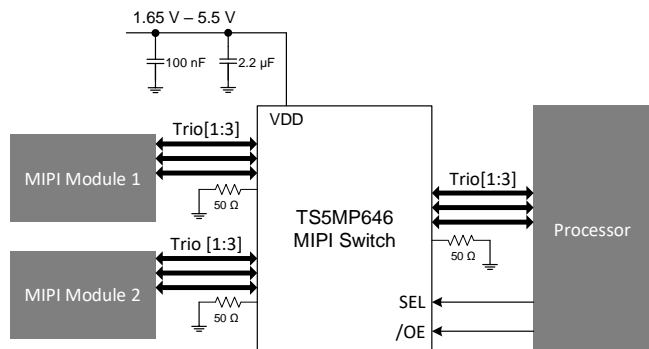
器件型号	封装	封装尺寸 (标称值)
TS5MP646	DSBGA (YFP)	2.42mm x 2.42mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

D-PHY 简化原理图



C-PHY 简化原理图



目录

1 特性	1	8.4 Device Functional Modes	19
2 应用	1	9 Application and Implementation	20
3 说明	1	9.1 Application Information	20
4 修订历史记录	2	9.2 Typical Application	20
5 Pin Configuration and Functions	3	10 Power Supply Recommendations	27
6 Specifications	4	11 Layout	28
6.1 Absolute Maximum Ratings	4	11.1 Layout Guidelines	28
6.2 ESD Ratings	4	11.2 Layout Example	28
6.3 Recommended Operating Conditions	5	12 器件和文档支持	29
6.4 Thermal Information	5	12.1 文档支持	29
6.5 Electrical Characteristics	5	12.2 接收文档更新通知	29
6.6 Typical Characteristics	9	12.3 社区资源	29
7 Parameter Measurement Information	10	12.4 商标	29
8 Detailed Description	16	12.5 静电放电警告	29
8.1 Overview	16	12.6 术语表	29
8.2 Functional Block Diagram	16	13 机械、封装和可订购信息	29
8.3 Feature Description	17		

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (January 2019) to Revision E	Page
• Added min differential bandwidth specification 2.7 GHz	8
• Changed typ differential bandwidth specification to 4.1 GHz	8

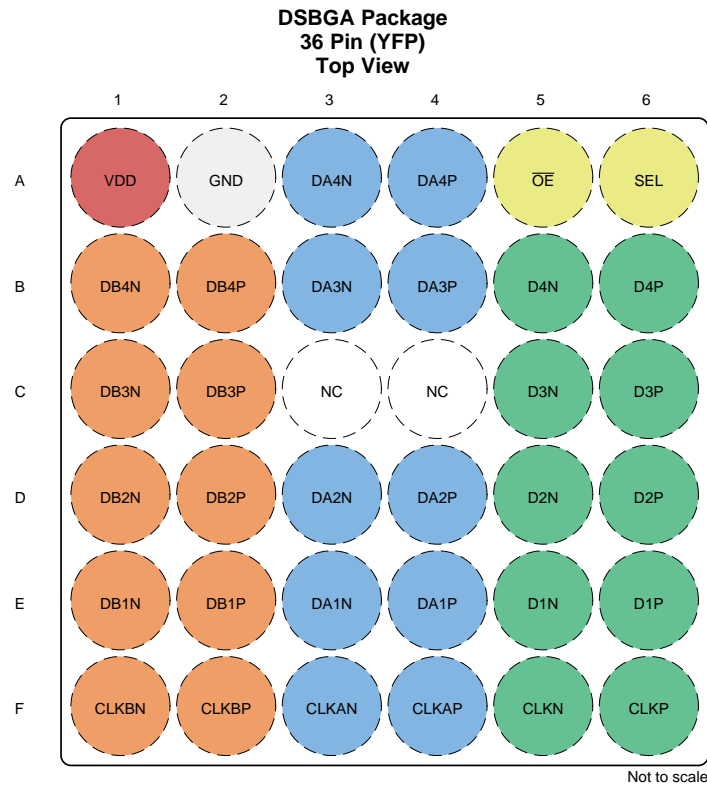
Changes from Revision C (August 2018) to Revision D	Page
• 添加了 D-PHY 以及 C-PHY 简化原理图	1
• Added the Typical D-PHY and C-PHY Application circuits	20
• Added Eye diagrams to the Application Curves section	22
• Added the <i>MIPI D-PHY Application</i> section	23
• Added the <i>MIPI C-PHY Application</i> section	25

Changes from Revision B (July 2018) to Revision C	Page
• 已更改 应用 列表	1

Changes from Revision A (March 2018) to Revision B	Page
---	-------------

Changes from Original (January 2018) to Revision A	Page
• 将器件信息 表中的“封装尺寸（标称值）”从 2.459 x 2.459 更改成了 2.42 x 2.42	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	A1	PWR	Power supply input
GND	A2	GND	Device Ground
DA4N	A3	I/O	Differential I/O
DA4P	A4	I/O	Differential I/O
$\overline{\text{OE}}$	A5	I	Output enable (Active Low)
SEL	A6	I	Channel Select
DB4N	B1	I/O	Differential I/O
DB4P	B2	I/O	Differential I/O
DA3N	B3	I/O	Differential I/O
DA3P	B4	I/O	Differential I/O
D4N	B5	I/O	Differential I/O
D4P	B6	I/O	Differential I/O
DB3N	C1	I/O	Differential I/O
DB3P	C2	I/O	Differential I/O
NC	C3	-	No connect
NC	C4	-	No connect
D3N	C5	I/O	Differential I/O
D3P	C6	I/O	Differential I/O
DB2N	D1	I/O	Differential I/O
DB2P	D2	I/O	Differential I/O
DA2N	D3	I/O	Differential I/O

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DA2P	D4	I/O	Differential I/O
D2N	D5	I/O	Differential I/O
D2P	D6	I/O	Differential I/O
DB1N	E1	I/O	Differential I/O
DB1P	E2	I/O	Differential I/O
DA1N	E3	I/O	Differential I/O
DA1P	E4	I/O	Differential I/O
D1N	E5	I/O	Differential I/O
D1P	E6	I/O	Differential I/O
CLKBN	F1	I/O	Differential I/O
CLKBP	F2	I/O	Differential I/O
CLKAN	F3	I/O	Differential I/O
CLKAP	F4	I/O	Differential I/O
CLKN	F5	I/O	Differential I/O
CLKP	F6	I/O	Differential I/O

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{DD}	Supply Voltage	-0.5	6	V
$V_{I/O}$	Analog voltage range (DxN, CLKN, DxP, CLKP, DAxN, CLKAN, DAxP, CLKAP, DBxN, CLKBN, DBxP, CLKBP)	-0.5	4	V
$V_{SEL}, \overline{V_{OE}}$	Digital Input Voltage (SEL, /OE)	-0.5	6	V
T_J	Junction temperature	-65	150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 500-V HBM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ± WWW V and/or ± XXX V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 250-V CDM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ± YYY V and/or ± ZZZ V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply Voltage	1.65		5.5	V
V _{I/O}	Analog voltage range (DxN, CLKN, DxP, CLKP, DAxN, CLKAN, DAxP, CLKAP, DBxN, CLKBN, DBxP, CLKBP)	0		3.6	V
V _(SEL) V _(OE)	Digital Input Voltage	0		5.5	V
I _{I/O}	Continuous I/O current	-35		35	mA
T _A	Operating ambient temperature	-40		85	°C
T _J	Junction temperature	-65		150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS5MP646			UNIT
		YFP			
		36			
R _{θJA}	Junction-to-ambient thermal resistance	57.6			°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.3			°C/W
R _{θJB}	Junction-to-board thermal resistance	12.6			°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2			°C/W
Ψ _{JB}	Junction-to-board characterization parameter	12.7			°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A			°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
POWER SUPPLY							
I _{DD}	VDD Active Supply Current	V _{DD} = 1.65 V to 5.5 V OE = 0 V SEL = 0 V to 5.5 V Dn, CLKn = 0 V		0	30	60	μA
I _{DD_PD}	Power-down Supply current	V _{DD} = 1.65 V to 5.5 V OE = V _{DD} SEL = 0 V to 5.5 V Dn, CLKn = 0 V		0	0.1	1	μA
I _{DD_PD_1.8}	Power-down Supply current	V _{DD} = 1.65 V to 5.5 V OE = 1.8 V SEL = 0 V to 5.5 V Dn, CLKn = 0 V		0	0.1	10	μA
DC CHARACTERISTICS							
R _{ON_HS}	On-state resistance	V _{DD} = 1.65 V to 5.5 V OE = 0 V Dn, CLKn = -8 mA, 0.2 V DAn, DBn, CLKAN, CLKBn = 0.2 V, -8 mA			6	9	Ω
R _{ON_LP}	On-state resistance	V _{DD} = 1.65 V to 5.5 V OE = 0 V Dn, CLKn = -8 mA, 1.2 V DAn, DBn, CLKAN, CLKBn = 1.2 V, -8 mA			6	10	Ω

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ON_flat_HS}$	On-state resistance flatness	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = -8 mA, 0 V to 0.3 V DAn, DBn, CLKAn, CLKBn = 0 V to 0.3 V, -8 mA		0.1		Ω
$R_{ON_flat_LP}$	On-state resistance flatness	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = -8 mA, 0 V to 1.3 V DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V, -8 mA		0.9		Ω
D_{RON_HS}	On-state resistance match between+and- paths	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = -8 mA, 0.2 V DAn, DBn, CLKAn, CLKBn = 0.2 V, -8 mA		0.1		Ω
D_{RON_LP}	On-state resistance match between+and- paths	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = -8 mA, 1.3 V DAn, DBn, CLKAn, CLKBn = 1.3 V, -8 mA		0.1		Ω
I_{OFF}	Switch off leakage current	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V to }5.5\text{ V}$ SEL = 0 V to 5.5 V Dn, CLKn = 0 V to 1.3 V DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V	-0.5		0.5	μA
$I_{OFF_3_6}$	Switch off leakage current	VDD = 0V,1.5V,1.65V,3.3V,5.5V /OE = 0V,1.5V,1.65V,3.3V,5.5V SEL= 0V,1.5V,1.65V,3.3V,5.5V DX,CLKX = 3.6V DAX,DBx,CLKAX,CLKBX = 3.6V	-10		10	μA
I_{ON}	Switch on leakage current	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ SEL = 0 V to 5.5 V Dn, CLKn = 0 V to 1.3 V DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V	-0.5		0.5	μA
$I_{ON_3_6}$	Switch on leakage current	VDD = 1.5V,1.65V,3.3V,5.5V /OE = 0V SEL= 0V,1.5V,1.65V,3.3V,5.5V DX,CLKX = 3.6V DAX,DBx,CLKAX,CLKBX = 3.6V	-50		50	μA
DYNAMIC CHARACTERISTICS						
t_{SWITCH}	Switching time between channels	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$			1.5	μs
t_{SWITCH_CP}	Switching time between channels by charge pump	VDD = 1.5V,1.65V,3.3V,5.5V /OE = 0V DX, CLKX = 0.6 V DAX, DBX, CLKAX, CLKBX: $R_L=50\Omega, C_L=5\text{pF}$			50	μs
f_{SEL_MAX}	Maximum toggling frequency for the SEL line	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$			100	kHz

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON_OE}	Device turnon-time \overline{OE} to switch on	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$		50	300	μs
t_{ON_VDD}	Device turnon-time VDD to switch on	$V_{DD} = 0\text{ V to }5.5\text{ V}$ Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$		50	300	μs
t_{OFF_OE}	Device turnoff time \overline{OE} to switch off	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$		0.5	1	μs
t_{OFF_VDD}	Device turnoff time VDD to switch off	$V_{DD} = 5\text{ V to }0\text{ V}$ V_{DD} ramp rate = 250 μs Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$		0.5	1	ms
t_{MIN_OE}	Minimum pulse width for \overline{OE}	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$	500			ns
t_{BBM}	Break before make time	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ DAn, DBn, CLKAn, CLKBn: 0.6 V	50			ns
t_{SKEW}	Intrapair skew	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = 0.3 V DnX, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$		1		ps
t_{SKEW}	Interpair Skew	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = 0.3 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$		4		ps
t_{PD}	Propagation delay with 100 ps rise time	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$ Dn, CLKn = 0.6 V DAn, DBn, CLKAn, CLKBn: $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $t_{RISE} = 100\text{ ps}$		40		ps
O_{ISO}	Differential off isolation	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$, V_{DD} SEL = 0 V, V_{DD} Dn, CLKn, DAn, DBn, CLKAn, CLKBn: $R_S = 50\ \Omega$, $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $V_{IO} = 200\text{ mV} + 200\text{ mV}_{PP}$ (differential) $f = 1250\text{ MHz}$		-20		dB
X_{TALK}	Differential channel to channel crosstalk	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$ $OE = 0\text{ V}$, V_{DD} SEL = 0 V, V_{DD} Dn, CLKn, DAn, DBn, CLKAn, CLKBn: $R_S = 50\ \Omega$, $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $V_{IO} = 200\text{ mV} + 200\text{ mV}_{PP}$ (differential) $f = 1250\text{ MHz}$		-40		dB

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Differential Bandwidth	$V_{DD} = 1.65 \text{ V to } 5.5 \text{ V}$ $OE = 0 \text{ V}$ $SEL = 0 \text{ V, } V_{DD}$ Dn, CLKn, DAn, DBn, CLKAn, CLKBn: $R_S = 50 \Omega, R_L = 50 \Omega, C_L = 1 \text{ pF}$ $V_{I/O} = 200 \text{ mV} + 200 \text{ mV}_{PP}$ (differential) $f = 1250 \text{ MHz}$	2.7	4.1		GHz
I_{LOSS}	Insertion Loss	$V_{DD} = 1.65 \text{ V to } 5.5 \text{ V}$ $OE = 0 \text{ V}$ $SEL = 0 \text{ V, } V_{DD}$ Dn, CLKn, DAn, DBn, CLKAn, CLKBn: $R_S = 50 \Omega, R_L = 50 \Omega, C_L = 1 \text{ pF}$ $V_{I/O} = 200 \text{ mV} + 200 \text{ mV}_{PP}$ (differential) $f = 100 \text{ kHz}$	-0.65			dB
C_{OFF}	Off capacitance	$V_{DD} = 1.65 \text{ V to } 5.5 \text{ V}$ $OE = 0 \text{ V, } V_{DD}$ $SEL = 0 \text{ V, } V_{DD}$ Dn, CLKn, DAn, DBn, CLKAn, CLKBn = $0 \text{ V, } 0.2 \text{ V}$ $f = 1250 \text{ MHz}$		1.5		pF
C_{ON}	On capacitance	$V_{DD} = 1.65 \text{ V to } 5.5 \text{ V}$ $OE = 0 \text{ V}$ $SEL = 0 \text{ V, } V_{DD}$ Dn, CLKn, DAn, DBn, CLKAn, CLKBn = $0 \text{ V, } 0.2 \text{ V}$ $f = 1250 \text{ MHz}$		1.5		pF
DIGITAL CHARACTERISTICS						
V_{IH}	Input logic high (SEL, \overline{OE})	$V_{I/O} = 0.6 \text{ V } R_L = 50 \Omega, C_L = 5 \text{ pF}$	1.425		5.5	V
V_{IL}	Input logic low (SEL, /OE)	$V_{I/O} = 0.6 \text{ V } R_L = 50 \Omega, C_L = 5 \text{ pF}$	0		0.5	V
I_{IH}	Input high leakage current (SEL, /OE)	$V_{I/O} = 0.6 \text{ V } R_L = 50 \Omega, C_L = 5 \text{ pF}$	-5		5	μA
I_{IL}	Input low leakage current (SEL, /OE)	$V_{I/O} = 0.6 \text{ V } R_L = 50 \Omega, C_L = 5 \text{ pF}$	-5		5	μA
R_{PD}	Internal pull-down resistance on digital input pins	$V_{I/O} = 0.6 \text{ V } R_L = 50 \Omega, C_L = 5 \text{ pF}$		6		M Ω
C_I	Digital Input capacitance (SEL, /OE)	$f = 1 \text{ MHz}$		5		pF

6.6 Typical Characteristics

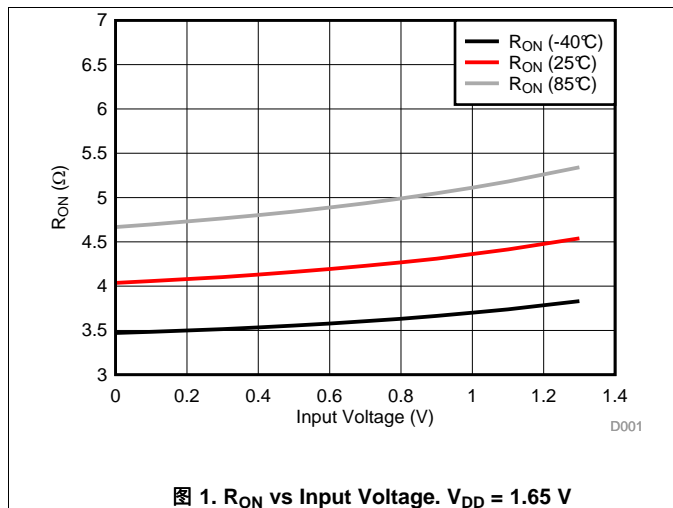


图 1. R_{ON} vs Input Voltage. $V_{DD} = 1.65\text{ V}$

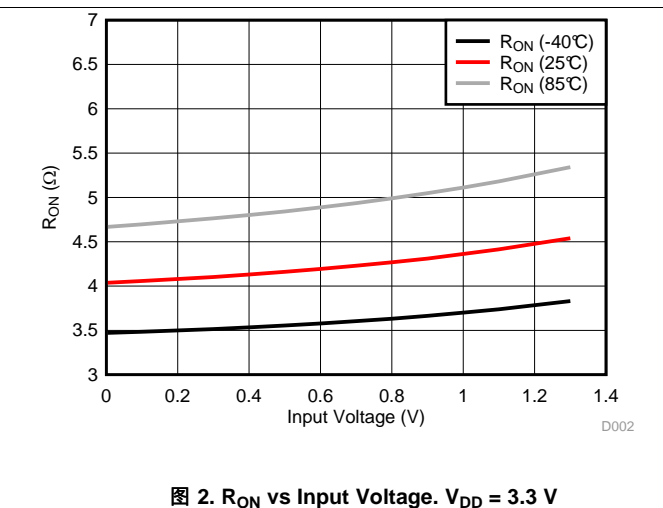


图 2. R_{ON} vs Input Voltage. $V_{DD} = 3.3\text{ V}$

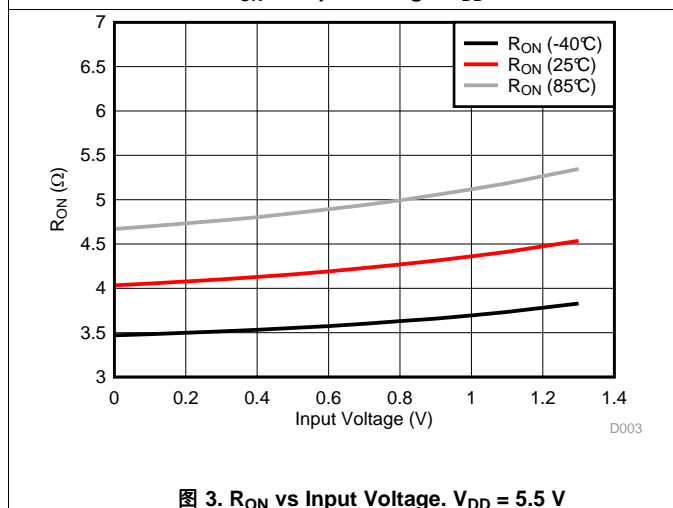


图 3. R_{ON} vs Input Voltage. $V_{DD} = 5.5\text{ V}$

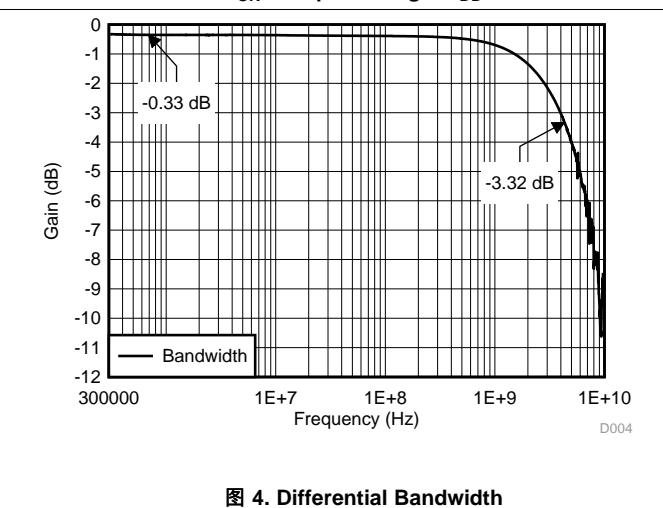


图 4. Differential Bandwidth

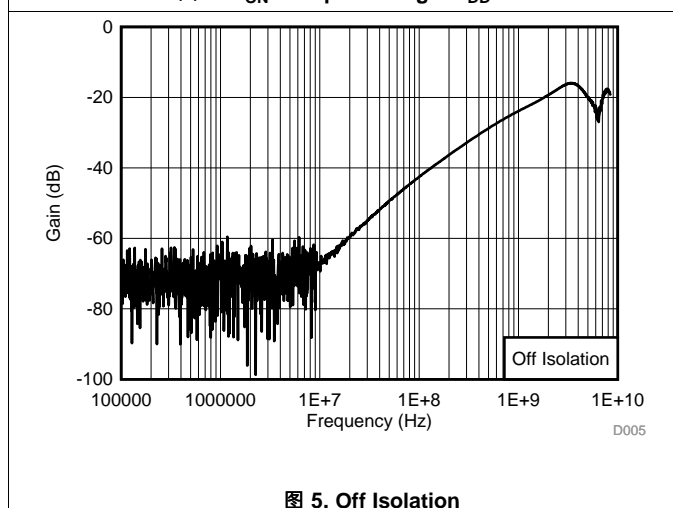


图 5. Off Isolation

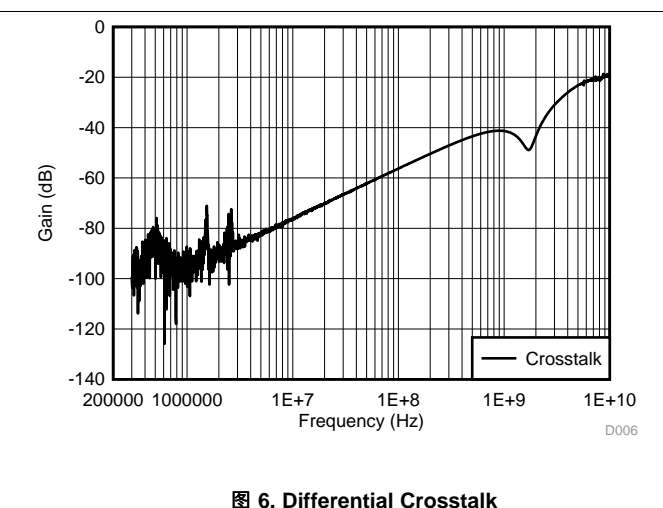
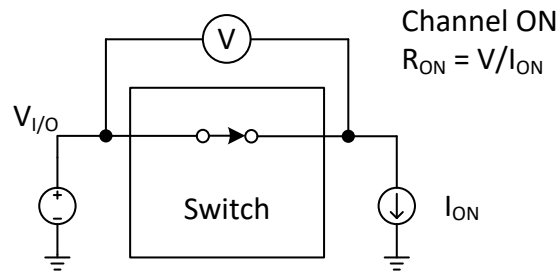


图 6. Differential Crosstalk

7 Parameter Measurement Information



Copyright © 2018, Texas Instruments Incorporated

图 7. On Resistance

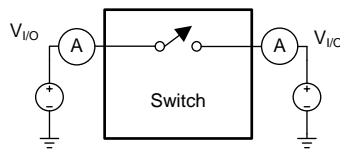


图 8. Off Leakage

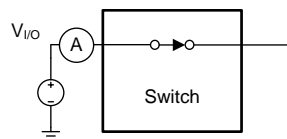
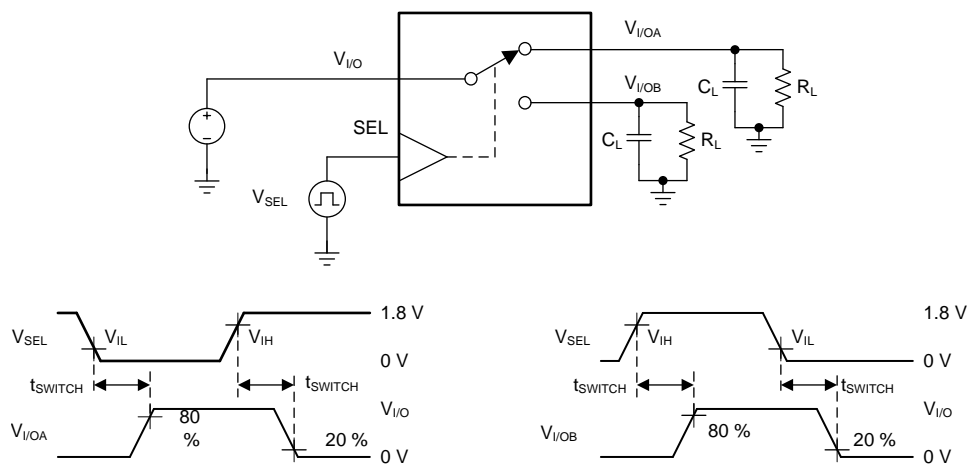


图 9. On Leakage

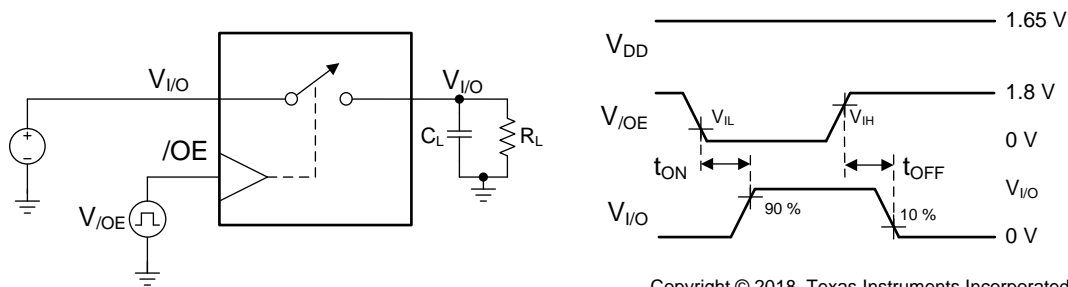


Copyright © 2018, Texas Instruments Incorporated

- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
- (2) C_L includes probe and jig capacitance.

图 10. t_{SWITCH} Timing

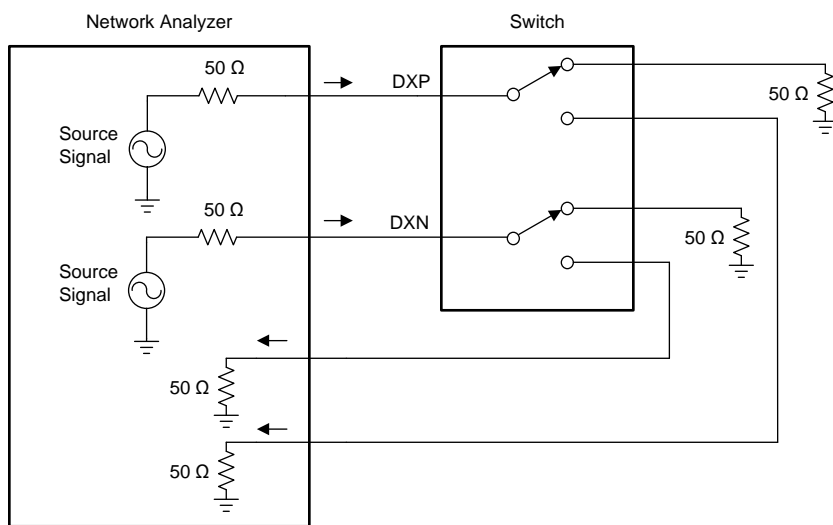
Parameter Measurement Information (接下页)



Copyright © 2018, Texas Instruments Incorporated

- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
- (2) C_L includes probe and jig capacitance.

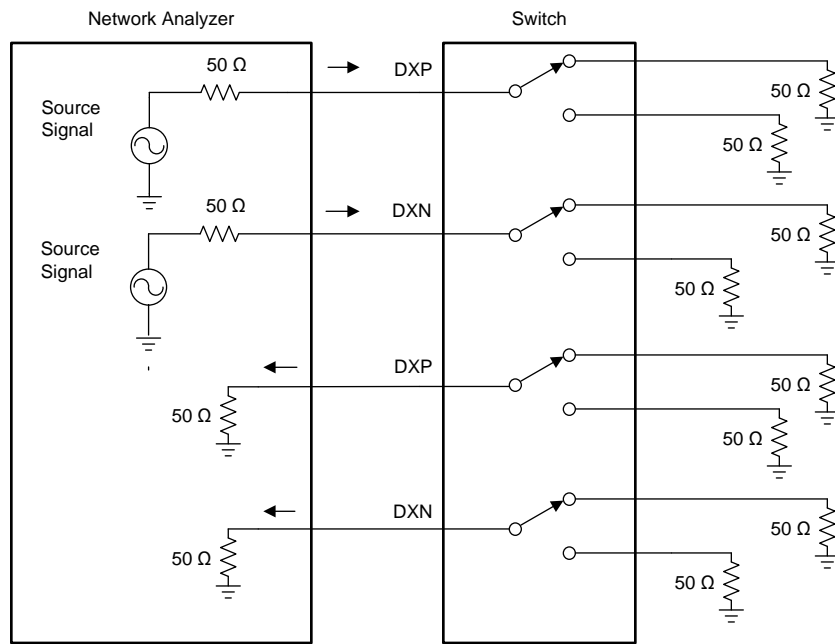
图 11. t_{ON} and t_{OFF} Timing for \overline{OE}



Copyright © 2018, Texas Instruments Incorporated

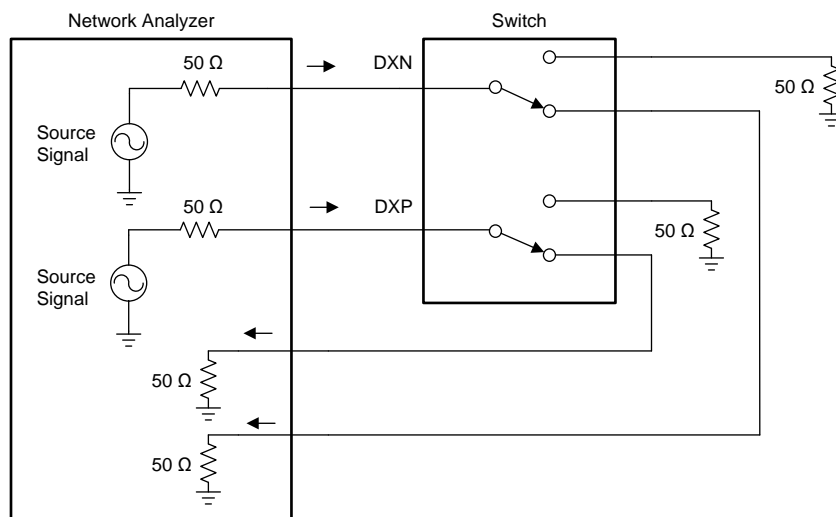
图 12. Off Isolation

Parameter Measurement Information (接下页)



Copyright © 2018, Texas Instruments Incorporated

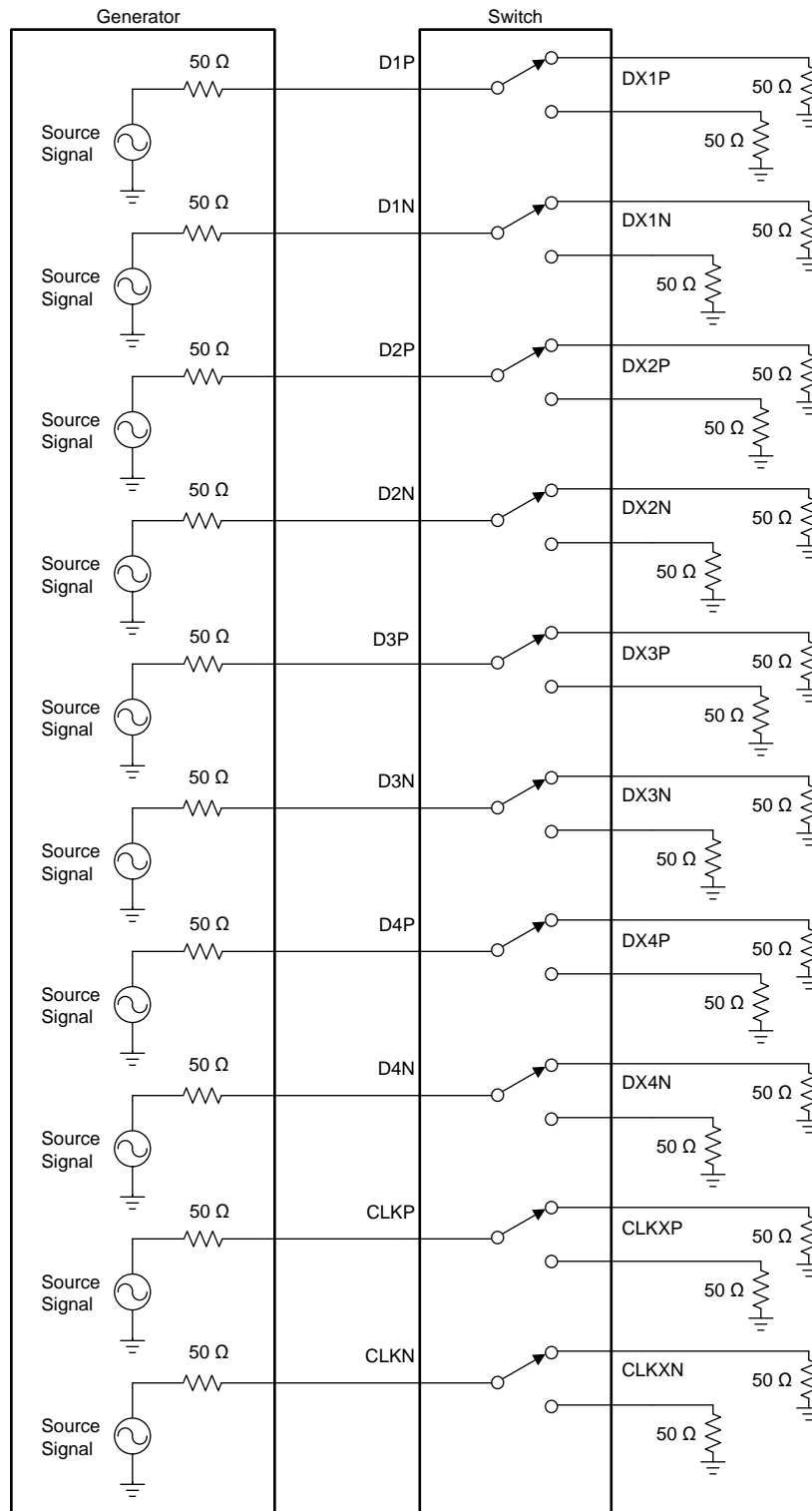
图 13. Crosstalk



Copyright © 2017, Texas Instruments Incorporated

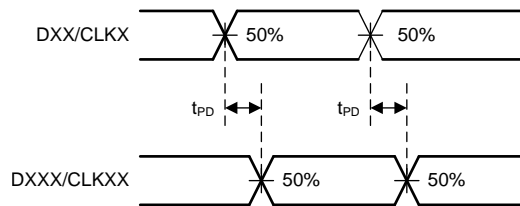
图 14. Bandwidth and Insertion Loss

Parameter Measurement Information (接下页)

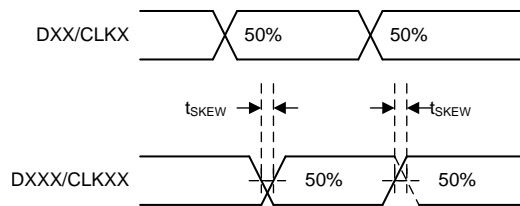


Copyright © 2017, Texas Instruments Incorporated

图 15. t_{PD} , $t_{SKEW(INTRA)}$ and $t_{SKEW(INTER)}$ Setup

Parameter Measurement Information (接下页)


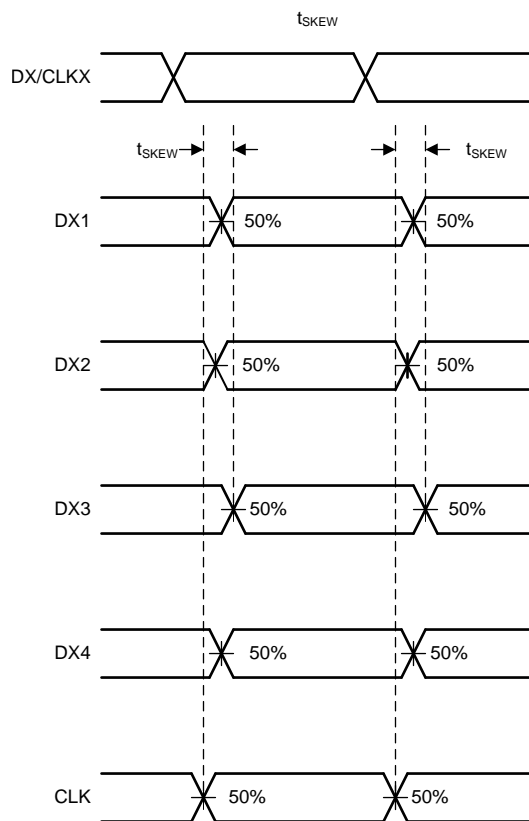
- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 100 \text{ ps}$, $t_f = 100 \text{ ps}$.
- (2) C_L includes probe and jig capacitance.

图 16. t_{PD}


- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 100 \text{ ps}$, $t_f = 100 \text{ ps}$.
- (2) C_L includes probe and jig capacitance.

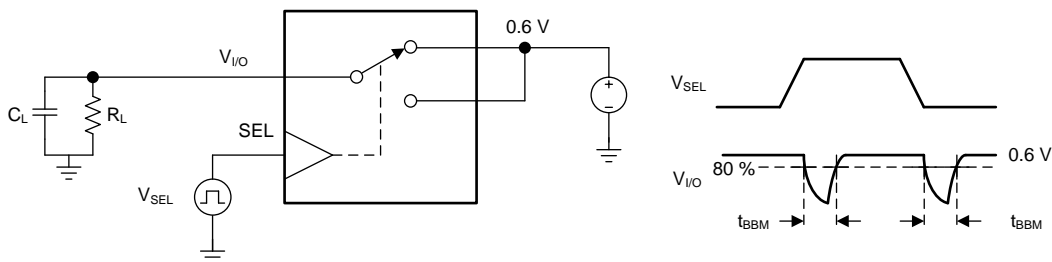
图 17. $t_{SKEW(INTRA)}$

Parameter Measurement Information (接下页)



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r = 100 ps, t_f = 100 ps.
- (2) C_L includes probe and jig capacitance.
- (3) t_{SKEW} is the max skew between all channels. Diagram exaggerates t_{SKEW} to show measurement technique

图 18. t_{SKEW(INTER)}



Copyright © 2017, Texas Instruments Incorporated

- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r = 3 ns, t_f = 3 ns.
- (2) C_L includes probe and jig capacitance.

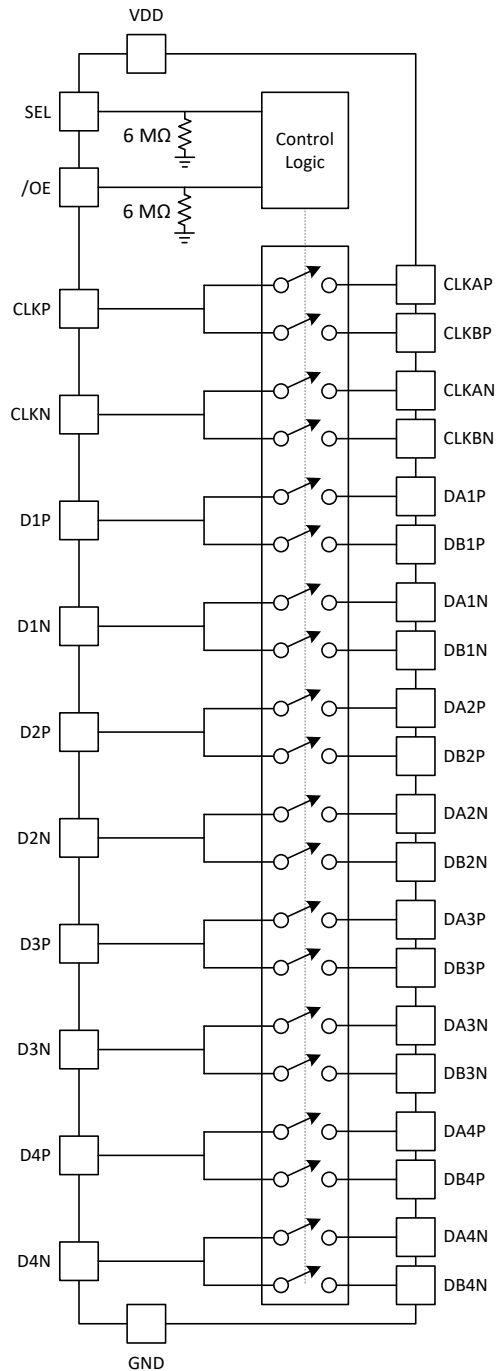
图 19. t_{BBM}

8 Detailed Description

8.1 Overview

The TS5MP646 is a high-speed 4 data lane 2:1 MIPI Switch. The device includes 10 channels (5 differential) with 4 differential data lanes and 1 differential clock lane for D-PHY, CSI or DSI. The switch allows a single MIPI port to interface between two MIPI modules, expanding the number of potential MIPI devices that can be used within a system that is MIPI port limited.

8.2 Functional Block Diagram



Copyright © 2018, Texas Instruments Incorporated

8.3 Feature Description

8.3.1 Powered-Off Protection

When the TS5MP646 is powered off ($V_{DD} = 0\text{ V}$) the I/Os and digital logic pins of the device remains in a high impedance state. The crosstalk, off-isolation, and leakage will remain within the electrical specifications. This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

Figure 20 shows an example system containing a switch without powered-off protection with the following system level scenario.

1. Subsystem A powers up and starts sending information to Subsystem B that remains unpowered.
2. The I/O voltage back powers the supply rail in Subsystem B.
3. The digital logic is back powered and turns on the switch. The signal is transmitted to Subsystem B before it is powered and damages it.

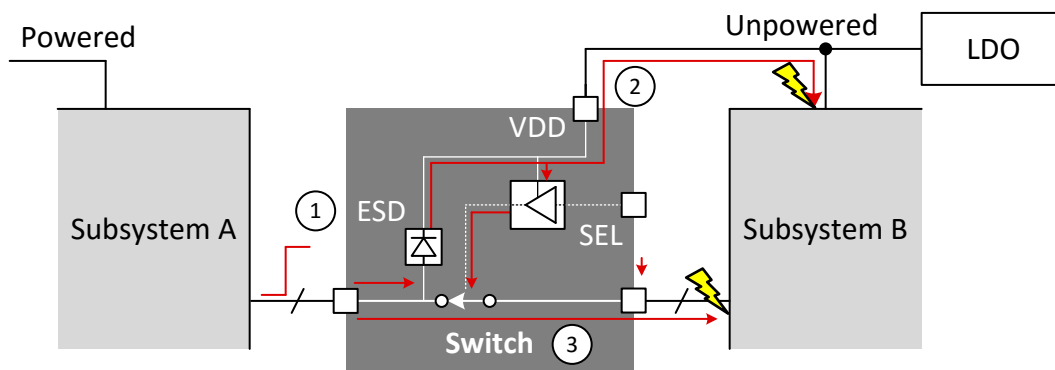


图 20. System Without Powered-Off Protection

With powered-off protection, the switch prevents back powering the supply and the switch remains high-impedance. Subsystem B remains protected.

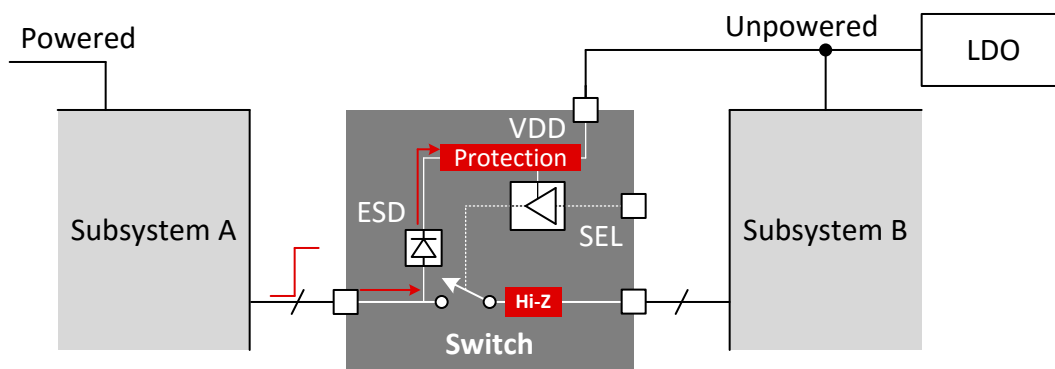


图 21. System With Powered-Off Protection

This features has the following system level benefits.

- Protects the system from damage.
- Prevents data from being transmitted unintentionally
- Eliminates the need for power sequencing solutions reducing BOM count and cost, simplifying system design and improving reliability.

Feature Description (接下页)

8.3.2 1.8-V Logic Compatible Inputs

The TS5MP646 has 1.8-V logic compatible digital inputs for switch control. Regardless of the V_{DD} voltage the digital input thresholds remained fixed, allowing a 1.8-V processor GPIO to control the TS5MP646 without the need for an external translator. This saves both space and BOM cost.

An example setup for a system without a 1.8-V logic compatible input is shown in 图 22. Here the supply mismatch between the processor and its GPIO output and the supply to the switch require a translator.

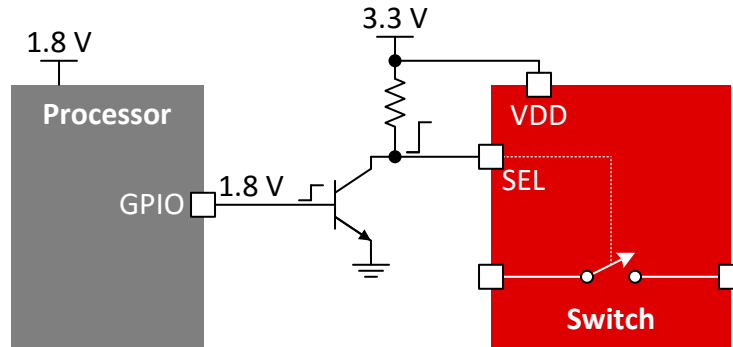


图 22. System Without 1.8 V Logic Compatible Inputs

With the 1.8 V logic compatibility in the TS5MP646, the translator is built in to the device so that the external components are no longer needed, simplifying the system design and overall cost.

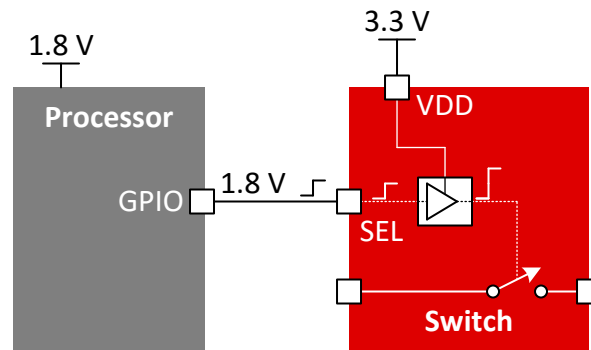


图 23. System With 1.8 V Logic Compatible Inputs

8.3.3 Low Power Disable Mode

The TS5MP646 has a low power mode that places all the signal paths in a high impedance state and lowers the current consumption while the device is not in use. To put the device in low power mode and disable the switch, the output enable pin \overline{OE} must be supplied with a logic high signal.

8.4 Device Functional Modes

8.4.1 Pin Functions

The SEL and \overline{OE} pins have a weak 6-M Ω pull-down to prevent floating input logic.

表 1. Function Table

\overline{OE}	SEL	Function
H	X	I/O pins High-Impedance
L	L	CLK(P/N) = CLKA(P/N)
		Dn(P/N) = DAn(P/N)
L	H	CLK(P/N) = CLKB(P/N)
		Dn(P/N) = DBn(P/N)

8.4.2 Low Power Disable Mode

While the output enable pin \overline{OE} is supplied with a logic high, the device remains in low power disabled state. This reduces the current consumption substantially and the switches are high impedance. The SEL pin is ignored while the \overline{OE} remains high. Upon exiting low power mode, the switch status reflects the SEL pin as seen in [表 1](#).

8.4.3 Switch Enabled Mode

While the output enable pin \overline{OE} is supplied with a logic low, the device remains in switch enabled mode.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

图 24 代表 TS5MP646 MIPI 开关的典型应用。TS5MP646 用于在多个 MIPI 模块和处理器上的单个 MIPI 端口之间切换信号。这扩展了单个端口的能力，使其能够处理多个 MIPI 模块。

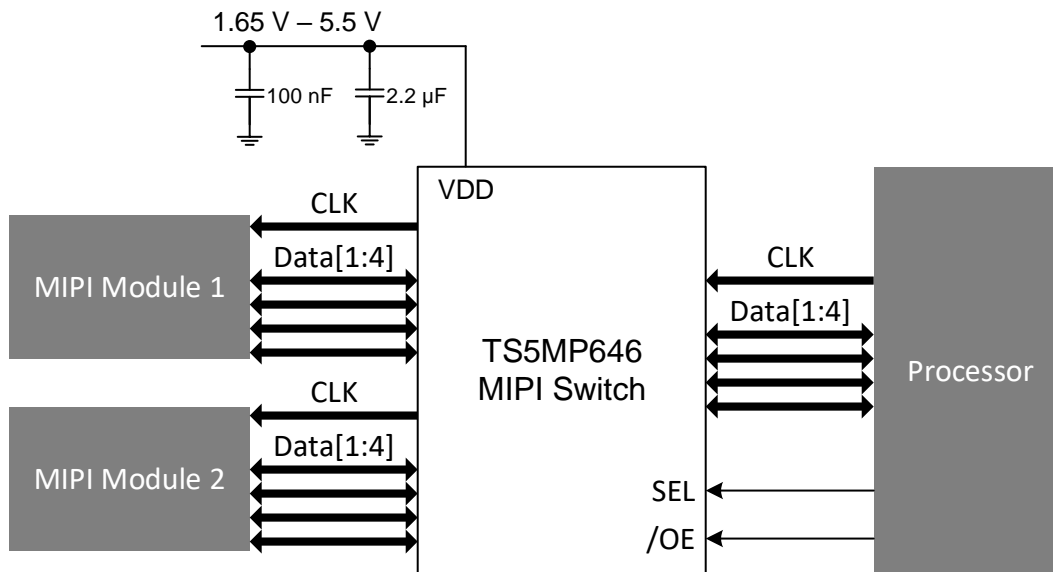


图 24. Typical D-PHY Application

Typical Application (接下页)

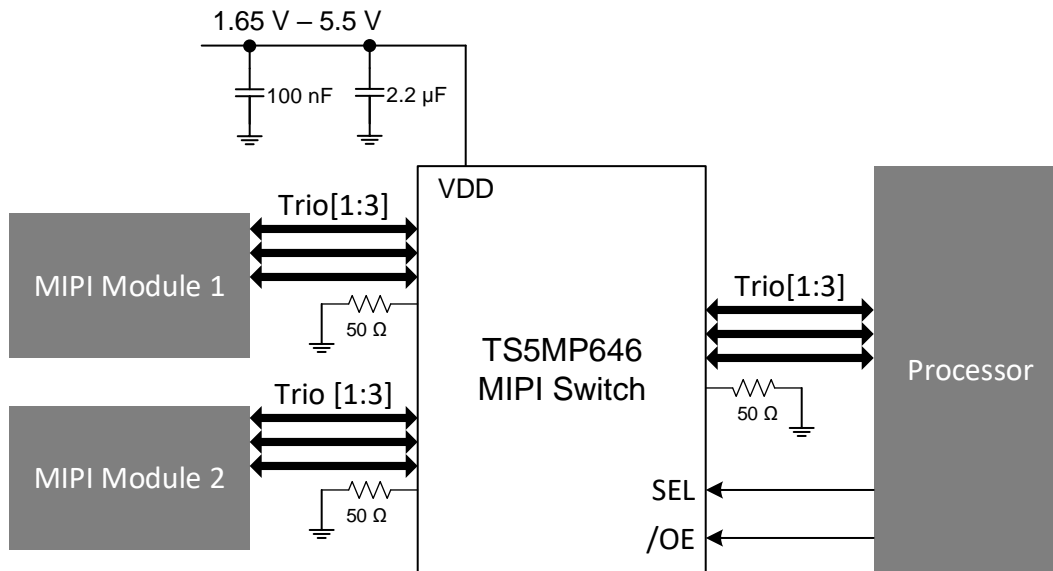


图 25. Typical C-PHY Application

9.2.1 Design Requirements

Design requirements of the MIPI standard must be followed. Supply pin decoupling capacitors of 2.2 μF and 100 nF are recommended for best performance. The TS5MP646 has internal 6-M Ω pulldown resistors on SEL and $\overline{\text{OE}}$. The pulldown on these pins ensure that the digital remains in a non-floating state during system power-up to prevent shoot through current spikes and an unknown switch status. By default the switch will power up enabled and with the A path selected until driven externally by the processor.

9.2.2 Detailed Design Procedure

The TS5MP646 can be properly operated without any external components. However, TI recommends that unused I/O signal pins be connected to ground through a 50 Ω resistor to prevent signal reflections and maintain device performance. The NC pins of the device do not require any external connections or terminations and have no connection to the rest of the device internally.

The clock and data lanes can be interchanged as necessary to facilitate the best layout possible for the application. For example, the clock can be placed on the D1 channel and a data lane can be used on the CLK channel if this improves the layout. In addition, the signal lines of the TS5MP646 are routed single ended on the chip die. This makes the device suitable for both differential and single-ended high-speed systems.

Typical Application (接下页)

9.2.3 Application Curves

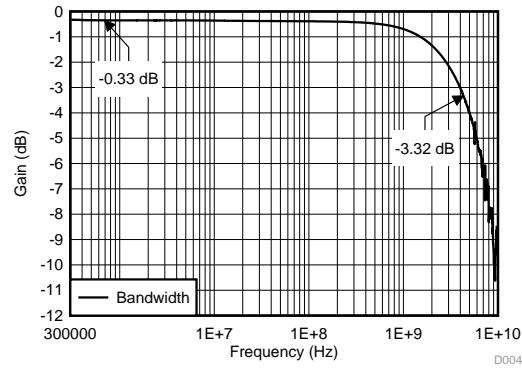
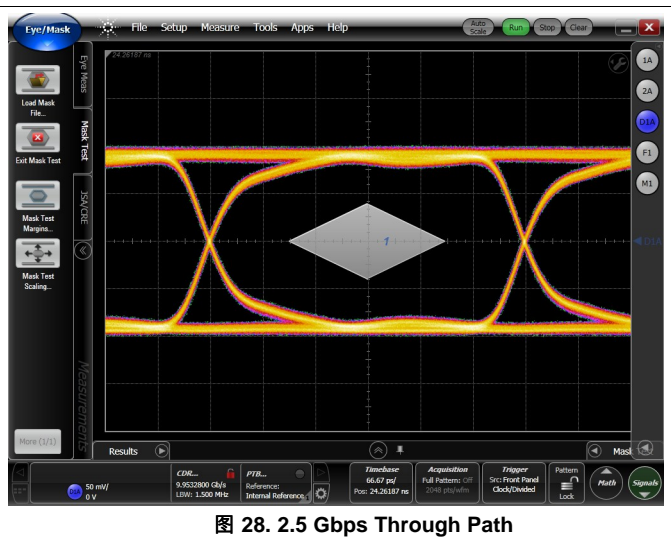
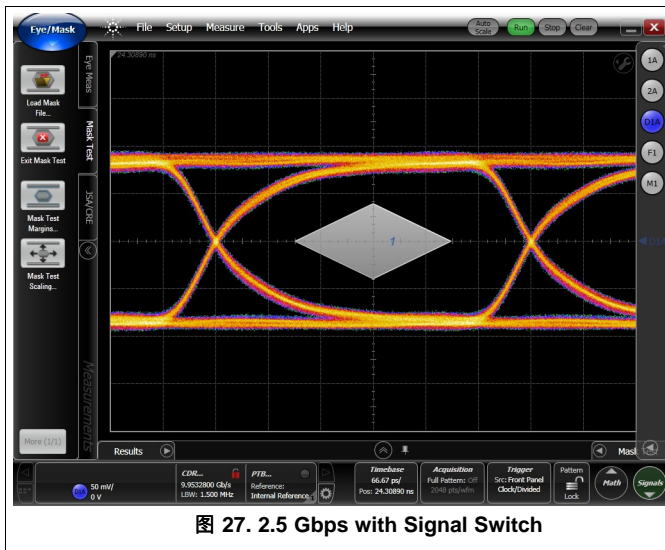


图 26. Differential Bandwidth



Typical Application (接下页)

9.2.3.1 MIPI D-PHY Application

The clock and data lanes can be interchanged as necessary to facilitate the best layout possible for the application. In addition, the signal lines of the TS5MP646 are routed single ended on the chip die. This makes the device suitable for both differential and single-ended high-speed systems. This also allows the positive and negative lines to be interchanged as necessary to facilitate the best layout possible for the application.

D-PHY application includes a differential clock and 4 differential datalanes. All the channels of the device perform similar and the clock or data signals may be interchanged as necessary to facilitate the best layout possible for the application.

Typical Application (接下页)

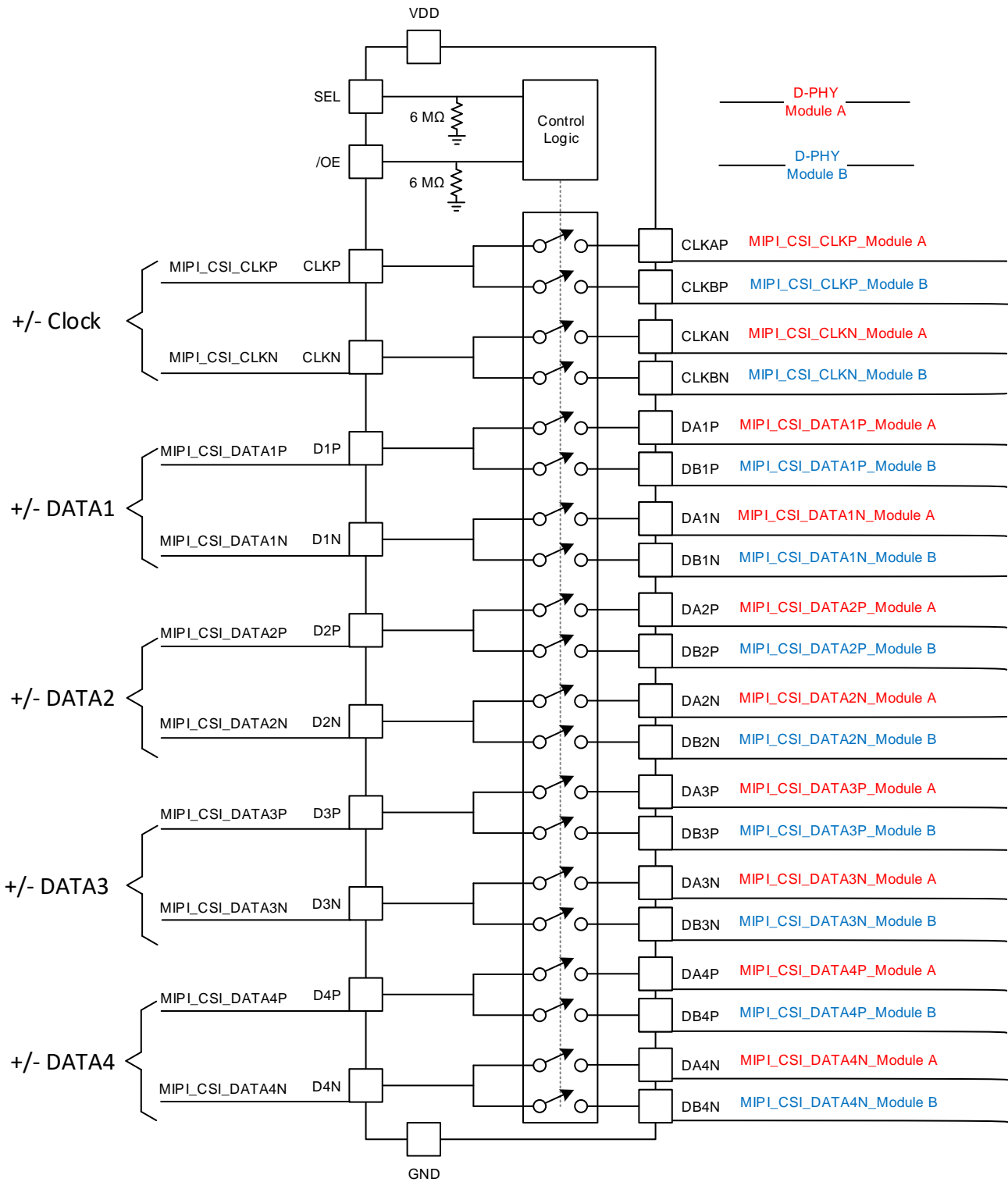


图 29. MIPI D-PHY Example Pinout

Typical Application (接下页)

9.2.3.2 MIPI C-PHY Application

The clock and data lanes can be interchanged as necessary to facilitate the best layout possible for the application. In addition, the signal lines of the TS5MP646 are routed single ended on the chip die. This makes the device suitable for both differential and single-ended high-speed systems. This also allows the positive and negative lines to be interchanged as necessary to facilitate the best layout possible for the application.

C-PHY application includes 3 trios of signals which may be routed on any channel which means there will be one unused channel on the TS5MP646. TI recommends that the unused I/O signal pin be connected to ground through a 50 Ω resistor to prevent signal reflections and maintain device performance.

Typical Application (接下页)

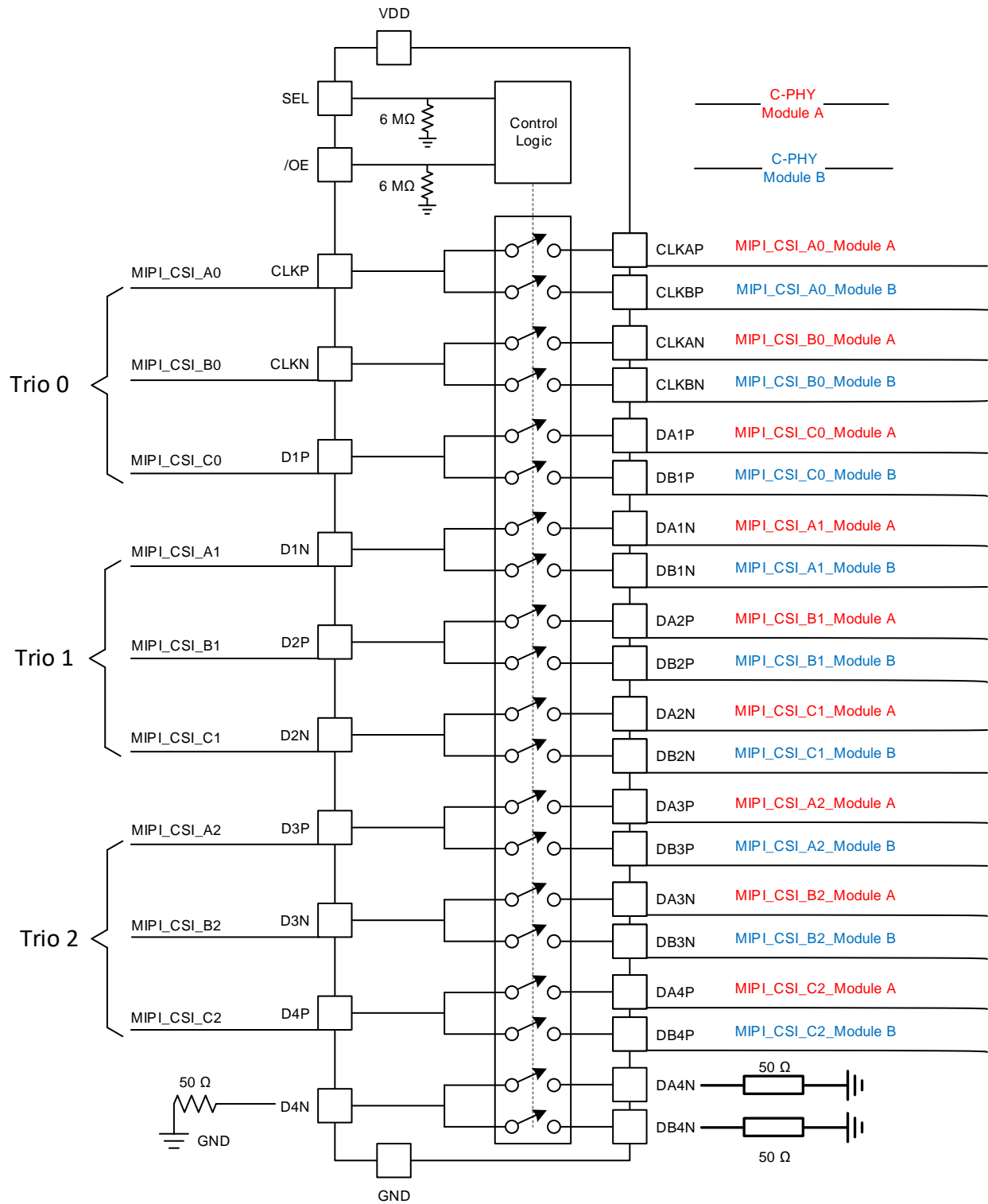


图 30. MIPI C-PHY Example Pinout

10 Power Supply Recommendations

When the TS5MP646 is powered off ($V_{DD} = 0\text{ V}$), the I/Os of the device remains in a high-Z state. The crosstalk, off-isolation, and leakage remain within the electrical *Specifications*. Power to the device is supplied through the VDD pin. Decoupling capacitors of 100 nF and 2.2 μF are recommended on the supply.

11 Layout

11.1 Layout Guidelines

Place the supply de-coupling capacitors as close to the VDD and GND pin as possible. The spacing between the power traces, supply and ground, and the signal I/O lines, clock and data, should be a minimum of three times the trace width of the signal I/O lines to maintain signal integrity.

The characteristic impedance of the trace(s) must match that of the receiver and transmitter to maintain signal integrity. Route the high-speed traces using a minimum amount of vias and corners. This will reduce the amount of impedance changes.

When it becomes necessary to make the traces turn 90°, use two 45° turns or an arc instead of making a single 90° turn.

Do not route high-speed traces near crystals, oscillators, external clock signals, switching regulators, mounting holes or magnetic devices.

Avoid stubs on the signal lines.

All I/O signal traces should be routed over a continuous ground plane with no interruptions. The minimum width from the edge of the trace to any break in the ground plane must be 3 times the trace width. When routing on PCB inner signal layers, the high speed traces should be between two ground planes and maintain characteristic impedance.

High speed signal traces must be length matched as much as possible to minimize skew between data and clock lines.

11.2 Layout Example

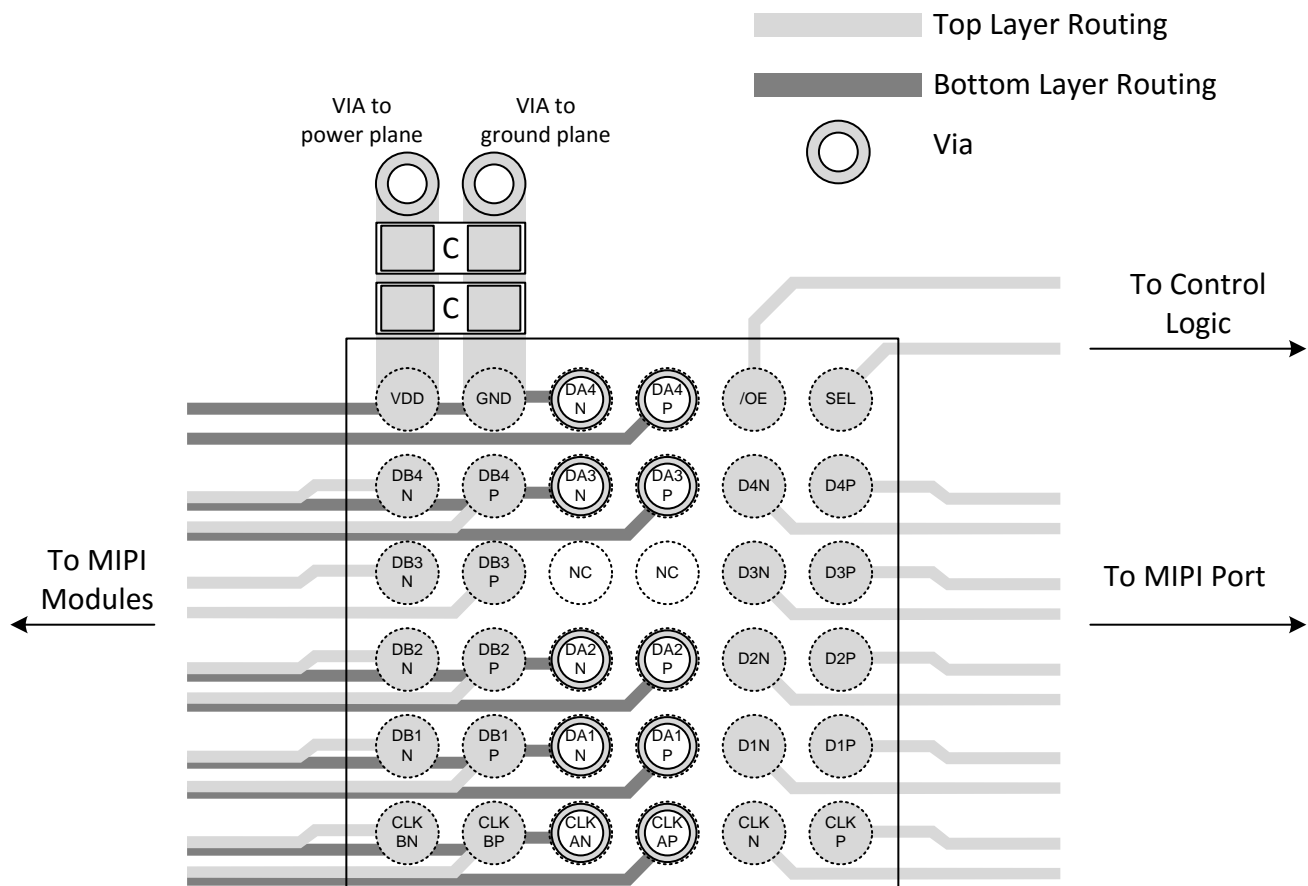


图 31. Layout Example

12 器件和文档支持

12.1 文档支持

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5MP646YFPR	NRND	DSBGA	YFP	36	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TS5MP646	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

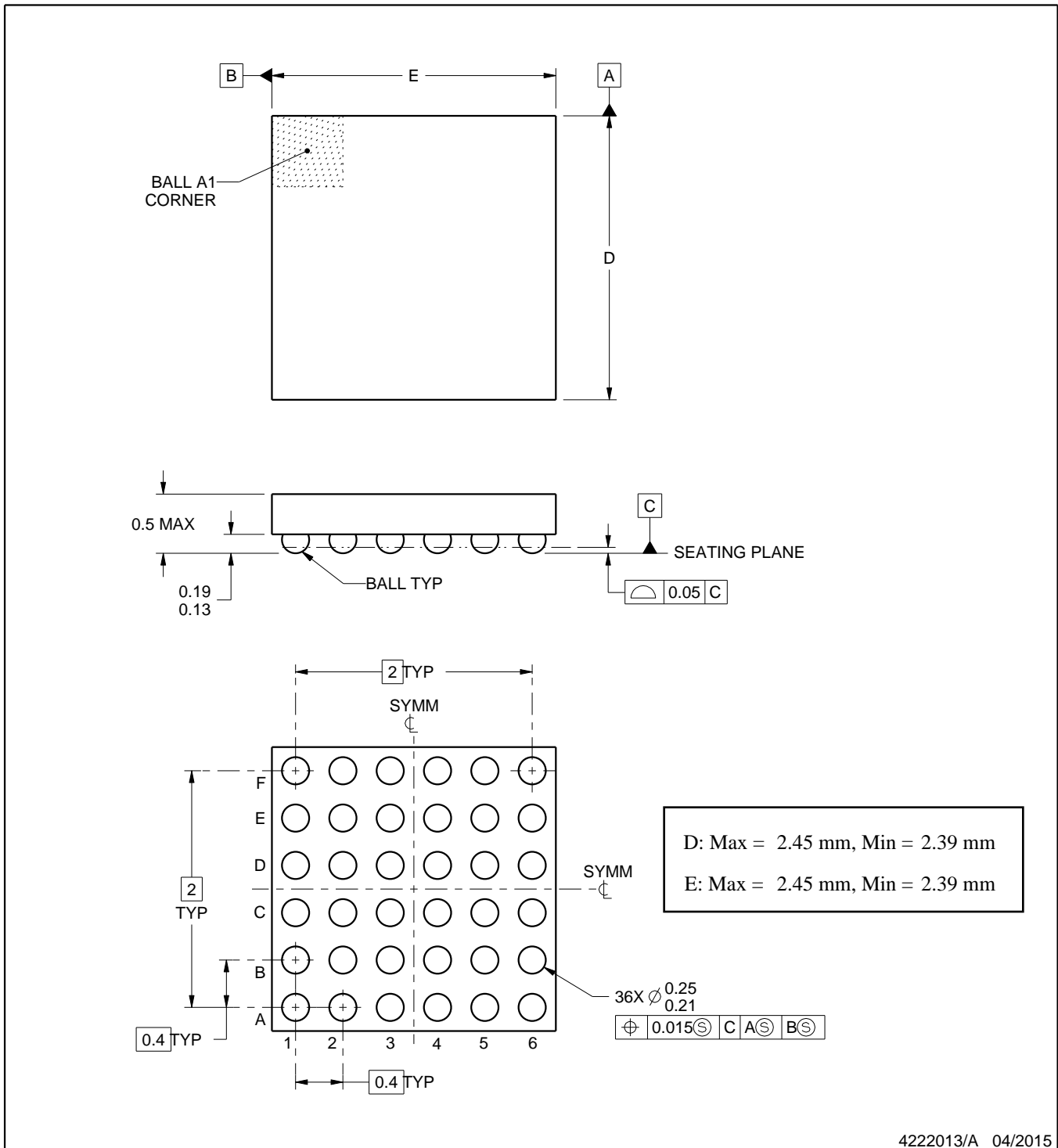
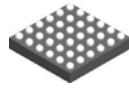

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5MP646YFPR	DSBGA	YFP	36	3000	330.0	12.4	2.58	2.58	0.62	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5MP646YFPR	DSBGA	YFP	36	3000	335.0	335.0	25.0



4222013/A 04/2015

NOTES:

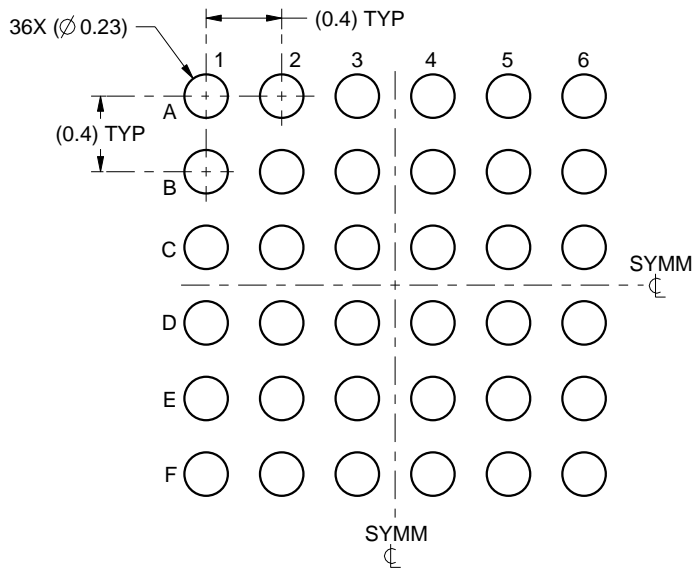
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

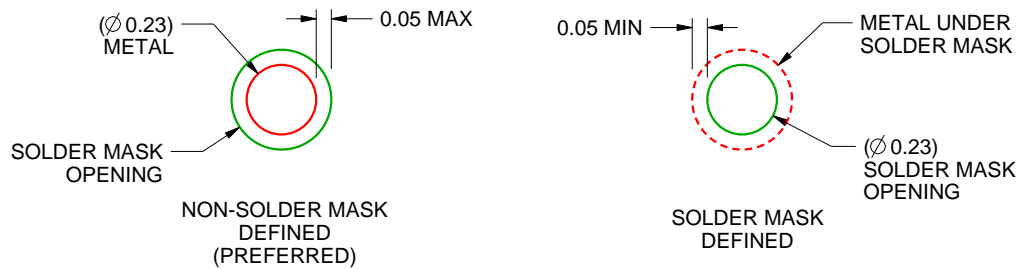
YFP0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4222013/A 04/2015

NOTES: (continued)

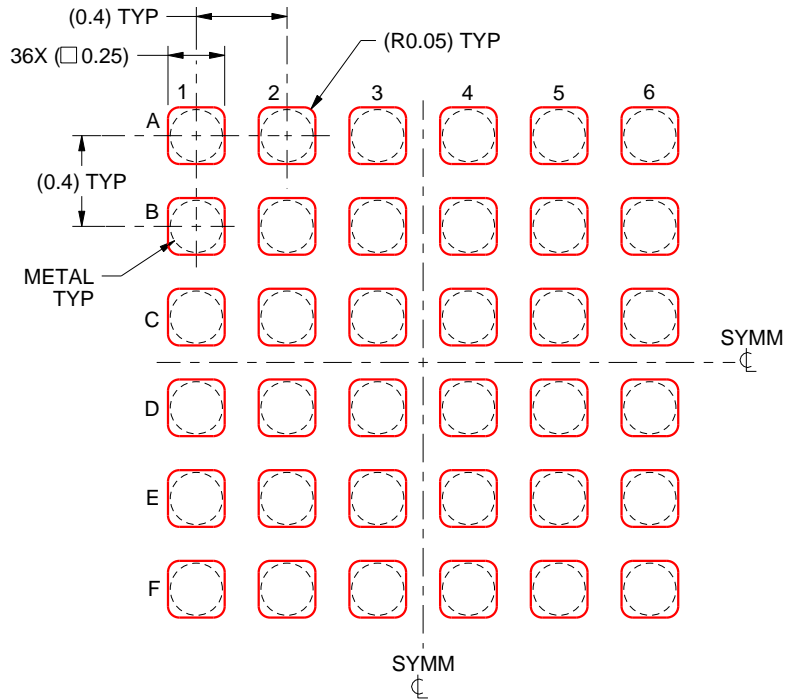
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222013/A 04/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司