

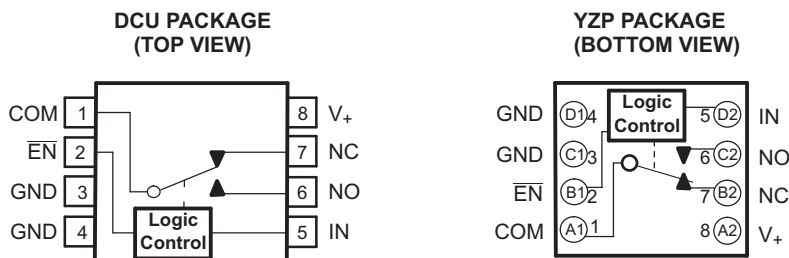
5-V/3.3-V SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Isolation in the Powered-Off Mode, $V_{+} = 0$
- Specified Break-Before-Make Switching
- Low ON-State Resistance ($1\ \Omega$)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



DESCRIPTION/ORDERING INFORMATION

The TS5A3153 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent on-resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|----------------|---|--------------|-----------------------|---------------------------------|
| –40°C to 85°C | NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | TS5A3153YZPR | ___J57 |
| | SSOP – DCU | Reel of 3000 | TS5A3153DCUR | JCD_ |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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FUNCTION TABLE

| $\overline{\text{EN}}$ | IN | NC TO COM, COM TO NC | NO TO COM, COM TO NO |
|------------------------|----|-------------------------|-------------------------|
| L | L | ON | OFF |
| L | H | OFF | ON |
| H | X | OFF | OFF |

Summary of Characteristics⁽¹⁾

| Configuration | Single-Pole, Double-Throw 2:1 Multiplexer/Demultiplexer (SPDT) |
|---|---|
| Number of channels | 1 |
| ON-state resistance (r_{on}) | 1.1 Ω |
| ON-state resistance match (Δr_{on}) | 0.1 Ω |
| ON-state resistance flatness ($r_{on(flat)}$) | 0.15 Ω |
| Turn-on/turn-off time (t_{ON}/t_{OFF}) | 20 ns/15 ns |
| Make-before-break time (t_{MKB}) | 12 ns |
| Charge injection (Q_C) | 36 pC |
| Bandwidth (BW) | 100 MHz |
| OFF isolation (O_{ISO}) | –65 dB at 1 MHz |
| Crosstalk (X_{TALK}) | –68 dB at 1 MHz |
| Total harmonic distortion (THD) | 0.01% |
| Leakage current ($I_{COM(OFF)}/I_{NC(OFF)}$) | ± 20 nA |
| Power-supply current (I_+) | 0.1 μA |
| Package option | 8-pin SSOP or DSBGA |

(1) $V_+ = 5$ V, $T_A = 25^\circ\text{C}$

ABSOLUTE MINIMUM AND MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---------------------------------------|---|--|------------|-------------|-------------|
| V_+ | Supply voltage range ⁽³⁾ | | –0.5 | 6.5 | V |
| V_{NC} , V_{NO} , V_{COM} | Analog voltage range ⁽³⁾⁽⁴⁾⁽⁵⁾ | | –0.5 | $V_+ + 0.5$ | V |
| I_K | Analog port diode current | $V_{NC}, V_{NO}, V_{COM} < 0$ or $V_{NO}, V_{NC}, V_{COM} > V_+$ | –50 | | mA |
| I_{NC} , I_{COM} , I_{NO} | On-state switch current | $V_{NC}, V_{NO}, V_{COM} = 0$ to V_+ | –200 | 200 | mA |
| | On-state peak switch current ⁽⁶⁾ | | –400 | 400 | |
| V_I | Digital input voltage range ⁽³⁾⁽⁴⁾ | | –0.5 | 6.5 | V |
| I_{IK} | Digital input clamp current | $V_I < 0$ | –50 | | mA |
| I_+ | Continuous current through V_+ | | | 100 | mA |
| I_{GND} | Continuous current through GND | | –100 | 100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁷⁾ | DCU package | | 227 | °C/W |
| | | YZP package | | 102 | |
| T_{stg} | Storage temperature range | | –65 | 150 | °C |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY⁽¹⁾

V₊ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T _A | V ₊ | MIN | TYP | MAX | UNIT | | |
|--|--|--|------------------------------|----------------|-------|------|----------------|------|-----|-----|
| Analog Switch | | | | | | | | | | |
| Analog signal range | V _{COM} , V _{NO} , V _{NC} | | | | 0 | | V ₊ | V | | |
| Peak ON resistance | r _{peak} | 0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | 0.9 | 1.1 | Ω | | |
| | | | | Full | | | 1.3 | | | |
| ON-state resistance | r _{on} | V _{NO} or V _{NC} = 2.5 V, I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | 0.8 | 0.9 | Ω | | |
| | | | | Full | | | 1.1 | | | |
| ON-state resistance matching between channels | Δr _{on} | V _{NO} or V _{NC} = 2.5 V, I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | 0.05 | 0.1 | Ω | | |
| | | | | Full | | | 0.1 | | | |
| ON-state resistance flatness | r _{on(flat)} | 0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | 0.15 | | Ω | | |
| | | | | Full | | | | | | |
| | | V _{NO} or V _{NC} = 1 V, 1.5 V, 2.5 V, I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | | 0.09 | 0.15 | | | |
| | | | | Full | | 0.15 | | | | |
| NC, NO OFF leakage current | I _{NC(OFF)} , I _{NO(OFF)} | V _{NC} or V _{NO} = 1 V, V _{COM} = 4.5 V, or V _{NC} or V _{NO} = 4.5 V, V _{COM} = 1 V, | Switch OFF, See Figure 14 | 25°C | 5.5 V | –20 | 2 | 20 | nA | |
| | | | | Full | | | –150 | | | 150 |
| | I _{NC(PWROFF)} , I _{NO(PWROFF)} | V _{NC} or V _{NO} = 0 to 5.5 V, V _{COM} = 5.5 V to 0, | Switch OFF, See Figure 14 | 25°C | | 0 V | –5 | 0.7 | 5 | μA |
| | | | | Full | | | | –25 | | |
| NC, NO ON leakage current | I _{NC(ON)} , I _{NO(ON)} | V _{NC} or V _{NO} = 1 V, V _{COM} = Open, or V _{NC} or V _{NO} = 4.5 V, V _{COM} = Open, | Switch ON, See Figure 15 | 25°C | 5.5 V | –20 | 2 | 20 | nA | |
| | | | | Full | | | –150 | | | 150 |
| COM OFF leakage current | I _{COM(OFF)} | V _{COM} = 1 V, V _{NC} or V _{NO} = 4.5 V, or V _{COM} = 4.5 V, V _{NC} or V _{NO} = 1 V, | Switch OFF, See Figure 14 | 25°C | 5.5 V | –20 | 2 | 20 | nA | |
| | | | | Full | | | –150 | | | 150 |
| | I _{COM(PWROFF)} | V _{NC} or V _{NO} = 0 to 5.5 V, V _{COM} = 5.5 V to 0, | Switch OFF, See Figure 14 | 25°C | | 0 V | –5 | 0.7 | 5 | μA |
| | | | | Full | | | | –25 | | |
| COM ON leakage current | I _{COM(ON)} | V _{COM} = 1 V, V _{NC} or V _{NO} = Open, or V _{COM} = 4.5 V, V _{NC} or V _{NO} = Open, | Switch ON, See Figure 15 | 25°C | 5.5 V | –20 | 2 | 20 | nA | |
| | | | | Full | | | –150 | | | 150 |
| Digital Control Inputs (IN, EN)⁽²⁾ | | | | | | | | | | |
| Input logic high | V _{IH} | | Full | | 2.4 | | 5.5 | V | | |
| Input logic low | V _{IL} | | Full | | 0 | | 0.8 | V | | |
| Input leakage current | I _{IH} , I _{IL} | V _I = 5.5 V or 0 V | 25°C | 5.5 V | –100 | 25 | 100 | nA | | |
| | | | Full | | | –100 | | | 100 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
 (2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (continued)
 $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|---------------------------|----------------------------------|---|--|-------|----------------|-----|-------|------|---------------|
| Dynamic | | | | | | | | | |
| Turn-on time | t_{ON} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 5 V | 1 | 12.5 | 16 | ns |
| | | | | Full | 4.5 V to 5.5 V | 1 | | 17.5 | |
| Turn-off time | t_{OFF} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 5 V | 2.5 | 8.5 | 15 | ns |
| | | | | Full | 4.5 V to 5.5 V | 2 | | 18 | |
| Break-before-make time | t_{MBB} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 5 V | 1 | 7 | 12 | ns |
| | | | | Full | 4.5 V to 5.5 V | 0.5 | | 15 | |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$, | $C_L = 1\text{ nF}$, See Figure 22 | 25°C | 5 V | | 12 | pC | |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch OFF, See Figure 16 | 25°C | 5 V | | 19 | pF | |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 5 V | | 57 | pF | |
| COM OFF capacitance | $C_{COM(OFF)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 5 V | | 36 | pF | |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 5 V | | 57 | pF | |
| Digital input capacitance | C_I | $V_I = V_+$ or GND, | See Figure 16 | 25°C | 5 V | | 2 | pF | |
| Bandwidth | BW | $R_L = 50\ \Omega$, | Switch ON, See Figure 19 | 25°C | 5 V | | 97 | MHz | |
| OFF isolation | O_{ISO} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch OFF, See Figure 20 | 25°C | 5 V | | -64 | dB | |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch ON, See Figure 21 | 25°C | 5 V | | -64 | dB | |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, | $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23 | 25°C | 5 V | | 0.004 | % | |
| Supply | | | | | | | | | |
| Positive supply current | I_+ | $V_I = V_+$ or GND, | Switch ON or OFF | 25°C | 5.5 V | | 0.02 | 0.1 | μA |
| | | | | Full | | | | 0.5 | |

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY⁽¹⁾

V₊ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T _A | V ₊ | MIN | TYP | MAX | UNIT | |
|--|--|--|------------------------------|----------------|-------|------|----------------|------|------|
| Analog Switch | | | | | | | | | |
| Analog signal range | V _{COM} , V _{NO} , V _{NC} | | | | 0 | | V ₊ | V | |
| Peak ON resistance | r _{peak} | 0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | 1.3 | 1.6 | Ω | |
| | | | | Full | | | | | 1.8 |
| ON-state resistance | r _{on} | V _{NO} or V _{NC} = 2 V, I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | 1.2 | 1.5 | Ω | |
| | | | | Full | | | | | 1.7 |
| ON-state resistance match between channels | Δr _{on} | V _{NO} or V _{NC} = 2 V, 0.8 V I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | 0.08 | 0.15 | Ω | |
| | | | | Full | | | | | 0.15 |
| ON-state resistance flatness | r _{on(flat)} | 0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | 0.2 | | Ω | |
| | | | | Full | | | | | |
| | | V _{NO} or V _{NC} = 2 V, 0.8 V, I _{COM} = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | 0.09 | 0.15 | | |
| | | | | Full | | 0.15 | | | |
| NC, NO OFF leakage current | I _{NC(OFF)} , I _{NO(OFF)} | V _{NC} or V _{NO} = 1 V, V _{COM} = 3 V, or V _{NC} or V _{NO} = 3 V, V _{COM} = 1 V, | Switch OFF, See Figure 14 | 25°C | 3.6 V | –20 | 2 | 20 | nA |
| | | | | Full | | –50 | 50 | | |
| | I _{NC(PWROFF)} , I _{NO(PWROFF)} | V _{NC} or V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0 V, | Switch OFF, See Figure 14 | 25°C | 0 V | –1 | 0.2 | 1 | μA |
| | | | | Full | | –15 | 15 | | |
| NC, NO ON leakage current | I _{NC(ON)} , I _{NO(ON)} | V _{NC} or V _{NO} = 1 V, V _{COM} = Open, or V _{NC} or V _{NO} = 3 V, V _{COM} = Open, | Switch ON, See Figure 15 | 25°C | 3.6 V | –20 | 2 | 20 | nA |
| | | | | Full | | –50 | 50 | | |
| COM OFF leakage current | I _{COM(OFF)} | V _{COM} = 1 V, V _{NC} or V _{NO} = 3 V, or V _{COM} = 3 V, V _{NC} or V _{NO} = 1 V, | Switch OFF, See Figure 14 | 25°C | 3.6 V | –20 | 2 | 20 | nA |
| | | | | Full | | –50 | 50 | | |
| | I _{COM(PWROFF)} | V _{NC} or V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0 V, | Switch OFF, See Figure 14 | 25°C | 0 V | –1 | 0.2 | 1 | μA |
| | | | | Full | | –15 | 15 | | |
| COM ON leakage current | I _{COM(ON)} | V _{COM} = 1 V, V _{NC} or V _{NO} = Open, or V _{COM} = 3 V, V _{NC} or V _{NO} = Open | Switch ON, See Figure 15 | 25°C | 3.6 V | –20 | 2 | 20 | nA |
| Full | –50 | 50 | | | | | | | |
| Digital Control Inputs (IN, EN)⁽²⁾ | | | | | | | | | |
| Input logic high | V _{IH} | | | Full | | 2 | 5.5 | V | |
| Input logic low | V _{IL} | | | Full | | 0 | 0.8 | V | |
| Input leakage current | I _{IH} , I _{IL} | V _I = 5.5 V or 0 | | 25°C | 3.6 V | –100 | 25 | 100 | nA |
| | | | | Full | | –100 | 100 | | |

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|---------------------------|----------------------------------|---|--|-------|--------------|------|------|---------------|----|
| Dynamic | | | | | | | | | |
| Turn-on time | t_{ON} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 3.3 V | 1 | 17 | 22 | ns |
| | | | | Full | 3 V to 3.6 V | 1 | | 24 | |
| Turn-off time | t_{OFF} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 3.3 V | 4.3 | 9.5 | 16 | ns |
| | | | | Full | 3 V to 3.6 V | 4 | | 19 | |
| Break-before-make time | t_{MBS} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 3.3 V | 2 | 12 | 22 | ns |
| | | | | Full | 3 V to 3.6 V | 1 | | 25 | |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$, | $C_L = 1\text{ nF}$, See Figure 22 | 25°C | 3.3 V | | 8 | pC | |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch OFF, See Figure 16 | 25°C | 3.3 V | | 19 | pF | |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 3.3 V | | 57 | pF | |
| COM OFF capacitance | $C_{COM(OFF)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See | 25°C | 3.3 V | | 36 | pF | |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 3.3 V | | 57 | pF | |
| Digital input capacitance | C_I | $V_I = V_+$ or GND, | See Figure 16 | 25°C | 3.3 V | | 2 | pF | |
| Bandwidth | BW | $R_L = 50\ \Omega$, | Switch ON, See Figure 19 | 25°C | 3.3 V | | 97 | MHz | |
| OFF isolation | O_{ISO} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch OFF, See Figure 20 | 25°C | 3.3 V | | -64 | dB | |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch ON, See Figure 21 | 25°C | 3.3 V | | -64 | dB | |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, | $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23 | 25°C | 3.3 V | | 0.01 | % | |
| Supply | | | | | | | | | |
| Positive supply current | I_+ | $V_I = V_+$ or GND, | Switch ON or OFF | 25°C | 3.6 V | 0.01 | 0.1 | μA | |
| | | | | Full | | | 0.25 | | |

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY⁽¹⁾

V₊ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T _A | V ₊ | MIN | TYP | MAX | UNIT | | |
|--|--|--|--|----------------|-------|------|----------------|------|-----|------|
| Analog Switch | | | | | | | | | | |
| Analog signal range | V _{COM} , V _{NO} , V _{NC} | | | | 0 | | V ₊ | V | | |
| Peak ON resistance | r _{peak} | 0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | 1.9 | 2.5 | Ω | | |
| | | | | Full | | | | | 2.7 | |
| ON-state resistance | r _{on} | V _{NO} or V _{NC} = 1.8 V, I _{COM} = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | 1.6 | 2.1 | Ω | | |
| | | | | Full | | | | | 2.5 | |
| ON-state resistance matching between channels | Δr _{on} | V _{NO} or V _{NC} = 1.8 V, I _{COM} = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | 0.12 | 0.2 | Ω | | |
| | | | | Full | | | | | 0.2 | |
| ON-state resistance flatness | r _{on(flat)} | 0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | 0.65 | | Ω | | |
| | | | | 25°C | | | | | 0.5 | 1 |
| | | | | Full | | | | | | |
| NC, NO OFF leakage current | I _{NC(OFF)} , I _{NO(OFF)} | V _{NC} or V _{NO} = 0.5 V, V _{COM} = 2.2 V, or V _{NC} or V _{NO} = 2.2 V, V _{COM} = 0.5 V, | Switch OFF, See Figure 14 | 25°C | 2.7 V | –20 | 2 | 20 | | |
| | | | | Full | | | | | –50 | 50 |
| | I _{NC(PWROFF)} , I _{NO(PWROFF)} | V _{NC} or V _{NO} = 0 to 2.7 V, V _{COM} = 2.7 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 V | –1 | 0.1 | 1 | | |
| | | | | Full | | | | | –10 | 10 |
| NC, NO ON leakage current | I _{NC(ON)} , I _{NO(ON)} | V _{NC} or V _{NO} = 0.5 V, V _{COM} = Open, or V _{NC} or V _{NO} = 2.2 V, V _{COM} = Open, | Switch ON, See Figure 15 | 25°C | 2.7 V | –20 | | 20 | | |
| | | | | Full | | | | | –50 | 50 |
| COM OFF leakage current | I _{COM(OFF)} | V _{COM} = 0.5 V, V _{NC} or V _{NO} = 2.2 V, or V _{COM} = 2.2 V, V _{NC} or V _{NO} = 0.5V, | Switch OFF, See Figure 14 | 25°C | 2.7 V | –20 | | 20 | | |
| | | | | Full | | | | | –50 | 50 |
| | | | | 25°C | | | | | 0 V | –1 |
| Full | –10 | 10 | | | | | | | | |
| COM ON leakage current | I _{COM(ON)} | V _{COM} = 0.5 V, V _{NC} or V _{NO} = Open, or V _{COM} = 2.2 V, V _{NC} or V _{NO} = Open, | Switch ON, See Figure 15 | 25°C | 2.7 V | –20 | | 20 | | |
| | | | | Full | | | | | –50 | 50 |
| Digital Control Inputs (I_N, $\overline{\text{EN}}$)⁽²⁾ | | | | | | | | | | |
| Input logic high | V _{IH} | | | Full | | 1.8 | | 5.5 | V | |
| Input logic low | V _{IL} | | | Full | | 0 | | 0.6 | V | |
| Input leakage current | I _{IH} , I _{IL} | V _I = 5.5 V or 0 | | 25°C | 2.7 V | –100 | 25 | 100 | nA | |
| | | | | Full | | | | | | –100 |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
 (2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|---------------------------|----------------------------------|---|--|-------|----------------|-------|-------|---------------|----|
| Dynamic | | | | | | | | | |
| Turn-on time | t_{ON} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 2.5 V | 1.7 | 24 | 31 | ns |
| | | | | Full | 2.3 V to 2.7 V | 1.5 | | 33.5 | |
| Turn-off time | t_{OFF} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 2.5 V | 5.2 | 10.5 | 17 | ns |
| | | | | Full | 2.3 V to 2.7 V | 5 | | 20 | |
| Break-before-make time | $t_{M\text{BB}}$ | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 2.5 V | 3 | 10 | 30 | ns |
| | | | | Full | 2.3 V to 2.7 V | 2 | | 40 | |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$, | $C_L = 1\text{ nF}$, See Figure 22 | 25°C | 2.5 V | | 6 | pC | |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch OFF, See Figure 16 | 25°C | 2.5 V | | 19 | pF | |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 2.5 V | | 57 | pF | |
| COM OFF capacitance | $C_{COM(OFF)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 2.5 V | | 36 | pF | |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 2.5 V | | 57 | pF | |
| Digital input capacitance | C_I | $V_I = V_+$ or GND, | See Figure 16 | 25°C | 2.5 V | | 2 | pF | |
| Bandwidth | BW | $R_L = 50\ \Omega$, | Switch ON, See Figure 19 | 25°C | 2.5 V | | 100 | MHz | |
| OFF isolation | O_{ISO} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch OFF, See Figure 20 | 25°C | 2.5 V | | -64 | dB | |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch ON, See Figure 21 | 25°C | 2.5 V | | -64 | dB | |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, | $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23 | 25°C | 2.5 V | | 0.020 | % | |
| Supply | | | | | | | | | |
| Positive supply current | I_+ | $V_I = V_+$ or GND, | Switch ON or OFF | 25°C | 2.7 V | 0.001 | 0.05 | μA | |
| | | | | Full | | | 0.15 | | |

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY⁽¹⁾

V₊ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T _A | V ₊ | MIN | TYP | MAX | UNIT | |
|--|--|--|----------------|----------------|-----|------|----------------|------|-----|
| Analog Switch | | | | | | | | | |
| Analog signal range | V _{COM} , V _{NO} , V _{NC} | | | | 0 | | V ₊ | V | |
| Peak ON resistance | r _{peak} | 0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –2 mA, | 25°C | 1.65 V | | 5.2 | 15 | Ω | |
| | | | Full | | | | | | 20 |
| ON-state resistance | r _{on} | V _{NO} or V _{NC} = 1.5 V, I _{COM} = –2 mA, | 25°C | 1.65 V | | 2 | 2.7 | Ω | |
| | | | Full | | | | | | 3.1 |
| ON-state resistance matching between channels | Δr _{on} | V _{NO} or V _{NC} = 1.5 V, I _{COM} = –2 mA, | 25°C | 1.65 V | | 0.16 | 0.3 | Ω | |
| | | | Full | | | | | | 0.3 |
| ON-state resistance flatness | r _{on(flat)} | 0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –2 mA, | 25°C | 1.65 V | | 3 | | Ω | |
| | | V _{NO} or V _{NC} = 0.6 V, 1.5 V, I _{COM} = –2 mA, | 25°C | | | | 3 | | 6 |
| | | | Full | | | | | | 8 |
| NC, NO OFF leakage current | I _{NC(OFF)} , I _{NO(OFF)} | V _{NC} or V _{NO} = 0.3 V, V _{COM} = 1.65 V, or V _{NC} or V _{NO} = 1.65 V, V _{COM} = 0.3 V, | 25°C | 1.95 V | | –20 | 1.5 | 20 | nA |
| | | | Full | | | | | –50 | |
| | I _{NC(PWROFF)} , I _{NO(PWROFF)} | V _{NC} or V _{NO} = 0 to 1.95 V, V _{COM} = 1.95 V to 0, | 25°C | 0 V | | –1 | 0.1 | 1 | μA |
| | | | Full | | | | | –10 | |
| NC, NO ON leakage current | I _{NC(ON)} , I _{NO(ON)} | V _{NC} or V _{NO} = 0.3 V, V _{COM} = Open, or V _{NC} or V _{NO} = 1.65 V, V _{COM} = Open, | 25°C | 1.95 V | | –20 | 1.5 | 20 | nA |
| | | | Full | | | | | –50 | |
| COM OFF leakage current | I _{COM(OFF)} | V _{NC} or V _{NO} = 1.65 V, V _{COM} = 0.3 V, or V _{NC} or V _{NO} = 0.3 V, V _{COM} = 1.65 V, | 25°C | 1.95 V | | –20 | 1.5 | 20 | nA |
| | | | Full | | | | | –50 | |
| | I _{COM(PWROFF)} | V _{NC} or V _{NO} = 1.95 V to 0, V _{COM} = 0 to 1.95 V, | 25°C | 0 V | | –1 | 0.06 | 1 | μA |
| | | | Full | | | | | –10 | |
| COM ON leakage current | I _{COM(ON)} | V _{NC} or V _{NO} = Open, V _{COM} = 0.3 V, or V _{NC} or V _{NO} = Open, V _{COM} = 1.65 V, | 25°C | 1.95 V | | –20 | 1.5 | 20 | nA |
| | | | Full | | | | | –50 | |
| Digital Control Inputs (IN, EN)⁽²⁾ | | | | | | | | | |
| Input logic high | V _{IH} | | Full | | 1.5 | | 5.6 | V | |
| Input logic low | V _{IL} | | Full | | 0 | | 0.6 | V | |
| Input leakage current | I _{IH} , I _{IL} | V _I = 5.5 V or 0 | 25°C | 1.95 V | | –100 | 25 | 100 | nA |
| | | | Full | | | | | –100 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
 (2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY (continued)
 $V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|---------------------------|----------------------------------|---|--|-------|------------------|-----|-------|------|---------------|
| Dynamic | | | | | | | | | |
| Turn-on time | t_{ON} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 5 V | 4.5 | 45 | 61 | ns |
| | | | | Full | 1.65 V to 1.95 V | 4 | | 63 | |
| Turn-off time | t_{OFF} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 5 V | 5.4 | 12 | 19 | ns |
| | | | | Full | 1.65 V to 1.95 V | 5 | | 21 | |
| Break-before-make time | t_{BBM} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 5 V | 4 | 31 | 60 | ns |
| | | | | Full | 1.65 V to 1.95 V | 3 | | 65 | |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$, | $C_L = 1\text{ nF}$, See Figure 22 | 25°C | 1.8 V | | 4 | pC | |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch OFF, See Figure 16 | 25°C | 1.8 V | | 19 | pF | |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 1.8 V | | 57 | pF | |
| COM OFF capacitance | $C_{COM(OFF)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 1.8 V | | 36 | pF | |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 1.8 V | | 57 | pF | |
| Digital input capacitance | C_I | $V_I = V_+$ or GND, | See Figure 16 | 25°C | 1.8 V | | 2 | pF | |
| Bandwidth | BW | $R_L = 50\ \Omega$, | Switch ON, See Figure 19 | 25°C | 1.8 V | | 100 | MHz | |
| OFF isolation | O_{ISO} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch OFF, See Figure 20 | 25°C | 1.8 V | | -64 | dB | |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch ON, See Figure 21 | 25°C | 1.8 V | | -64 | dB | |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, | $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23 | 25°C | 1.8 V | | 0.060 | % | |
| Supply | | | | | | | | | |
| Positive supply current | I_+ | $V_I = V_+$ or GND, | Switch ON or OFF | 25°C | 1.95 V | | 0.001 | 0.05 | μA |
| | | | | Full | | | 0.1 | | |

TYPICAL PERFORMANCE

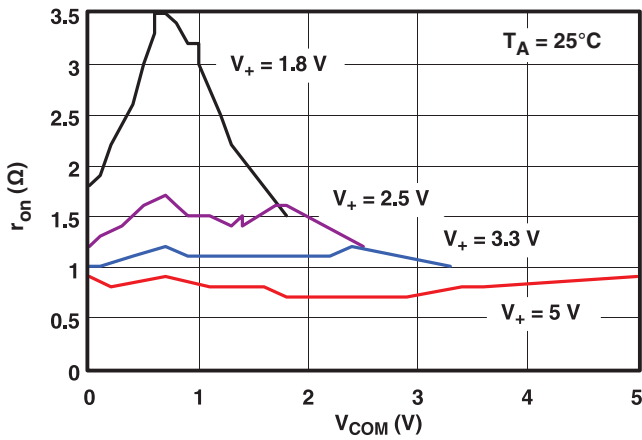


Figure 1. r_{on} vs V_{COM}

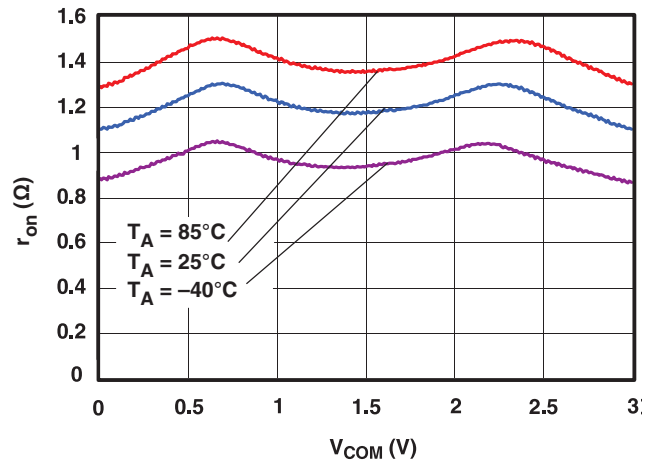


Figure 2. r_{on} vs V_{COM} ($V_+ = 3$ V)

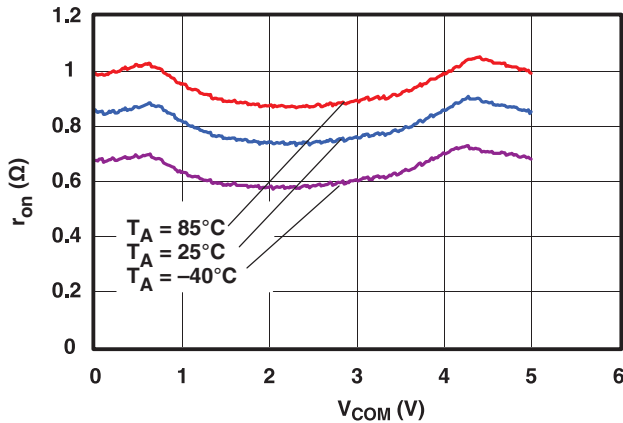


Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)

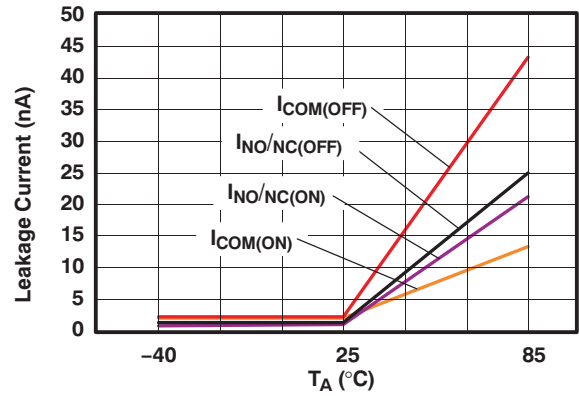


Figure 4. Leakage Current vs Temperature ($V_+ = 5.5$ V)

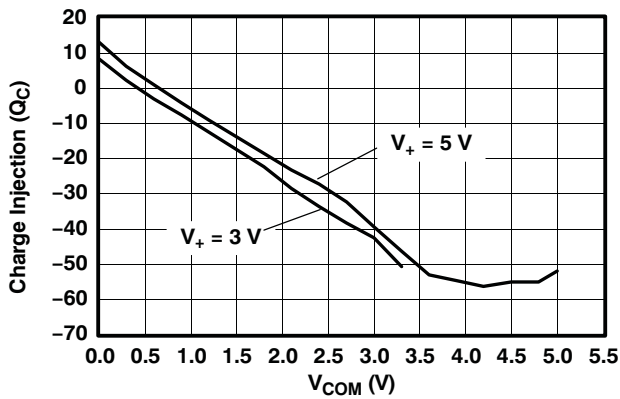


Figure 5. Charge Injection (Q_C) vs V_{COM}

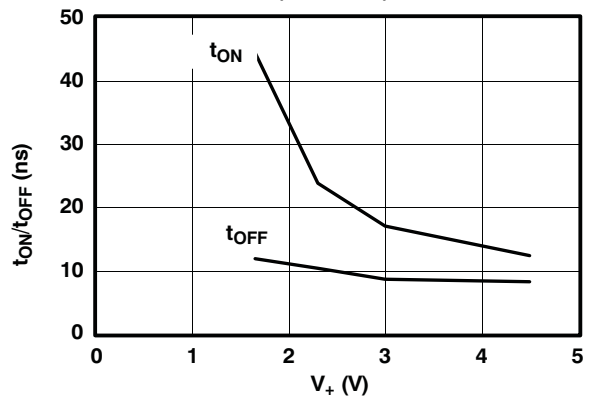


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE (continued)

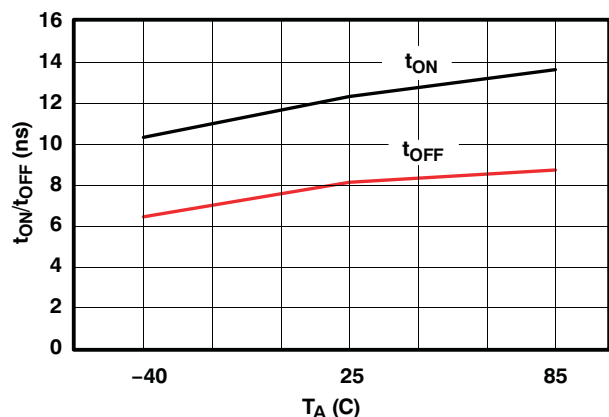


Figure 7. t_{ON} and t_{OFF} vs Temperature ($V_+ = 5\text{ V}$)

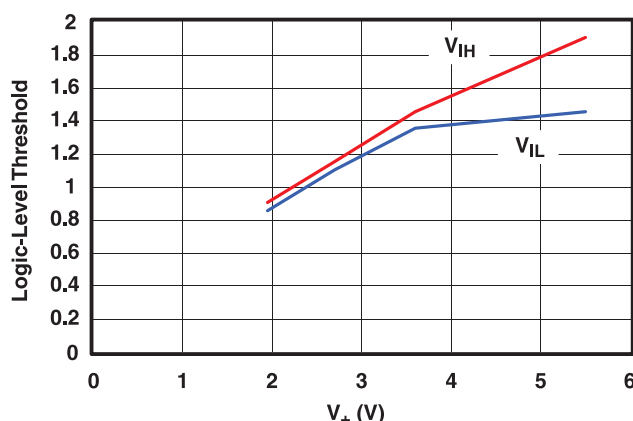


Figure 8. Logic-Level Threshold vs V_+

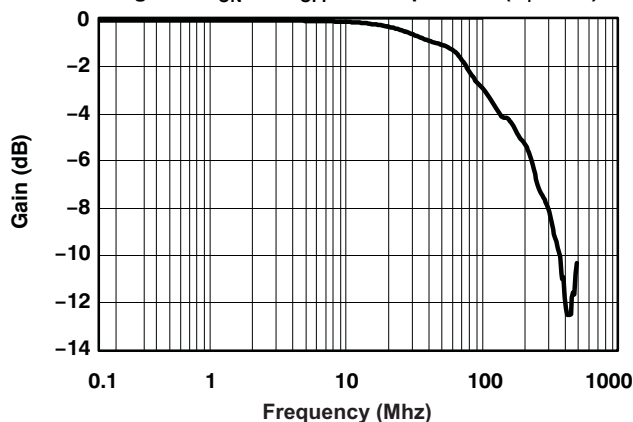


Figure 9. Bandwidth ($V_+ = 5\text{ V}$)

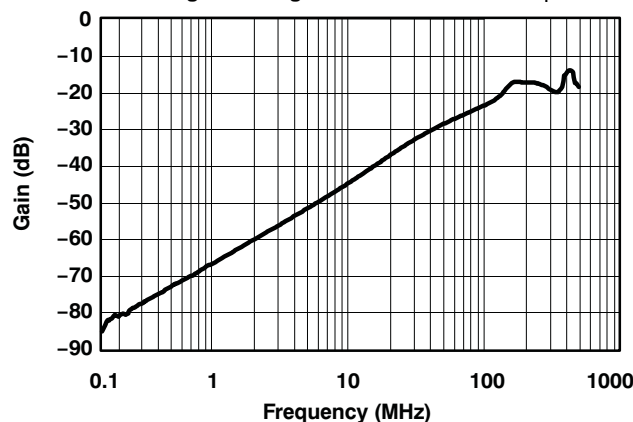


Figure 10. OFF Isolation and Crosstalk ($V_+ = 5\text{ V}$)

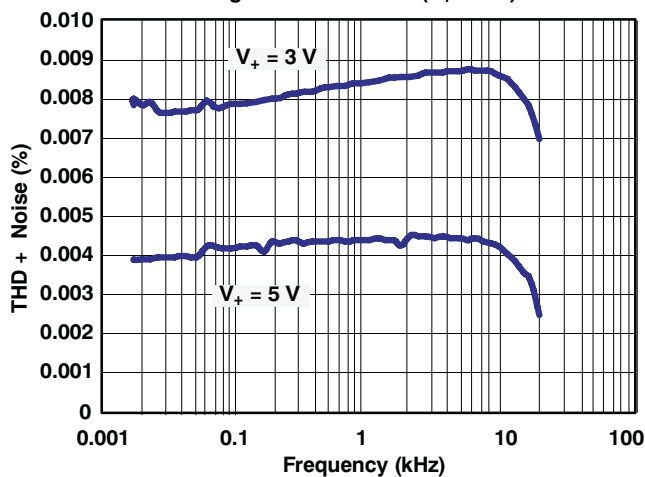


Figure 11. Total Harmonic Distortion (THD) vs Frequency

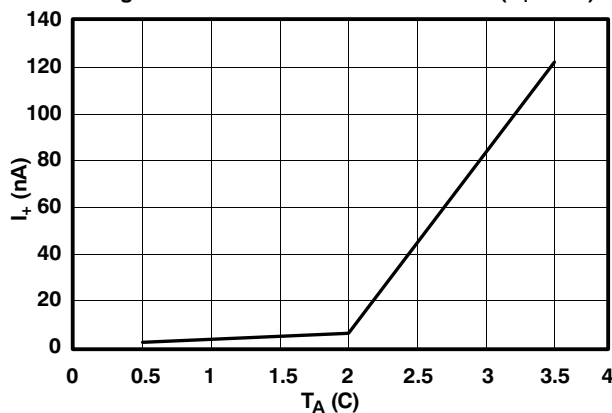


Figure 12. Power Supply Current vs Temperature ($V_+ = 5\text{ V}$)

PIN DESCRIPTION

| PIN NO. | NAME | DESCRIPTION |
|---------|------------------------|--|
| 1 | COM | Common |
| 2 | $\overline{\text{EN}}$ | Enable control input |
| 3 | GND | Digital ground |
| 4 | GND | Digital ground |
| 5 | IN | Digital control to connect the COM to NO or NC |
| 6 | NO | Normally open |
| 7 | NC | Normally closed |
| 8 | V_+ | Power supply |

PARAMETER DESCRIPTION

| SYMBOL | DESCRIPTION |
|--------------------------------|---|
| V_{COM} | Voltage at COM |
| V_{NC} | Voltage at NC |
| V_{NO} | Voltage at NO |
| r_{on} | Resistance between COM and NC or COM and NO ports when the channel is ON |
| r_{peak} | Peak on-state resistance over a specified voltage range |
| Δr_{on} | Difference of r_{on} between channels in a specific device |
| $r_{\text{on(flat)}}$ | Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions |
| $I_{\text{NC(OFF)}}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions |
| $I_{\text{NC(PWROFF)}}$ | Leakage current measured at the NC port during the power-off condition, $V_+ = 0$ |
| $I_{\text{NO(OFF)}}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions |
| $I_{\text{NO(PWROFF)}}$ | Leakage current measured at the NO port during the power-off condition, $V_+ = 0$ |
| $I_{\text{NC(ON)}}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open |
| $I_{\text{NO(ON)}}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open |
| $I_{\text{COM(ON)}}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open |
| $I_{\text{COM(OFF)}}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the OFF state and the output (NC or NO) open |
| $I_{\text{COM(PWROFF)}}$ | Leakage current measured at the COM port during the power-off condition, $V_+ = 0$ |
| V_{IH} | Minimum input voltage for logic high for the control input (IN, $\overline{\text{EN}}$) |
| V_{IL} | Maximum input voltage for logic low for the control input (IN, $\overline{\text{EN}}$) |
| V_{i} | Voltage at the control input (IN, $\overline{\text{EN}}$) |
| $I_{\text{IH}}, I_{\text{IL}}$ | Leakage current measured at the control input (IN, $\overline{\text{EN}}$) |
| t_{ON} | Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON. |
| t_{OFF} | Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF. |
| t_{BBM} | Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state. |
| Q_{C} | Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_{\text{C}} = C_{\text{L}} \times \Delta V_{\text{COM}}$, C_{L} is the load capacitance, and ΔV_{COM} is the change in analog output voltage. |
| $C_{\text{NC(OFF)}}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is OFF |
| $C_{\text{NO(OFF)}}$ | Capacitance at the NO port when the corresponding channel (NO to COM) is OFF |
| $C_{\text{NC(ON)}}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is ON |
| $C_{\text{NO(ON)}}$ | Capacitance at the NO port when the corresponding channel (NO to COM) is ON |

PARAMETER DESCRIPTION (continued)

| SYMBOL | DESCRIPTION |
|----------------|--|
| $C_{COM(ON)}$ | Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON |
| $C_{COM(OFF)}$ | Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is OFF |
| C_i | Capacitance of control input (IN) |
| O_{ISO} | OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. |
| X_{TALK} | Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB. |
| BW | Bandwidth of the switch. This is the frequency where the gain of an ON channel is -3 dB below the DC gain. |
| THD | Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic. |
| I_+ | Static power-supply current with the control (IN, \overline{EN}) pin at V_+ or GND |

PARAMETER MEASUREMENT INFORMATION

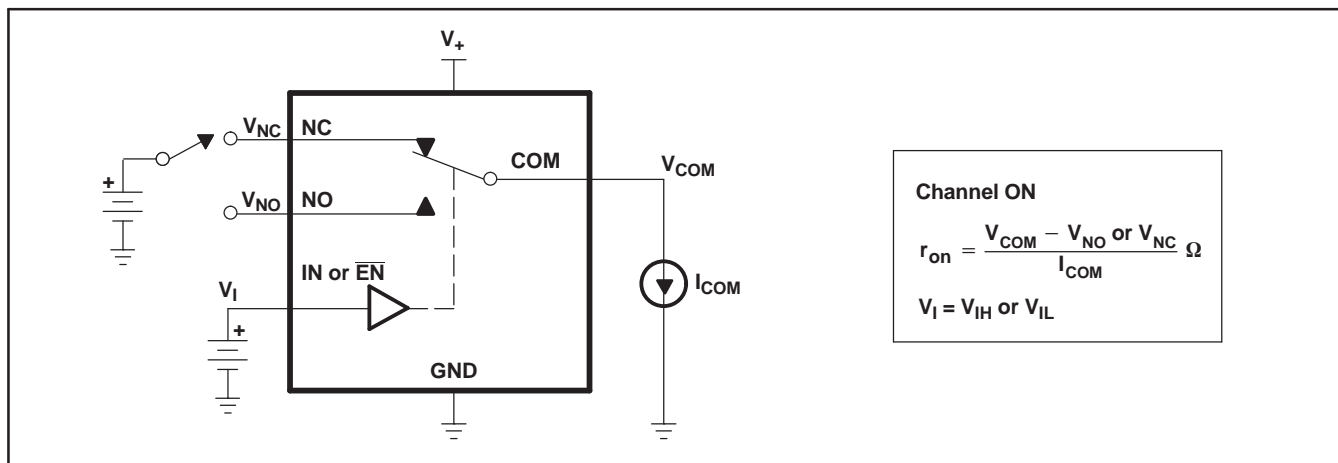


Figure 13. ON-State Resistance (r_{on})

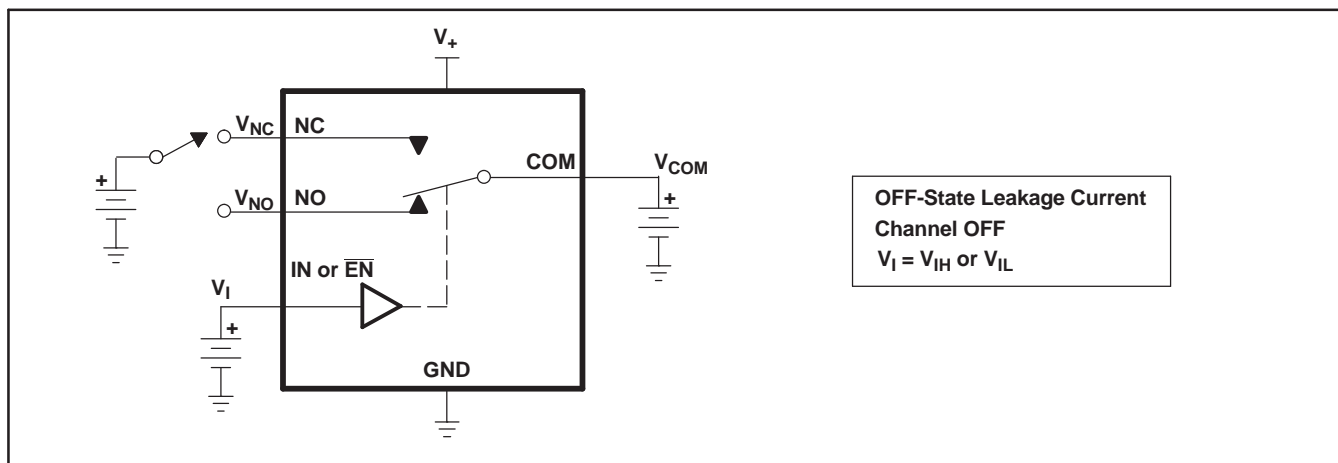


Figure 14. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(PWROFF)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

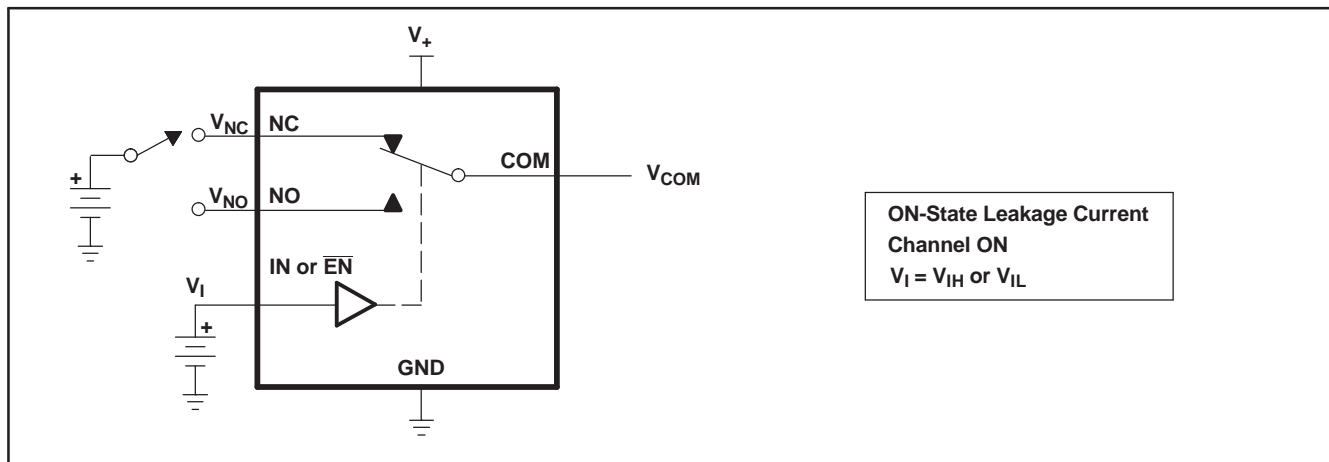


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

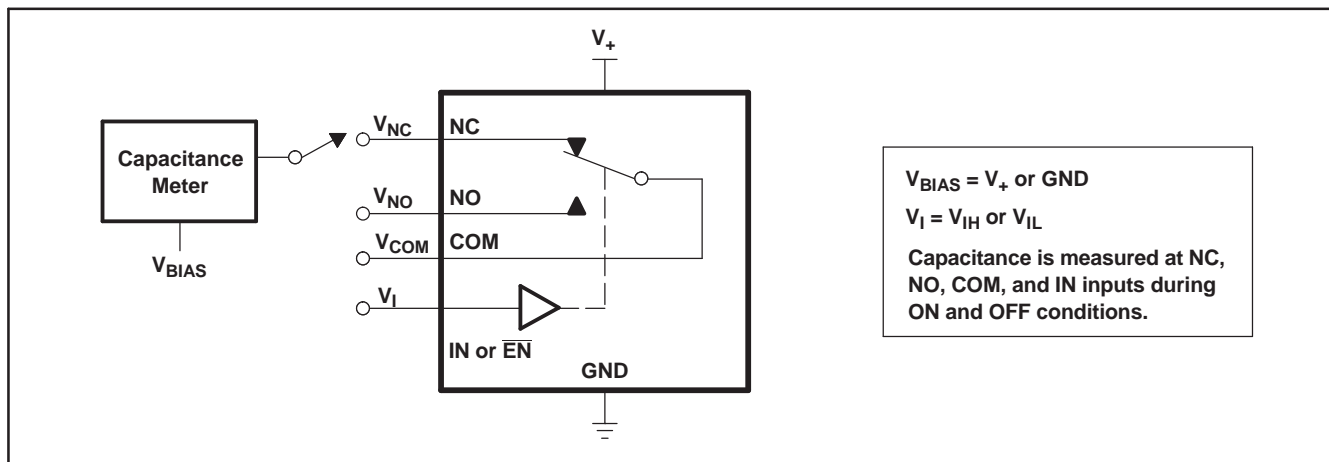
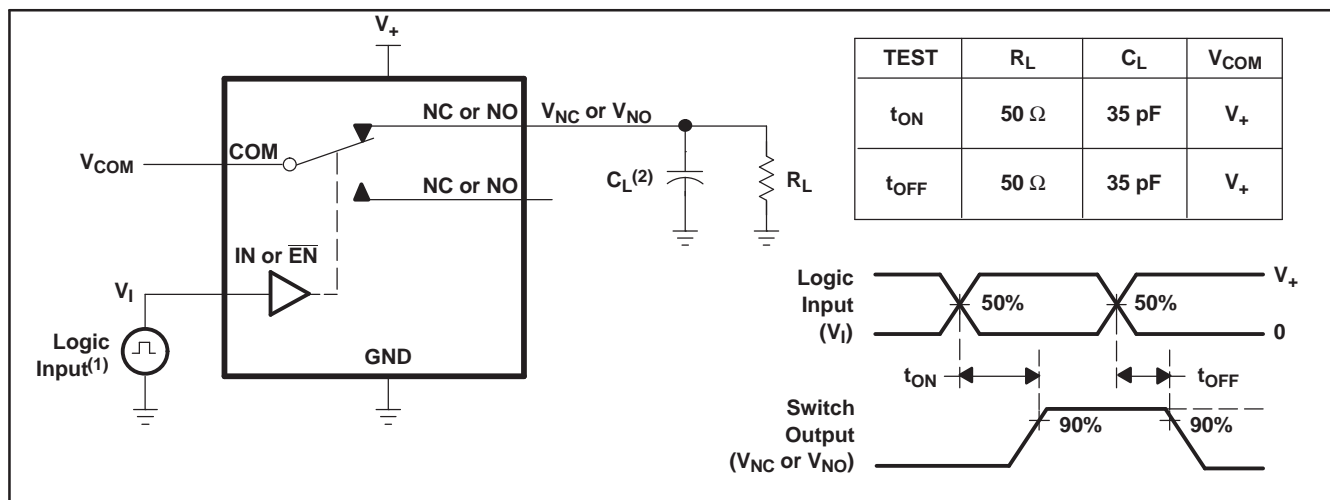


Figure 16. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

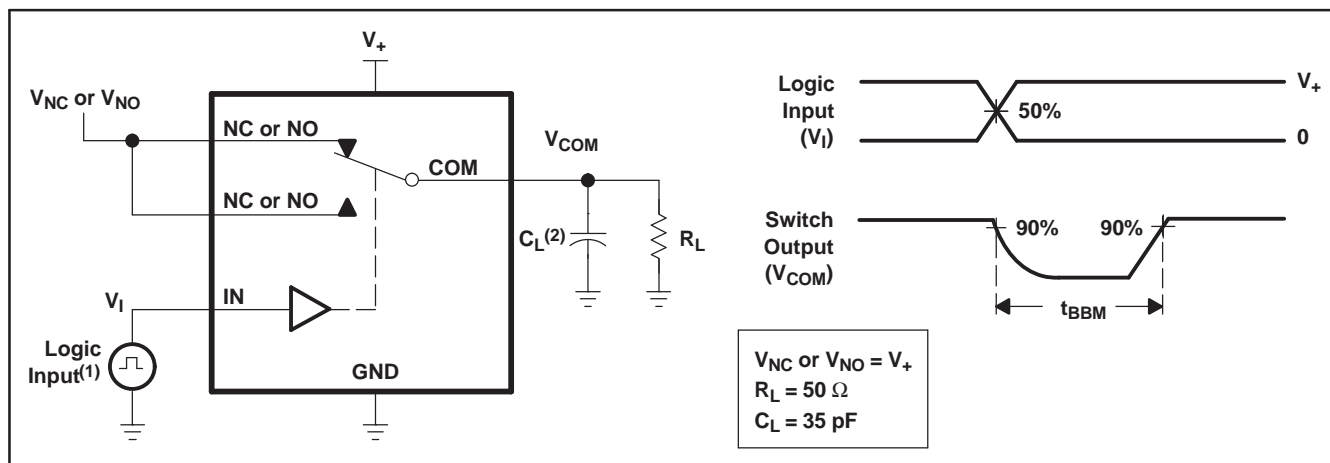
PARAMETER MEASUREMENT INFORMATION (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, tr < 5 ns, tf < 5 ns.

(2) CL includes probe and jig capacitance.

Figure 17. Turn-On (tON) and Turn-Off Time (tOFF)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, tr < 5 ns, tf < 5 ns.

(2) CL includes probe and jig capacitance.

Figure 18. Make-Before-Break Time (tMBB)

PARAMETER MEASUREMENT INFORMATION (continued)

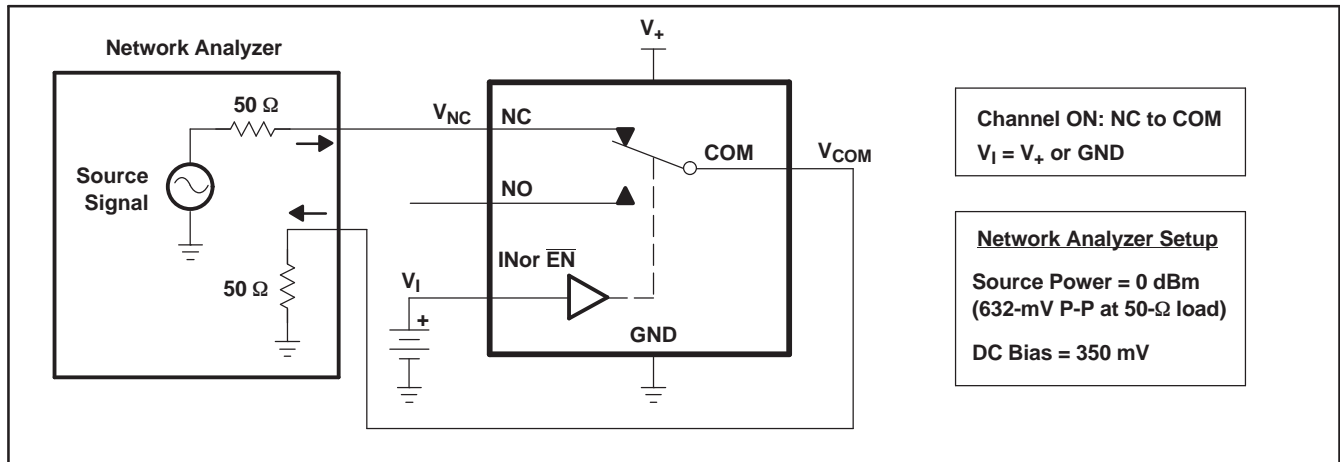


Figure 19. Bandwidth (BW)

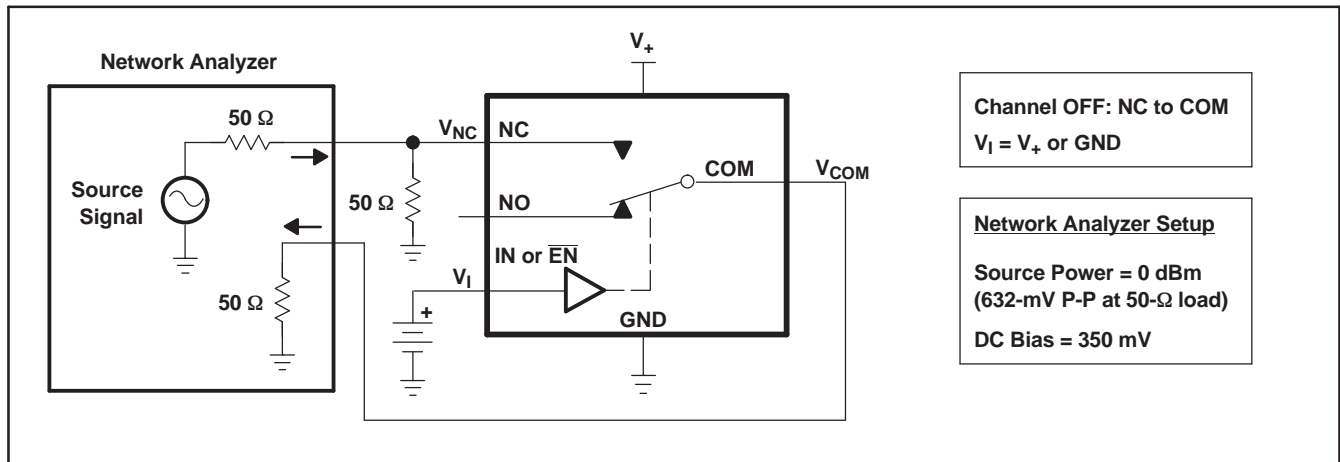


Figure 20. OFF Isolation (O_{ISO})

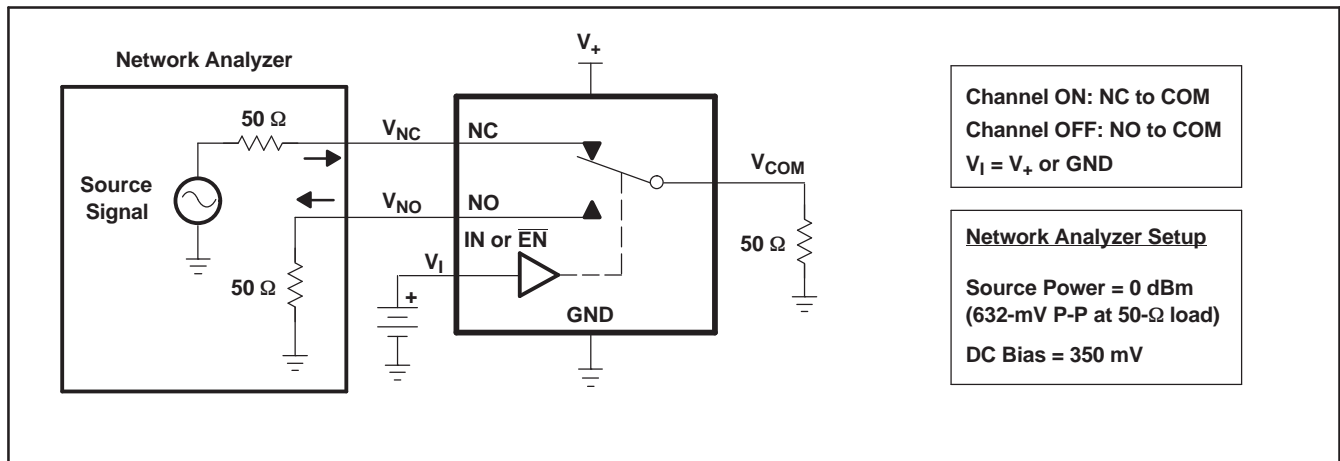
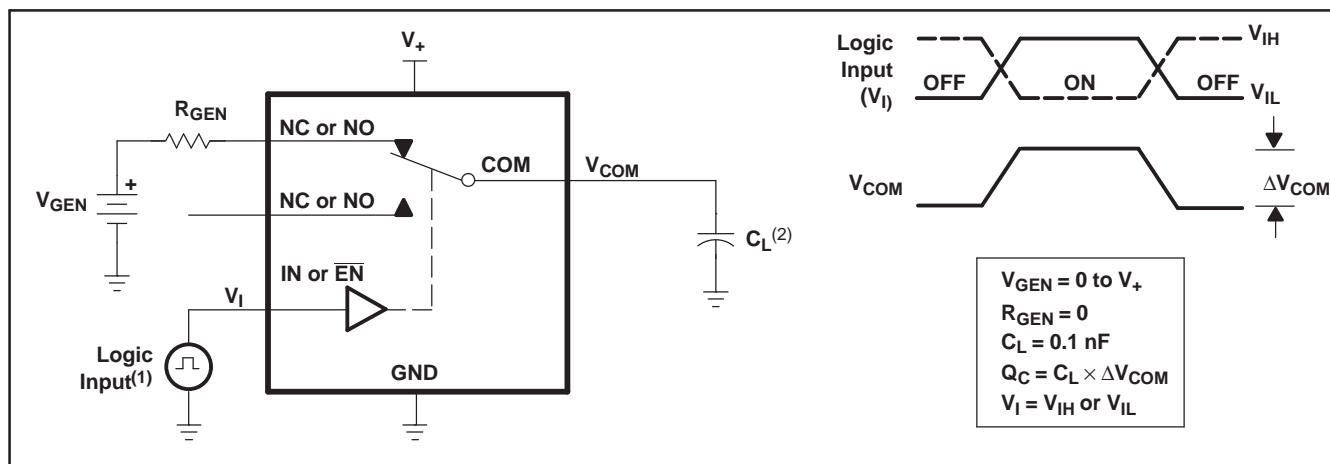


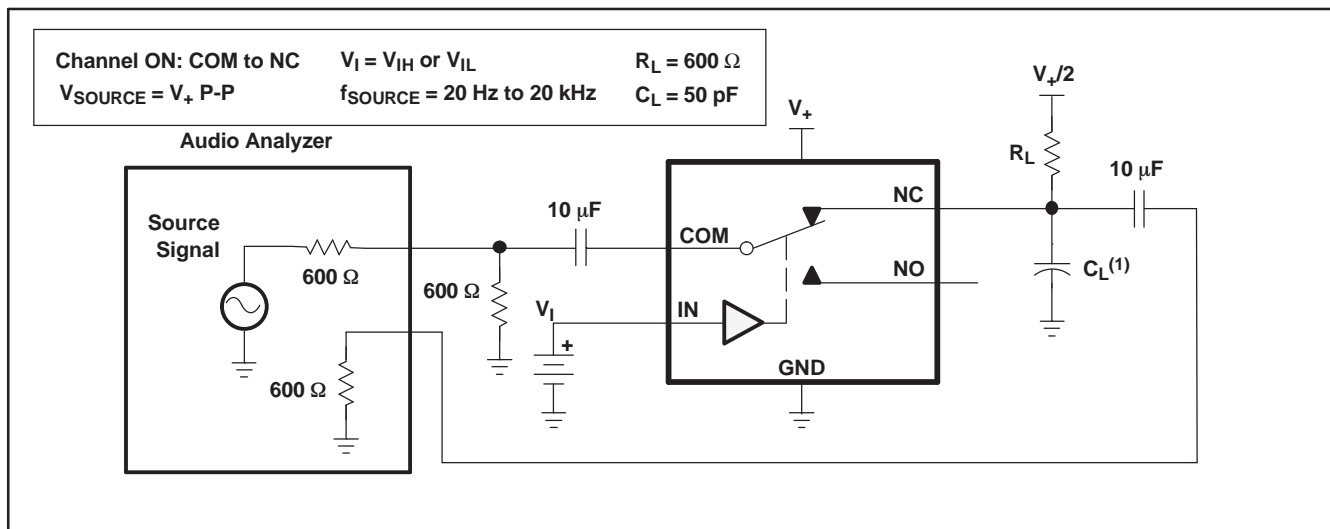
Figure 21. Crosstalk (X_{TALK})

PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
- (2) C_L includes probe and jig capacitance.

Figure 22. Charge Injection (Q_C)



- (1) C_L includes probe and jig capacitance.

Figure 23. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TS5A3153DCUR | ACTIVE | VSSOP | DCU | 8 | 3000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | (JCDQ, JCDR) | Samples |
| TS5A3153YZPR | ACTIVE | DSBGA | YZP | 8 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | J5N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS5A3153DCUR | VSSOP | DCU | 8 | 3000 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| TS5A3153DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| TS5A3153YZPR | DSBGA | YZP | 8 | 3000 | 178.0 | 9.2 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

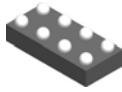
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS5A3153DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| TS5A3153DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| TS5A3153YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 35.0 |

YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4225266/A 09/2014

NOTES:

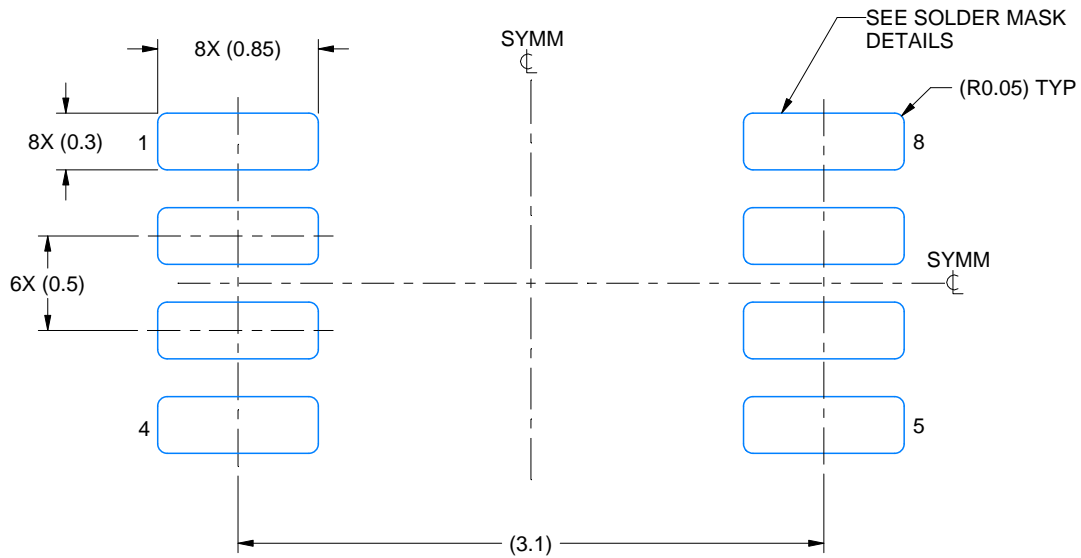
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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