TS5A2053
SINGLE-CHANNEL 10-Ω SPDT ANALOG SWITCH WITH ENABLE

SCDS183A – JANUARY 2005 – REVISED APRIL 2006

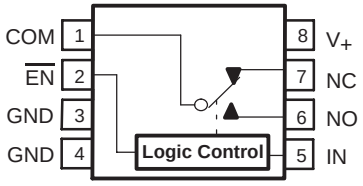
Description

The TS5A2053 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V_+ can be transmitted in either direction.

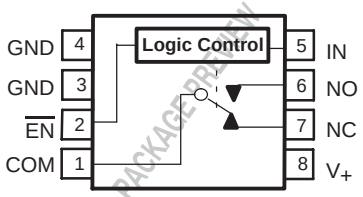
Applications

- **Cell Phones**
- **Portable Audio Video Equipment**
- **Battery-Powered Equipment**
- **Low-Voltage Data-Acquisition Systems**
- **Test Equipment**
- **Communication Circuits**

SSOP OR VSSOP PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



FUNCTION TABLE

$\overline{EN}$	IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

Features

- **Low ON-State Resistance (10 Ω)**
- **Control Inputs Are 5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

Summary of Characteristics

V_+ = 5 V and T_A = 25 °C

Configuration	Single Pole Double Throw (SPDT)
Number of channels	1
ON-state resistance (r_{on})	7.5 Ω
ON-state resistance match (Δr_{on})	0.8 Ω
ON-state resistance flatness ($r_{on(flat)}$)	1.7 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	6.8 ns/4.1 ns
Charge injection (Q_C)	3 pC
Bandwidth (BW)	330 MHz
OFF isolation (O_{ISO})	−64 dB at 10 MHz
Crosstalk (X_{TALK})	−68 dB at 10 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{COM(OFF)}$)	±10 nA
Power-supply current (I_+)	0.1 µA
Package options	8-pin DSBGA, SSOP, or VSSOP

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
−40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	TS5A2053YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		TS5A2053YZPR	
	SSOP – DCT	Tape and reel	TS5A2053DCTR	JAF_ _ _
	VSSOP – DCU	Tape and reel	TS5A2053DCUR	JAF_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

Absolute Minimum and Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		−0.5	6.5	V
V_{NO} V_{NC} V_{COM}	Analog voltage range(3)(4)(5)		−0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NO}, V_{NC}, V_{COM} > V_+	−50	50	mA
I_{NO} I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	−50	50	mA
V_I	Digital input voltage range(3)(4)		−0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	−50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		−100		mA
θ_{JA}	Package thermal impedance(6)	DCT package		220	°C/W
		DCU package		227	
		YEP/YZP package		102	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −32 mA,	Switch ON, See Figure 13	25°C	4.5 V		7.5	13.8	Ω
				Full				16	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 3.15 V, I_{COM} = −32 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.8		Ω
				Full				4.5	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −32 mA,	Switch ON, See Figure 13	25°C	4.5 V		1.7		Ω
				Full				4.5	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 1 V, V_{COM} = 4.5 V, or V_{NO} or V_{NC} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	–100	5	100	nA
				Full		–200		200	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} or V_{NC} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} or V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	–100	−1	100	nA
				Full		–200		200	
NO, NC ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–100	5.5	100	nA
				Full		–200		200	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} or V_{NC} = Open, or V_{COM} = 4.5 V, V_{NO} or V_{NC} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–100	−1	100	nA
				Full		–200		200	
Digital Control Inputs (IN, $\overline{EN}$)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	−0.1	0.05	0.1	µA
				Full		−1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 5-V Supply(1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	3.8	5.3	6.8	ns
				Full	4.5 V to 5.5 V	3		7.1	
Turn-off time	t_{OFF}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	0.8	1.9	4.1	ns
				Full	4.5 V to 5.5 V	0.4		4.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 21	25°C	5 V		3		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	V_{NO} or V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		9.5		pF
NO, NC ON capacitance	$C_{NO(ON)}$, $C_{NC(ON)}$	V_{NO} or V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		18		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		18		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	5 V		330		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	5 V		−64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	5 V		−68		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	5 V		0.01		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.1	1	µA
				Full				5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −24 mA,	Switch ON, See Figure 13	25°C	3 V		13.2		Ω
				Full				20	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.1 V, I_{COM} = −24 mA,	Switch ON, See Figure 13	25°C	3 V		1		Ω
				Full				5.5	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −24 mA,	Switch ON, See Figure 13	25°C	3 V		5.3		Ω
				Full				11	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 1 V, V_{COM} = 3 V, or V_{NO} or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–100	4	100	nA
				Full		–200		200	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} or V_{NC} = 3 V, or V_{COM} = 3 V, V_{NO} or V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–100	−1	100	nA
				Full		–200		200	
NO, NC ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 1 V, V_{COM} = Open, or V_{NO} or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–100	4.5	100	nA
				Full		–200		200	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} or V_{NC} = Open, or V_{COM} = 3 V, V_{NO} or V_{NC} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–100	−1	100	nA
				Full		–200		200	
Digital Control Inputs (IN, $\overline{EN}$)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	−0.1	0.05	0.1	µA
				Full		−1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3.3-V Supply(1) (continued)

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	5	6.4	7.9	ns
				Full	3 V to 3.6 V	4.5		8.2	
Turn-off time	t_{OFF}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1.1	2.4	4.7	ns
				Full	3 V to 3.6 V	0.3		5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 21	25°C	3.3 V		1		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$	V_{NO} or V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		9.5		pF
NO, NC ON capacitance	$C_{NO(ON)}$	V_{NO} or V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		18.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		18.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	3.3 V		320		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		−64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25 °C	3.3 V		−68		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	3.3 V		0.035		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.1	1	µA
				Full				5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −8 mA,	Switch ON, See Figure 13	25°C	2.3 V		20		Ω
				Full				40	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.6 V, I_{COM} = −8 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.1		Ω
				Full				6	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −8 mA,	Switch ON, See Figure 13	25°C	2.3 V		15		Ω
				Full				20	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.5 V, V_{COM} = 2.2 V, or V_{NO} or V_{NC} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	–100	3.5	100	nA
				Full		–200		200	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0.5 V, V_{NO} or V_{NC} = 2.2 V, or V_{COM} = 2.2 V, V_{NO} or V_{NC} = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	–100	−2	100	nA
				Full		–200		200	
NO, NC ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.5 V, V_{COM} = Open, or V_{NO} or V_{NC} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–100	4	100	nA
				Full		–200		200	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.5 V, V_{NO} or V_{NC} = Open, or V_{COM} = 2.2 V, V_{NO} or V_{NC} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–100	−2	100	nA
				Full		–200		200	
Digital Control Inputs (IN, $\overline{EN}$)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	−0.1	0.05	0.1	µA
				Full		−1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply(1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	5.9	7.1	9.3	ns
				Full	2.3 V to 2.7 V	5.1		10	
Turn-off time	t_{OFF}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	2.1	3.2	5.1	ns
				Full	2.3 V to 2.7 V	1.2		5.2	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0	C_L = 0.1 nF, See Figure 21	25°C	2.5 V		0.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$ $C_{NC(OFF)}$	V_{NO} or V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		6.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		10		pF
NO, NC ON capacitance	$C_{NO(ON)}$ $C_{NC(ON)}$	V_{NO} or V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		18.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		18.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.5 V		320		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		−64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25 °C	2.5 V		−68		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	2.5 V		0.26		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.1	1	μA
				Full				5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = −4 mA,	Switch ON, See Figure 13	25°C	1.65 V		85		Ω
				Full				120	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.15 V, I_{COM} = −4 mA,	Switch ON, See Figure 13	25°C	1.65 V		2		Ω
				Full				7.5	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = −4 mA,	Switch ON, See Figure 13	25°C	1.65 V		76		Ω
				Full				100	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 14	25°C	1.95 V	–100	3.5	100	nA
				Full		–200		200	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0.3 V, V_{NO} = 1.65 V, or V_{COM} = 1.65 V, V_{NO} = 0.3 V,	Switch OFF, See Figure 14	25°C	1.95 V	–100	1	100	nA
				Full		–200		200	
NO, NC ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–100	4	100	nA
				Full		–200		200	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.3 V, V_{NO} or V_{NC} = Open, or V_{COM} = 1.65 V, V_{NO} or V_{NC} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–100	1	100	nA
				Full		–200		200	
Digital Control Inputs (IN, $\overline{EN}$)									
Input logic high	V_{IH}			Full		$V_+ \times 0.65$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.35$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	−0.1	0.05	0.1	µA
				Full		−1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply(1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	10.2	11.8	14.5	ns
				Full	1.65 V to 1.95 V	8.4		15.5	
Turn-off time	t_{OFF}	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	2.9	4.3	6.5	ns
				Full	1.65 V to 1.95 V	2.2		7	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0	C_L = 0.1 nF, See Figure 21	25°C	1.8 V		0.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	V_{NO} or V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		6.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		10		pF
NO, NC ON capacitance	$C_{NO(ON)}$, $C_{NC(ON)}$	V_{NO} or V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		19		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		14		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	1.8 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	1.8 V		320		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	1.8 V		−64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25 °C	1.8 V		−68		dB
Total harmonic distortion	THD	R_L = 10 kΩ, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	1.8 V		2.6		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.1	1	µA
				Full				5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

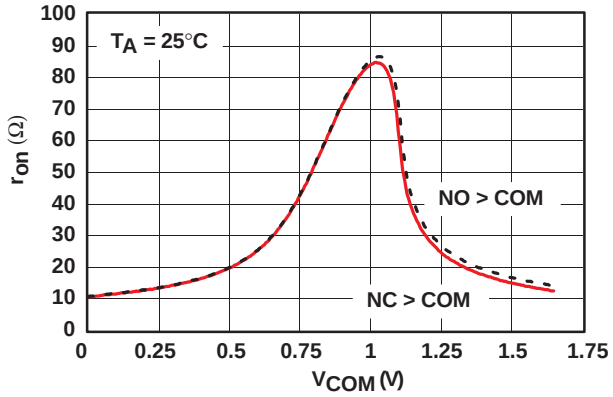


Figure 1A. r_{on} vs V_{COM} (V_+ = 1.65 V)

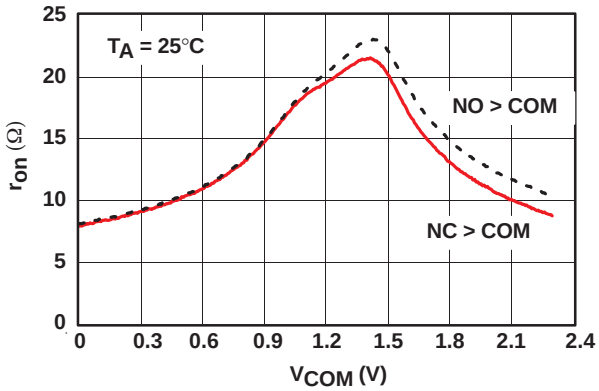


Figure 1B. r_{on} vs V_{COM} (V_+ = 2.3 V)

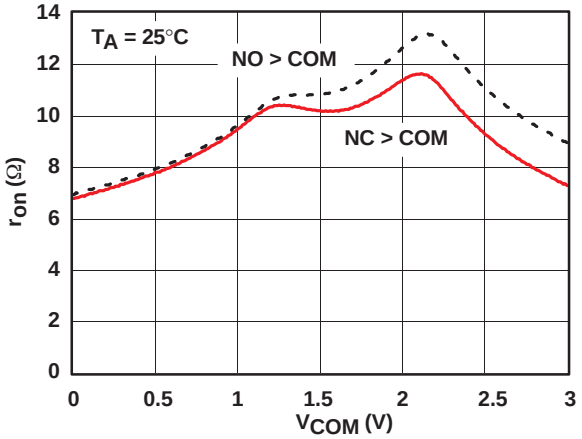


Figure 1C. r_{on} vs V_{COM} (V_+ = 3 V)

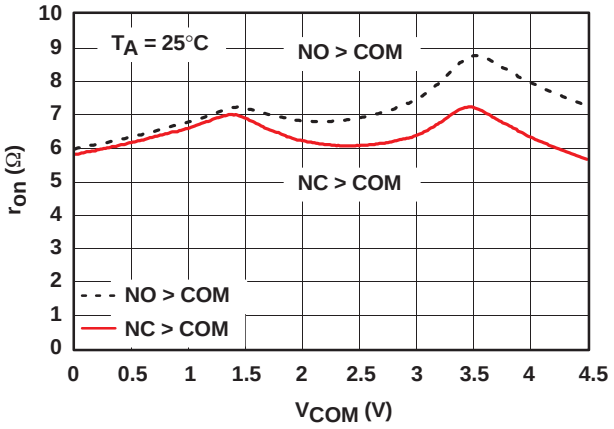


Figure 1D. r_{on} vs V_{COM} (V_+ = 4.5 V)

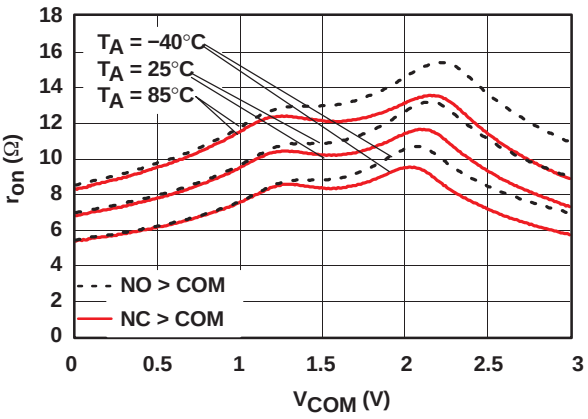


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

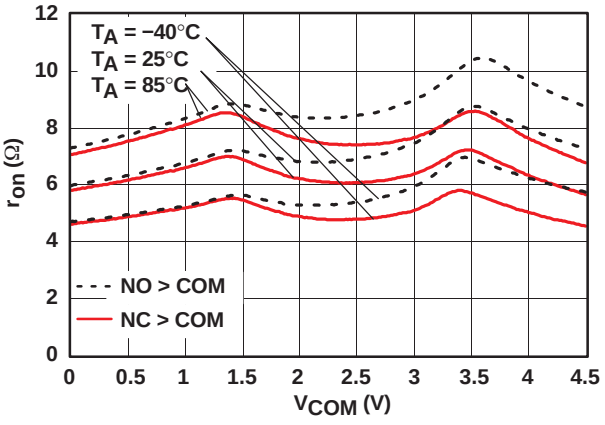


Figure 3. r_{on} vs V_{COM} (V_+ = 4.5 V)

TYPICAL PERFORMANCE (continued)

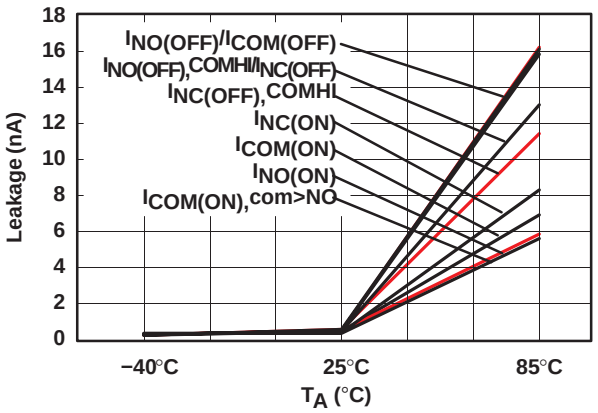


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

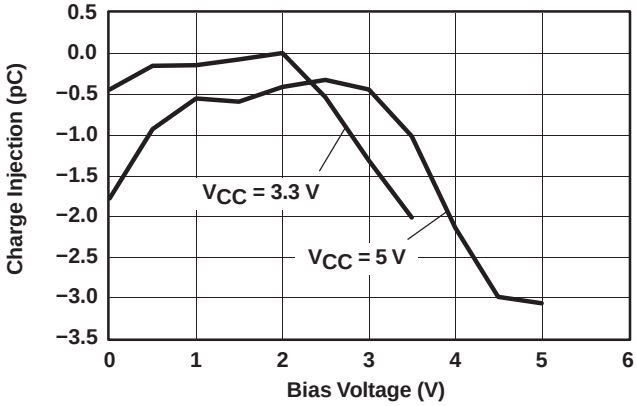


Figure 5. Charge Injection (Q_C) vs V_{COM}

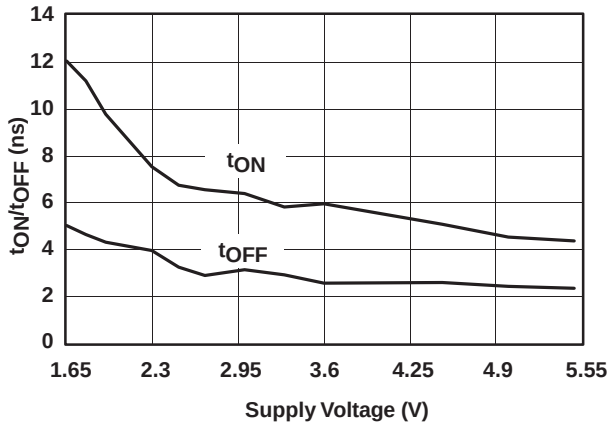


Figure 6. t_{ON} and t_{OFF} vs V_+

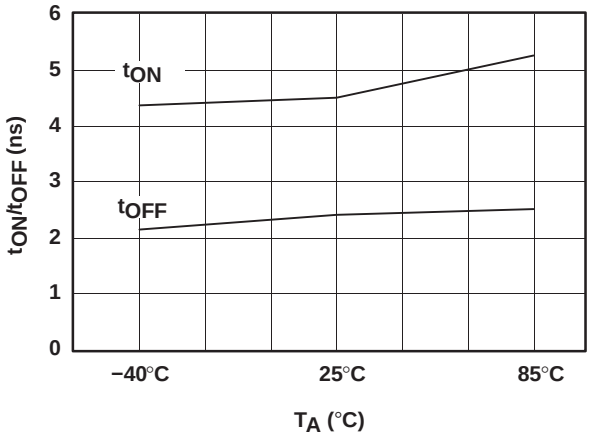


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

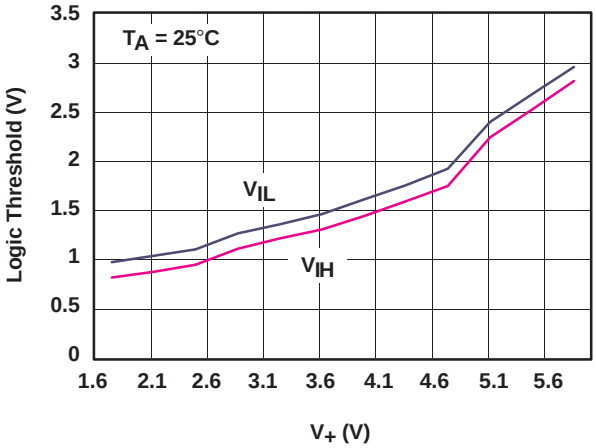


Figure 8. Logic Threshold vs V_+

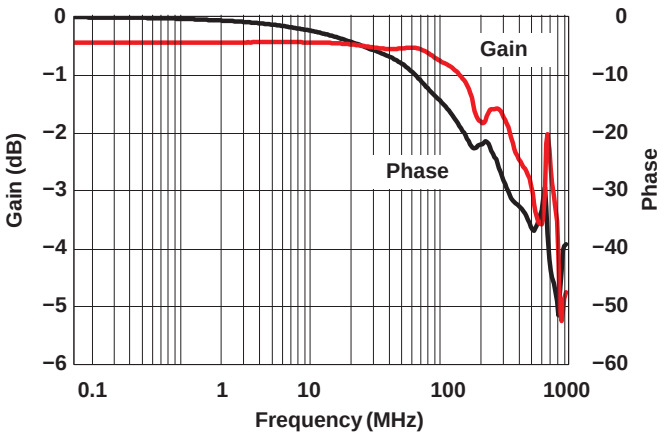


Figure 9. Bandwidth (V_+ = 5 V)

TYPICAL PERFORMANCE (continued)

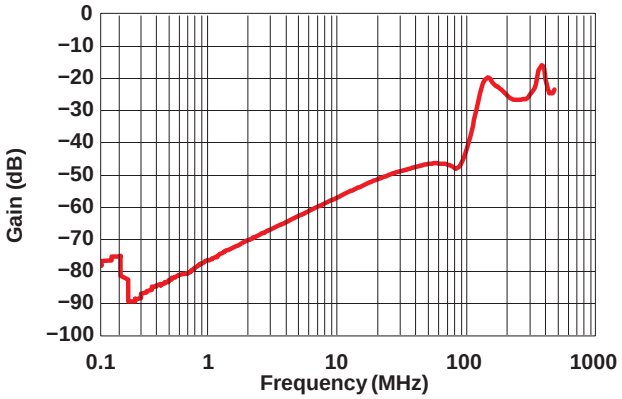


Figure 10. OFF Isolation (V_+ = 5 V)

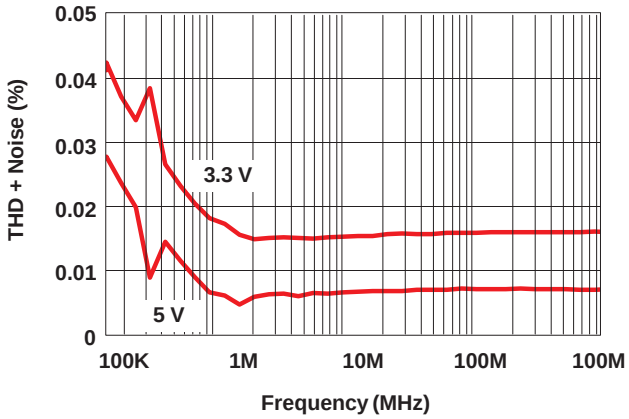


Figure 11. Total Harmonic Distortion vs Frequency

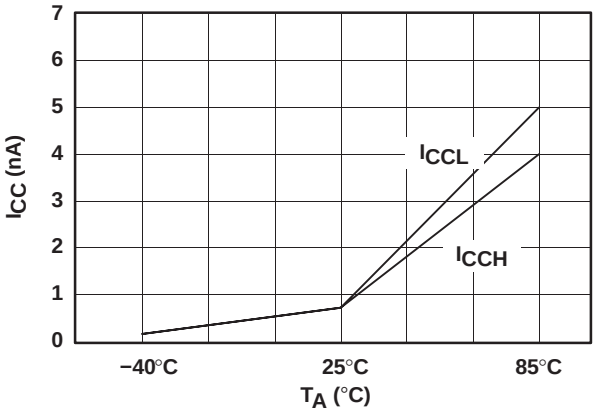


Figure 12. Power-Supply Current vs Temperature (V_+ = 5 V)

PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	COM	Common
2	$\overline{EN}$	Chip enable (active low)
3	GND	Digital ground
4	GND	Digital ground
5	IN	Digital control to connect COM to NC or NO
6	NO	Normally open
7	NC	Normally closed
8	V_+	Power supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the OFF state and the output (NC or NO) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$)
V_{IL}	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$)
V_I	Voltage at the control input (IN, $\overline{EN}$)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, $\overline{EN}$)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_I	Capacitance of control input (IN, $\overline{EN}$)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is −3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic.
I_+	Static power-supply current with the control (IN, $\overline{EN}$) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

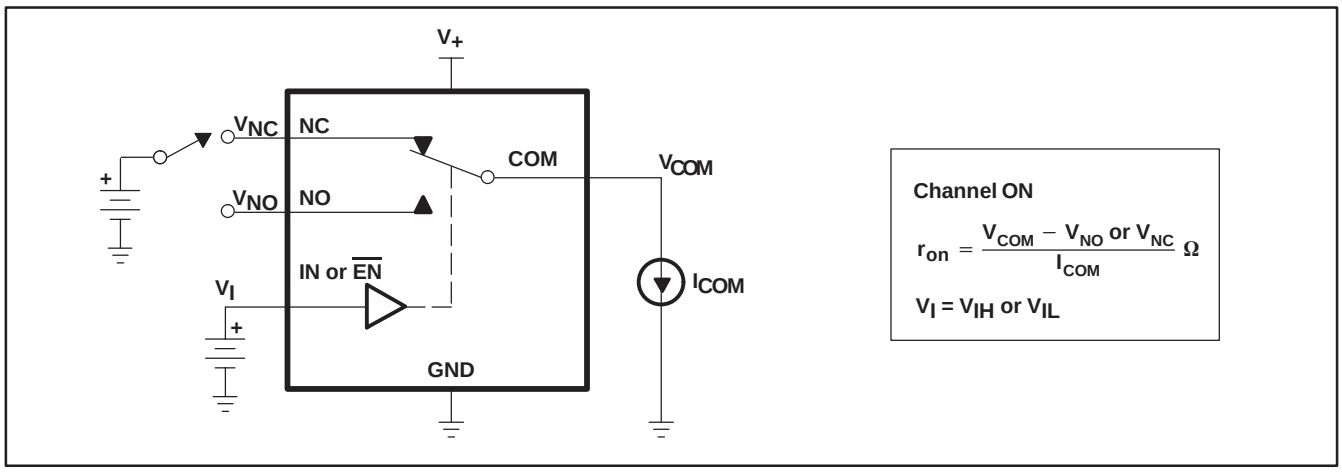


Figure 13. ON-State Resistance (r_{on})

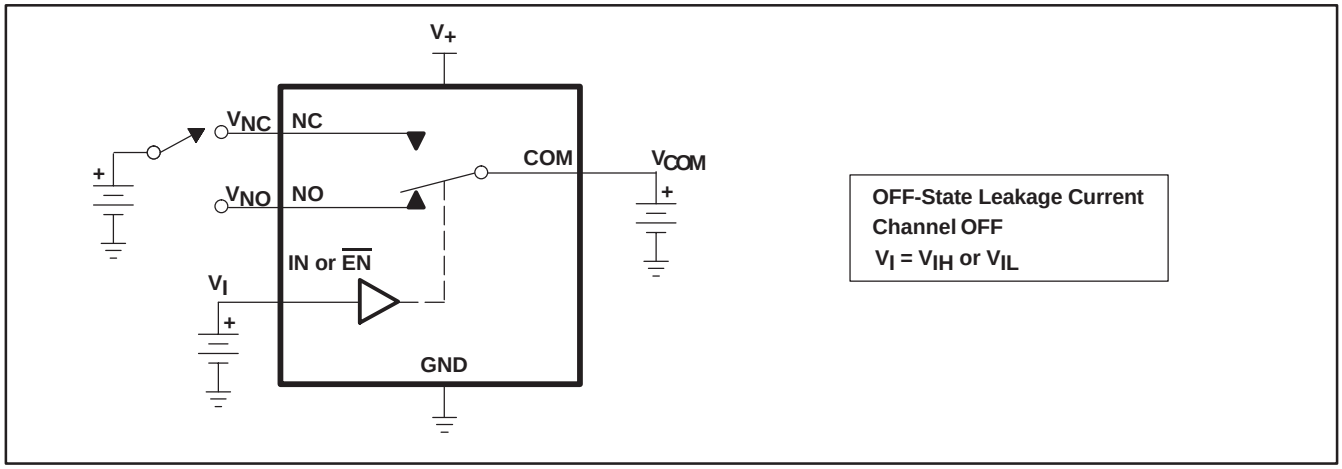


Figure 14. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{COM(OFF)}$)

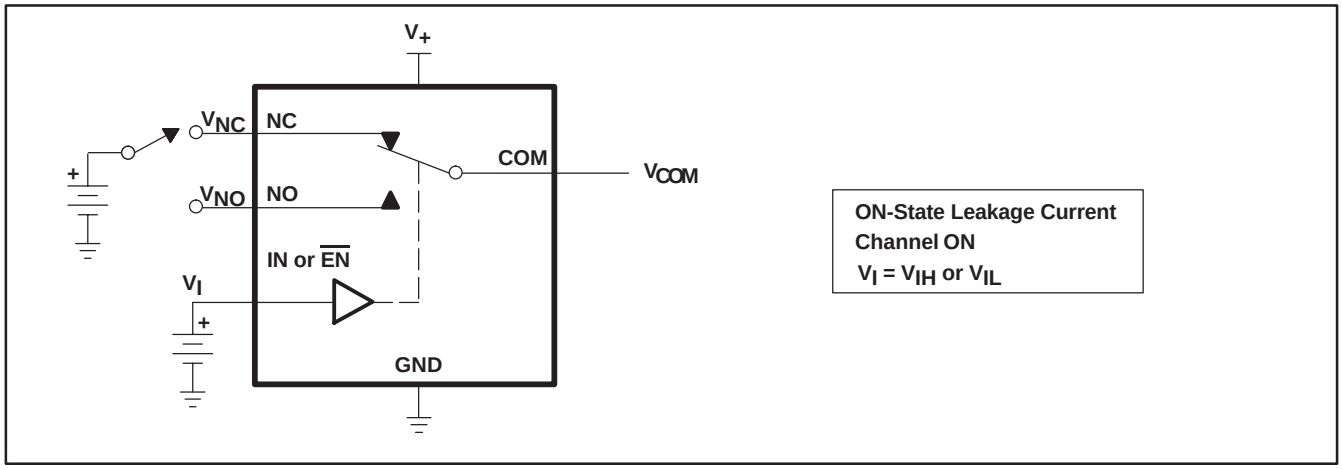


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

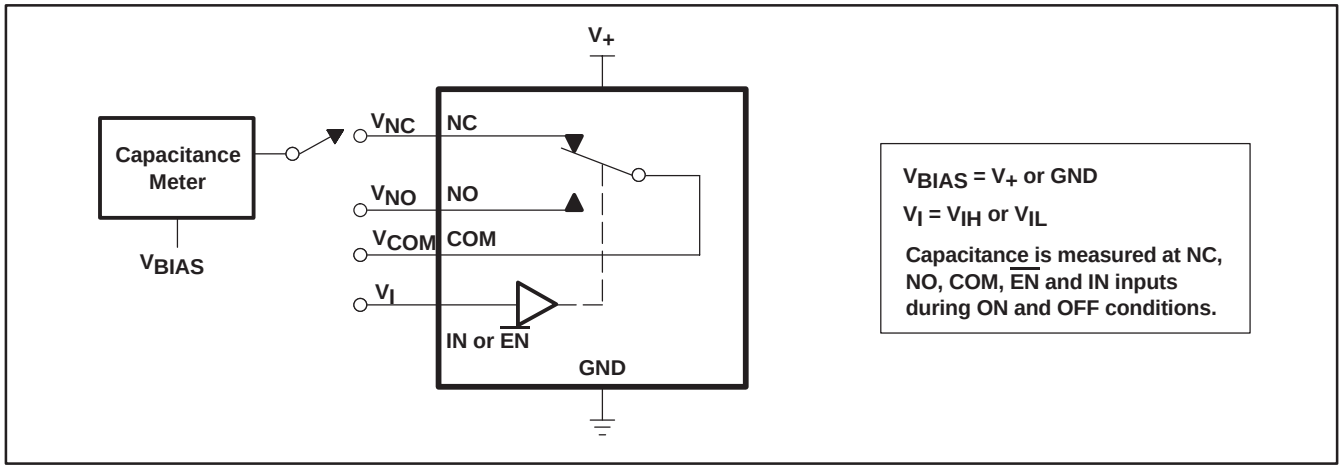
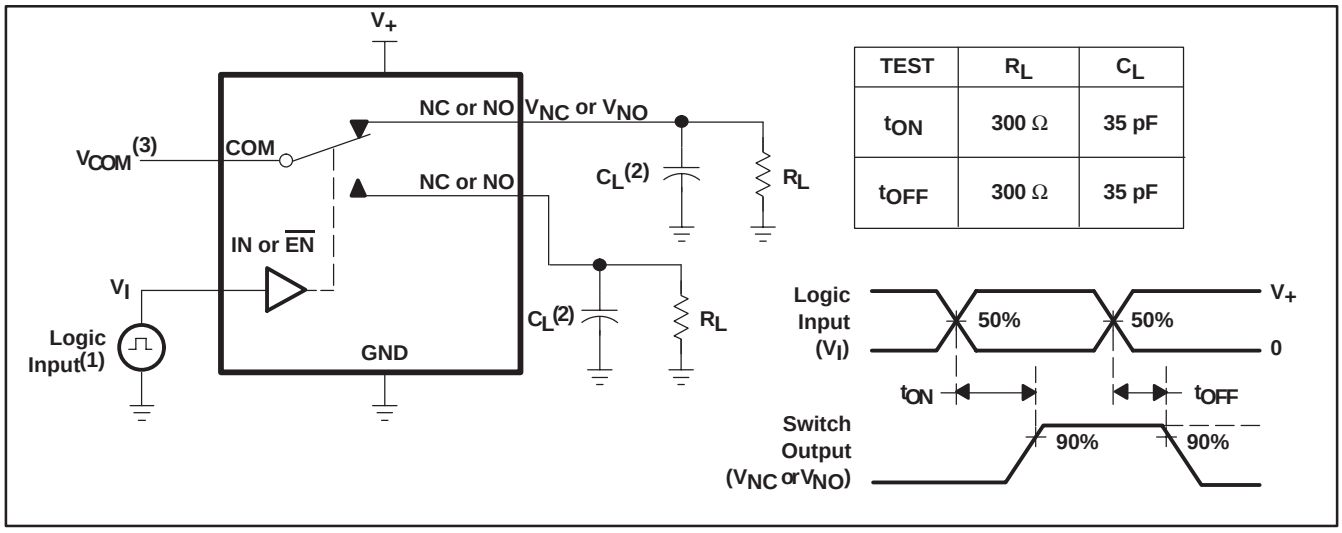


Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.
(3) See Electrical Characteristics for V_{COM}.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

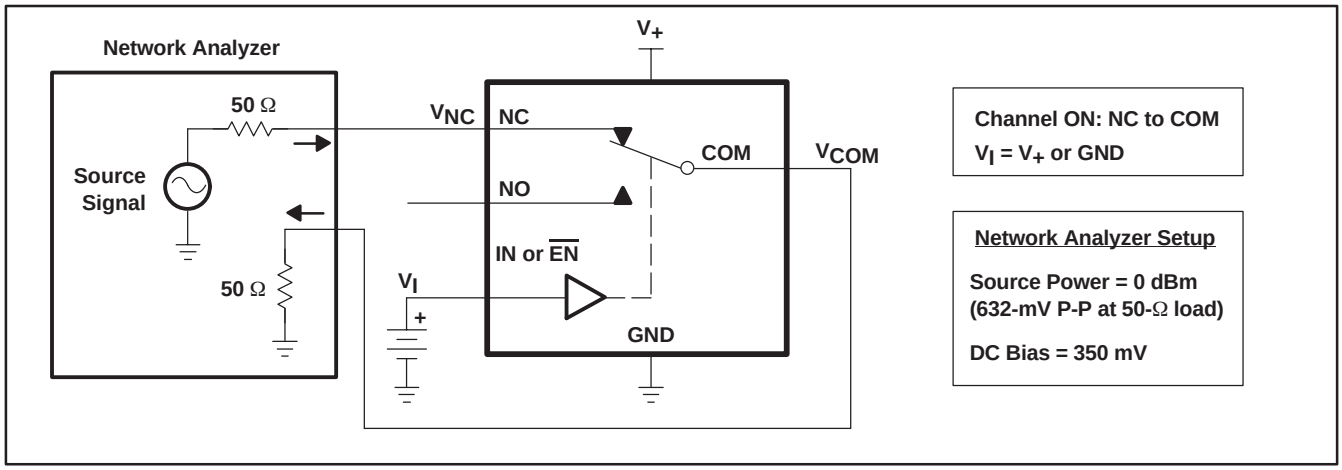


Figure 18. Bandwidth (BW)

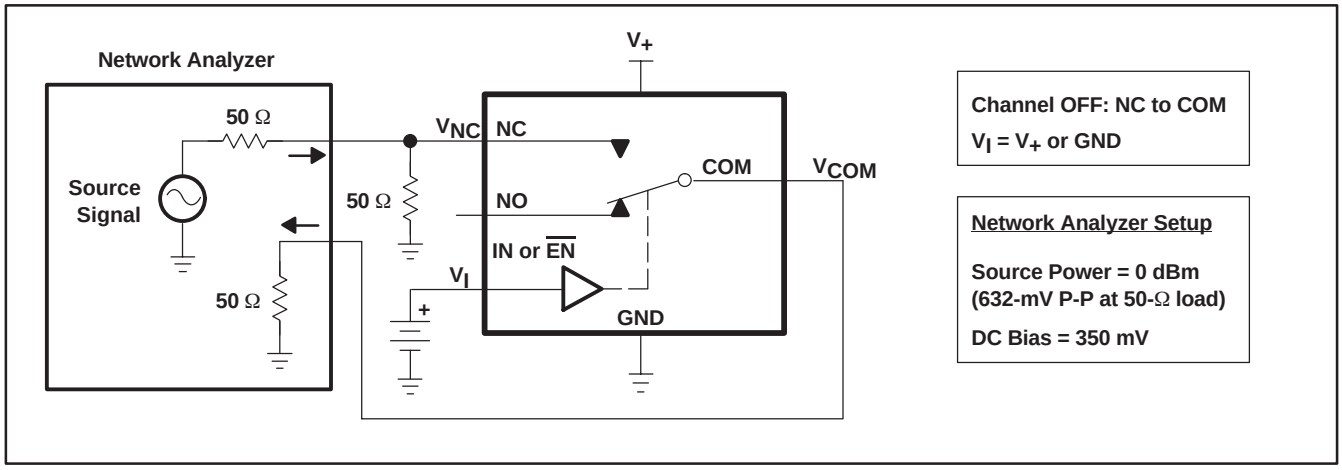


Figure 19. OFF Isolation (O_{ISO})

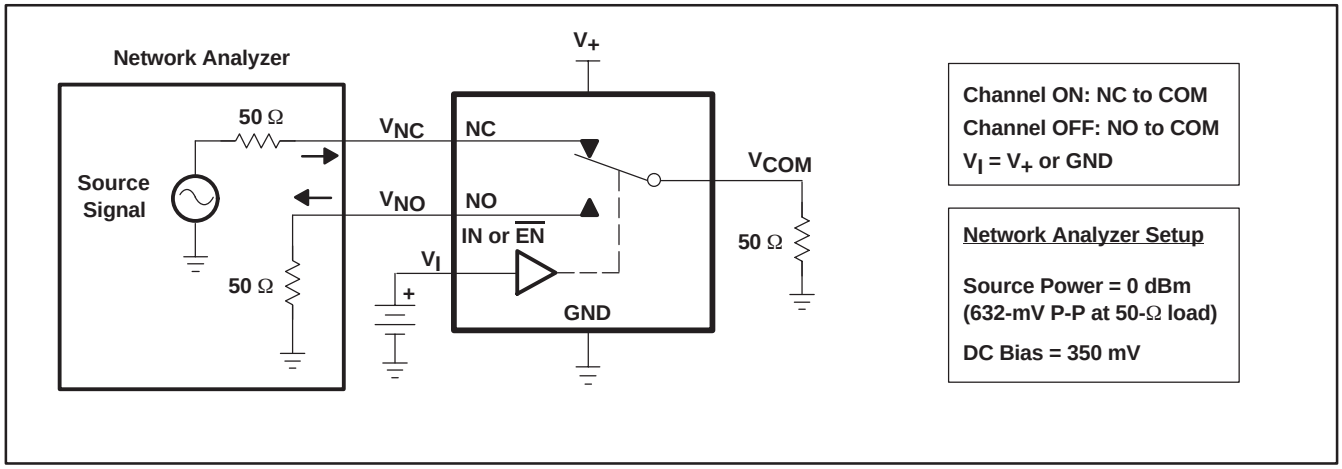
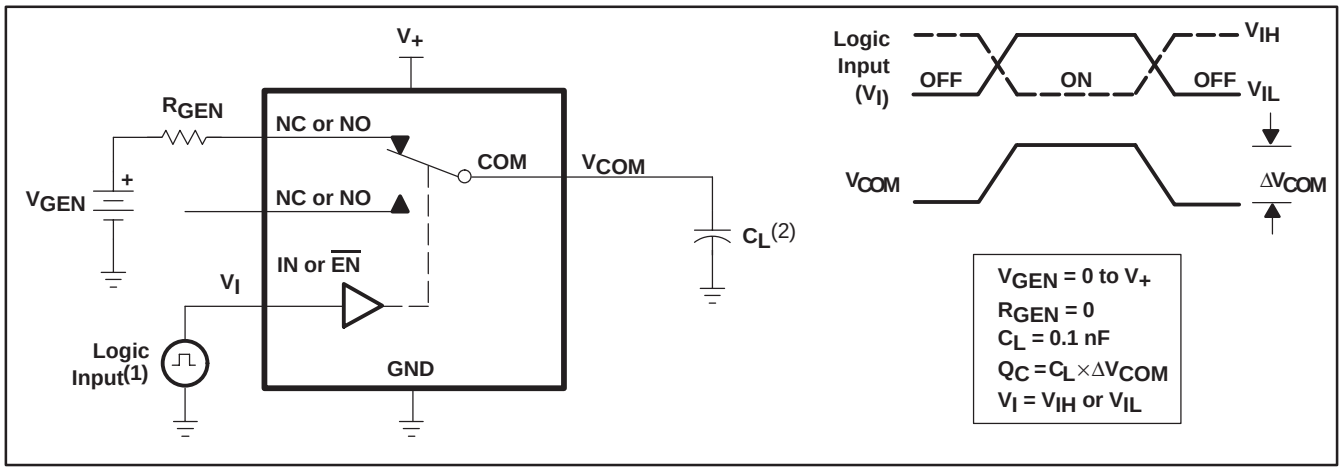
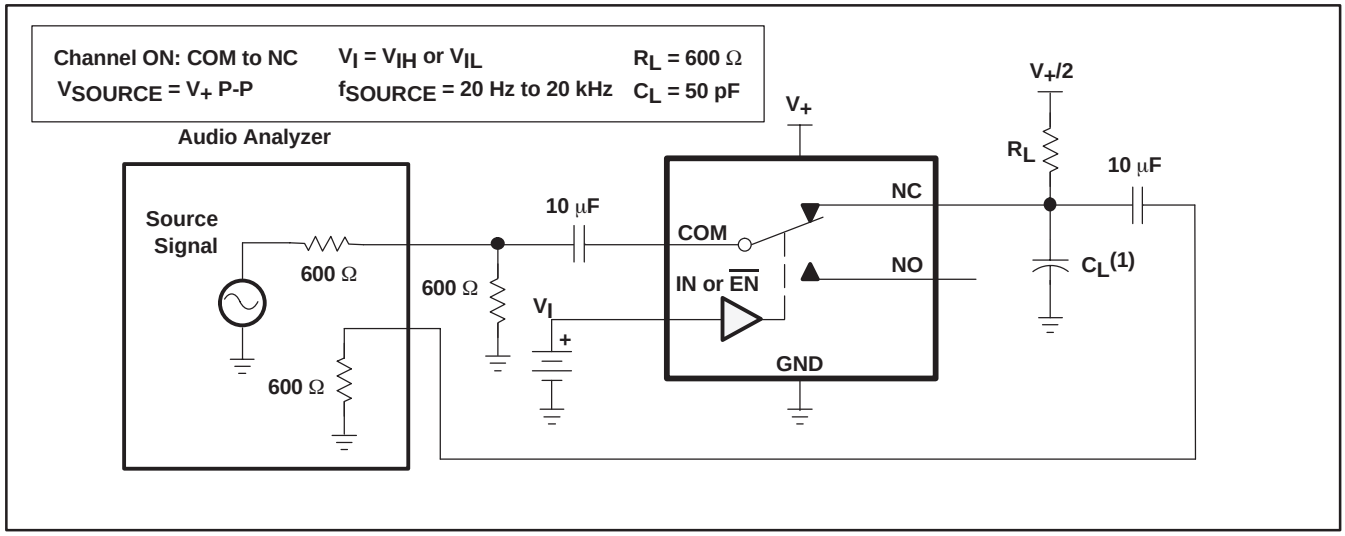


Figure 20. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 21. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 22. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A2053DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAF (R, Z)	Samples
TS5A2053DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(AF, JAFQ, JAFR) JZ	Samples
TS5A2053DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAFR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

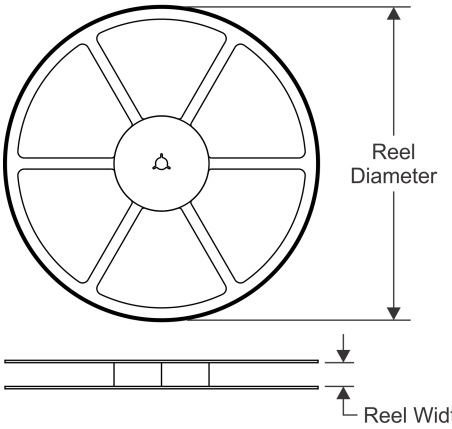
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

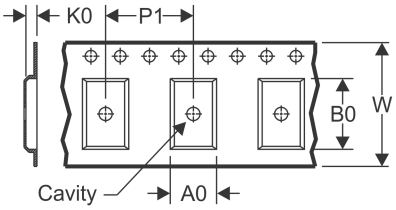
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

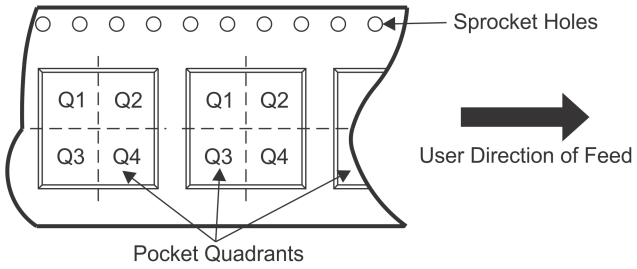


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

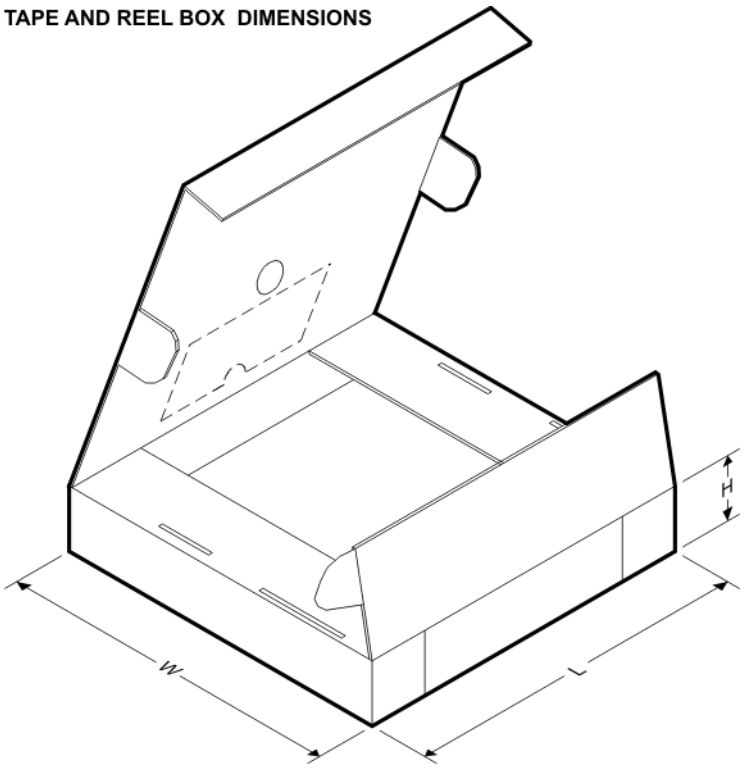
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A2053DCTR	SM8	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TS5A2053DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
TS5A2053DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
TS5A2053DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A2053DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

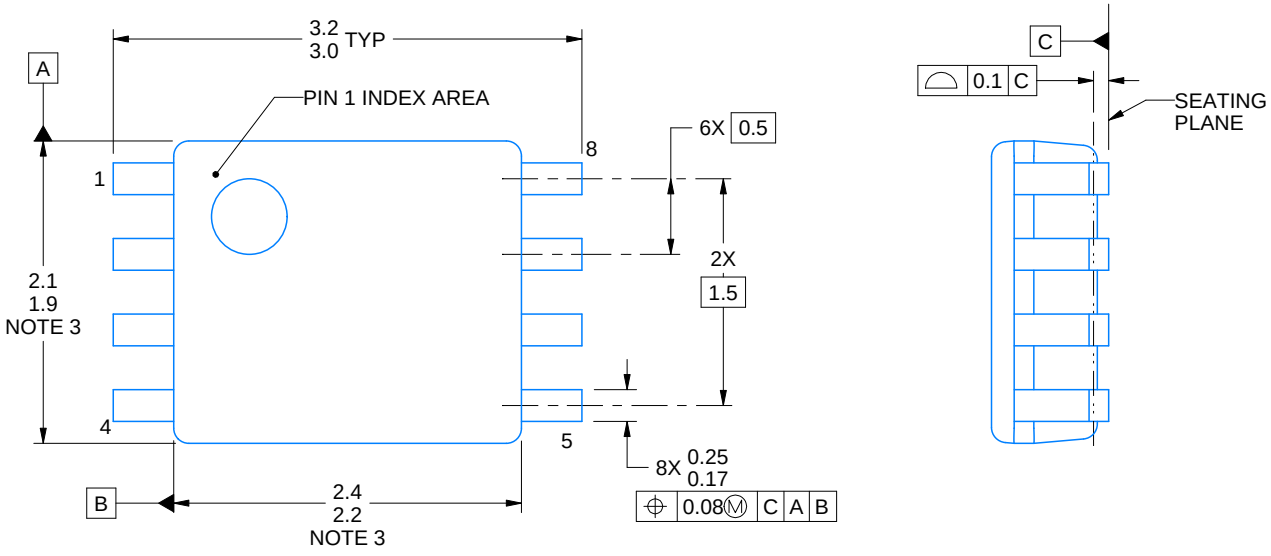
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A2053DCTR	SM8	DCT	8	3000	183.0	183.0	20.0
TS5A2053DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
TS5A2053DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
TS5A2053DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A2053DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0

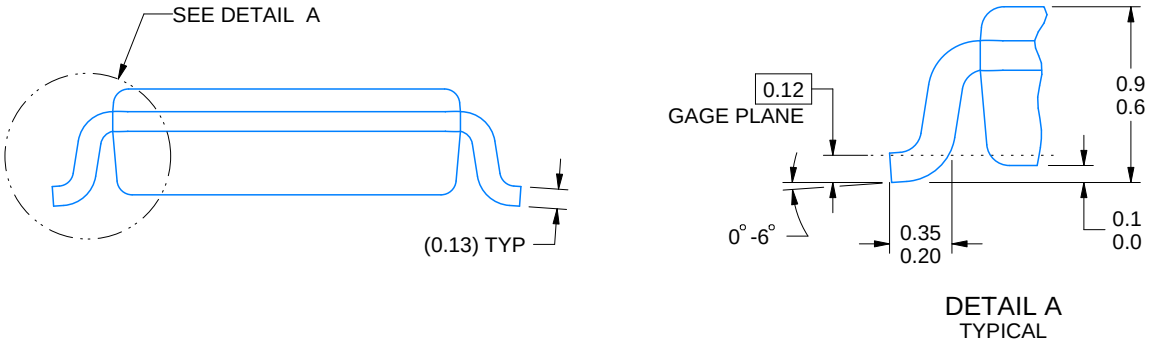
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

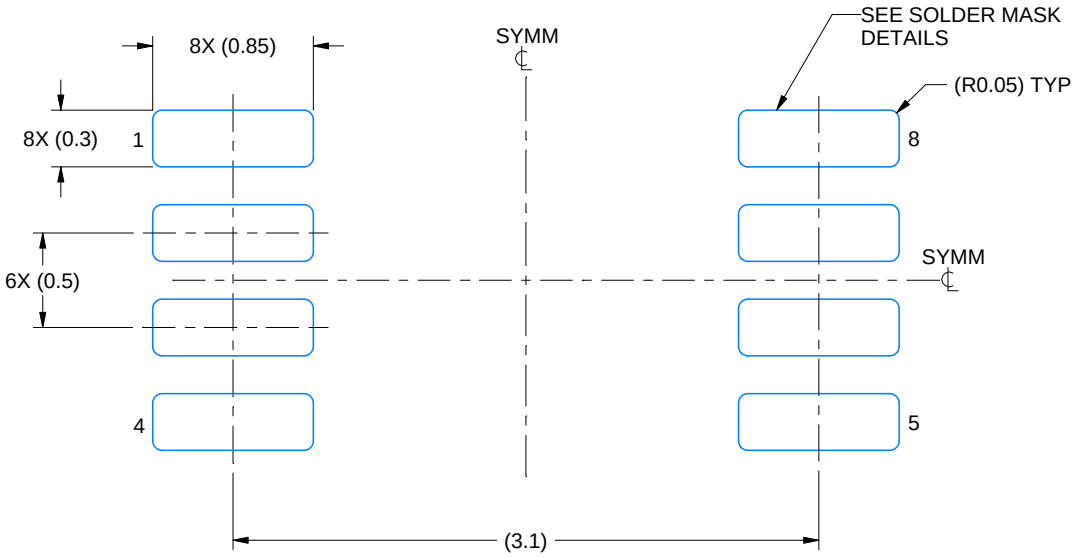




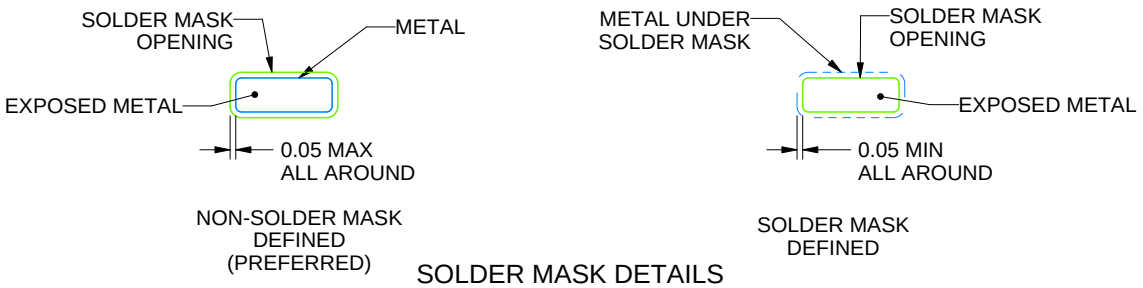
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

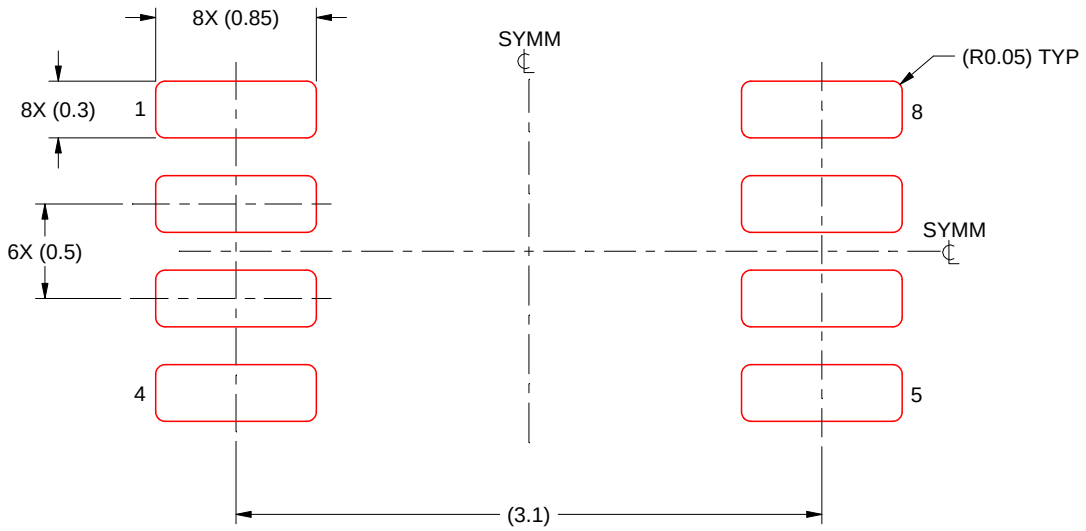


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

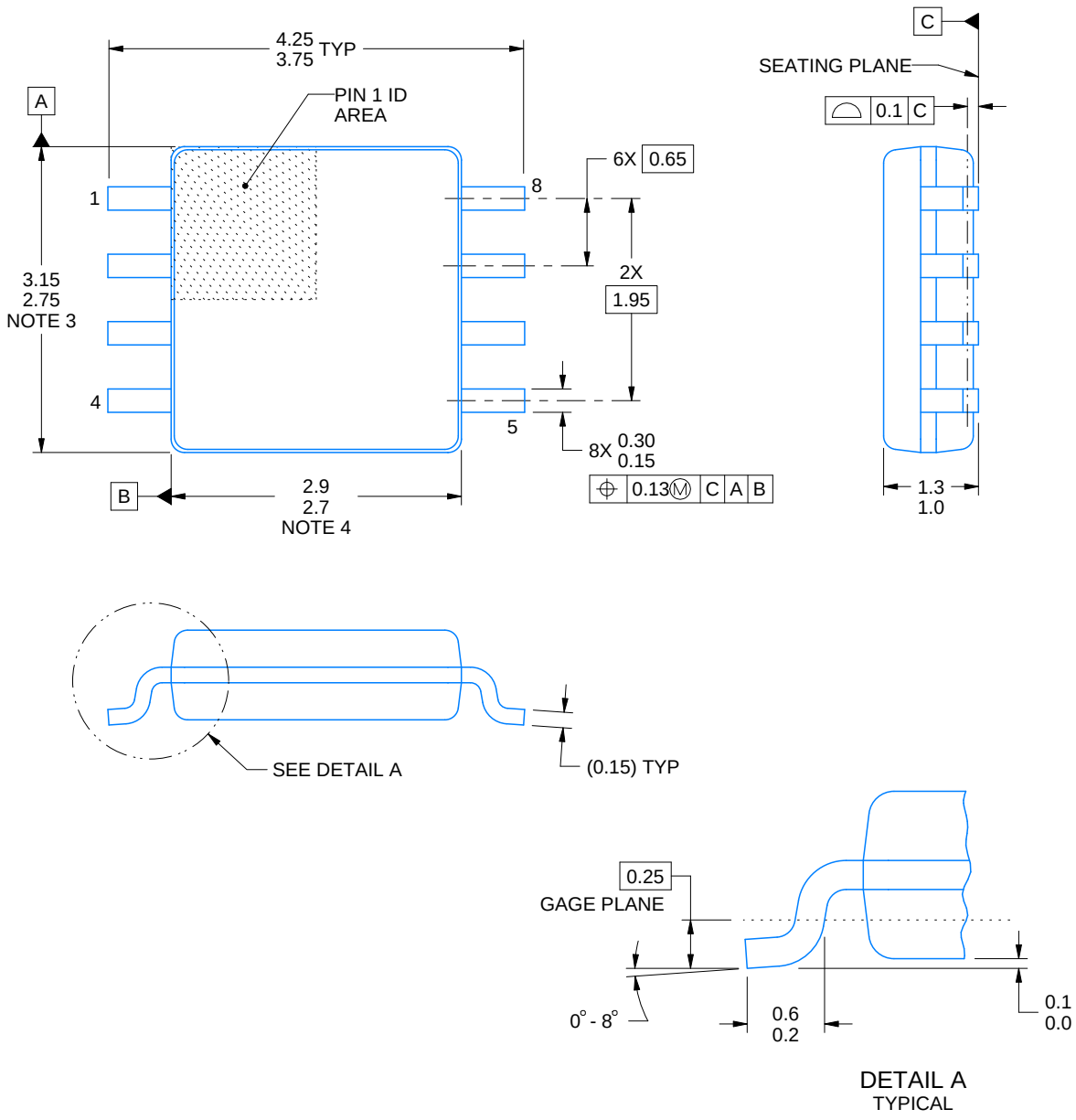
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

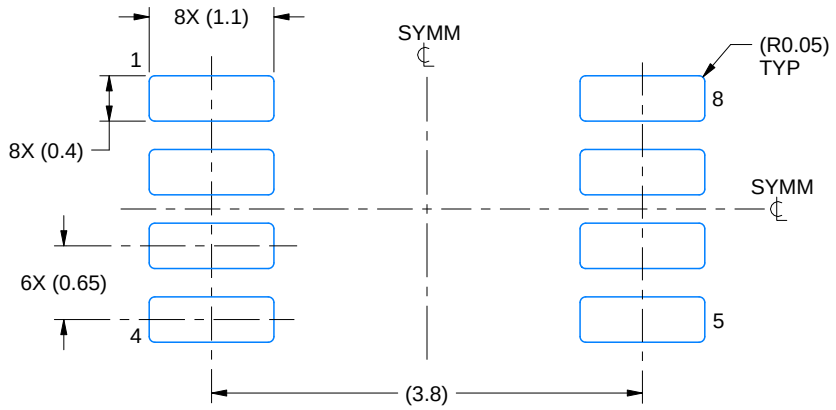
SMALL OUTLINE PACKAGE



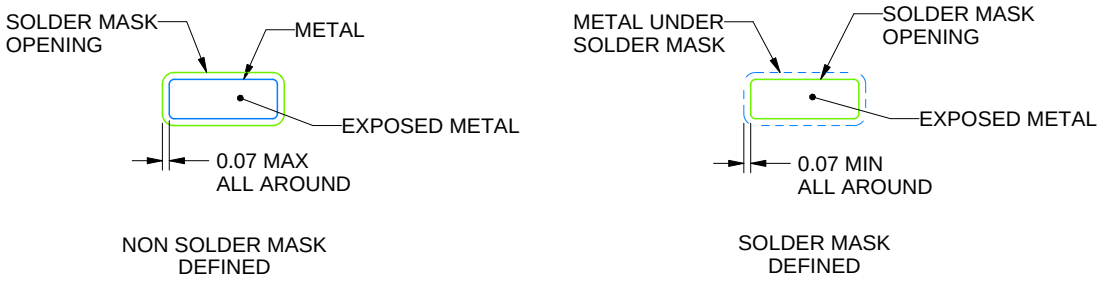
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

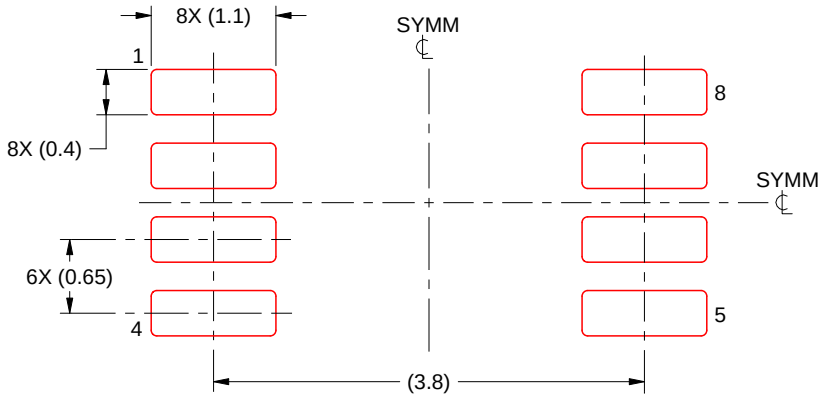


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

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8. Board assembly site may have different recommendations for stencil design.

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