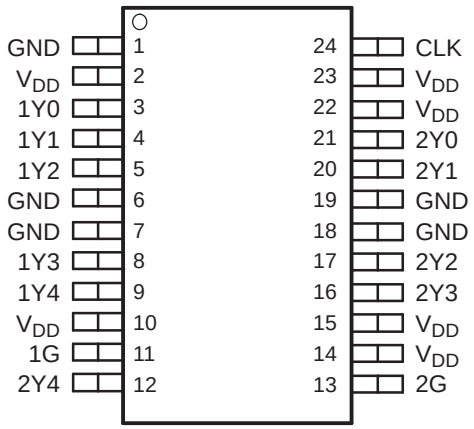
2.5V 至 3.3V 高性能时钟缓冲器

查询样品: CDCVF2310-EP

特性

- 高性能 **1:10** 时钟驱动器
- 在 V_{DD}为 **3.3V** 时，运行频率高达 **200MHz**
- 在 V_{DD}为 **3.3V** 时，引脚到引脚偏斜小于 **100ps**
- V_{DD}范围：**2.3V** 至 **3.6V**
- 输出使能毛刺脉冲抑制
- 将一个时钟输入分频至五个输出的两个组
- **25Ω** 片载串联阻尼电阻器
- 采用 **24** 引脚薄型小尺寸封装 **(TSSOP)**

PW PACKAGE
(TOP VIEW)



应用范围

- 通用应用

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 支持军用（**-55°C** 至 **125°C**）温度范围 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

(1) 可定制工作温度范围

说明

CDCVF2310 是一款运行频率高达 200MHz 的高性能、低偏斜时钟缓冲器。 五个输出的两个组中的每一个组提供 CLK 的低偏斜副本。 加电后，无论控制引脚的状态如何，输出的缺省状态为低电平。 对于正常运行，当控制引脚（分别为 1G 或 2G）被保持在低电平并且在 CLK 输入上检测到一个负时钟边沿时，组 1Y[0:4] 或 2Y[0:4] 的输出可被置于低电平状态。 当控制引脚（1G 和 2G）被保持在高电平并且在 CLK 输入上检测到一个负时钟边沿时，组 1Y[0:4] 或 2Y[0:4] 的输出可被切换至缓冲器模式。 此器件运行在一个 2.5V 和 3.3V 环境中。 内置的输出使能毛刺脉冲抑制可确保一个已同步的输出使能序列以分配完全周期时钟信号。

CDCVF2310 运行温度范围为 -55°C 至 125°C。

Table 1. ORDERING INFORMATION (1)

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	TSSOP - PW	CDCVF2310MPWREP	CKV2310EP	V62/13603-01XE
		CDCVF2310MPWEP	CKV2310EP	V62/13603-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

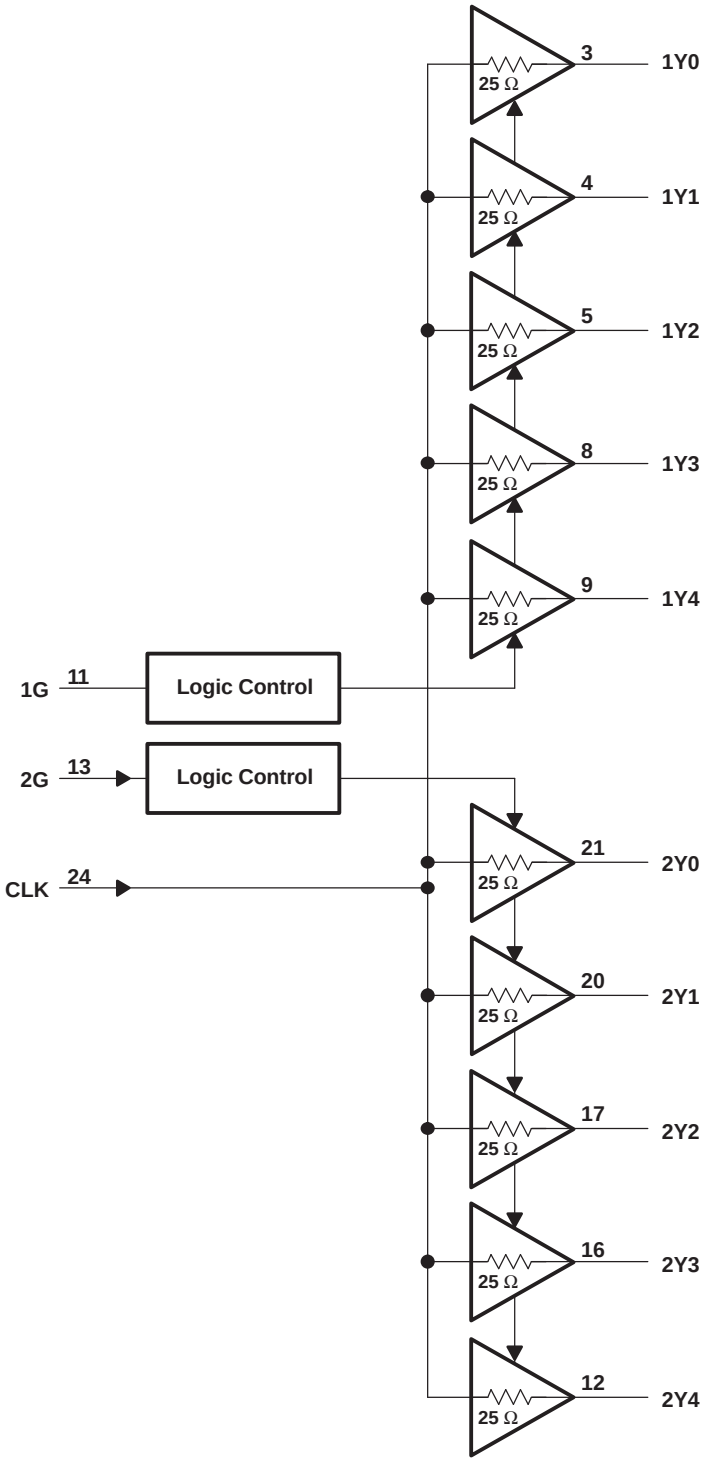

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Table 2. FUNCTION TABLE

INPUT			OUTPUT	
1G	**2G**	**CLK**	**1Y[0:4]**	**2Y[0:4]**
L	L	↓	L	L
H	L	↓	CLK(1)	L
L	H	↓	L	CLK(1)
H	H	↓	CLK(1)	CLK(1)

(1) After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
1G	11	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
2G	13	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
1Y[0:4]	3, 4, 5, 8, 9	O	Buffered output clocks
2Y[0:4]	21, 20, 17, 16, 12	O	Buffered output clocks
CLK	24	I	Input reference frequency
GND	1, 6, 7, 18, 19		Ground
V_{DD}	2, 10, 14, 15, 22, 23		DC power supply, 2.3 V – 3.6 V

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range (unless otherwise noted) (1)

Supply voltage range, V_{DD}	–0.5 V to 4.6 V
Input voltage range, V_I (2) (3)	–0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O (2) (3)	–0.5 V to V_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I> V_{DD})	±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD})	±50 mA
Storage temperature range T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.6 V maximum.

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THERMAL INFORMATION

THERMAL METRIC(1)		CDCVF2310 PW 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	91.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	31.2	
θ_{JB}	Junction-to-board thermal resistance(4)	46.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	45.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS (1)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3	2.5		V
			3.3	3.6	
Low-level input voltage, V_{IL}	V_{DD} = 3 V to 3.6 V			0.8	V
	V_{DD} = 2.3 V to 2.7 V			0.7	
High-level input voltage, V_{IH}	V_{DD} = 3 V to 3.6 V	2			V
	V_{DD} = 2.3 V to 2.7 V	1.7			
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	V_{DD} = 3 V to 3.6 V			12	mA
	V_{DD} = 2.3 V to 2.7 V			6	
Low-level output current, I_{OL}	V_{DD} = 3 V to 3.6 V			12	mA
	V_{DD} = 2.3 V to 2.7 V			6	
Operating junction temperature, T_J		–55		125	°C

(1) Unused inputs must be held high or low to prevent them from floating.

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ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V,	I_I = –18 mA			–1.2	V
I_I	Input current	V_I = 0 V or V_{DD}				±5	µA
I_{DD} (2)	Static device current	CLK = 0 V or V_{DD},	I_O = 0 mA			100	µA
C_I	Input capacitance	V_{DD} = 2.3 V to 3.6 V,	V_I = 0 V or V_{DD}		2.5		pF
C_O	Output capacitance	V_{DD} = 2.3 V to 3.6 V,	V_I = 0 V or V_{DD}		2.8		pF
V_{DD} = 3.3 V ±0.3 V							
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 µA	V_{DD} – 0.2			V
		V_{DD} = 3 V	I_{OH} = –12 mA	2.1			
			I_{OH} = –6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = –100 µA			0.2	V
		V_{DD} = 3 V	I_{OL} = 12 mA			0.8	
			I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3 V,	V_O = 1 V	–28			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		–36		
		V_{DD} = 3.6 V,	V_O = 3.135 V			–14	
I_{OL}	Low-level output current	V_{DD} = 3 V,	V_O = 1.95 V	28			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		36		
		V_{DD} = 3.6 V,	V_O = 0.4 V			14	
V_{DD} = 2.5 V ±0.2 V							
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 µA	V_{DD} – 0.2			V
		V_{DD} = 2.3 V	I_{OH} = –6 mA	1.8			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 100 µA			0.2	V
		V_{DD} = 2.3 V	I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 2.3 V,	V_O = 1 V	–15			mA
		V_{DD} = 2.5 V,	V_O = 1.25 V		–25		
		V_{DD} = 2.7 V,	V_O = 2.375 V			–10	
I_{OL}	Low-level output current	V_{DD} = 2.3 V,	V_O = 1.2 V	15			mA
		V_{DD} = 2.5 V,	V_O = 1.25 V		25		
		V_{DD} = 2.7 V,	V_O = 0.3 V			10	

(1) All typical values are at respective nominal V_{DD}.
(2) For I_{CC} over frequency, see Figure 6.

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TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating junction temperature

			MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency	V_{DD} = 3 V to 3.6 V	0		200	MHz
		V_{DD} = 2.3 V to 2.7 V	0		170	

JITTER CHARACTERISTICS

Characterized using CDCVF2310 Performance EVM when V_{DD}=3.3 V. Outputs not under test are terminated to 50 Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{jitter}	Additive phase jitter from input to output 1Y0	12 kHz to 5 MHz, f_{out} = 30.72 MHz		52		fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz		45		

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} = 3.3 V ±0.3 V (see Figure 2)						
t_{PLH} / t_{PHL}	CLK to Yn	f = 0 MHz to 200 MHz For circuit load, see Figure 2.	1.3		3.3	ns
$t_{sk(o)}$	Output skew (Ym to Yn) (1) (see Figure 4)				100	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				570	ps
$t_{sk(pp)}$	Part-to-part skew				500	ps
t_r	Rise time (see Figure 3)	V_O = 0.4 V to 2 V	0.7		2.2	V/ns
t_f	Fall time (see Figure 3)	V_O = 2 V to 0.4 V	0.7		2.2	V/ns
$t_{su(en)}$	Enable setup time, G_high before CLK ↓		0.1			ns
$t_{su(dis)}$	Disable setup time, G_low before CLK ↓		0.1			ns
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4			ns
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4			ns
V_{DD} = 2.5 V ±0.2 V (see Figure 2)						
t_{PLH} / t_{PHL}	CLK to Yn	f = 0 MHz to 170 MHz For circuit load, see Figure 2.	1.5		4	ns
$t_{sk(o)}$	Output skew (Ym to Yn) (1) (see Figure 4)				170	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				680	ps
$t_{sk(pp)}$	Part-to-part skew				600	ps
t_r	Rise time (see Figure 3)	V_O = 0.4 V to 1.7 V	0.5		1.4	V/ns
t_f	Fall time (see Figure 3)	V_O = 1.7 V to 0.4 V	0.5		1.4	V/ns
$t_{su(en)}$	Enable setup time, G_high before CLK ↓		0.1			ns
$t_{su(dis)}$	Disable setup time, G_low before CLK ↓		0.1			ns
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4			ns
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4			ns

(1) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

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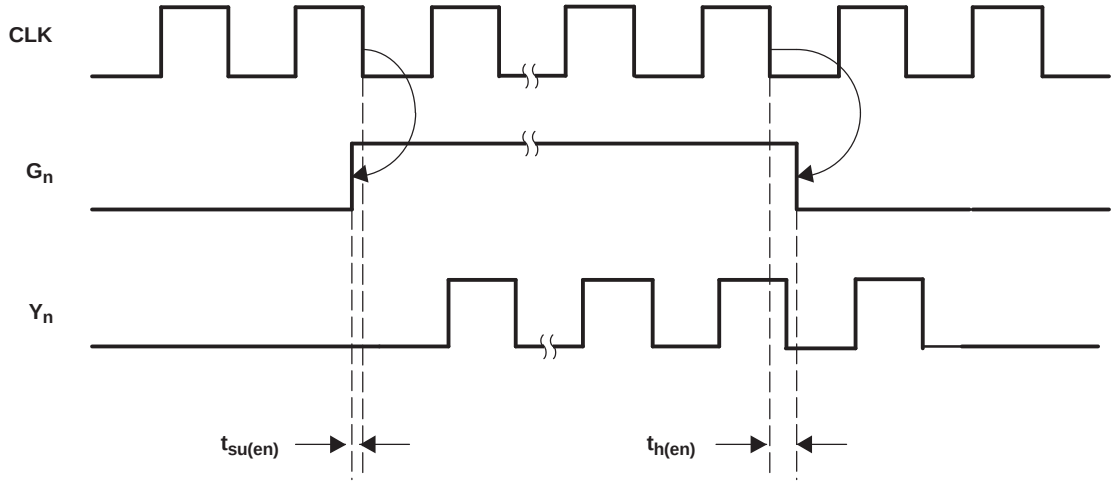
DETAILED DESCRIPTION

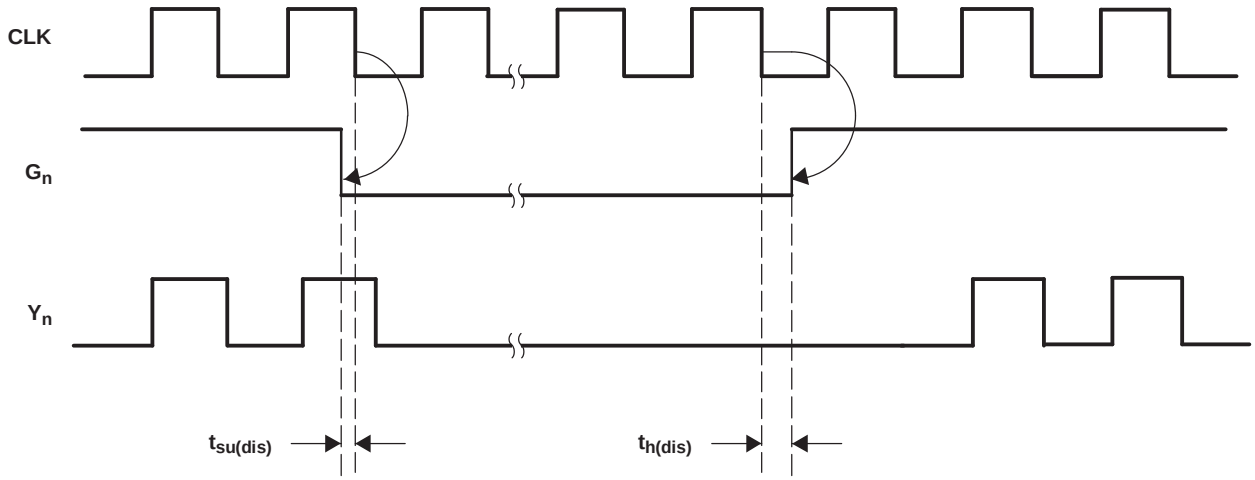
Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 1).

The G input must fulfill the timing requirements (t_{su}, t_h) according to the *Switching Characteristics* table for predictable operation.



a) Enable Mode



b) Disable Mode

Figure 1. Enable and Disable Mode Relative to CLK↓

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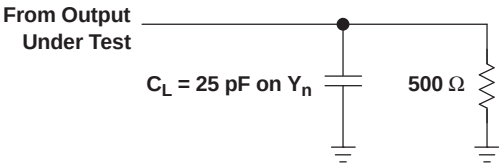
PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 200 MHz, Z_O = 50 Ω, t_r < 1.2 ns, t_f < 1.2 ns.

Figure 2. Test Load Circuit

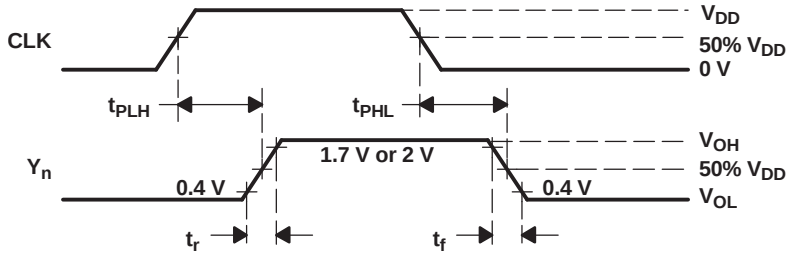


Figure 3. Voltage Waveforms Propagation Delay Times

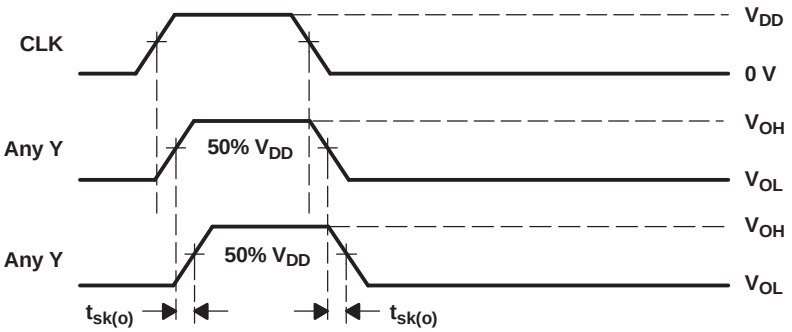
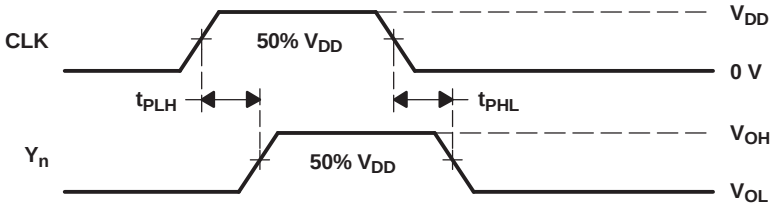


Figure 4. Output Skew



NOTE: $t_{sk(p)} = | t_{PLH} - t_{PHL} |$

Figure 5. Pulse Skew

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PARAMETER MEASUREMENT INFORMATION (continued)

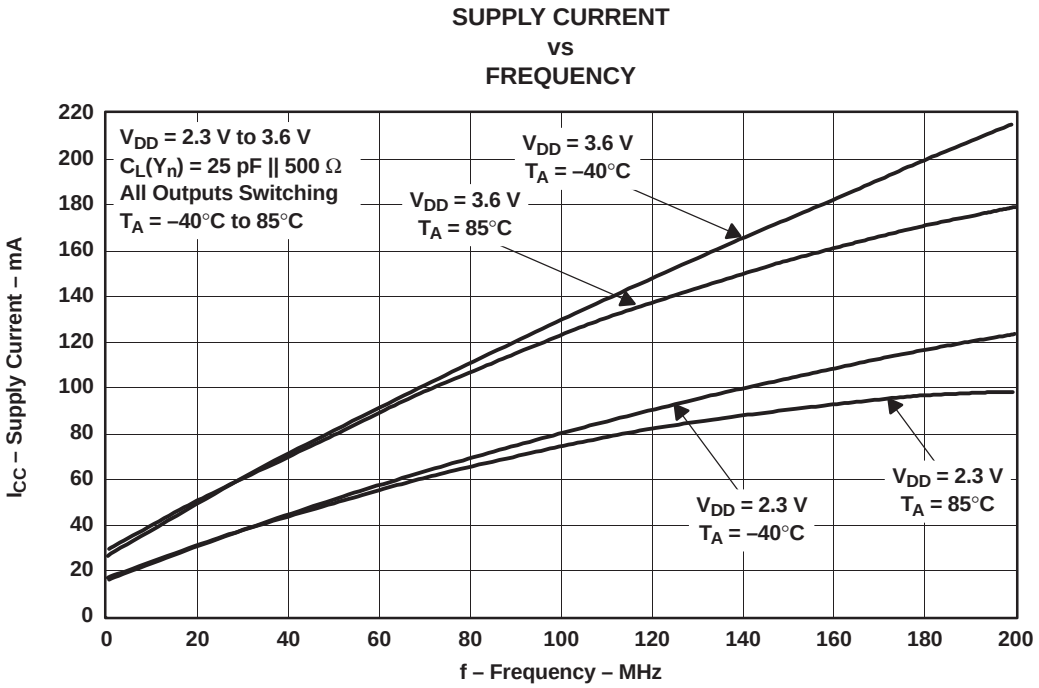

Figure 6.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF2310MPWEP	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	Samples
CDCVF2310MPWREP	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	Samples
V62/13603-01XE	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	Samples
V62/13603-01XE-T	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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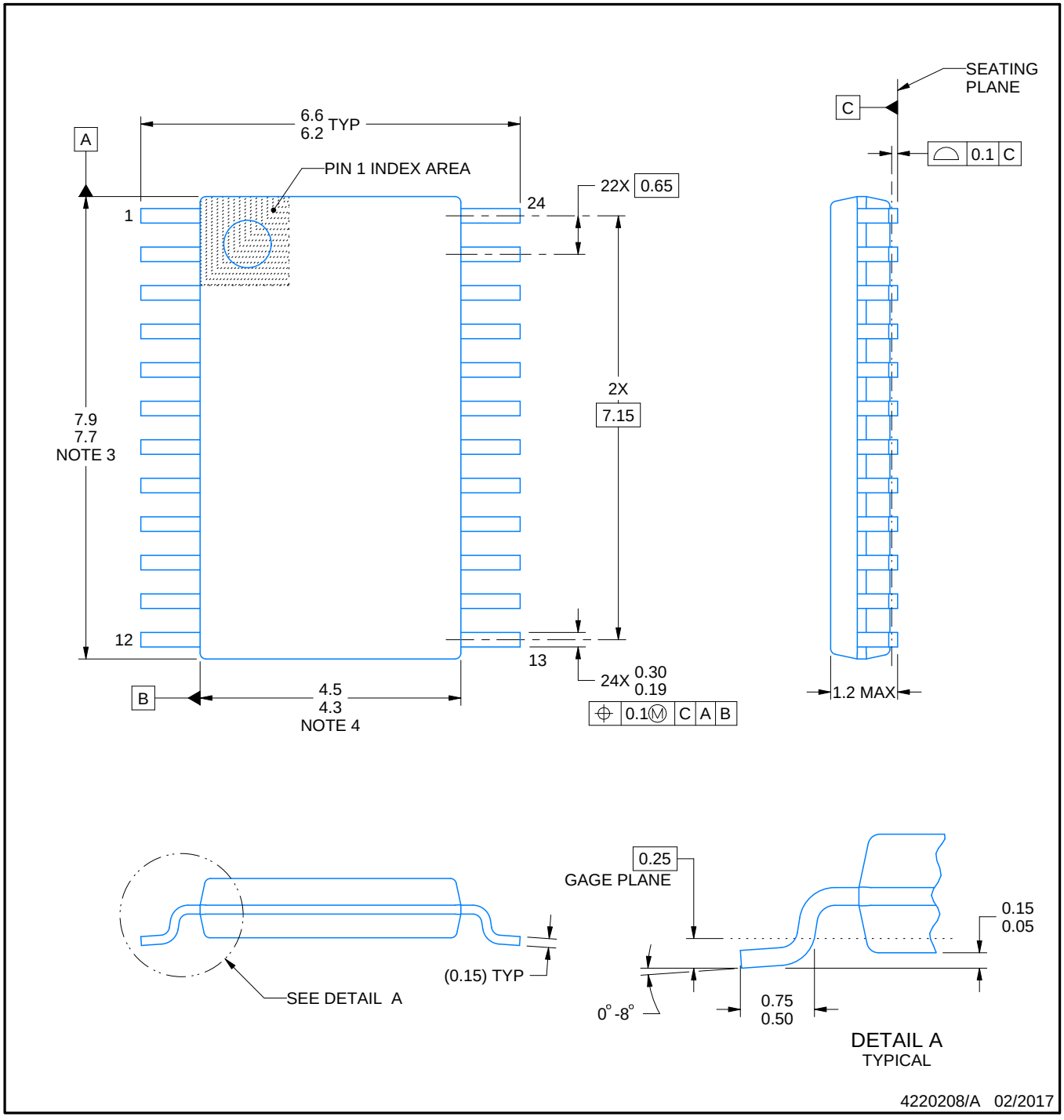
PACKAGE OUTLINE

PW0024A

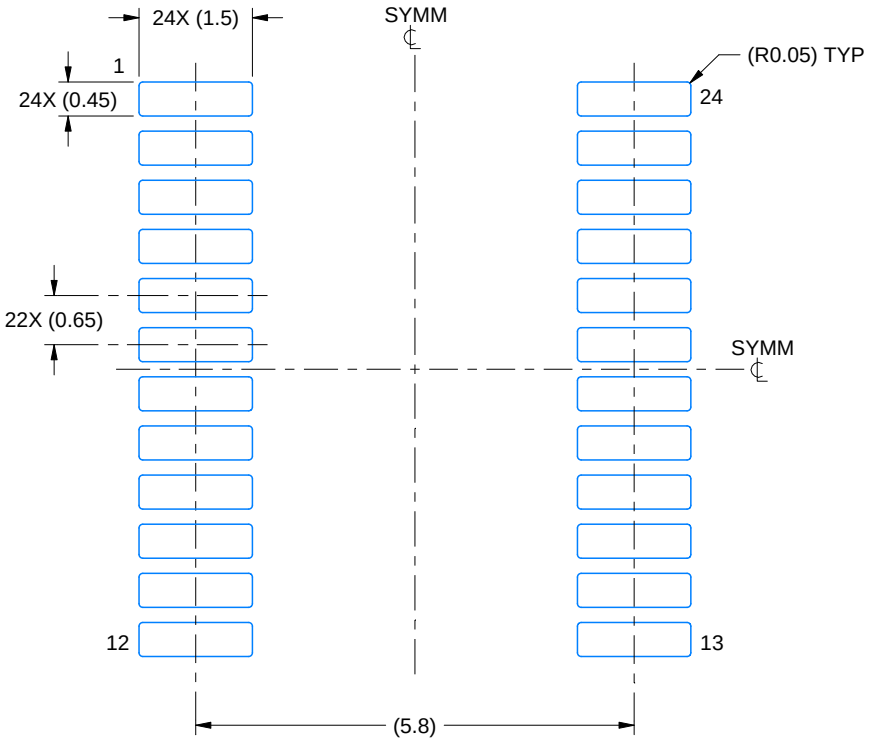
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

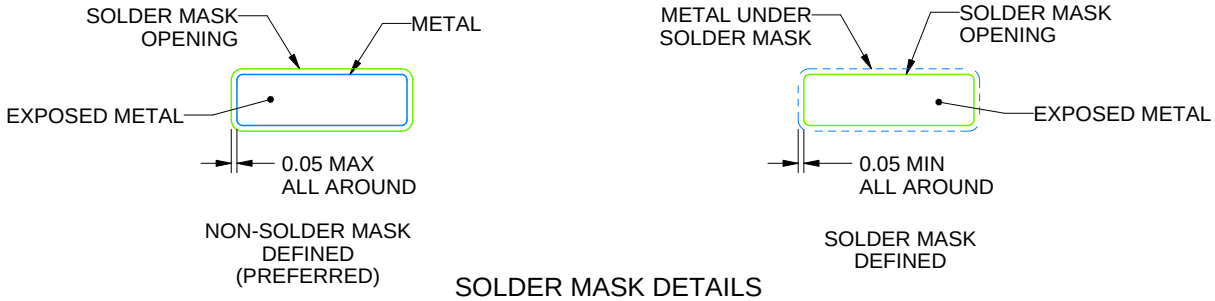


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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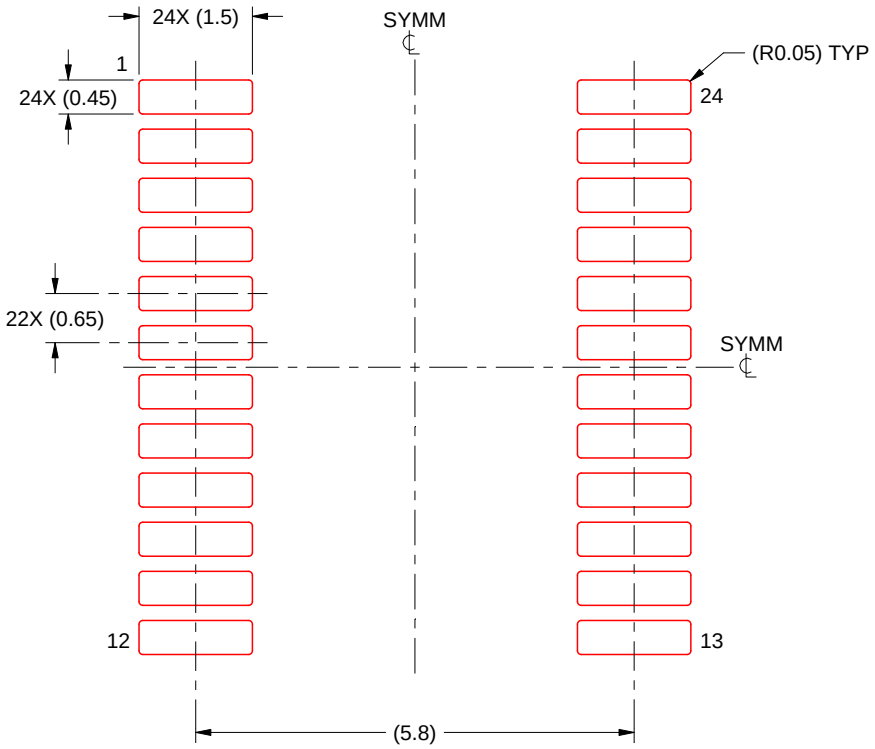
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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