

SN74CBTLV3253 低电压、双 4 选 1 FET 多路复用器/多路信号分离器

1 特性

- 在功能上与 QS3253 等效
- 两个端口间使用 5Ω 开关连接
- 数据 I/O 端口上的轨至轨开关
- I_{off} 支持局部关断模式运行
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 视频广播：基于 IP 的多格式转码器
- 视频通信系统

3 说明

SN74CBTLV3253 器件是一款双 4 选 1 高速 FET 多路复用器和多路信号分离器。此开关具有低导通状态电阻，可以在最短传播延迟情况下建立连接。

选择 (S0, S1) 输入端控制数据流。当相关输出使能 (\overline{OE}) 输入为高电平时，FET 多路复用器/多路信号分离器被禁用。

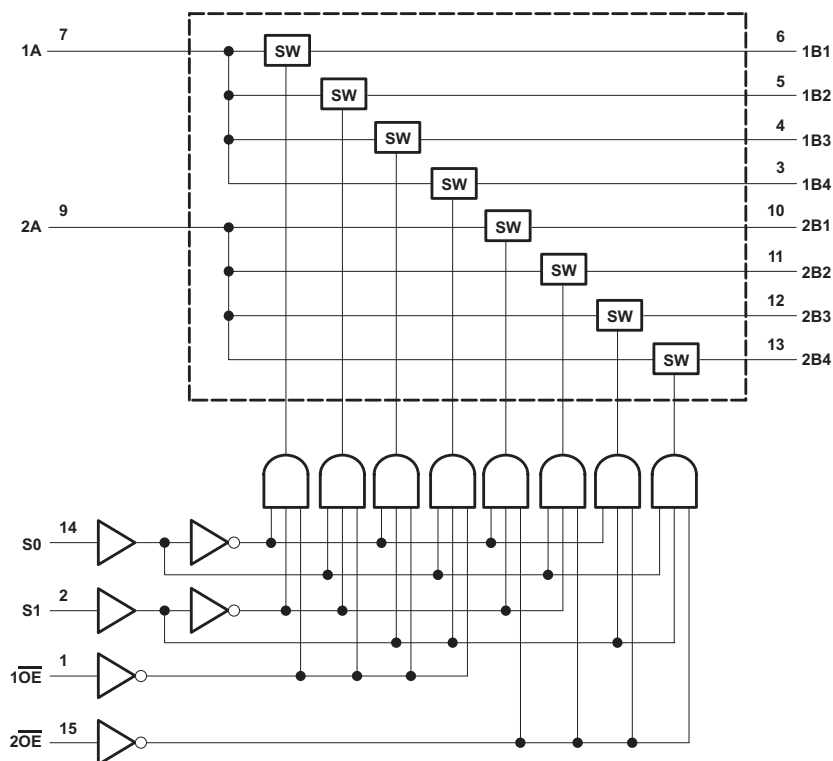
SN74CBTLV3253 器件完全适用于使用 I_{off} 的局部掉电应用。 I_{off} 特性确保在关断时防止损坏电流通过器件回流。该器件可在关断时提供隔离。

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CBTLV3253D	SOIC (16)	9.90mm x 3.90mm
SN74CBTLV3253DBQ	SSOP (16)	4.90mm x 3.90mm
SN74CBTLV3253DGV	TVSOP (16)	3.60mm x 4.40mm
SN74CBTLV3253RGY	VQFN (16)	4.00mm x 3.50mm
SN74CBTLV3253PW	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

逻辑图（正逻辑）



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision I (February 2014) to Revision J Page

- Changed the *Thermal Information* table **4**

Changes from Revision H (February 2014) to Revision I Page

- 已添加应用部分、器件信息表、引脚配置和功能部分、ESD 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 **1**

Changes from Revision G (February 2014) to Revision H Page

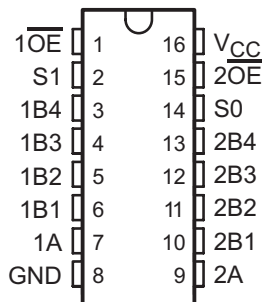
- 更新了产品说明书 - 无特定更改 **1**

Changes from Revision F (July 2012) to Revision G Page

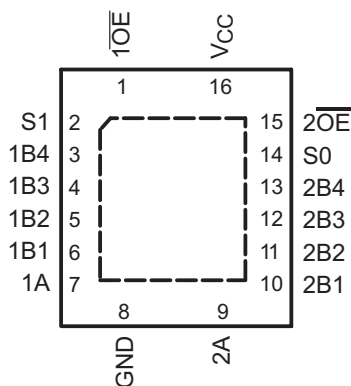
- 已删除 订购信息表。 **1**

5 Pin Configuration and Functions

D, DBQ, DGV, or PW Package
16-Pin SOIC, SSOP, TVSOP, or TSSOP
Top View



RGY Package
16-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{1OE}$	1	I	Output Enable 1 Active-Low
S1	2	I	Select Pin 1
1B4	3	I/O	Channel 1 I/O 4
1B3	4	I/O	Channel 1 I/O 3
1B2	5	I/O	Channel 1 I/O 2
1B1	6	I/O	Channel 1 I/O 1
1A	7	I/O	Channel 1 common
GND	8	—	Ground
2A	9	I/O	Channel 2 common
2B1	10	I/O	Channel 2 I/O 1
2B2	11	I/O	Channel 2 I/O 2
2B3	12	I/O	Channel 2 I/O 3
2B4	13	I/O	Channel 2 I/O 4
S0	14	I	Select Pin 0
$\overline{2OE}$	15	I	Output Enable 2 Active-Low
V _{CC}	16	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	4.6	V
V _{IN}	Control input voltage ⁽²⁾	-0.5	4.6	V
V _{I/O}	Switch I/O voltage ⁽²⁾	-0.5	4.6	V
I _{IK}	Control input clamp current	V _{IN} < 0	-50	mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0	-50	mA
Continuous current through V _{CC} or GND			±128	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT	
V _{ESD}	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	+2000	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	+1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	V
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0.8	
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74CBTLV3253					UNIT	
	D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)		
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	86.7	112.4	123.1	110.9	47.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	47.8	63.6	48.7	45.8	58.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.7	54.8	54.9	56.0	24.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	12.3	17.0	5.2	5.4	1.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	43.5	54.4	54.3	55.4	24.0	°C/W
R _{θJC(bottom)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	9.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I		$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND			± 1	μA
I_{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 3.6 V			15	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$,	$I_O = 0$,			10	μA
ΔI_{CC} ⁽²⁾	Control inputs	$V_{CC} = 3.6\text{ V}$,	One input at 3 V,			300	μA
			Other inputs at V_{CC} or GND				
C_i	Control inputs	$V_I = 3\text{ V}$ or 0			3		pF
$C_{io(OFF)}$	A port	$V_O = 3\text{ V}$ or 0,	$\overline{OE} = V_{CC}$		20.5		pF
	B port				5.5		
r_{on} ⁽³⁾	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	8	Ω	
			$I_I = 24\text{ mA}$	5	8		
		$V_I = 1.7\text{ V}$,	$I_I = 15\text{ mA}$	27	40		
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	7		
			$I_I = 24\text{ mA}$	5	7		
		$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$	10	15		

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B ⁽¹⁾	B or A		0.15		0.25	ns
	S	A or B	1	6.8	1	5.5	
t_{en}	S	A or B	1	4.3	1	4	ns
t_{dis}	S	A or B	1	5.1	1	5.5	ns
t_{en}	\overline{OE}	A or B	1	5	1	4.8	ns
t_{dis}	\overline{OE}	A or B	1	5.5	1	5.4	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristics

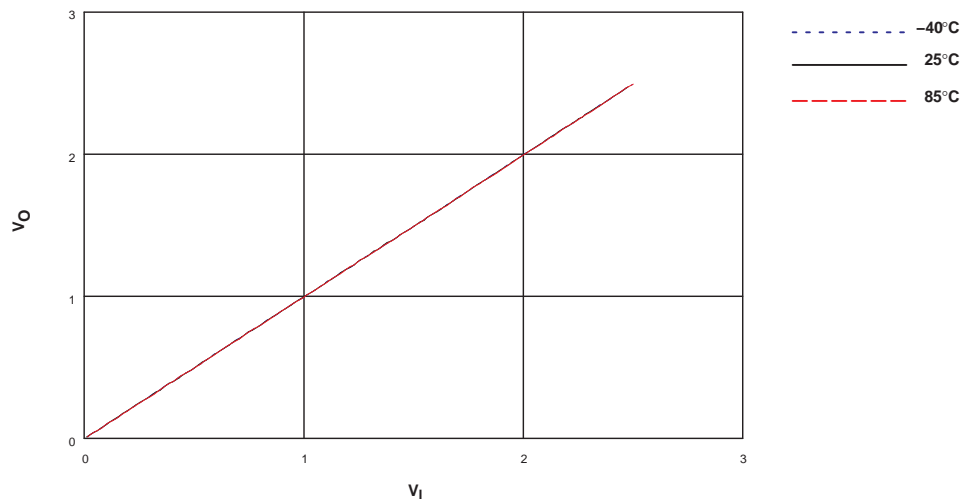
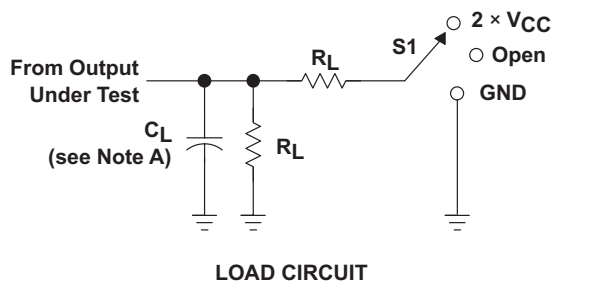


Figure 1. V_O vs V_I , $V_{CC} = 2.5$ V

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5\text{ V} \pm 0.2\text{ V}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	50 pF	500 Ω	0.3 V

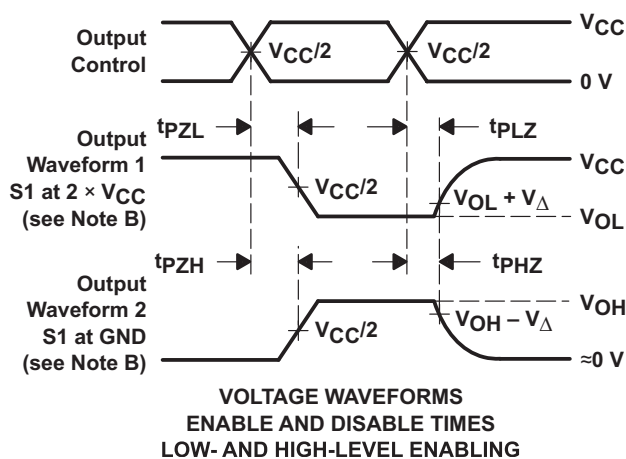
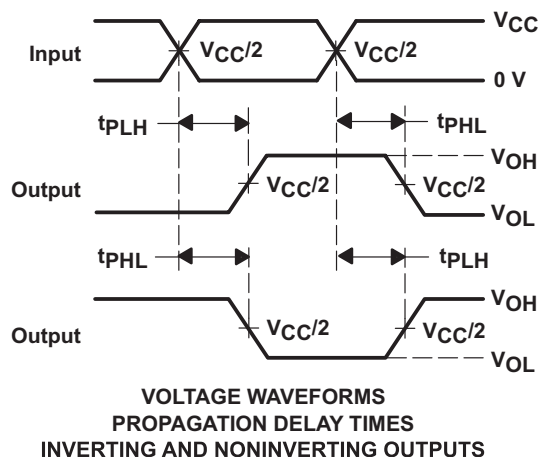
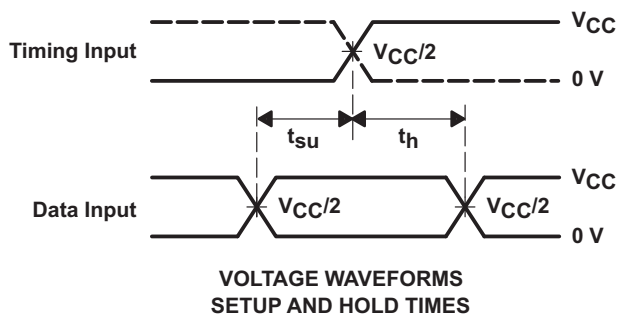
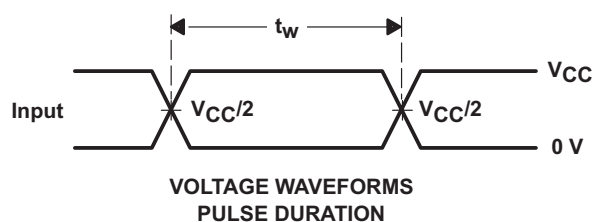


Figure 2. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

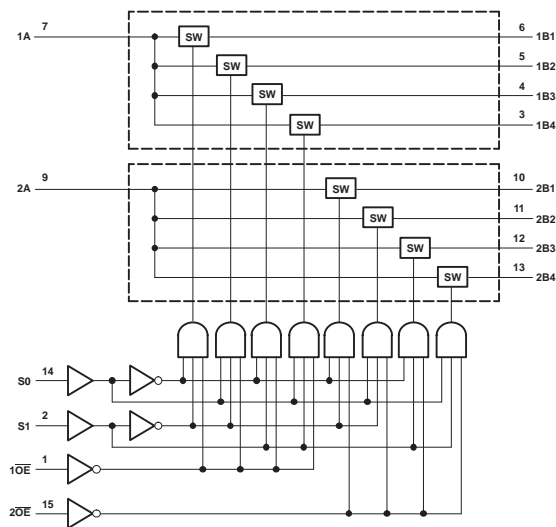
The SN74CBTLV3253 device is a dual 1-of-4 high-speed FET multiplexer/demultiplexer. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S0, S1) inputs control the data flow. The FET multiplexers and demultiplexers are disabled when the associated output-enable (\overline{OE}) input is high.

The SN74CBTLV3253 device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

The SN74CBTLV3253 device is functionally equivalent to the QS3253 and has a 5- Ω switch connection between two ports

It also has rail-to-rail switching on data I/O ports as well as I_{off} supporting partial-power-down mode operation

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74CBTLV3253.

**Table 1. Function Table
(Each Multiplexer/Demultiplexer)**

INPUTS			FUNCTION
\overline{OE}	S1	S0	
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBTLV3253 can be used to multiplex and demultiplex up to 2 channels simultaneously in a 4:1 configuration. The application shown here is a 2-bit bus being multiplexed between two devices. the \overline{OE} and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations.

9.2 Typical Application

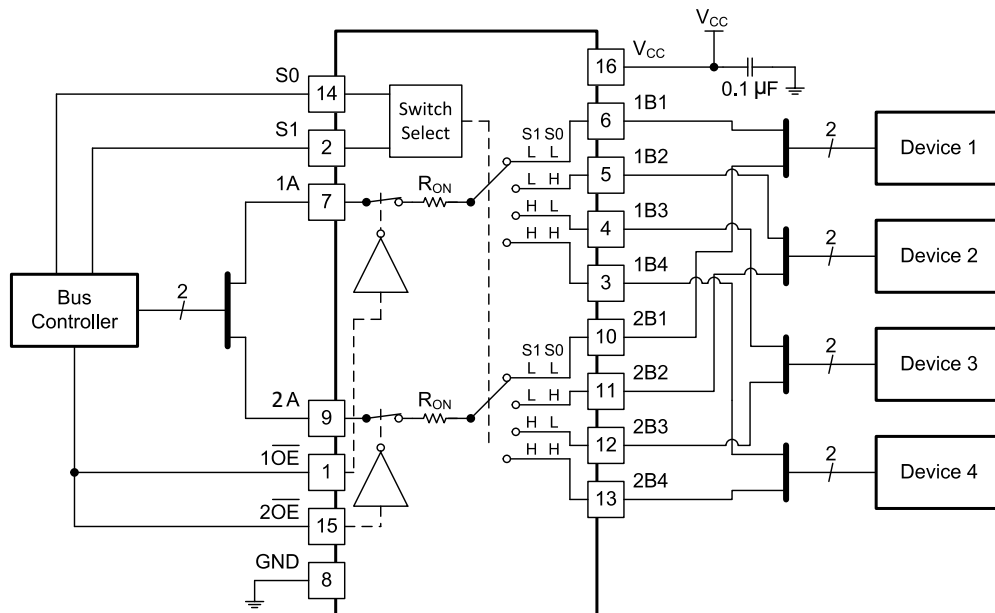


Figure 3. Typical Application of the SN74CBTLV3253

9.2.1 Design Requirements

The 0.1µF capacitor should be placed as close as possible to the device.

9.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - For specified high and low levels, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#).
 - Inputs and outputs are overvoltage tolerant allowing them to go as high as 4.6 V at any valid V_{CC} .
- Recommended Output Conditions:
 - Load currents should not exceed ± 128 mA per channel.
- Frequency Selection Criterion:
 - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in [Layout](#).

Typical Application (continued)

9.2.3 Application Curve

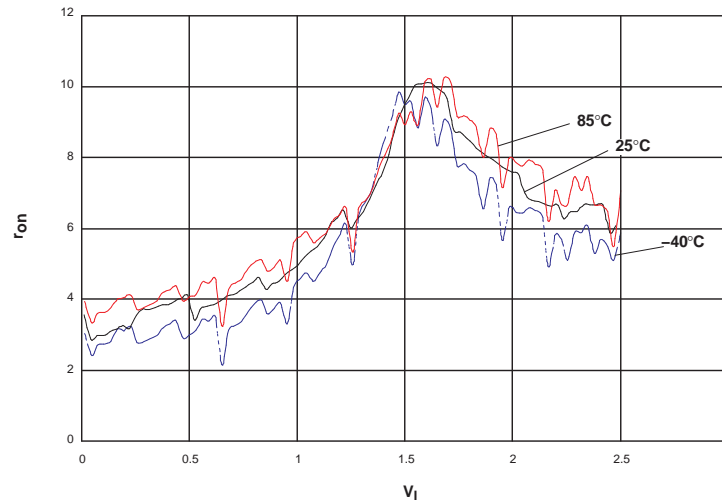


Figure 4. r_{on} vs V_I , $V_{CC} = 2.5$ V

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 5 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

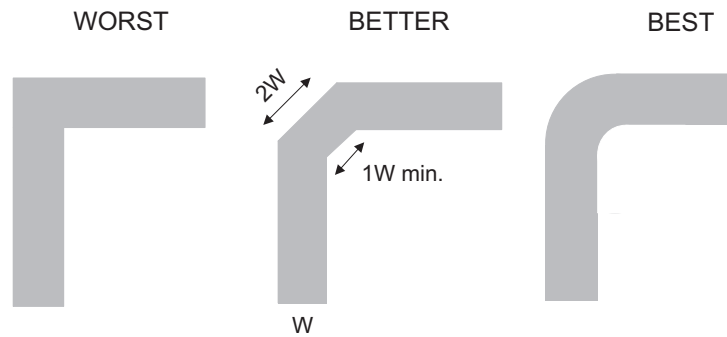


Figure 5. Trace Example

12 器件和文档支持

12.1 Documentation Support

12.1.1 相关文档

请参阅如下相关文档：

《CMOS 输入缓慢变化或悬空的影响》， [SCBA004](#)

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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12.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTLV3253PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253	Samples
SN74CBTLV3253D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253	Samples
SN74CBTLV3253DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253	Samples
SN74CBTLV3253DE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253	Samples
SN74CBTLV3253DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253	Samples
SN74CBTLV3253DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253	Samples
SN74CBTLV3253PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253	Samples
SN74CBTLV3253PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253	Samples
SN74CBTLV3253RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3253DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3253DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBTLV3253PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3253RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3253DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBTLV3253DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74CBTLV3253DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74CBTLV3253PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CBTLV3253RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBTLV3253D	D	SOIC	16	40	507	8	3940	4.32
SN74CBTLV3253DE4	D	SOIC	16	40	507	8	3940	4.32
SN74CBTLV3253PW	PW	TSSOP	16	90	530	10.2	3600	3.5

EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

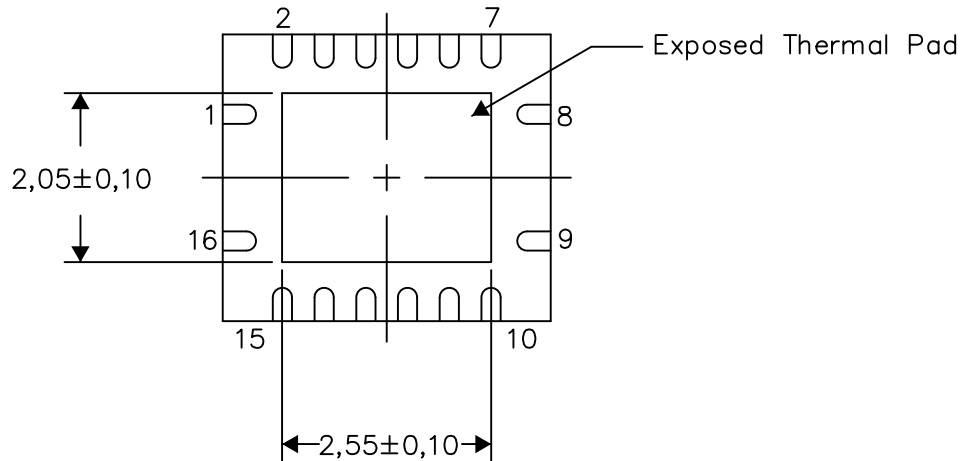
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD





4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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