

# SN74CB3Q3305 双路 FET 总线开关

## 2.5V 或 3.3V 低压高带宽总线开关

### 1 特性

- 高带宽数据路径 (高达 500MHz)<sup>1</sup>
- 可耐受 5V 电压并支持器件上电或断电的 I/O
- 在运行范围内具有平缓的低通态电阻 ( $r_{on}$ ) 特性 ( $r_{on}$  典型值 = 3Ω)
- 数据 I/O 端口支持超出电源电压范围的输入电压
  - 3.3V  $V_{CC}$  时, 开关范围为 0 至 5V
  - 2.5V  $V_{CC}$  时, 开关范围为 0 至 3.3V
- 具有接近零传播延迟的双向数据流
- 低输入和输出电容可更大程度减小负载和信号失真 ( $C_{io(OFF)}$  典型值 = 3.5pF)
- 快速开关频率 ( $f_{OE}$  最大值 = 20MHz)
- 数据与控制输入提供下冲钳位二极管
- 低功耗 ( $I_{CC}$  典型值 = 0.25mA)
- $V_{CC}$  工作范围为 2.3V 至 3.6V
- 数据 I/O 支持 0 至 5V 信号电平 (0.8V、1.2V、1.5V、1.8V、2.5V、3.3V 和 5V)
- 控制输入可由 TTL 或 5V/3.3V CMOS 输出驱动
- $I_{off}$  支持局部断电模式运行
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范

### 2 应用

- IP 电话: 有线和无线
- 光学模块
- 光纤网络: 光纤和 EPON 视频
- 专用分支交换机 (PBX)
- WiMAX 和无线基础设施设备
- USB、差分信号接口
- 总线隔离

### 3 描述

SN74CB3Q3305 器件是一款高带宽 FET 总线开关, 此开关利用一个电荷泵来提升通道晶体管的栅极电压, 从而提供一个平缓的低通态电阻 ( $r_{on}$ )。平缓的低通态电阻可实现非常短的传播延迟, 并且支持在数据输入/输出 (I/O) 端口上开关超出电源电压范围的输入电压。该器件还具有低的数据 I/O 电容, 以更大限度地减少数据总线上的容性负载和信号失真。SN74CB3Q3305 器件专为支持高带宽应用而设计, 提供优化的接口解决方案, 非常适合宽带通信、网络和数据密集型计算系统。

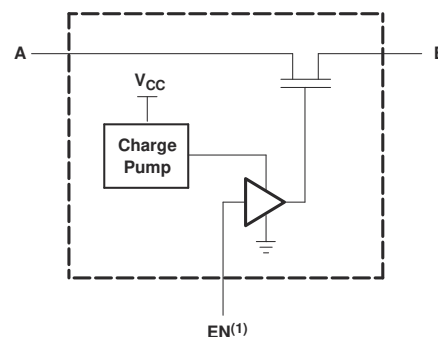
该器件完全符合使用  $I_{off}$  的部分断电应用的规范要求。 $I_{off}$  电路可防止在器件断电时电流回流对器件造成损坏。该器件可在关闭时提供隔离。

为确保在加电或断电期间处于高阻抗状态, 应将 OE 通过下拉电阻器接地; 该电阻器的最小值取决于驱动器的拉电流能力。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
SN74CB3Q3305	VSSOP (8)	2.00 mm × 3.10 mm
	TSSOP (8)	3.00 mm × 6.10 mm

- (1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



(1) EN is the internal enable signal applied to the switch.

#### 每个 FET 开关 (SW) 的简化版原理图

<sup>1</sup> 有关 CB3Q 系列器件性能特性的更多信息, 请参阅 TI 应用报告《CBT-C、CB3T 和 CB3Q 信号开关系列》, SCDA008。



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision C (October 2015) to Revision D (September 2021)</b>	<b>Page</b>
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 更新了数据表以包含丰富的术语.....	1

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<b>Changes from Revision B (October 2009) to Revision C (October 2015)</b>	<b>Page</b>
• 添加了引脚配置和功能部分、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

## 5 Pin Configuration and Functions

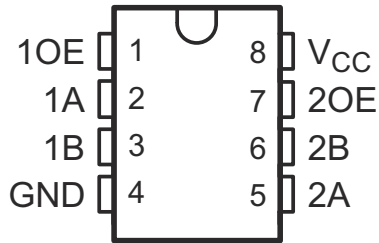


图 5-1. PW Package  
 8-Pin TSSOP  
 Top View

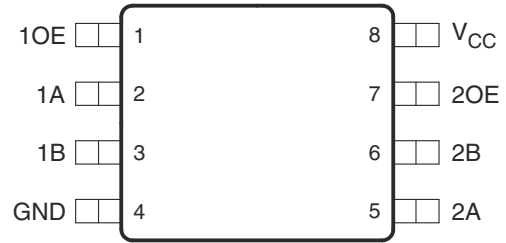


图 5-2. DCU Package  
 8-Pin VSSOP  
 Top View

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	2	I/O	Channel 1 A port
1B	3	I/O	Channel 1 B port
1OE	1	I	Output Enable for switch 1
2A	5	I/O	Channel 2 A port
2B	6	I/O	Channel 2 B port
2OE	7	I	Output Enable for switch 2
GND	4	P	Ground
V <sub>cc</sub>	8	P	Power supply

(1) I = input, O = output, I/O = input and output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	- 0.5	4.6	V
V <sub>IN</sub>	Control input voltage <sup>(2)</sup> <sup>(3)</sup>	- 0.5	7	V
V <sub>I/O</sub>	Switch I/O voltage <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup>	- 0.5	7	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0	- 50	mA
I <sub>I/OK</sub>	I/O port clamp current	V <sub>I/O</sub> < 0	- 50	mA
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>		±64	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(6)</sup>		88	°C/W
T <sub>j</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I/O</sub>	Data input/output voltage	0	5.5	V
T <sub>A</sub>	Operating free-air temperature	- 40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74CB3Q3305	SN74CB3Q3305	UNIT
		DCU (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183	190.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.2	74.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.5	119.4	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	4.3	120.0	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	62.1	117.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 3.6\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.8	V
$I_{IN}$	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	$V_{IN} = 0\text{ to }5.5\text{ V}$			±1	µA
$I_{OZ}$ <sup>(3)</sup>		$V_{CC} = 3.6\text{ V}$ ,	$V_O = 0\text{ to }5.5\text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$			±1	µA
$I_{off}$		$V_{CC} = 0$ ,	$V_O = 0\text{ to }5.5\text{ V}$ , $V_I = 0$			1	µA
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ ,	$I_{IO} = 0$ , Switch ON or OFF, $V_{IN} = V_{CC}\text{ or GND}$		0.25	0.7	mA
$\Delta I_{CC}$ <sup>(4)</sup>	Control inputs	$V_{CC} = 3.6\text{ V}$ , One input at 3 V, Other inputs at $V_{CC}$ or GND				25	µA
$I_{CCD}$ <sup>(5)</sup>	Per control input	$V_{CC} = 3.6\text{ V}$ ,	A and B ports open, Control input switching at 50% duty cycle		0.040	0.045	mA/MHz
$C_{in}$	Control inputs	$V_{CC} = 3.3\text{ V}$ ,	$V_{IN} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		2.5	3.5	pF
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$ ,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$ , $V_{IO} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		3.5	5	pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$ ,	Switch ON, $V_{IN} = V_{CC}\text{ or GND}$ , $V_{IO} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		8	10.5	pF
$r_{on}$ <sup>(6)</sup>		$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0, I_O = 30\text{ mA}$		3	8	Ω
			$V_I = 1.7\text{ V}, I_O = -15\text{ mA}$		3.5	9	
		$V_{CC} = 3\text{ V}$	$V_I = 0, I_O = 30\text{ mA}$		3	6	
			$V_I = 2.4\text{ V}, I_O = -15\text{ mA}$		3.5	8	

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see [Figure 9-2](#)).

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	MIN	MAX	UNIT
f <sub>OE</sub> <sup>(1)</sup>	OE	A or B	V <sub>CC</sub> = 2.5 V ± 0.2 V		10	MHz
			V <sub>CC</sub> = 3.3 V ± 0.3 V		20	
t <sub>pd</sub> <sup>(2)</sup>	A or B	B or A	V <sub>CC</sub> = 2.5 V ± 0.2 V		0.09	ns
			V <sub>CC</sub> = 3.3 V ± 0.3 V		0.15	
t <sub>en</sub>	OE	A or B	V <sub>CC</sub> = 2.5 V ± 0.2 V	1	5	ns
			V <sub>CC</sub> = 3.3 V ± 0.3 V	1	4.5	
t <sub>dis</sub>	OE	A or B	V <sub>CC</sub> = 2.5 V ± 0.2 V	1	4.5	ns
			V <sub>CC</sub> = 3.3 V ± 0.3 V	1	5	

- (1) Maximum switching frequency for control input (V<sub>O</sub> > V<sub>CC</sub>, V<sub>I</sub> = 5 V, R<sub>L</sub> ≥ 1 MΩ, C<sub>L</sub> = 0).
- (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## 6.7 Typical Characteristics

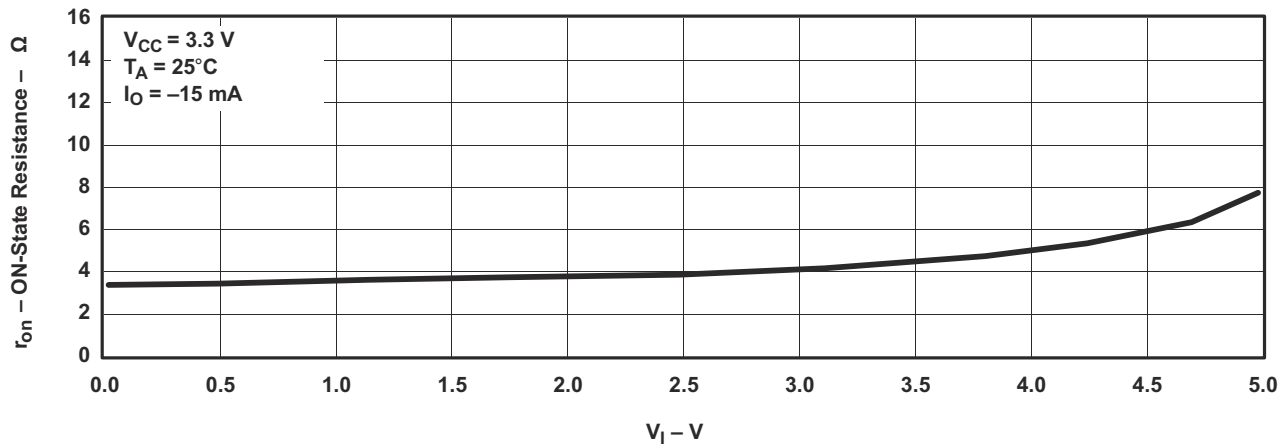
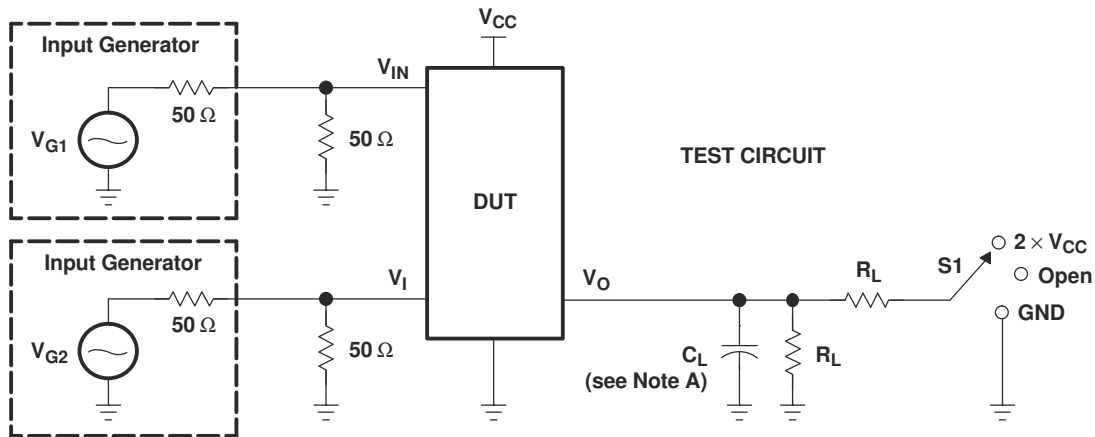
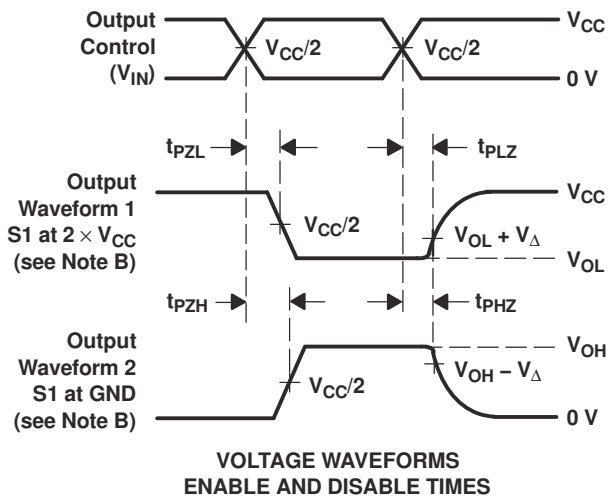
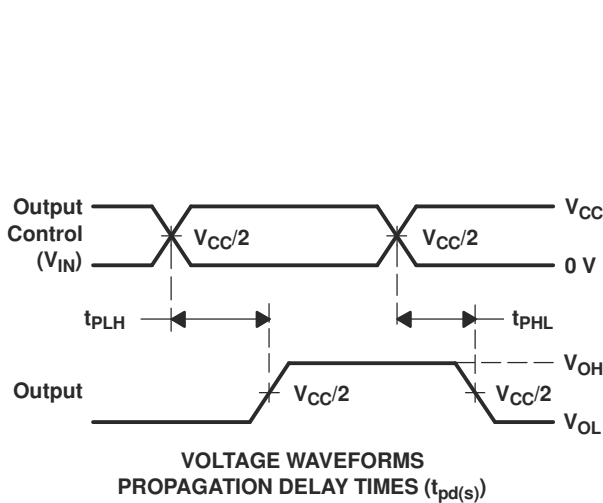


图 6-1. Typical  $r_{on}$  vs  $V_I$

## 7 Parameter Measurement Information



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub>	2.5 V ± 0.2 V	Open	500 Ω	V <sub>CC</sub> or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	GND	500 Ω	V <sub>CC</sub>	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - All parameters and waveforms are not applicable to all devices.

图 7-1. Test Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74CB3Q3305 device is organized as two 1-bit switches with separate output-enable (1OE and 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF and a high-impedance state exists between the A and B ports.

### 8.2 Functional Block Diagram

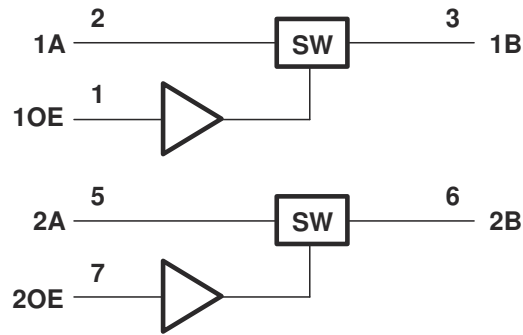


图 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

The device supports High-Bandwidth data path up to 500 MHz. The I/O ports are 5 V tolerant when powered up or powered down due to  $I_{OFF}$ . The charge pump creates low and flat ON-state resistance characteristics over the whole operating temperature range.

Switching input voltage beyond the supply is supported on data I/O ports: 0 V to 5 V with 3.3 V  $V_{CC}$  or 0 V to 3.3 V with 2.5 V  $V_{CC}$ .

The data flow is bidirectional with near-zero propagation delay. Reduced input/output capacitance for higher speed applications. OE can be toggled at the high speeds of 20 MHz for fast switching applications.

### 8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74CB3Q3305.

表 8-1. Function Table (Each Bus Switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect



## 9 Application and Implementation

### Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

图 9-1 显示 SN74CB3Q3305 可以作为双向开关使用。控制器在 5 V 下工作，且外围设备可以接受 5 V。即使 SN74CB3Q3305 的  $V_{CC}$  为 3 V，两个端口也可以连接以传递 5 V 信号。控制器使用 OE 引脚控制开关。这是一个非常通用的示例，可能适用于许多情况。对于只需要 1 位（例如，一个通道）的应用，将未使用的 OE 引脚拉低并将未使用的端口 A 和 B 连接到高电平或低电平（未显示）。

### 9.2 Typical Application

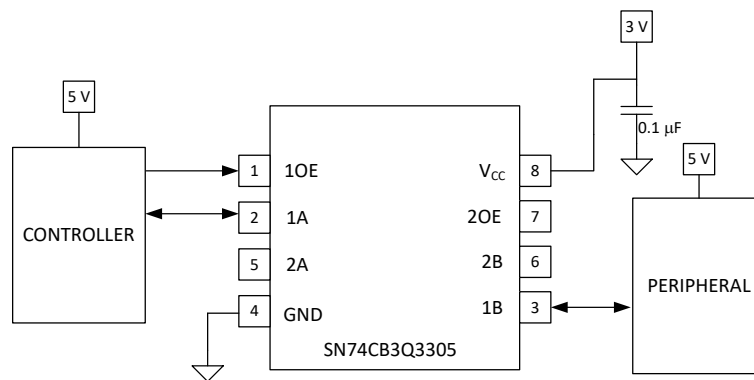


图 9-1. Typical Application of the SN74CB3Q3305

#### 9.2.1 Design Requirements

- Recommended Input Conditions:
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in 节 6.3.
  - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
- Absolute Maximum Conditions:
  - I/O currents should not exceed  $\pm 64$  mA per channel.
  - Continuous current through GND or  $V_{CC}$  should not exceed  $\pm 100$  mA.
- Frequency Selection Criterion:
  - Maximum frequency tested is 500 MHz.
  - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in 节 11.

#### 9.2.2 Detailed Design Procedure

The 0.1  $\mu$ F capacitor should be placed as close as possible to the device.

### 9.2.3 Application Curve

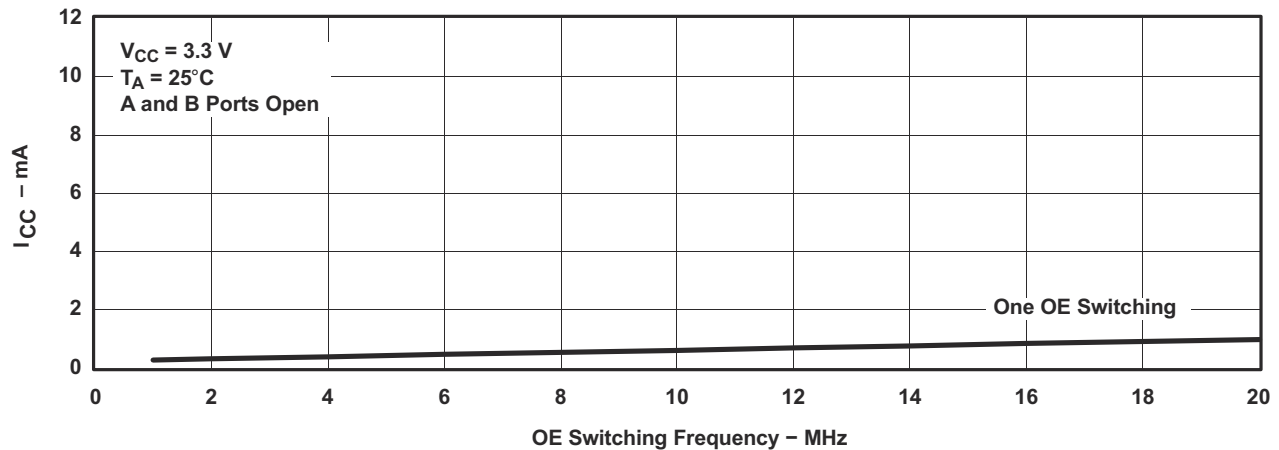


图 9-2. Typical  $I_{CC}$  vs OE Switching Frequency

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in 节 6.1 table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a  $0.1 \mu\text{F}$  bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a  $0.01 \mu\text{F}$  or  $0.022 \mu\text{F}$  capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a  $0.1 \mu\text{F}$  bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of  $0.1 \mu\text{F}$  and  $1 \mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a  $90^\circ$  angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 11.2 Layout Example

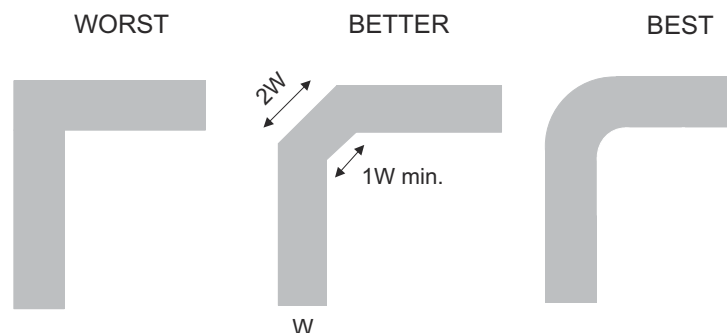


图 11-1. Trace Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [CBT-C, CB3T, and CB3Q Signal-Switch Families application report](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application report](#)
- Texas Instruments, [Selecting the Right Texas Instruments Signal Switch application report](#)

### 12.2 接收文档更新通知

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### 12.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CB3Q3305DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GARR	<a href="#">Samples</a>
SN74CB3Q3305DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(GARQ, GARR)	<a href="#">Samples</a>
SN74CB3Q3305PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	<a href="#">Samples</a>
SN74CB3Q3305PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	<a href="#">Samples</a>
SN74CB3Q3305PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	BU305	<a href="#">Samples</a>
SN74CB3Q3305PWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	<a href="#">Samples</a>
SN74CB3Q3305PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3305PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3305PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
SN74CB3Q3305PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CB3Q3305PW	PW	TSSOP	8	150	530	10.2	3600	3.5
SN74CB3Q3305PWG4	PW	TSSOP	8	150	530	10.2	3600	3.5



# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

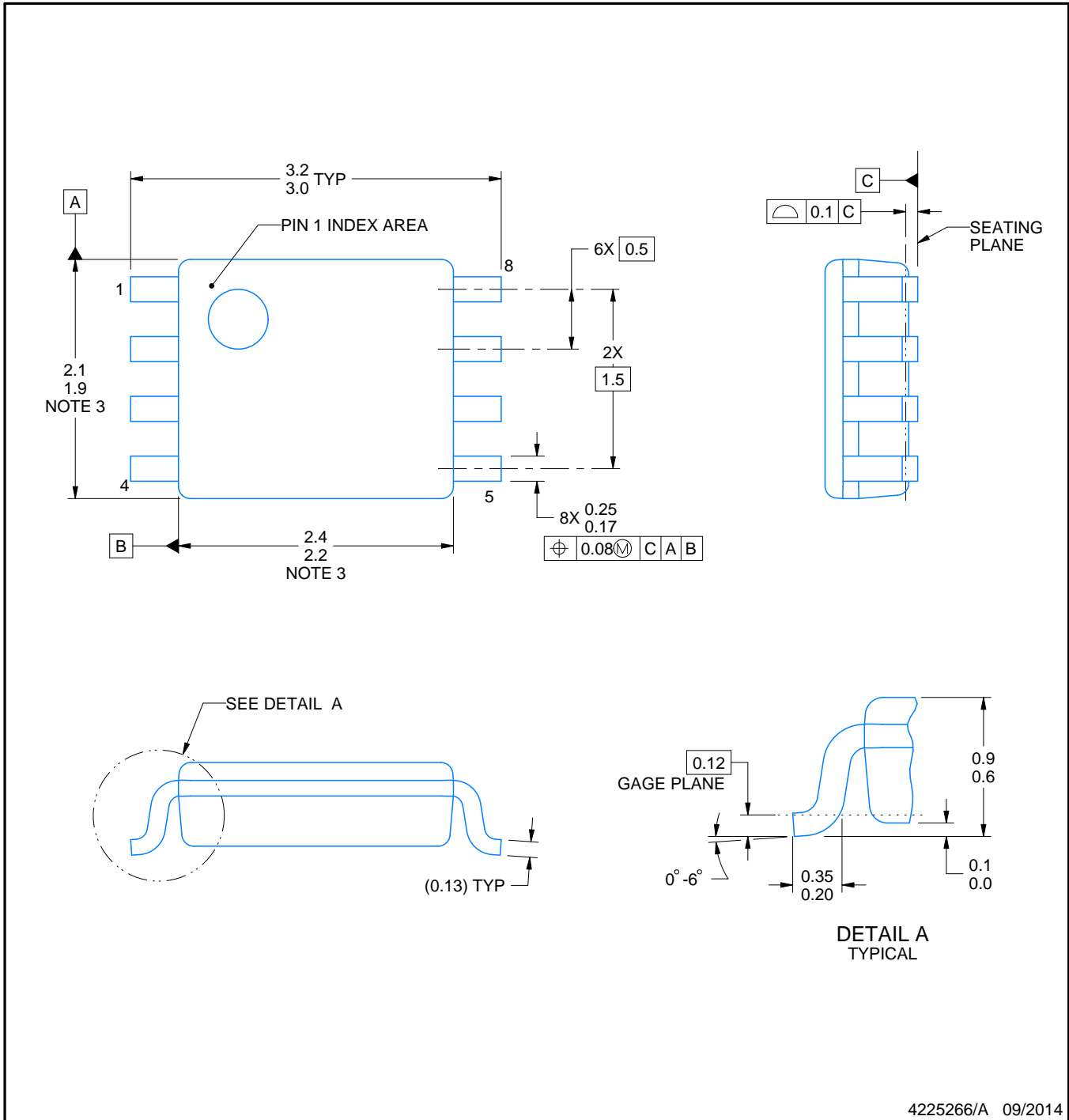
# DCU0008A



# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

**NOTES:**

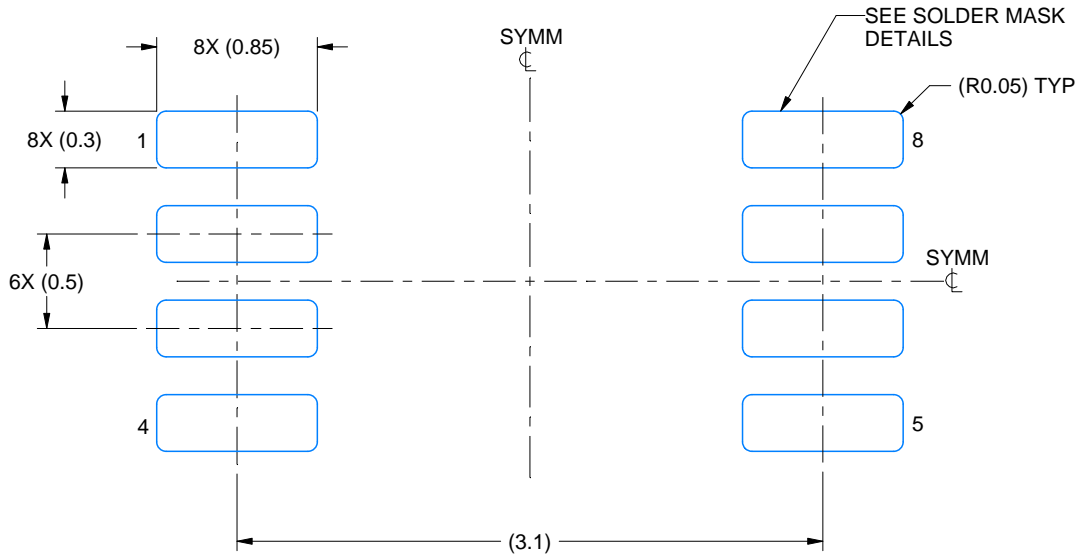
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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