UCC27528-Q1 基于 CMOS 输入阈值逻辑的双通道 5A 高速低侧栅极驱动器

1 特性

- 符合汽车应用要求
- AEC-Q100 器件温度等级 1
- 工业标准引脚分配
- 两个独立的栅极驱动通道
- 5A 峰值供源和吸收驱动电流
- 互补金属氧化物半导体 (CMOS) 输入逻辑阈值（VDD 引脚上的电源电压的函数）
- 实现高抗噪性的滞后逻辑阈值
- 针对每个输出的独立使能功能
- 输入和使能引脚电压电平不受 VDD 引脚偏置电源电压限制
- 4.5V 至 18V 单电源范围
- VDD 欠压闭锁 (UVLO) 期间输出保持低电平（确保加电和断电时无毛刺脉冲运行）
- 快速传播延迟（典型值 17ns）
- 快速上升和下降时间（典型值 7ns 和 6ns）
- 两通道间的延迟匹配时间典型值为 1ns
- 当输入浮动时输出保持低电平
- 小外形尺寸集成电路 (SOIC)-8 封装
- 工作温度范围 -40°C 至 140°C
- 输入引脚具有 -5V 负电压处理能力

2 应用范围

- 汽车
- 开关模式电源
- 直流到直流转换器
- 电机控制，太阳能
- 用于诸如 GaN 等新兴宽带隙电源器件的栅极驱动

3 说明

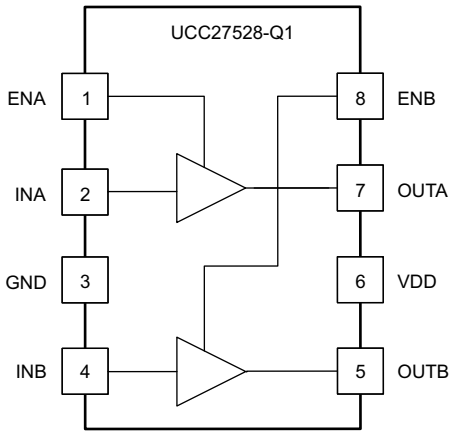
UCC27528-Q1 器件是一款双通道、高速、低侧栅极驱动器，能够高效地驱动金属氧化物半导体场效应晶体管 (MOSFET) 和绝缘栅极型功率管 (IGBT) 电源开关。UCC27528-Q1 器件采用的设计方案可最大程度减少击穿电流，从而为电容负载提供高达 5A 的峰值拉/灌电流脉冲，同时提供轨到轨驱动能力以及超短的传播延迟（典型值为 17ns）。 除此之外，此驱动器特有两个通道间相匹配的内部传播延迟，这一特性使得此驱动器非常适合于诸如同步整流器等对于双栅极驱动有严格计时要求的应用。 输入引脚阈值基于 CMOS 逻辑，此逻辑是 VDD 电源电压的一个函数。 高低阈值间的宽滞后提供了出色的抗噪性。 使能引脚基于 TTL 和 COMS 兼容逻辑，与 VDD 电源电压无关。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC27528-Q1	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

双路非反相输入



目录

4 修订历史记录

Changes from Original (December 2015) to Revision A **Page**

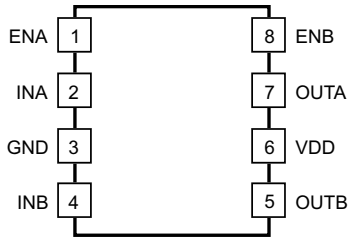
- 已更改 器件状态从 *产品预览* 更改为 *量产数据* 1

5 说明（续）

UCC27528-Q1 是一款双通道同相驱动器。 当输入引脚处于悬空状态时，UCC27528-Q1 器件可通过输入引脚上的内部上拉和下拉电阻确保输出保持在低电平。 UCC27528-Q1 器件特有使能引脚（ENA 和 ENB），能够更好地控制此驱动器应用的运行。 这些引脚内部上拉至 VDD 电源以实现高电平有效逻辑运行，并且可保持断开连接状态以实现标准运行。

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ENA	I	Enable input for Channel A: ENA biased low Disables Channel A output regardless of INA state, ENA biased high or floating Enables Channel A output, ENA allowed to float.
2	INA	I	Input to Channel A: Non-Inverting Input in UCC27528-Q1, OUTA held low if INA is unbiased or floating.
3	GND	—	Ground: All signals referenced to this pin.
4	INB	I	Input to Channel B: Non-Inverting Input in UCC27528-Q1, OUTB held low if INB is unbiased or floating.
5	OUTB	O	Output of Channel B
6	VDD	I	Bias supply input
7	OUTA	O	Output of Channel A
8	ENB	I	Enable input for Channel B: ENB biased low Disables Channel B output regardless of INB state, ENB biased high or floating Enables Channel B output, ENB allowed to float.

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	20	V
INA, INB, voltage(3)		–6.5	20	V
ENA, ENB voltage(3)		–0.3	20	V
OUTA, OUTB voltage	DC	–0.3	VDD + 0.3	V
	Repetitive pulse < 200 ns(4)	–2	VDD + 0.3	
Output continuous source and sink current	I_{OUT_DC}		0.3	A
Output pulsed source and sink current (0.5 µs)	I_{OUT_pulsed}		5	A
Operating virtual junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 s		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) The maximum voltage on the Input and Enable pins is not restricted by the voltage on the VDD pin.
(4) Values are verified by characterization on bench.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	12	18	V
	Input voltage	INA, INB	–5		18	V
	Enable voltage	ENA and ENB	0		18	V
	Operating junction temperature		–40		140	°C

7.4 Thermal Information

THERMAL METRIC(1)		D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	68.5	
ψ_{JT}	Junction-to-top characterization parameter	20.7	
ψ_{JB}	Junction-to-board characterization parameter	68	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{DD} = 12 V, T_A = T_J = –40 °C to 140 °C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal (unless otherwise noted,)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
$I_{DD(off)}$	Startup current	V_{DD} = 3.4 V, INA = VDD, INB = VDD	55	125	225	µA
		V_{DD} = 3.4 V, INA = GND, INB = GND	25	125	225	
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{ON}	Supply start threshold	T_J = 25°C	3.91	4.2	4.5	V
		T_J = –40°C to 140°C	3.75	4.2	4.65	
V_{OFF}	Minimum operating voltage after supply start		3.6	3.9	4.4	
VDD_H	Supply voltage hysteresis		0.2	0.3	0.5	
INPUTS (INA, INB)						
V_{IN_H}	Input signal high threshold	Output high for non-inverting input pins Output low for inverting input pins		55	70	%V_{DD}
V_{IN_L}	Input signal low threshold	Output low for non-inverting input pins Output high for inverting input pins	30	38		
V_{IN_HYS}	Input hysteresis			17		
ENABLE (ENA, ENB)						
V_{EN_H}	Enable signal high threshold	Output enabled	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output disabled	0.95	1.10	1.25	
V_{EN_HYS}	Enable hysteresis		0.7	0.8	1.1	
OUTPUTS (OUTA, OUTB)						
$I_{SNK/SRC}$	Sink and source peak current(1)	C_{LOAD} = 0.22 µF, f_{SW} = 1 kHz		±5		A
V_{DD}–V_{OH}	High output voltage	I_{OUT} = –10 mA			0.075	V
V_{OL}	Low output voltage	I_{OUT} = 10 mA			0.01	
R_{OH}	Output pullup resistance(2)	I_{OUT} = –10 mA	2.5	5	7.5	Ω
R_{OL}	Output pulldown resistance	I_{OUT} = 10 mA	0.15	0.5	1	Ω

(1) Ensured by design.
(2) R_{OH} represents on-resistance of only the P-Channel MOSFET device in pullup structure of UCC27528-Q1 output stage.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	C_{LOAD} = 1.8 nF, V_{DD} = 10 V		7		ns
t_F	Fall time	C_{LOAD} = 1.8 nF, V_{DD} = 10 V		6		ns
t_M	Delay matching between 2 channels	INA = INB, OUTA and OUTB at 50% transition point, V_{DD} = 10 V		1	4	ns
t_{PW}	Minimum input pulse width that changes the output state	V_{DD} = 10 V		15		ns
t_{D1}, t_{D2}	Input to output propagation delay, See Figure 2.	C_{LOAD} = 1.8 nF, 7-V input pulse, V_{DD} = 10 V	6	17	26	ns
t_{D3}, t_{D4}	EN to output propagation delay, See Figure 1 .	C_{LOAD} = 1.8 nF, 7-V enable pulse, V_{DD} = 10 V	6	13	23	ns

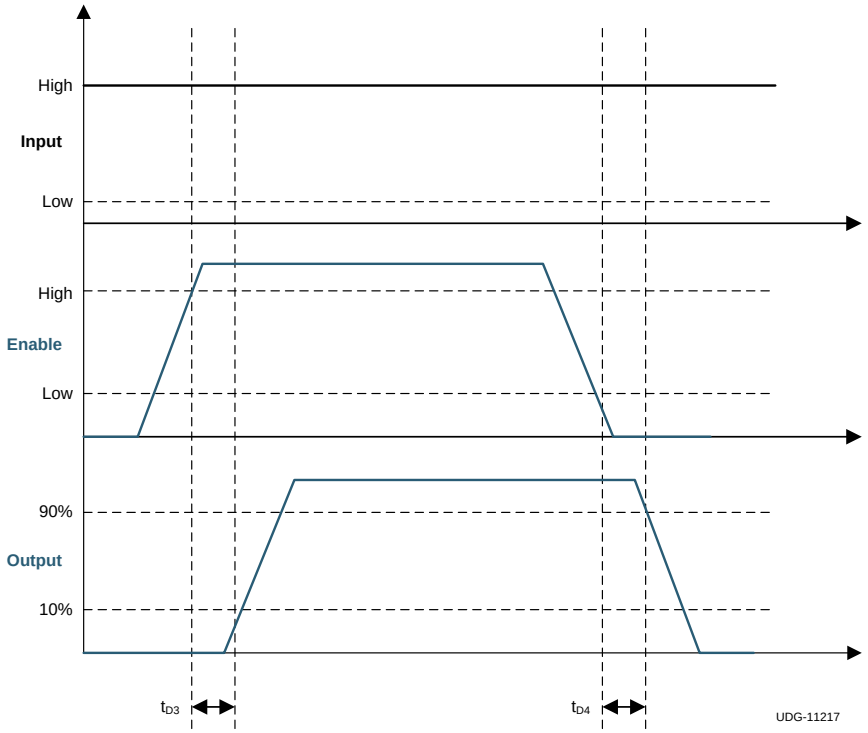


Figure 1. Enable Function
(Non-Inverting Input Driver Operation)

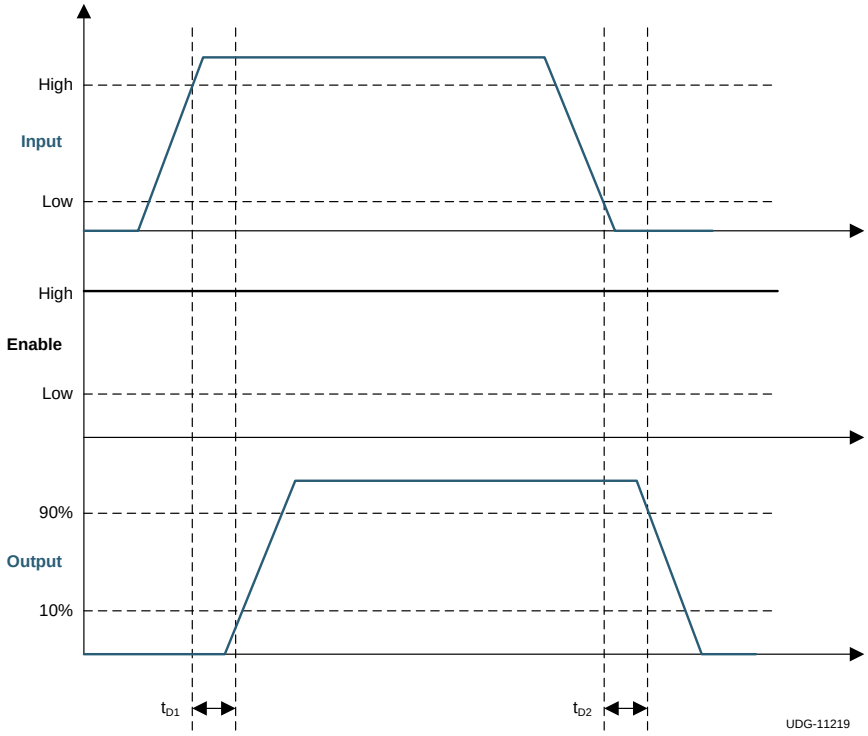


Figure 2. Non-Inverting Input Driver Operation

7.7 Typical Characteristics

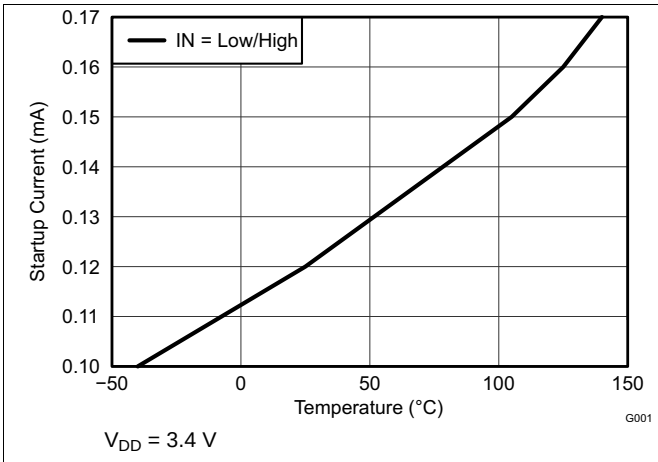


Figure 3. Startup Current vs Temperature

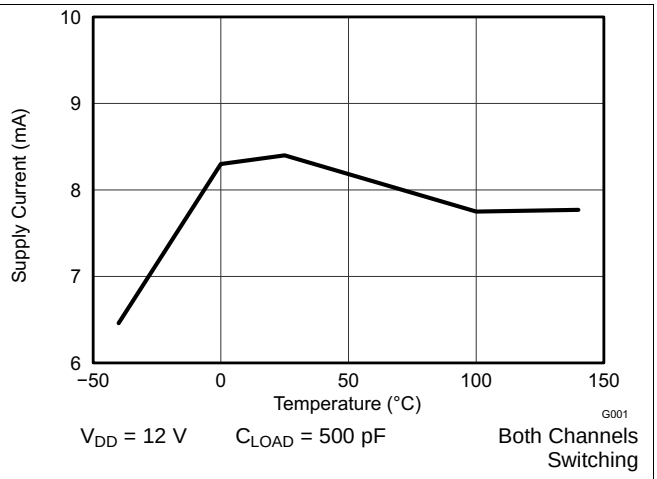


Figure 4. Operating Supply Current vs Temperature (Outputs Switching)

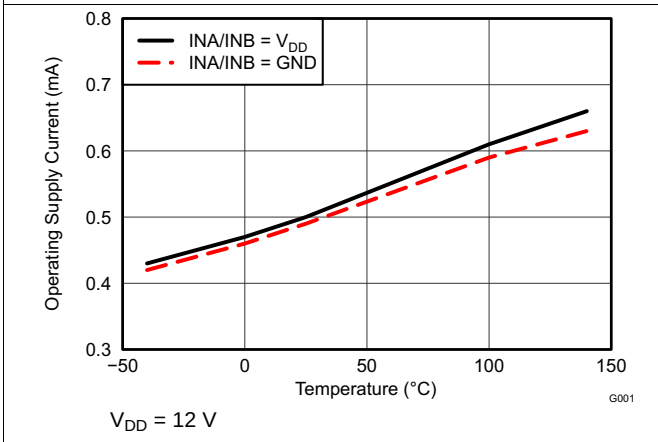


Figure 5. Supply Current vs Temperature (Outputs In DC On/Off Condition)

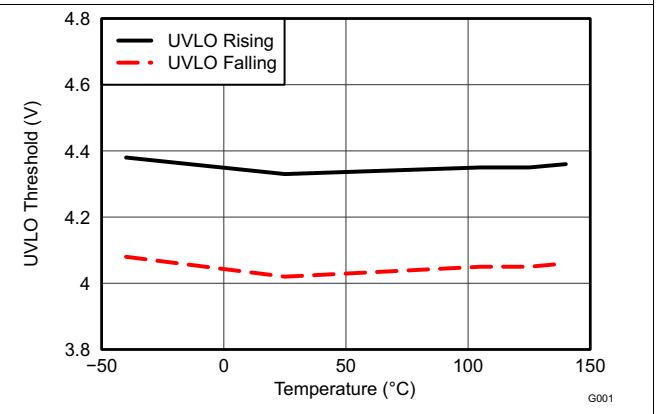


Figure 6. UVLO Threshold vs Temperature

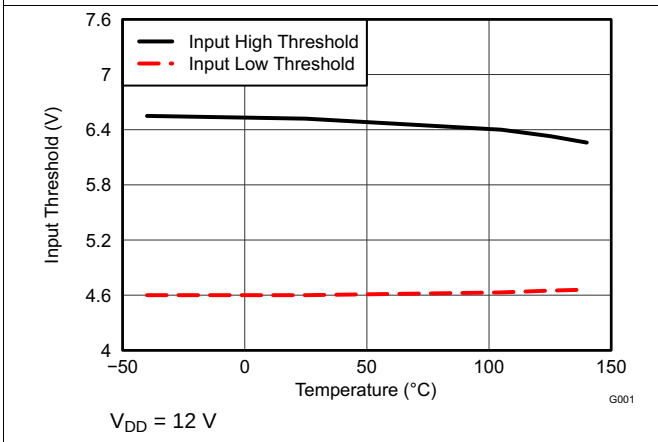


Figure 7. Input Threshold vs Temperature

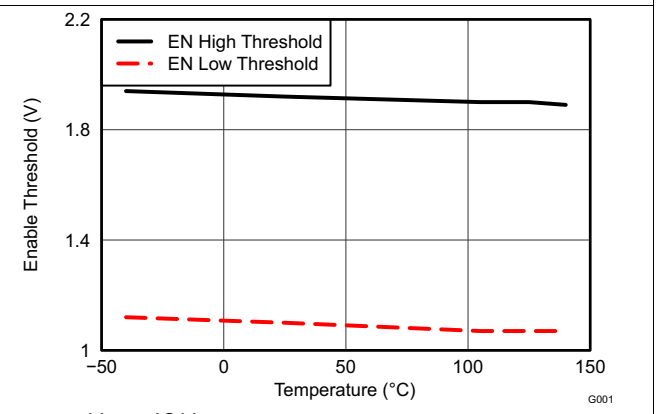
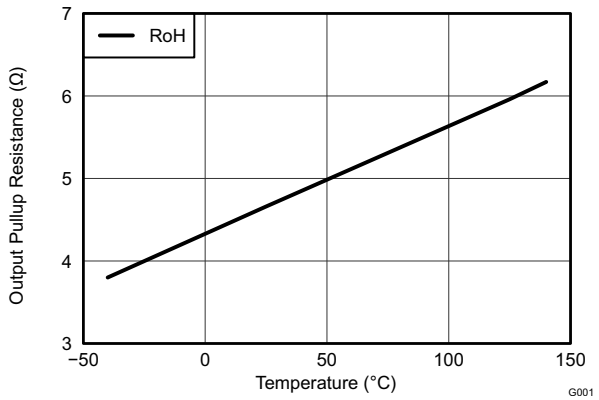


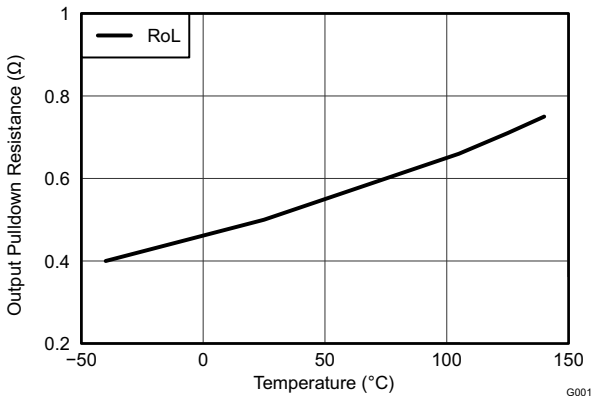
Figure 8. Enable Threshold vs Temperature

Typical Characteristics (continued)



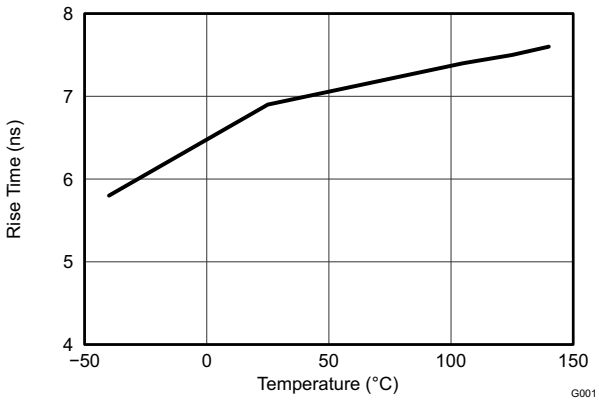
V_{DD} = 12 V I_{OUT} = 10 mA

Figure 9. Output Pullup Resistance vs Temperature



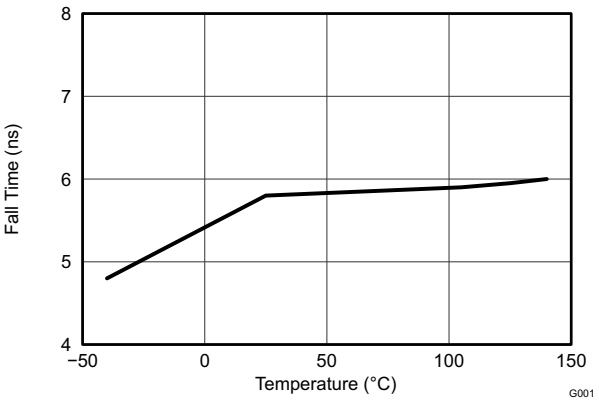
V_{DD} = 12 V I_{OUT} = 10 mA

Figure 10. Output Pulldown Resistance vs Temperature



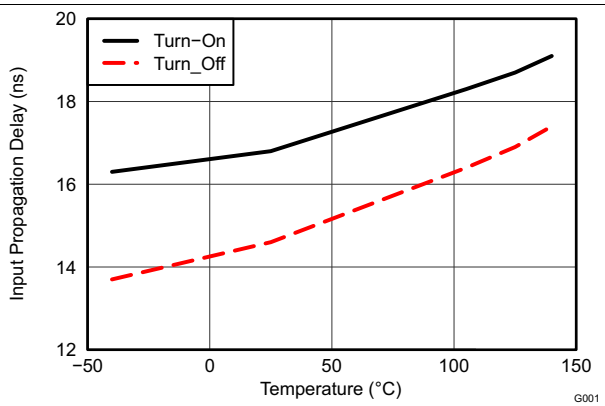
V_{DD} = 10 V C_{LOAD} = 1.8 nF

Figure 11. Rise Time vs Temperature



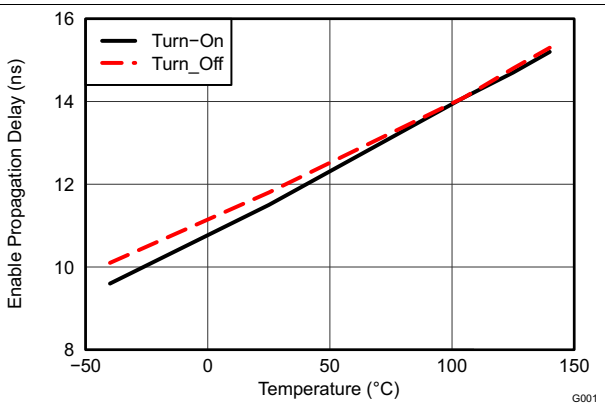
V_{DD} = 10 V C_{LOAD} = 1.8 nF

Figure 12. Fall Time vs Temperature



V_{DD} = 10 V

Figure 13. Input To Output Propagation Delay vs Temperature



V_{DD} = 10 V

Figure 14. En To Output Propagation Delay vs Temperature

Typical Characteristics (continued)

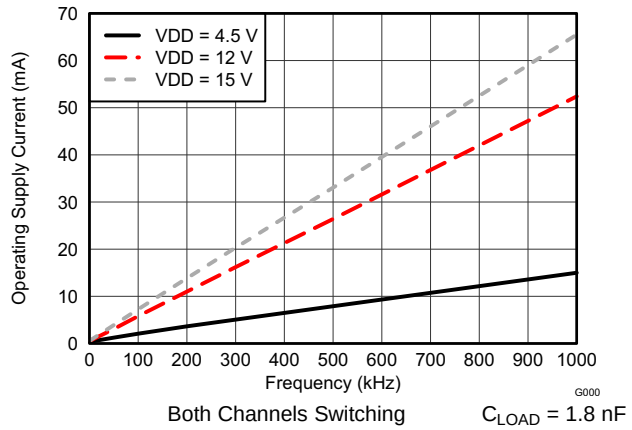


Figure 15. Operating Supply Current vs Frequency

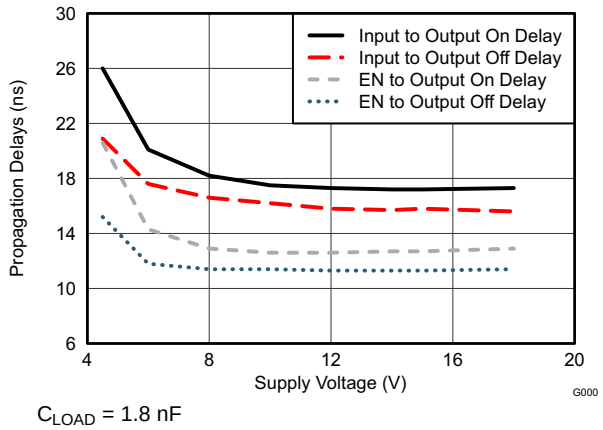


Figure 16. Propagation Delays vs Supply Voltage

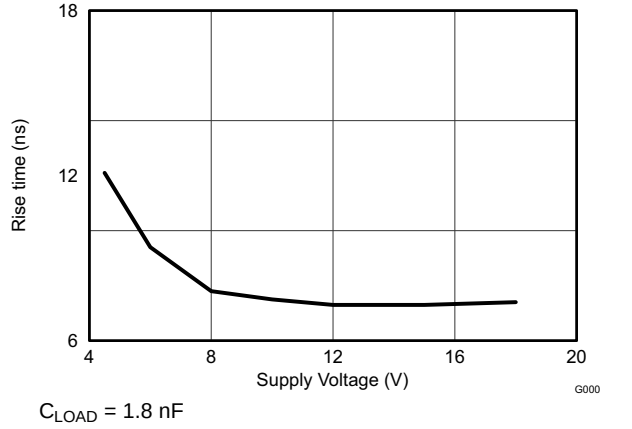


Figure 17. Rise Time vs Supply Voltage

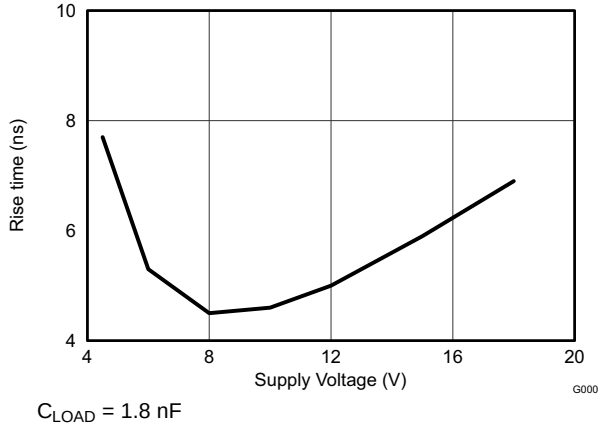


Figure 18. Fall Time vs Supply Voltage

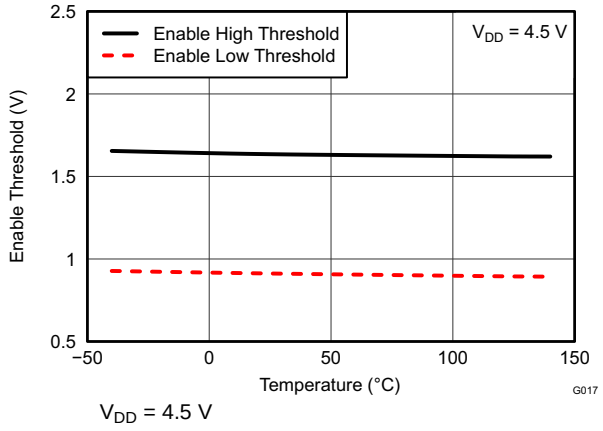


Figure 19. Enable Threshold vs Temperature

8 Detailed Description

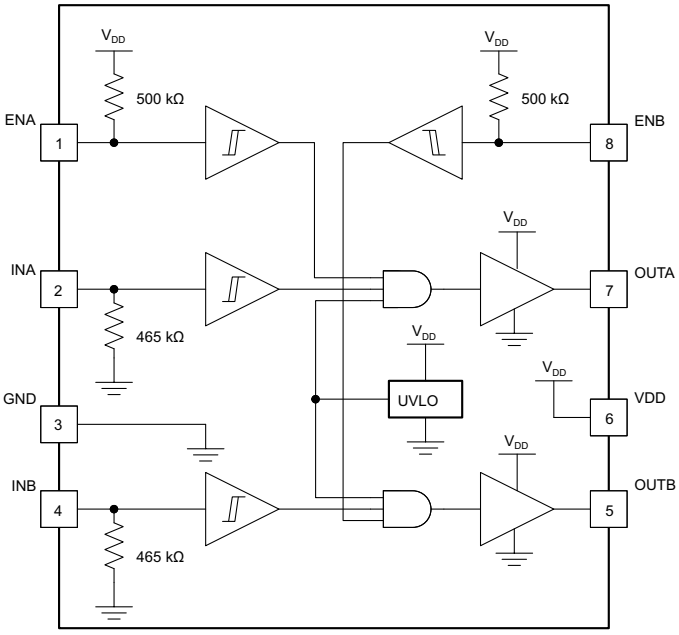
8.1 Overview

The UCC27528-Q1 device represents Texas Instruments' latest generation of dual-channel, low-side high-speed gate driver devices featuring 5-A source- and sink current capability, industry best-in-class switching characteristics, and many other features listed in Table 1 all of which combine to provide efficient, robust, and reliable operation in high-frequency switching power circuits.

Table 1. UCC27528-Q1 Features and Benefits

FEATURE	BENEFIT
Best-in-class 13-ns (typical) propagation delay	Extremely low pulse-transmission distortion
1-ns (typical) delay matching between channels	Ease of paralleling outputs for higher (2×) current capability, ease of driving parallel power switches
Expanded VDD operating range of 4.5 V to 18 V	Flexibility in system design
Expanded operating temperature range of –40 °C to 140 °C (See the *Electrical Characteristics* table)	
VDD UVLO protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power up and power down
Outputs held low when the input pins (INx) are in floating condition	Feature which is specifically useful in passing abnormal condition tests during certification
Outputs enabled when the enable pins (ENx) are in floating condition	Pin-to-pin compatibility with the UCC2732x family of device from TI, in designs where pin 1 and pin 8 are in the floating condition
CMOS input threshold logic	Enhanced noise immunity, higher threshold leve,l and wider hysteresis which is a function of the VDD supply voltage and ability to employ RCD delay circuits on input pins.
The input and enable pins are able to handle voltage levels not restricted by VDD pin bias voltage	System simplification, specifically related to auxiliary bias supply architecture

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 V_{DD} and Undervoltage Lockout

The UCC27528-Q1 device has internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply-circuit blocks. When the VDD supply is rising and the level is still below UVLO threshold, the circuit (as shown in the *Functional Block Diagram*) holds the output low, regardless of the status of the inputs. The UVLO threshold is 4.25 V (typical) with 350-mV hysteresis (typical). This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when droops in the VDD bias voltage occur when the system commences switching and a sudden increase in the I_{DD} current occurs. The ability to operate at low-voltage levels, such as below 5 V, along with best-in-class switching characteristics, is well suited for driving emerging GaN-power semiconductor devices.

For example, at power-up, the UCC27528-Q1 driver device output remains low until the V_{DD} voltage reaches the UVLO threshold if the enable pin is active or floating. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. The non-inverting operation in Figure 20 shows that the output remains low until the UVLO threshold is reached. The output is then in-phase with the input.

Because the device draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, to help deliver the high-current peaks required by the load, a larger capacitor (such as a 1-µF capacitor) with relatively low ESR should be connected in parallel and close proximity. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

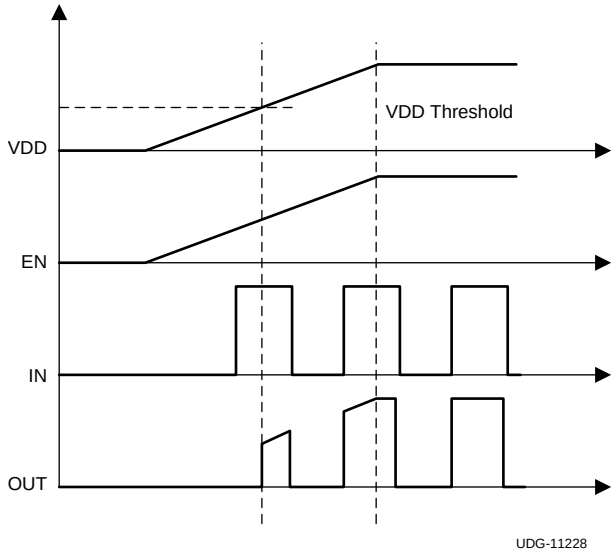


Figure 20. Power-Up Non-Inverting Driver

8.3.2 Operating Supply Current

The UCC27528-Q1 device features very low quiescent I_{DD} currents. Figure 3, Figure 4, and Figure 5 list the typical operating supply current in the UVLO state and fully-on state (under static and switching conditions). The I_{DD} current that is present when the device is fully on and the outputs are in a static state (DC high or DC low, see Figure 4) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current from switching, and any current related to pullup resistors on the enable pins and inverting input pins.

Figure 15 shows a complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load in both channels. The strikingly linear variation and close correlation with the theoretical value of the average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to the high-speed characteristics.

8.3.3 Input Stage

The input pins of UCC27528-Q1 gate driver device are based on CMOS input threshold logic. In CMOS input threshold logic the threshold voltage level is a function of the bias voltage on the VDD pin of the device. The typical high threshold is 55% of the VDD supply voltage and the typical low threshold is 38% of the VDD supply voltage. Built-in hysteresis is available which is typically 17% of the VDD supply voltage.

In most applications, the absolute value of the threshold voltage offered by the CMOS logic is higher (for example, V_{IN_H} = 5.5 V if V_{DD} = 10 V) than what is offered by the more common TTL and CMOS-compatible input threshold logic where V_{IN_H} is typically less than 3 V. The same is true of the input-threshold hysteresis parameter as well. This feature offers the following benefits:

- Better noise immunity which is desirable in high power systems.
- Ability to accept slow dV/dt input signals, which allows designers to use RCD circuits on the input pin to program propagation delays in the application, as shown in Figure 21.

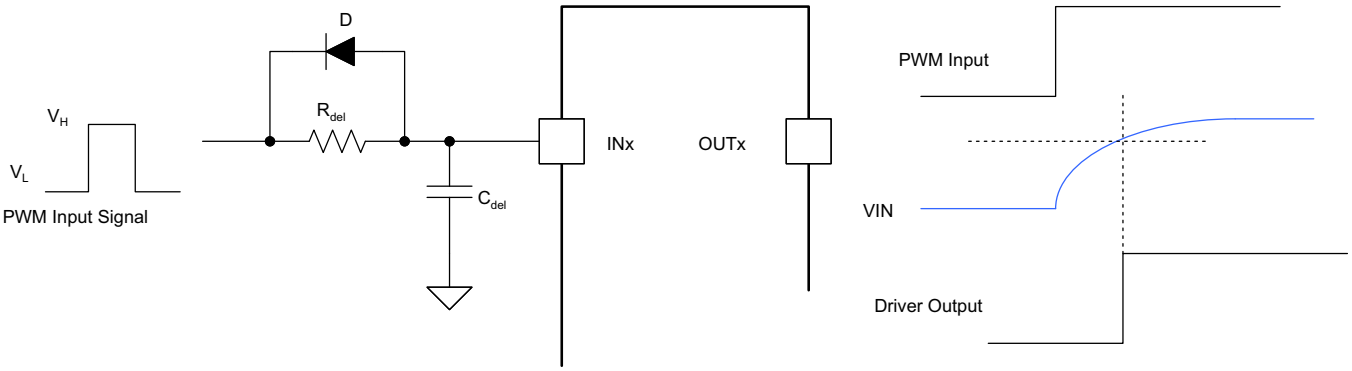


Figure 21. Using RCD Circuits

$$t_{del} = -R_{del}C_{del} \times \ln\left(\frac{V_L - V_{IN\_H}}{V_H - V_L} + 1\right) \quad (1)$$

The UCC27528-Q1 device features an important feature, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. Holding the respective channel in the low state is achieved by using GND pulldown resistors on all the non-inverting input pins (INA, INB), as shown in the *Functional Block Diagram*.

- To drive channel x (x = A or B) in a non-inverting configuration, apply the PWM control input signal to one of the IN pins. In this case, the unused IN pin must be biased low (for example, tied to GND) to enable the output of this channel.
  - Alternately, the unused IN pin can be used to implement the enable and disable function using an external logic signal. The output pin is disabled when the unused IN pin is biased high and the OUT pin is enabled when the unused IN pin is biased low.

See Table 2 and Figure 24 for additional clarification.

8.3.4 Enable Function

The enable function is an extremely beneficial feature in gate driver devices, especially for certain applications such as synchronous rectification where the driver outputs can be disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27528-Q1 device has independent enable pins, ENx, for exclusive control of the operation of each driver channel. The enable pins are based on a non-inverting configuration (active-high operation). Therefore, when the ENx pins are driven high the drivers are enabled and when ENx pins are driven low and the drivers are disabled. Similar to the input pins, the enable pins are also based on a TTL and CMOS-compatible input threshold logic that is independent of the supply voltage and can be effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The UCC27528-Q1 device also features tight control of the enable-function threshold voltage levels which eases system design considerations and ensures stable operation across temperature (see Figure 8). The ENx pins are internally pulled up to the VDD supply using pullup resistors as a result of which the outputs of the device are enabled in the default state. Therefore, the ENx pins can be left

floating or not connected (NC) for standard operation in which case the enable feature is not needed. This ability allows the UCC27528-Q1 device to be pin-to-pin compatible with TI's previous-generation drivers, the UCC27323, UCC273234, and UCC273235 device, where pin 1 and pin 8 are NC pins. If the Channel A and Channel B inputs and outputs are connected in parallel to increase the driver current capacity, the ENA and ENB pins should be connected and driven together.

8.3.5 Output Stage

The UCC27528-Q1 output stage features a unique architecture on the pullup structure which delivers the highest-peak source current when it is most needed during the Miller plateau region of the power-switch turn-on transition (when the power switch drain and collector voltage experiences dV/dt). The output-stage pullup structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The N-Channel MOSFET provides a brief boost in the peak sourcing current which enables fast turn-on. This boost is accomplished by briefly turning on the N-Channel MOSFET during a short time frame when the output is changing state from low to high.

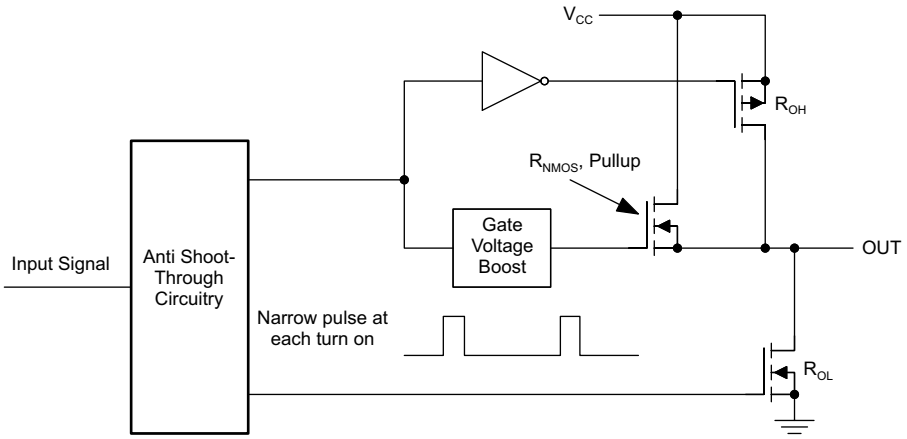


Figure 22. UCC27528-Q1 Gate Driver Output Structure

The R_{OH} parameter (see the *Electrical Characteristics* table) is a DC measurement and is representative of the on-resistance of the P-Channel device only because the N-Channel device is held in the off state in DC condition and is turned on only for a short time frame when the output changes state from low to high. Therefore, the effective resistance of UCC27528-Q1 pullup stage during turn-on instant is much lower than what is represented by R_{OH} parameter.

The pulldown structure in the UCC27528-Q1 device is simply composed of a N-Channel MOSFET. The R_{OL} parameter (see the *Electrical Characteristics* table), which is also a DC measurement, is representative of the impedance of the pulldown stage in the device. In the UCC27528-Q1 device, the effective resistance of the hybrid pullup structure during turnon is estimated on design considerations as approximately 1.5 × R_{OL}.

Each output stage in the UCC27528-Q1 device is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND, providing rail-to-rail operation because of the MOS output stage which delivers very-low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots which means that in many cases, external Schottky diode clamps can be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

The UCC27528-Q1 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by the OUTA and OUTB pins, with the inputs INA and INB driven complementary to each other. The device is well suited for these applications because of the extremely low dropout offered by the MOS output stage of the device, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

8.3.6 Low Propagation Delays and Tightly Matched Outputs

The UCC27528-Q1 driver devices offer a very low propagation delay of 17-ns (typical) between input and output which offers lowest level of pulse transmission distortion available in the industry for high-frequency switching applications. For example in synchronous rectifier applications, the SR MOSFETs can be driven with very low distortion when a single driver device is used to drive both the SR MOSFETs. Further, the driver devices also feature an extremely accurate, 1-ns (typ) matched internal propagation delays between the two channels which is beneficial for applications requiring dual gate drives with critical timing. For example in a PFC application, a pair of paralleled MOSFETs may be driven independently using each output channel, which the inputs of both channels are driven by a common control signal from the PFC controller device. In this case the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion with the minimum of turn-on delay difference.

Since the CMOS input threshold of UCC27528-Q1 allows the use of slow dV/dt input signals, when paralleling outputs for obtaining higher peak output current capability, it is recommended to connect external gate resistors directly to the output pins to avoid shoot-through current conduction between the 2 channels, as shown in Figure 23. While the two channels are inherently very well matched (4-ns Max propagation delay), it should be noted that there may be differences in the input threshold voltage level between the two channels or differences in the input signals which can cause the delay between the two outputs.

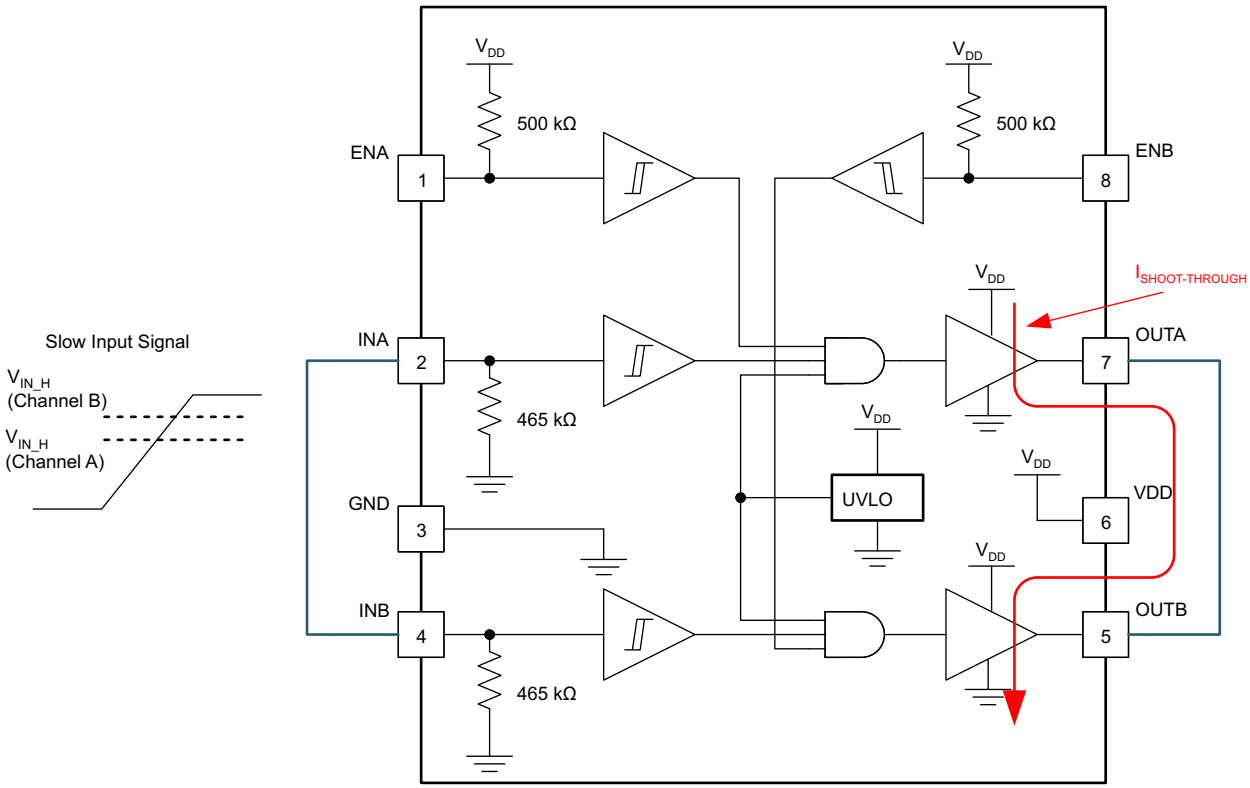


Figure 23. Slow Input Signal May Cause Shoot-Through Between Channels During Paralleling

8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *V_{DD} and Undervoltage Lockout* section for information on the UVLO operation mode. In the normal mode the output state is dependent on the state of the IN pins. Table 2 lists the output states for different input-pin combinations.

Table 2. Device Logic Table

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x(1)	x(1)	L	L
x(1)	x(1)	L	L	L	L
x(1)	x(1)	L	H	L	H
x(1)	x(1)	H	L	H	L
x(1)	x(1)	H	H	H	H

(1) Floating condition

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. To implement fast switching in power devices and reduce associated switching power losses, a powerful gate-driver device can be employed between the PWM output of control devices and the gates of the power semiconductor devices.

Furthermore, gate driver devices are indispensable when having the PWM-controller device directly drive the gates of the switching devices is not feasible. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is typically a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar transistors in totem-pole arrangement are emitter follower configurations. These circuits prove inadequate with digital power because they lack level-shifting capability.

Gate driver devices effectively combine both the level-shifting and buffer drive functions. Gate driver devices also satisfy other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate drive transformers and controlling floating power device gates which reduces power dissipation and thermal stress in controller devices by moving gate charge power losses into itself. In summary Gate-driver devices are an extremely important component in switching power combining benefits of high performance, low cost, component count, board-space reduction, and simplified system design.

9.2 Typical Application

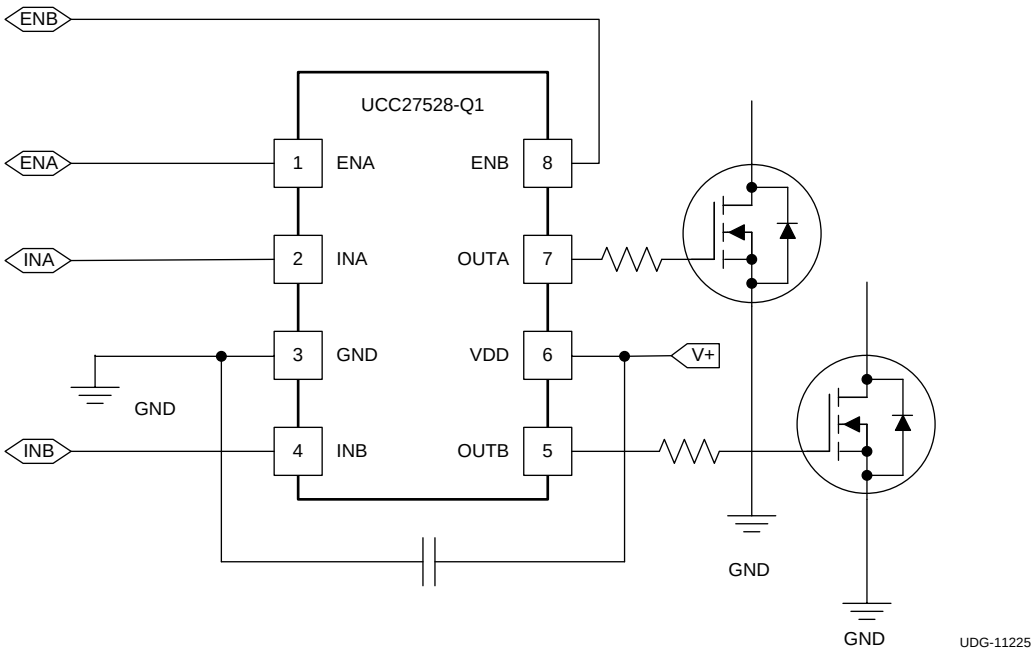


Figure 24. UCC27528-Q1 Typical Application Diagram

Typical Application (continued)

9.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are input-to-output Logic, enable and disable function, supply voltage (VDD), propagation delay, and power dissipation.

The design requirements include the following:

- Supply voltage (V_{DD})
- Type of input threshold (CMOS or TTL)
- Propagation delay
- Delay matching
- Peak drive current
- Enable function (whether or not it exists)
- Operating temperature range

9.2.2 Detailed Design Procedure

9.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. The UCC27528-Q1 device can only provide dual non-inverting input-to-output with enable control.

9.2.2.2 Enable and Disable Function

Certain applications demand independent control of the output state of the driver. The UCC27528-Q1 device offers two independent enable pins ENx pins for exclusive control of each driver channels as listed in Table 2. The ENA, ENB pins in the UCC27528-Q1 device can be in the floating condition during standard operation with the outputs enabled.

9.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the *Recommended Operating Conditions* table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC27528-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs (for example, V_{GS} = 4.5 V, 10V, 12 V), IGBTs (V_{GE} = 15 V, 18 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate pins).

9.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27528-Q1 device features fast 17-ns (typical) propagation delays which ensures very-little pulse distortion and allows operation at very high-frequencies. See the *Switching Characteristics* table for the propagation and switching characteristics of the UCC27528-Q1 device. For certain application that require programmable propagation delay, The UCC27528-Q1 device can accept slow dv/dt input signals which allows designers to use RCD circuits on the input pin to program propagation as shown in Figure 21.

Typical Application (continued)

9.2.2.5 Drive Current and Power Dissipation

The UCC27528-Q1 driver device is capable of delivering 5 A of current to a MOSFET gate for a period of several hundred nanoseconds at V_{DD} = 12 V. High peak current is required to quickly turn on the device. Then, to turn off the device, the driver is required to sink a similar amount of current to ground. This process repeats at the operating frequency of the power device. The power dissipated in the gate-driver device package depends on the following factors:

- The gate charge required of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} because of low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

Because the UCC27528-Q1 device features very-low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, the effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load, calculating the power that is required from the bias supply fairly simple. Use Equation 2 to calculate the energy that must be transferred from the bias supply to charge the capacitor.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \quad (2)$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver

An equal amount of energy is dissipated when the capacitor is charged which leads to a total power loss given by Equation 3.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \quad (3)$$

where

- f_{SW} is the switching frequency

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f_{SW} = 300 kHz, use Equation 4 to calculate the power loss.

$$P_G = 10\ \text{nF} \times 12\ \text{V}^2 \times 300\ \text{kHz} = 0.432\ \text{W} \quad (4)$$

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge required to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Use the gate charge Q_g to determine the power that must be dissipated when charging a capacitor by using the equivalence $Q_g = C_{LOAD} V_{DD}$ to provide Equation 5 for power.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (5)$$

Assuming that the UCC27528-Q1 device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, use Equation 6 to calculate the gate-charge related power loss.

$$P_G = 2 \times 60\ \text{nC} \times 12\ \text{V} \times 300\ \text{kHz} = 0.432\ \text{W} \quad (6)$$

This power, P_G, is dissipated in the resistive elements of the circuit when the MOSFET is turned on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET or IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, use Equation 7 to calculate the driver power dissipation during switching.

Typical Application (continued)

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pullup structure) = 1.5 × R_{OL} (7)

In addition to the previously calculated gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits, such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. Referring to Figure 4, the quiescent current is less than 0.6 mA even in the highest case. Use Equation 8 to calculate the quiescent power dissipation.

$$P_Q = I_{DD} V_{DD} \quad (8)$$

Assuming, I_{DD} = 6 mA, use Equation 9 to calculate the power loss.

$$P_Q = 0.6\ \text{mA} \times 12\ \text{V} = 7.2\ \text{mW} \quad (9)$$

Clearly, this power loss is insignificant compared to gate-charge related power dissipation that was calculated previously.

With a 12-V supply, the bias current can be estimated as shown in Equation 10, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ \text{W}}{12\ \text{V}} = 0.036\ \text{A} \quad (10)$$

9.2.3 Application Curves

V_{DD} = 5 V, Load = 2 RJK0453DPB (power FET)

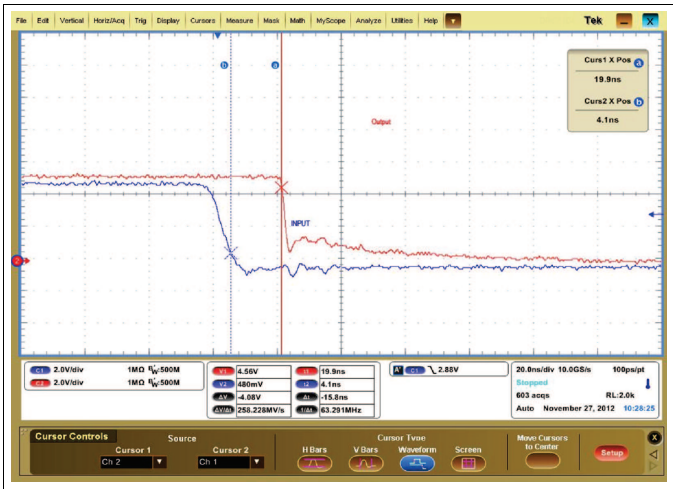


Figure 25. Typical Turnon Waveform

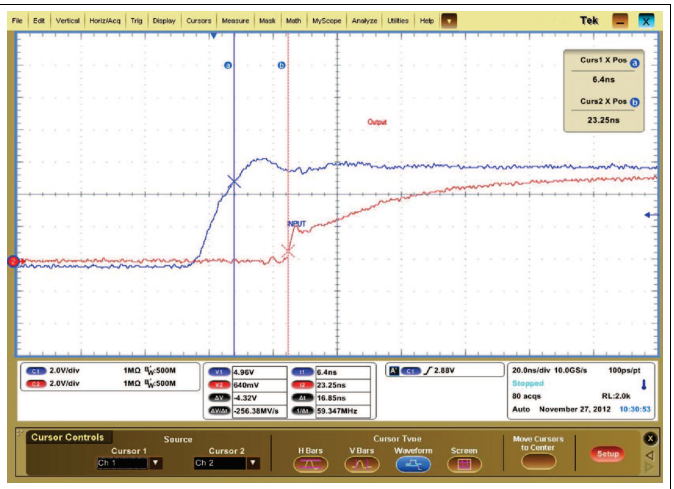


Figure 26. Typical Turnoff Waveform

10 Power Supply Recommendations

The bias supply voltage range for which the UCC27528-Q1 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the V_{ON} supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute-maximum voltage rating of the VDD pin of the device (which is a stress rating). Maintaining a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This hysteresis function means that when the VDD pin bias voltage exceeds the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification, VDD_H. Therefore, ensuring that, while operating at or near the 4.2-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the V_{OFF} threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the VDD pin voltage has exceeded above the V_{ON} threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA or OUTB pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is a must. TI recommends having 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

11 Layout

11.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27528-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very-fast rise and fall times at the gate of the power MOSFET to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (5-A peak current is at V_{DD} = 12 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers:

- Locate the driver device as close as possible to power device to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between the VDD and GND pins as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support the high peak current that is drawn from the VDD pin during turn-on of power MOSFET. The use of low inductance SMD components, such as chip resistors and chip capacitors, is highly recommended.
- The turn-on and turn-off current-loop paths (driver device, power MOSFET, and VDD bypass capacitor) should be minimized as much as possible to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances: during turn-on transients and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power MOSFET.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as the source of power MOSFET, the ground of PWM controller, and other sources at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at the OUTx pin may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation.

11.2 Layout Example

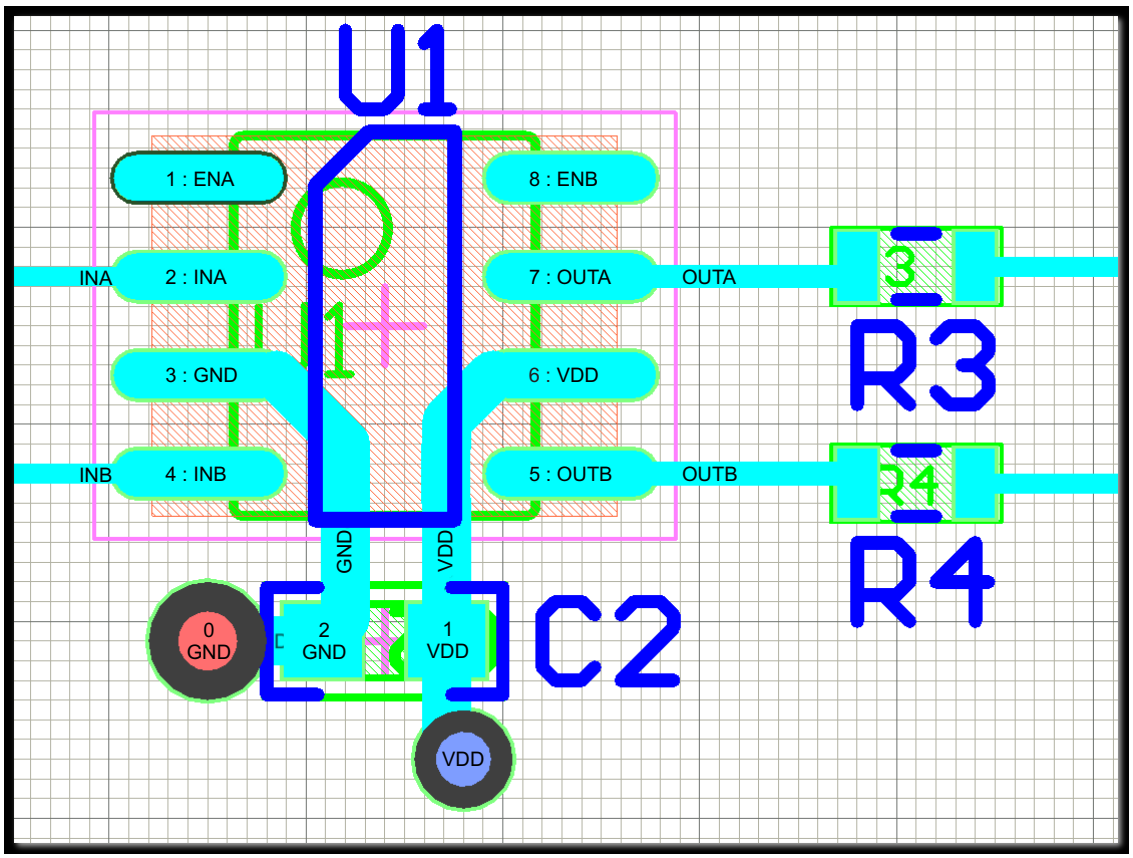


Figure 27. Layout Example for UCC27528-Q1

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits.

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27528QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27528Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

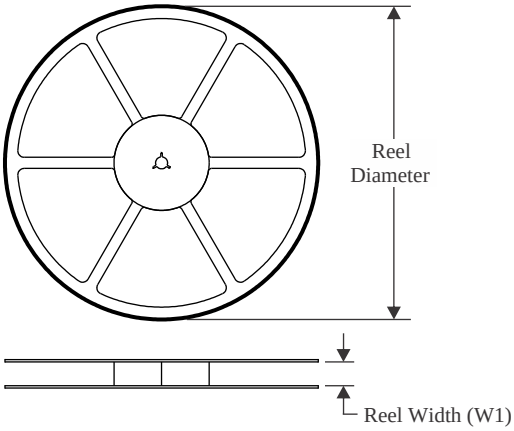
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

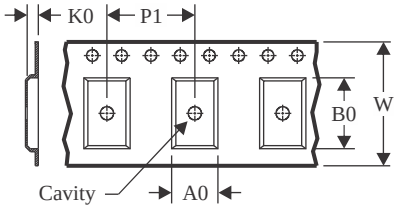
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

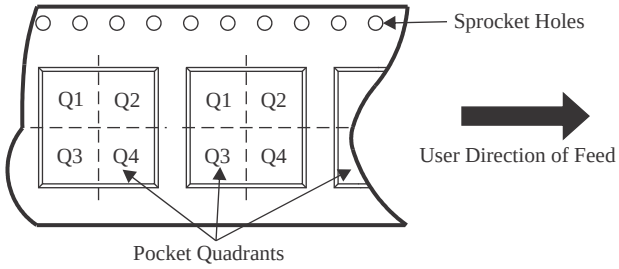


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

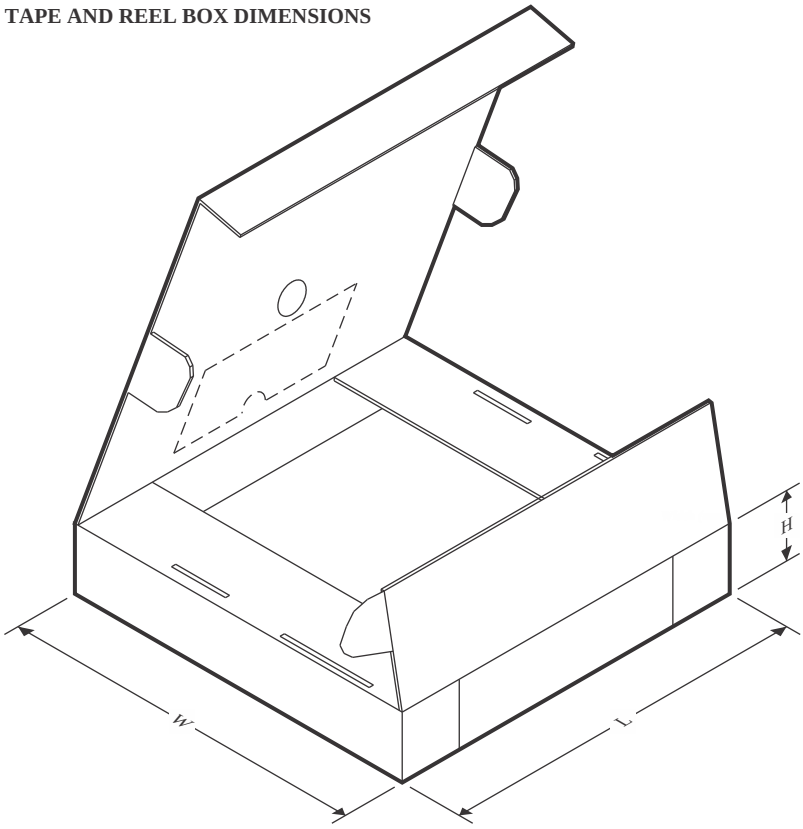
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

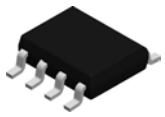
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27528QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27528QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

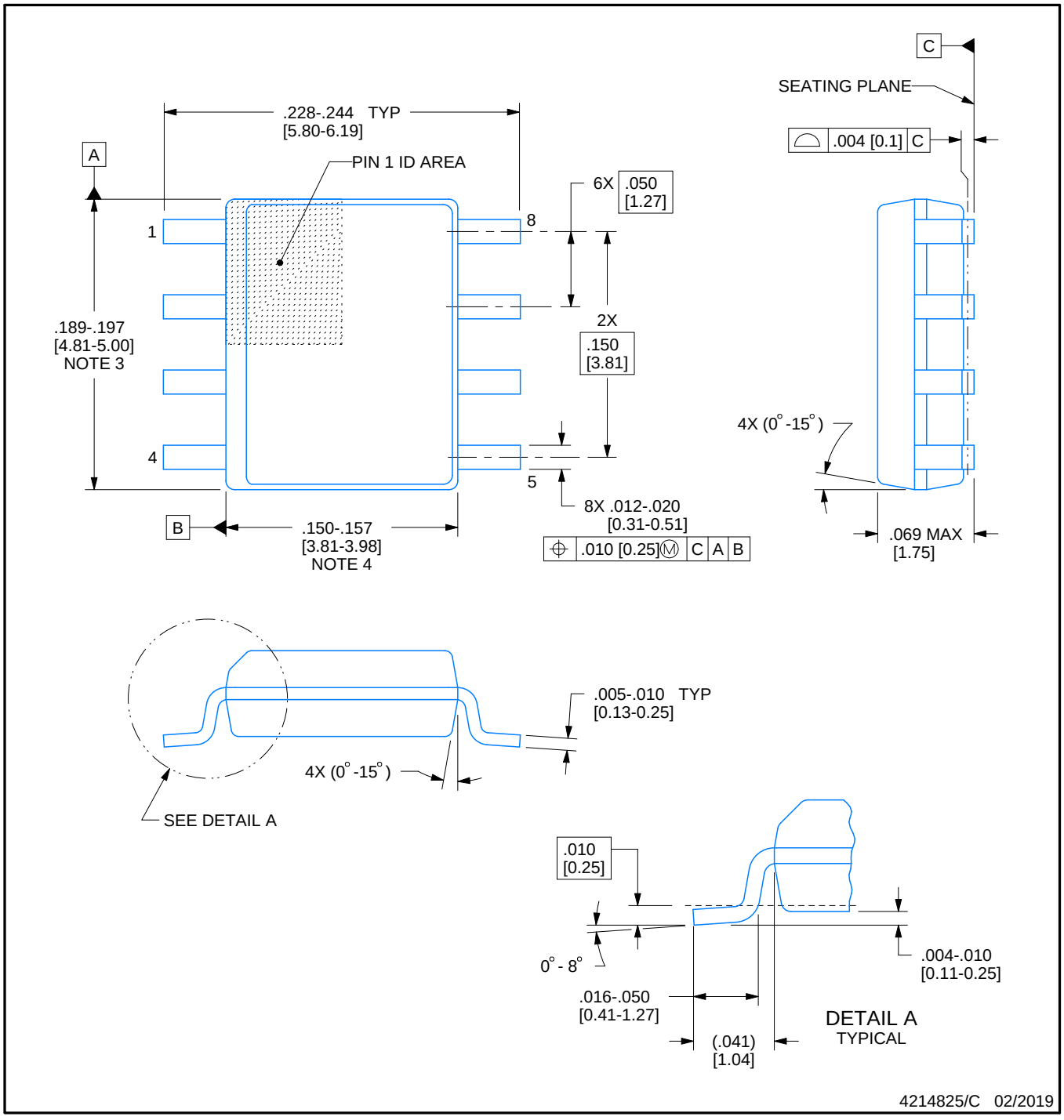


PACKAGE OUTLINE

D0008A

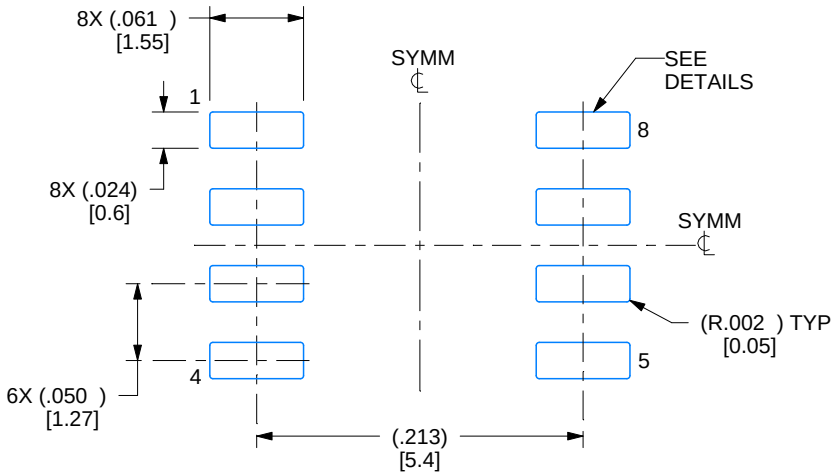
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

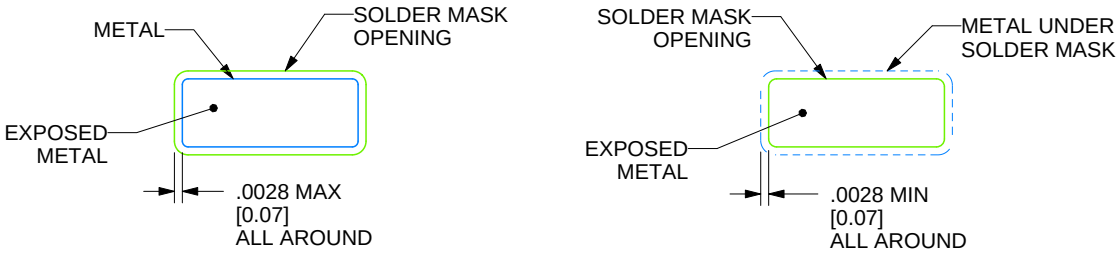


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

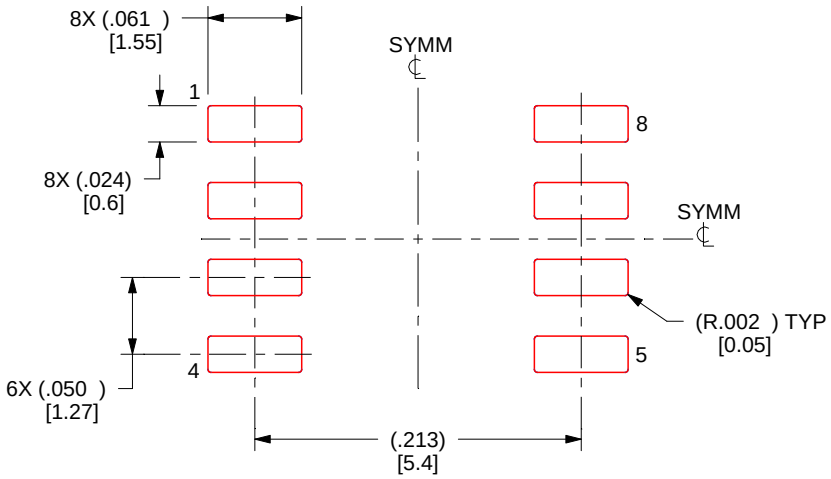
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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