LM4940 Boomer® Audio Power Amplifier Series 6W Stereo Audio Power Amplifier

Check for Samples: LM4940

FEATURES

- **Click and Pop Circuitry Eliminates Noise During Turn-On and Turn-Off Transitions**
- **Low Current, Active-Low Shutdown Mode**
- **Low Quiescent Current**
- **Stereo 6W Output, R_L = 4Ω**
- **Short Circuit Protection**
- **Unity-Gain Stable**
- **External Gain Configuration Capability**

APPLICATIONS

- **Flat Panel Monitors**
- **Flat Panel TVs**
- **Computer Sound Cards**

KEY SPECIFICATIONS

- **Quiescent Power Supply Current: 40mA (max) (SE)**
- **P_{OUT}**
  V_{DD} = 14.4V, R_L = 4Ω, 10% THD+N: 6 W (typ)
- **Shutdown Current: 40µA (typ)**

DESCRIPTION

The LM4940 is a dual audio power amplifier primarily designed for demanding applications in flat panel monitors and TVs. It is capable of delivering 6 watts per channel to a 4Ω load with less than 10% THD+N while operating on a 14.4V_{DC} power supply.

Boomer™ audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4940 does not require bootstrap capacitors or snubber circuits. Therefore, it is ideally suited for display applications requiring high power and minimal size.

The LM4940 features a low-power consumption active-low shutdown mode. Additionally, the LM4940 features an internal thermal shutdown protection mechanism along with short circuit protection.

The LM4940 contains advanced pop and click circuitry that eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4940 is a unity-gain stable and can be configured by external gain-setting resistors.

TYPICAL APPLICATION

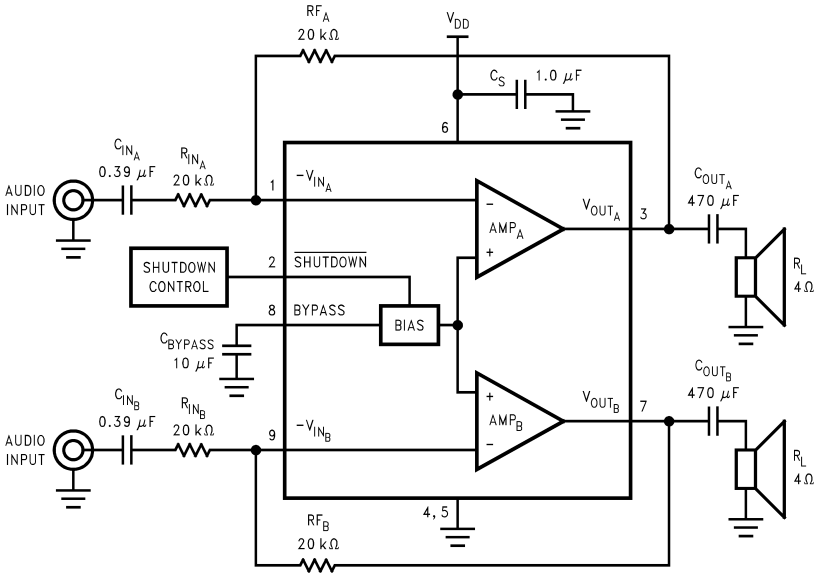

Figure 1. Typical Stereo Audio Amplifier Application Circuit

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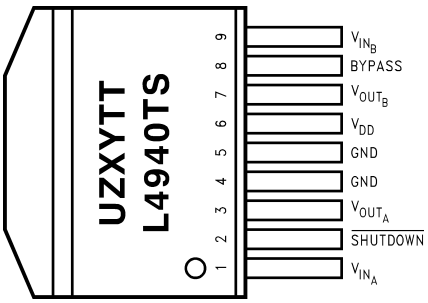
CONNECTION DIAGRAM



U = Wafer Fab Code, Z = Assembly Plant Code, XY = Date Code, TT = Die Traceability

Plastic Package, DDPAK
Top View
See Package Number KTW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Supply Voltage (pin 6, referenced to GND, pins 4 and 5)		18.0V
Storage Temperature		−65°C to +150°C
Input Voltage	Pins 3 and 7	−0.3V to V_{DD} + 0.3V
	Pins 1, 2, 8, and 9	−0.3V to 9.5V
Power Dissipation(4)		Internally limited
ESD Susceptibility(5)		2000V
ESD Susceptibility(6)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JC} (KTW)	4°C/W
	θ_{JA} (KTW)(4)	20°C/W
	θ_{JC} (NEC)	4°C/W
	θ_{JA} (NEC)(4)	20°C/W

(1) All voltages are measured with respect to the GND pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the given in Absolute Maximum Ratings, whichever is lower. For the LM4940 typical application (shown in Figure 1) with V_{DD} = 12V, R_L = 4Ω stereo operation the total power dissipation is 3.65W. θ_{JA} = 20°C/W for both DDPAK and TO–220 packages mounted to 16in^2 heatsink surface area.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine Model, 220pF–240pF discharged through all pins.

OPERATING RATINGS

Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	−40°C ≤ T_A ≤ 85°C
Supply Voltage	10V ≤ V_{DD} ≤ 16V

ELECTRICAL CHARACTERISTICS V_{DD} = 12V(1)(2)

The following specifications apply for V_{DD} = 12V, A_V = 10, R_L = 4Ω, f = 1kHz unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4940		Units (Limits)
			Typical(3)	Limit(4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, No Load	16	40	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND(6)	40	100	µA (max)
V_{SDIH}	Shutdown Voltage Input High			2.0 V_{DD}/2	V (min) V (max)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
P_O	Output Power	Single Channel			W (min)
		THD+N = 1%	3.1	2.8	
		THD+N = 10%	4.2		
		V_{DD} = 14.4V, THD+N = 10%	6.0		
THD+N	Total Harmomic Distortion + Noise	P_O = 1W_{RMS}, A_V = 10, f = 1kHz	0.15		%
ε_{OS}	Output Noise	A-Weighted Filter, V_{IN} = 0V, Input Referred	10		µV
X_{TALK}	Channel Separation	P_O = 1W	70		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{p-p} f_{RIPPLE} = 1kHz	56		dB

(1) All voltages are measured with respect to the GND pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Shutdown current is measured in a normal room environment. The Shutdown pin should be driven as close as possible to GND for minimum shutdown current.

TYPICAL APPLICATION

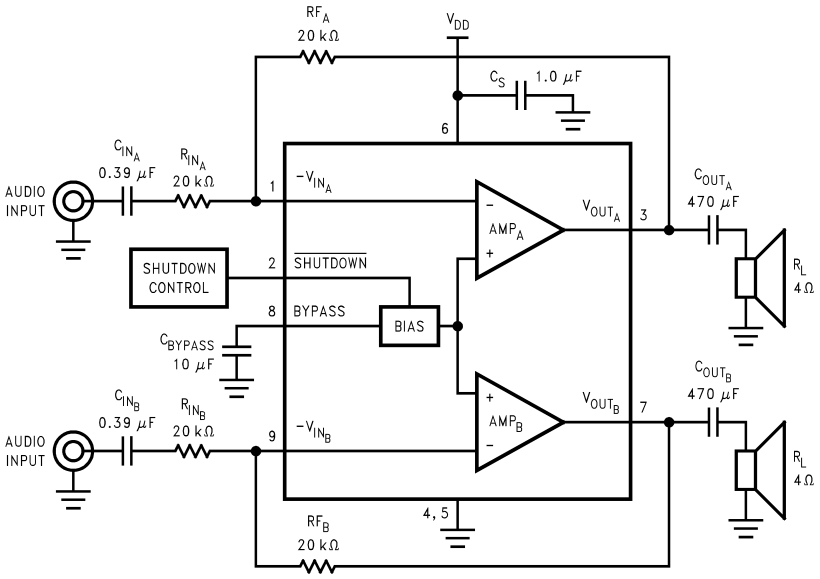


Figure 2. Typical Stereo Audio Amplifier Application Circuit

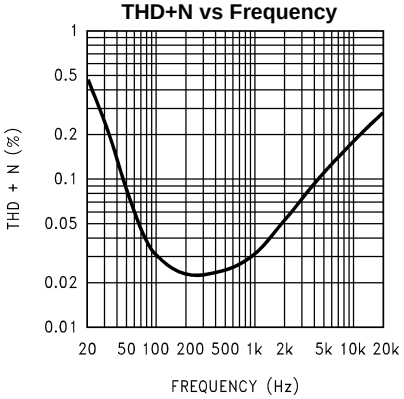
EXTERNAL COMPONENTS DESCRIPTION

Refer to Figure 1.

Components		Functional Description
1.	R_{IN}	This is the inverting input resistance that, along with R_F, sets the closed-loop gain. Input resistance R_{IN} and input capacitance C_{IN} form a high pass filter. The filter's cutoff frequency is $f_C = 1/(2\pi R_{IN}C_{IN})$.
2.	C_{IN}	This is the input coupling capacitor. It blocks DC voltage at the amplifier's inverting input. C_{IN} and R_{IN} create a highpass filter. The filter's cutoff frequency is $f_C = 1/(2\pi R_{IN}C_{IN})$. Refer to the SELECTING EXTERNAL COMPONENTS section for an explanation of determining C_{IN}'s value.
3.	R_F	This is the feedback resistance that, along with R_i, sets closed-loop gain.
4.	C_S	The supply bypass capacitor. Refer to the POWER SUPPLY BYPASSING section for information about properly placing, and selecting the value of, this capacitor.
5.	C_{BYPASS}	This capacitor filters the half-supply voltage present on the BYPASS pin. Refer to the SELECTING EXTERNAL COMPONENTS for information about properly placing, and selecting the value of, this capacitor.
6.	C_{OUT}	This is the output coupling capacitor. It blocks the nominal $V_{DD}/2$ voltage present at the output and prevents it from reaching the load. C_{OUT} and R_L form a high pass filter whose cutoff frequency is $f_C = 1/(2\pi R_L C_{OUT})$. Refer to the SELECTING EXTERNAL COMPONENTS section for an explanation of determining C_{OUT}'s value.

TYPICAL PERFORMANCE CHARACTERISTICS

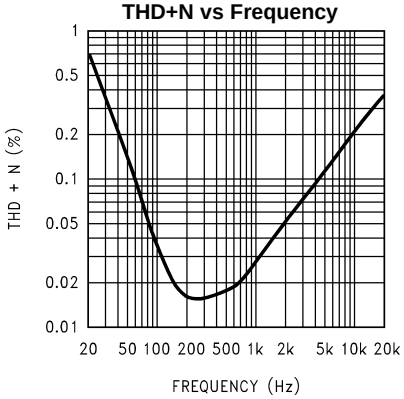
THD+N vs Frequency



V_{DD} = 12V, R_L = 4Ω, SE operation,
both channels driven and loaded (average shown)
P_{OUT} = 1W, A_V = 1

Figure 3.

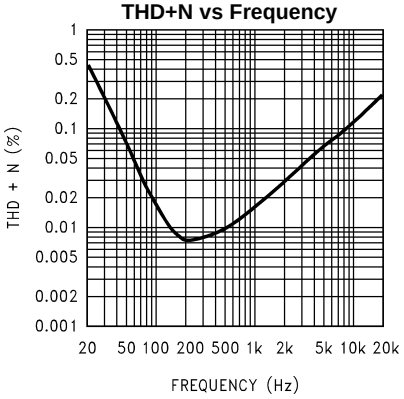
THD+N vs Frequency



V_{DD} = 12V, R_L = 4Ω, SE operation,
both channels driven and loaded (average shown),
P_{OUT} = 2.5W, A_V = 1

Figure 4.

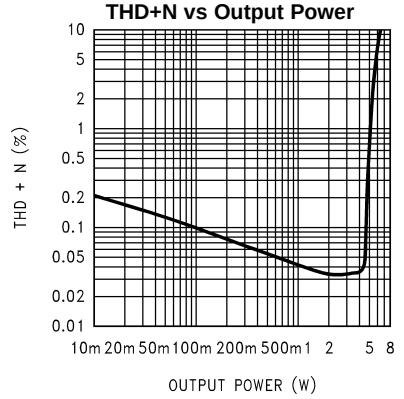
THD+N vs Frequency



V_{DD} = 12V, R_L = 8Ω, SE operation,
both channels driven and loaded (average shown),
P_{OUT} = 1W, A_V = 1

Figure 5.

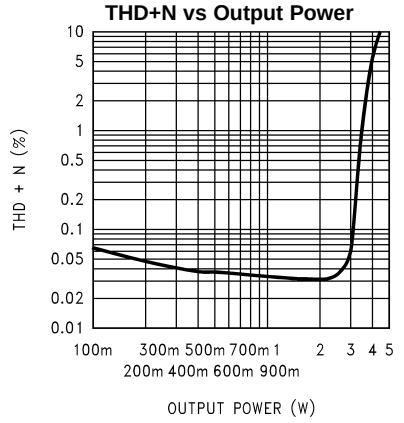
THD+N vs Output Power



V_{DD} = 14.4V, R_L = 4Ω, SE operation, A_V = 1
single channel driven/single channel measured,
f_{IN} = 1kHz

Figure 6.

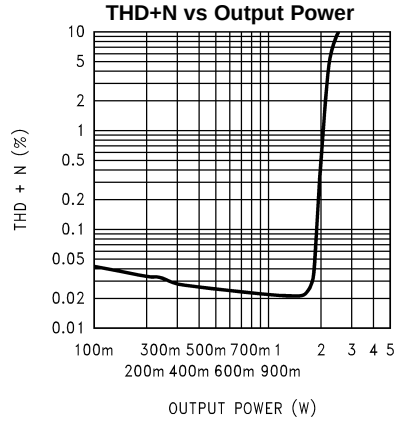
THD+N vs Output Power



V_{DD} = 12V, R_L = 4Ω, SE operation, A_V = 1
single channel driven/single channel measured,
f_{IN} = 1kHz

Figure 7.

THD+N vs Output Power

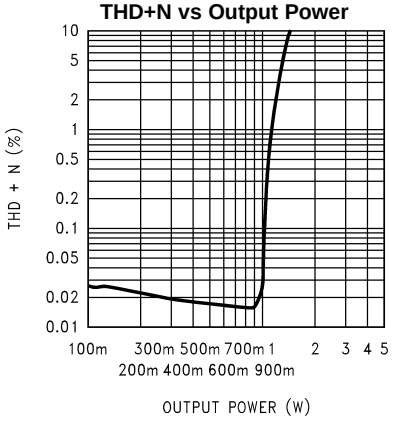


V_{DD} = 12V, R_L = 8Ω, SE operation, A_V = 1
single channel driven/single channel measured,
f_{IN} = 1kHz

Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

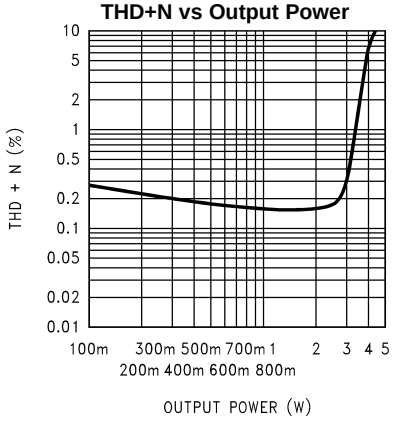
THD+N vs Output Power



V_{DD} = 12V, R_L = 16Ω, SE operation, A_V = 1
single channel driven/single channel measured,
f_{IN} = 1kHz

Figure 9.

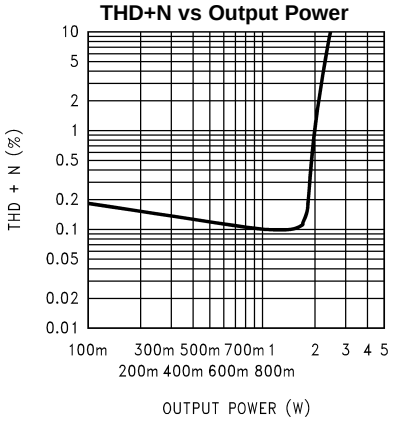
THD+N vs Output Power



V_{DD} = 12V, R_L = 4Ω, SE operation, A_V = 10
single channel driven/single channel measured,
f_{IN} = 1kHz

Figure 10.

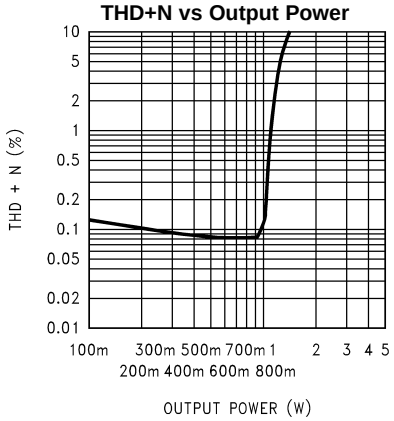
THD+N vs Output Power



V_{DD} = 12V, R_L = 8Ω, SE operation, A_V = 10
single channel driven/single channel measured,
f_{IN} = 1kHz

Figure 11.

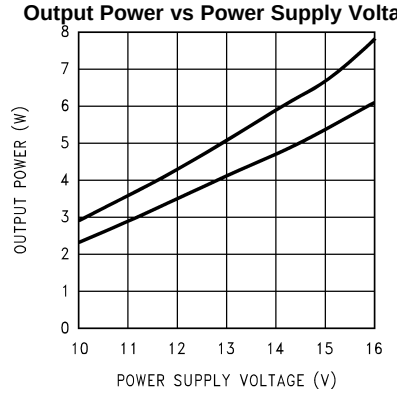
THD+N vs Output Power



V_{DD} = 12V, R_L = 16Ω, SE operation, A_V = 10
single channel driven/single channel measured,
f_{IN} = 1kHz

Figure 12.

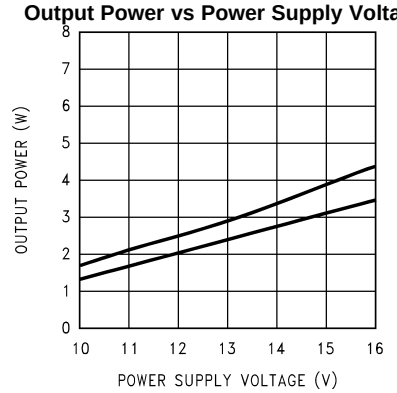
Output Power vs Power Supply Voltage



R_L = 4Ω, SE operation, f_{IN} = 1kHz,
both channels driven and loaded (average shown),
at (from top to bottom at 12V): THD+N = 10%,
THD+N = 1%

Figure 13.

Output Power vs Power Supply Voltage

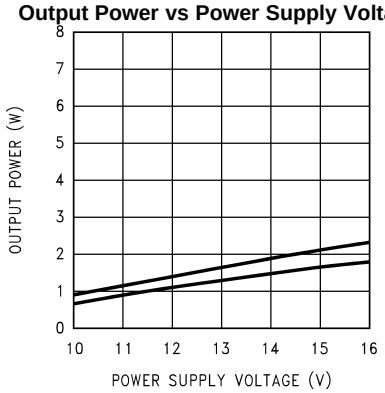


R_L = 8Ω, SE operation, f_{IN} = 1kHz,
both channels driven and loaded (average shown),
at (from top to bottom at 12V): THD+N = 10%,
THD+N = 1%

Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

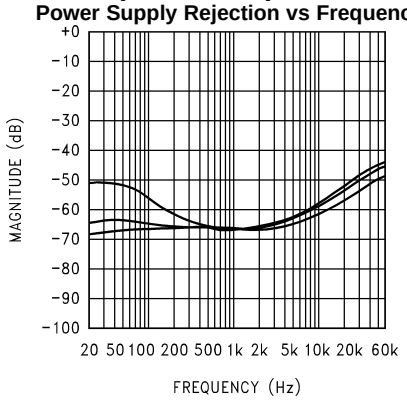
Output Power vs Power Supply Voltage



R_L = 16Ω, SE operation, f_{IN} = 1kHz,
both channels driven and loaded (average shown),
at (from top to bottom at 12V): THD+N = 10%,
THD+N = 1%

Figure 15.

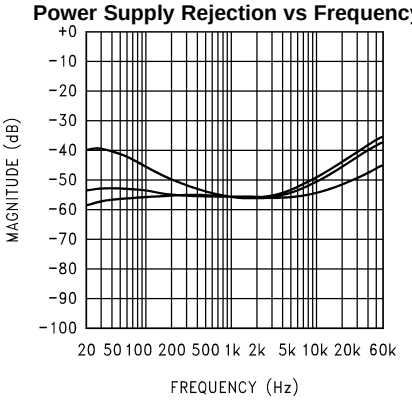
Power Supply Rejection vs Frequency



V_{DD} = 12V, R_L = 8Ω, SE operation,
V_{RIPPLE} = 200mV_{p-p}, at (from top to bottom at 60Hz):
C_{BYPASS} = 1µF, C_{BYPASS} = 4.7µF, C_{BYPASS} = 10µF

Figure 16.

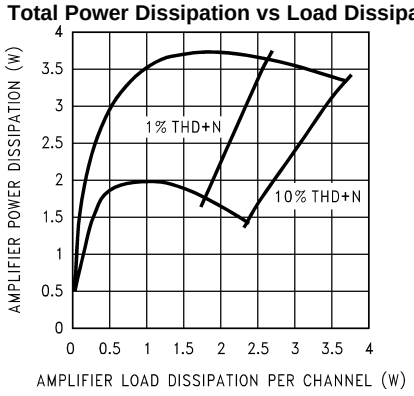
Power Supply Rejection vs Frequency



V_{DD} = 12V, R_L = 8Ω, SE operation, V_{RIPPLE} = 200mV_{p-p},
A_V = 10, at (from top to bottom at 60Hz):
C_{BYPASS} = 1µF, C_{BYPASS} = 4.7µF, C_{BYPASS} = 10µF

Figure 17.

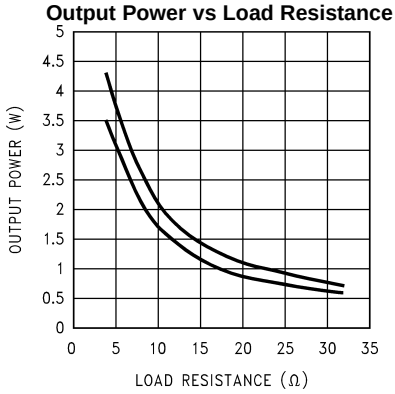
Total Power Dissipation vs Load Dissipation



V_{DD} = 12V, SE operation, f_{IN} = 1kHz,
at (from top to bottom at 1W):
R_L = 4Ω, R_L = 8Ω

Figure 18.

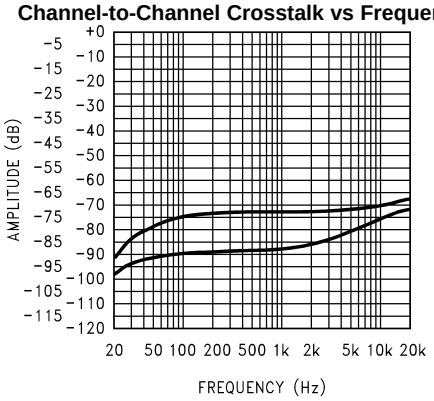
Output Power vs Load Resistance



V_{DD} = 12V, SE operation, f_{IN} = 1kHz,
both channels driven and loaded,
at (from top to bottom at 15Ω):
THD+N = 10%, THD+N = 1%

Figure 19.

Channel-to-Channel Crosstalk vs Frequency

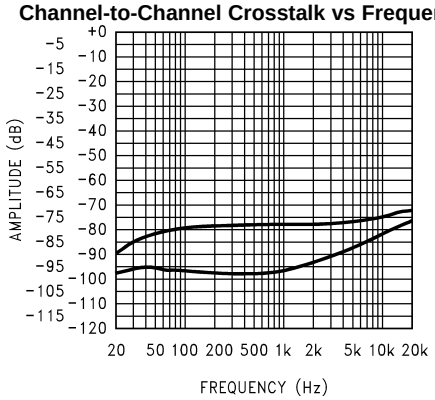


V_{DD} = 12V, R_L = 4Ω, P_{OUT} = 1W, SE operation,
at (from top to bottom at 1kHz): V_{INB} driven,
V_{OUTA} measured; V_{INA} driven, V_{OUTB} measured

Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

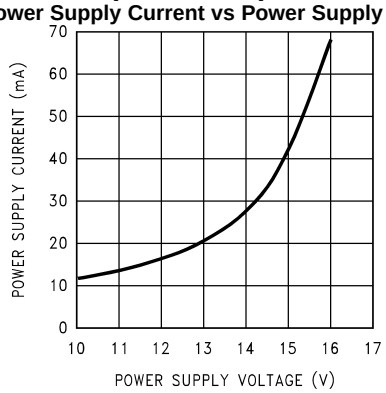
Channel-to-Channel Crosstalk vs Frequency



V_{DD} = 12V, R_L = 8Ω, P_{OUT} = 1W, SE operation,
at (from top to bottom at 1kHz): V_{INB} driven,
V_{OUTA} measured; V_{INA} driven, V_{OUTB} measured

Figure 21.

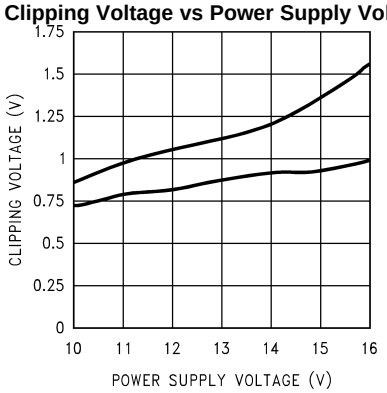
Power Supply Current vs Power Supply Voltage



R_L = 4Ω, SE operation
V_{IN} = 0V, R_{SOURCE} = 50Ω

Figure 22.

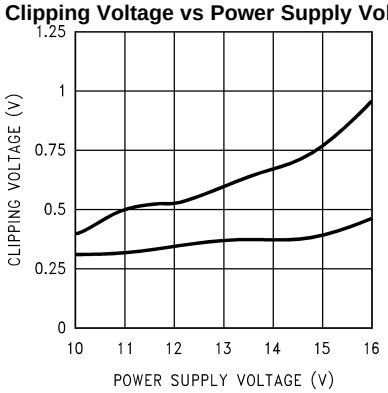
Clipping Voltage vs Power Supply Voltage



R_L = 4Ω, SE operation, f_{IN} = 1kHz
both channels driven and loaded,
at (from top to bottom at 13V):
negative signal swing, positive signal swing

Figure 23.

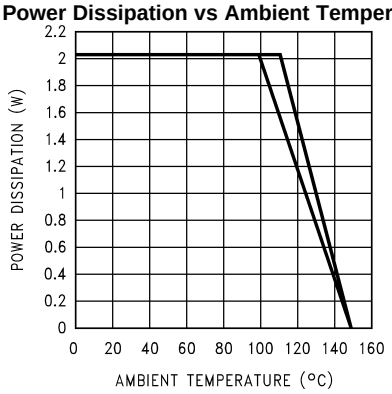
Clipping Voltage vs Power Supply Voltage



R_L = 8Ω, SE operation, f_{IN} = 1kHz
both channels driven and loaded,
at (from top to bottom at 13V):
negative signal swing, positive signal swing

Figure 24.

Power Dissipation vs Ambient Temperature



V_{DD} = 12V, R_L = 8Ω (SE), f_{IN} = 1kHz,
(from top to bottom at 120°C):
16in^2 copper plane heatsink area,
8in^2 copper plane heatsink area

Figure 25.

APPLICATION INFORMATION

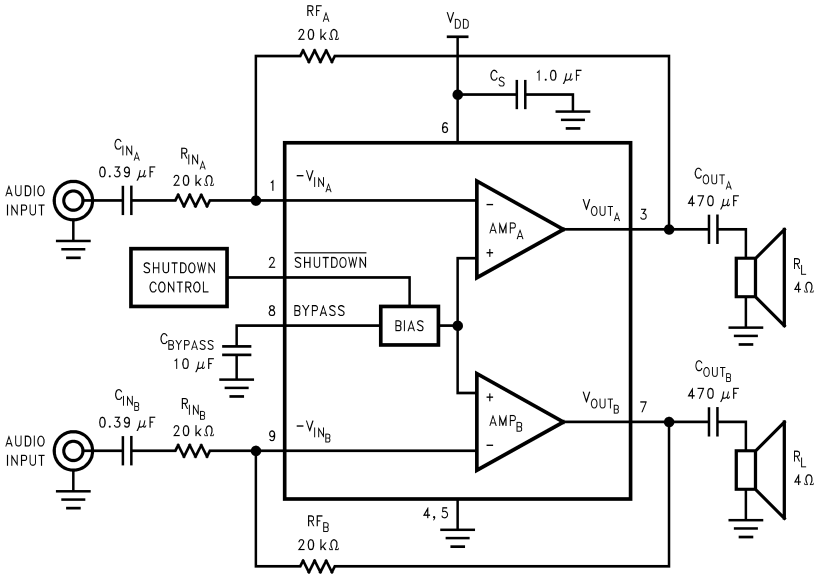


Figure 26. Typical LM4940 Stereo Amplifier Application Circuit

HIGH VOLTAGE BOOMER WITH INCREASED OUTPUT POWER

Unlike previous 5V Boomer amplifiers, the LM4940 is designed to operate over a power supply voltages range of 10V to 15V. Operating on a 12V power supply, the LM4940 will deliver 3.1W per channel into 4Ω loads with no more than 1% THD+N.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended amplifier. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX\text{-}SE} = (V_{DD})^2 / (2\pi^2 R_L): \quad \text{Single Ended} \tag{1}$$

The LM4940's dissipation is twice the value given by Equation 1 when driving two SE loads. For a 12V supply and two 8Ω SE loads, the LM4940's dissipation is 1.82W.

The maximum power dissipation point (twice the value given by Equation 1 must not exceed the power dissipation given by Equation 2:

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \tag{2}$$

The LM4940's T_{JMAX} = 150°C. In the KTW package, the LM4940's θ_{JA} is 20°C/W when the metal tab is soldered to a copper plane of at least 16in^2. This plane can be split between the top and bottom layers of a two-sided PCB. Connect the two layers together under the tab with a 5x5 array of vias. For the NEC package, use an external heatsink with a thermal impedance that is less than 20°C/W. At any given ambient temperature T_A, use Equation 3 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 3 and substituting P_{DMAX} for P_{DMAX}' results in Equation 4. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4940's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX\text{-}SE}\theta_{JA} \quad (3)$$

For a typical application with a 12V power supply and two 4Ω SE loads, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 113°C for the KTW package.

$$T_{JMAX} = P_{DMAX\text{-}SE}\theta_{JA} + T_A \quad (4)$$

Equation 4 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4940's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation 3 is greater than that of Equation 4, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. Further, ensure that speakers rated at a nominal 4Ω do not fall below 3Ω. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pins, supply pin and amplifier output pins. Refer to the TYPICAL PERFORMANCE CHARACTERISTICS curves for power dissipation information at lower output power levels.

POWER SUPPLY VOLTAGE LIMITS

Continuous proper operation is ensured by never exceeding the voltage applied to any pin, with respect to ground, as listed in the Absolute Maximum Ratings section.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a voltage regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4940's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4940's power supply pin and ground as short as possible. Connecting a 10µF capacitor, C_{BYPASS}, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_{BYPASS}, depends on desired PSRR requirements, click and pop performance (as explained in the section, SELECTING EXTERNAL COMPONENTS), system cost, and size constraints.

MICRO-POWER SHUTDOWN

The LM4940 features an active-low shutdown mode that disables the amplifier's bias circuitry, reducing the supply current to 40µA (typ). Connect SHUTDOWN to a voltage between 2V to $V_{DD}/2$ for normal operation. Connect SHUTDOWN to GND to disable the device. A voltage that is greater than GND can increase shutdown current.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Two quantities determine the value of the input coupling capacitor: the lowest audio frequency that requires amplification and desired output transient suppression.

As shown in Figure 26, the input resistor (R_{IN}) and the input capacitor (C_{IN}) produce a high pass filter cutoff frequency that is found using Equation 5.

$$f_C = 1/2\pi R_i C_i \quad (5)$$

As an example when using a speaker with a low frequency limit of 50Hz, C_i, using Equation 5 is 0.159µF. The 0.39µF C_{INA} shown in Figure 26 allows the LM4940 to drive high efficiency, full range speaker whose response extends below 30Hz.

Output Coupling Capacitor Value Selection

The capacitors C_{OUTA} and C_{OUTB} that block the $V_{DD}/2$ output DC bias voltage and couple the output AC signal to the amplifier loads also determine low frequency response. These capacitors, combined with their respective loads create a highpass filter cutoff frequency. The frequency is also given by Equation 5.

Using the same conditions as above, with a 4Ω speaker, C_{OUT} is 820µF (nearest common valve).

Bypass Capacitor Value

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_{BYPASS}, the capacitor connected to the BYPASS pin. Since C_{BYPASS} determines how fast the LM4940 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4940's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_{BYPASS} equal to 10µF along with a small value of C_{IN} (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_{IN} no larger than necessary for the desired bandwidth helps minimize clicks and pops.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4940 contains circuitry that eliminates turn-on and shutdown transients ("clicks and pops"). For this discussion, turn-on refers to either applying the power supply voltage or when the micro-power shutdown mode is deactivated.

As the $V_{DD}/2$ voltage present at the BYPASS pin ramps to its final value, the LM4940's internal amplifiers are configured as unity gain buffers and are disconnected from the AMP_A and AMP_B pins. An internal current source charges the capacitor connected between the BYPASS pin and GND in a controlled manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage applied to the BYPASS pin.

The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches $V_{DD}/2$. As soon as the voltage on the bypass pin is stable, the device becomes fully operational and the amplifier outputs are reconnected to their respective output pins. Although the BYPASS pin current cannot be modified, changing the size of C_{BYPASS} alters the device's turn-on time. Here are some typical turn-on times for various values of C_{BYPASS}:

C_B (µF)	T_{ON} (ms)
1.0	120
2.2	120
4.7	200
10	440

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops".

There is a relationship between the value of C_{IN} and C_{BYPASS} that ensures minimum output transient when power is applied or the shutdown mode is deactivated. Best performance is achieved by setting the time constant created by C_{IN} and $R_i + R_f$ to a value less than the turn-on time for a given value of C_{BYPASS} as shown in the table above.

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 3W into a 4Ω load

The following are the desired operational parameters:

Power Output	$3W_{RMS}$
Load Impedance	4Ω
Input Level	$0.3V_{RMS}$ (max)
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Power Supply Voltage curve in the TYPICAL PERFORMANCE CHARACTERISTICS section. Another way, using Equation 6, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Clipping Dropout Voltage vs Power Supply Voltage in the TYPICAL PERFORMANCE CHARACTERISTICS curves, must be added to the result obtained by Equation 6. The result is Equation 7.

$$V_{opeak} = \sqrt{(2R_L P_O)} \tag{6}$$

$$V_{DD} = V_{OUTPEAK} + V_{ODTOP} + V_{ODBOT} \tag{7}$$

The Figure 13 graph for an 8Ω load indicates a minimum supply voltage of 11.8V. The commonly used 12V supply voltage easily meets this. The additional voltage creates the benefit of headroom, allowing the LM4940 to produce an output power of 3W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the POWER DISSIPATION section. After satisfying the LM4940's power dissipation requirements, the minimum differential gain needed to achieve 3W dissipation in a 4Ω BTL load is found using Equation 8.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{8}$$

Thus, a minimum gain of 11.6 allows the LM4940's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_V = 12. The amplifier's overall BTL gain is set using the input (RIN_A) and feedback (R) resistors of the first amplifier in the series BTL configuration. Additionaly, $A_{V\text{-}BTL}$ is twice the gain set by the first amplifier's R_{IN} and R_f. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation 9.

$$R_f / R_{IN} = A_V \tag{9}$$

The value of R_f is 240kΩ. The nominal output power is 3W.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB-desired limit. The results are an

$$f_L = 100Hz / 5 = 20Hz \quad (10)$$

and

$$f_L = 20kHz \times 5 = 100kHz \quad (11)$$

As mentioned in the SELECTING EXTERNAL COMPONENTS section, R_{INA} and C_{INA}, as well as C_{OUT} and R_L, create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation 14.

$$C_{IN} = 1 / 2\pi R_{IN} f_L \quad (12)$$

The result is

$$1 / (2\pi \times 20k\Omega \times 20Hz) = 0.398\mu F = C_{IN} \quad (13)$$

and

$$1 / (2\pi \times 4\Omega \times 20Hz) = 1989\mu F = C_{OUT} \quad (14)$$

Use a 0.39µF capacitor for C_{IN} and a 2000µF capacitor for C_{OUT}, the closest standard values.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A_V, determines the upper passband response limit. With A_V = 12 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 1.2mHz. This is less than the LM4940's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance restricting bandwidth limitations.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 27 through Figure 29 show the recommended two-layer PC board layout that is optimized for the DDPAK-packaged LM4940 and associated external components. This circuit board is designed for use with an external 12V supply and 4Ω (min) speakers.

This circuit board is easy to use. Apply 12V and ground to the board's V_{DD} and GND pads, respectively. Connect a speaker between the board's OUT_A and OUT_B outputs and their respective GND terminals.

Demonstration Board Layout

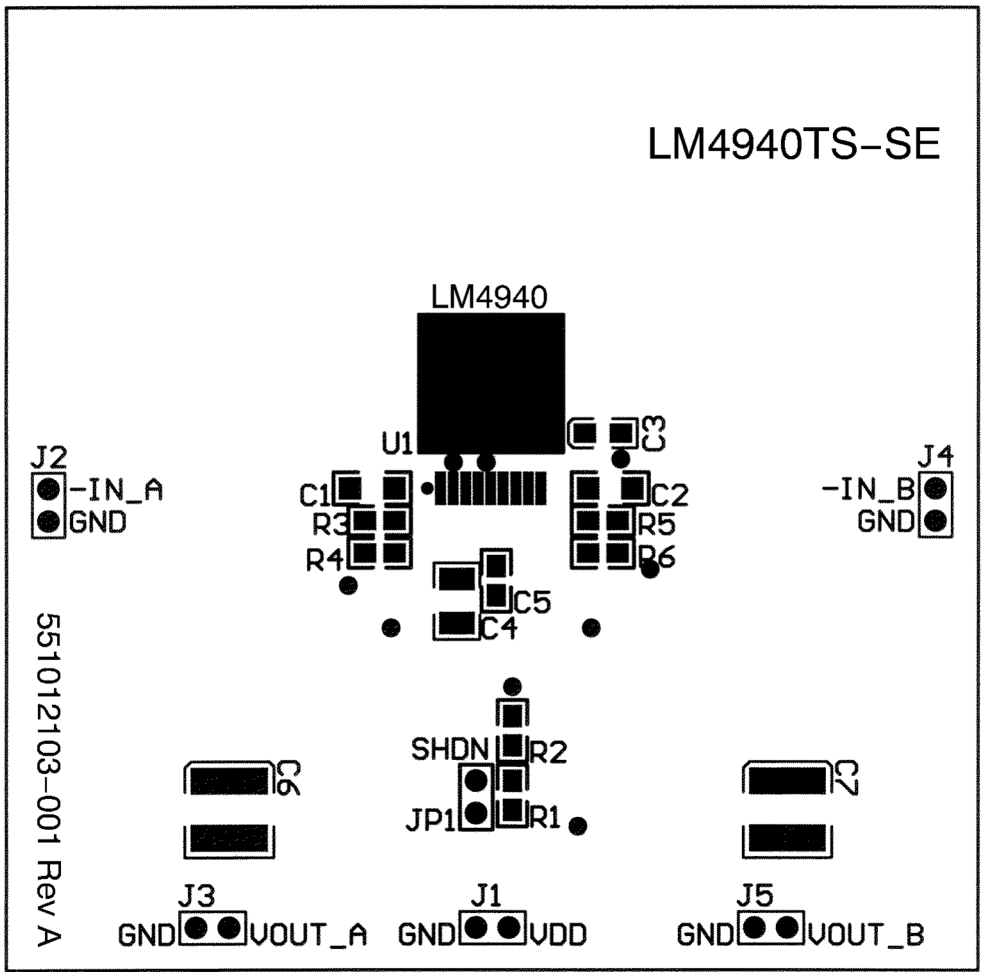


Figure 27. Recommended KTW PCB Layout: Top Silkscreen

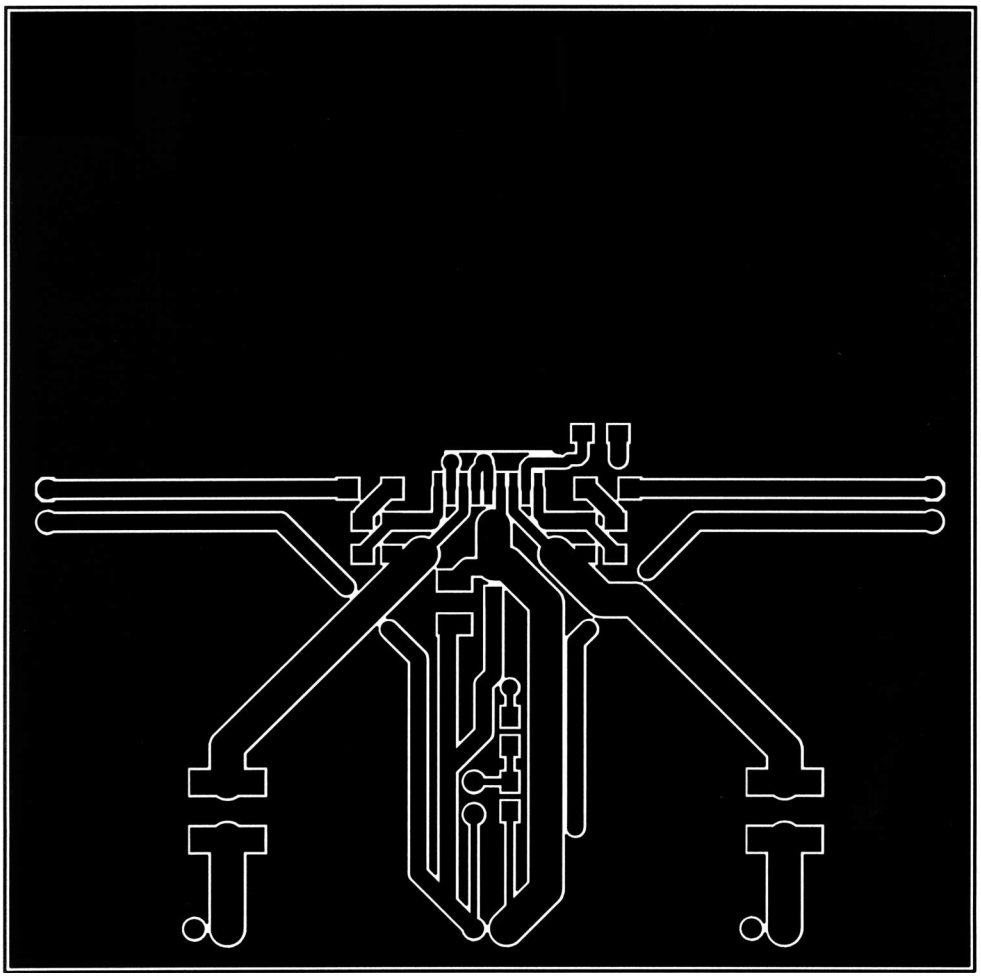


Figure 28. Recommended KTW PCB Layout: Top Layer

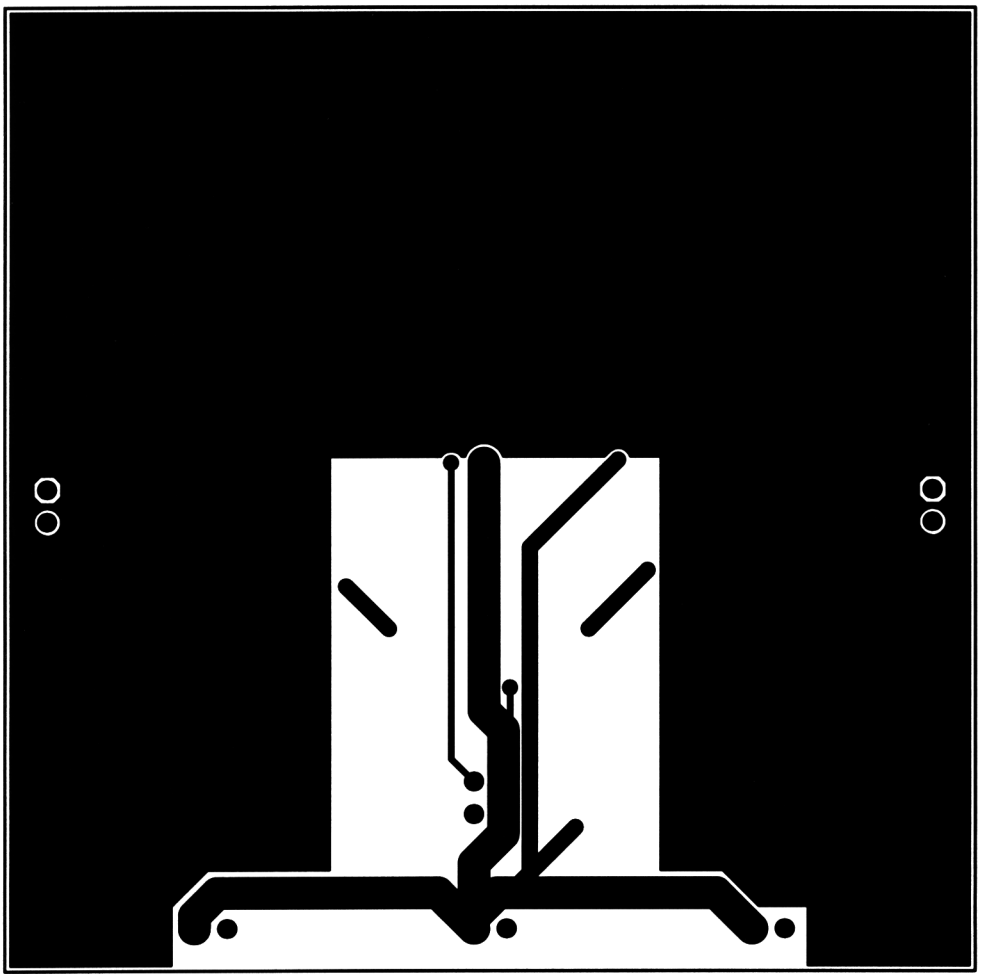


Figure 29. Recommended KTW PCB Layout: Bottom Layer

REVISION HISTORY

Changes from Revision B (May 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4940TS/NOPB	ACTIVE	DDPAK/ TO-263	KTW	9	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 85	L4940TS	Samples
LM4940TSX/NOPB	ACTIVE	DDPAK/ TO-263	KTW	9	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 85	L4940TS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

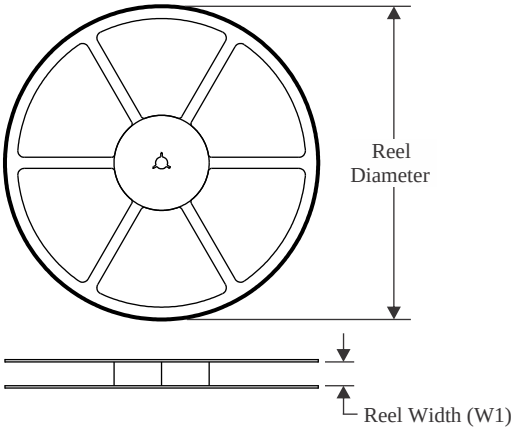
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

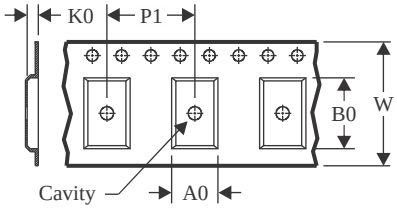
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

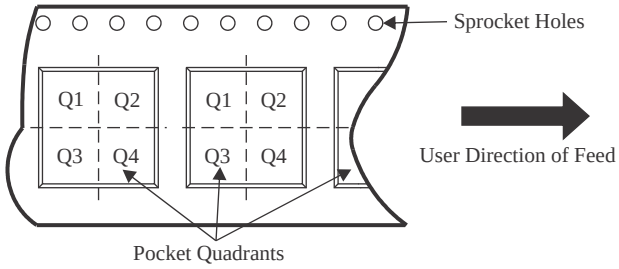


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

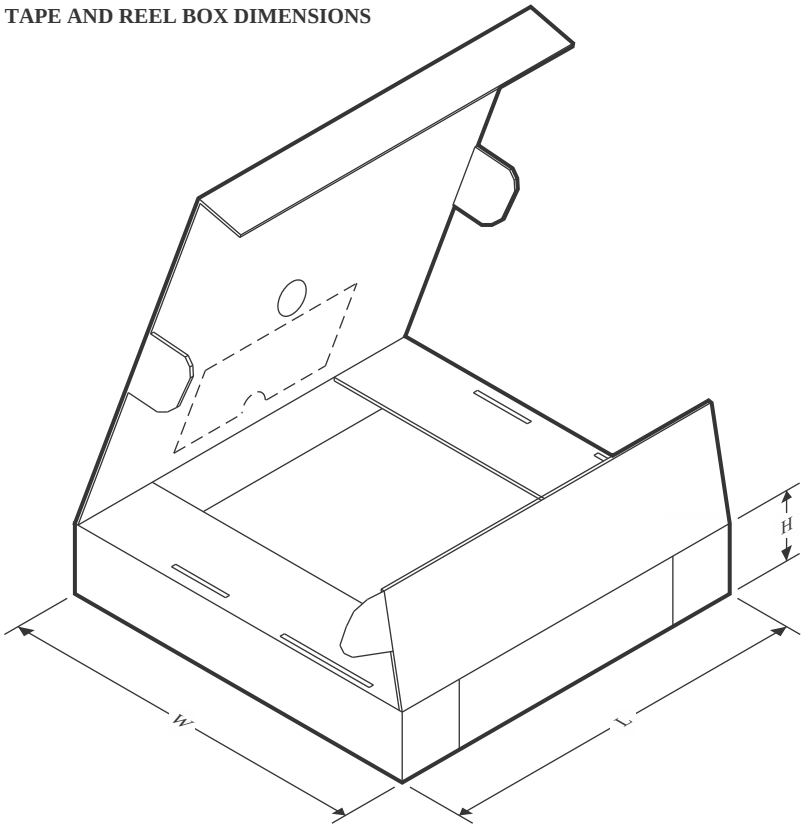
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4940TSX/NOPB	DDPAK/ TO-263	KTW	9	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

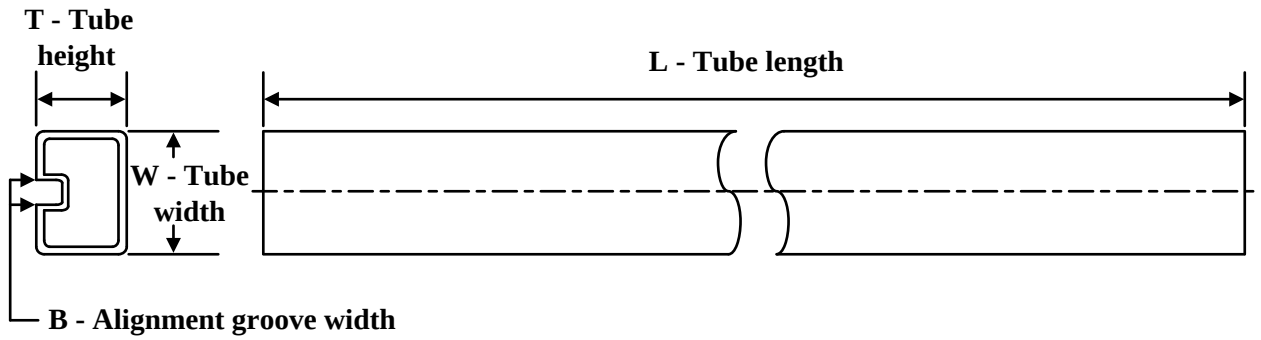
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4940TSX/NOPB	DDPAK/TO-263	KTW	9	500	367.0	367.0	45.0

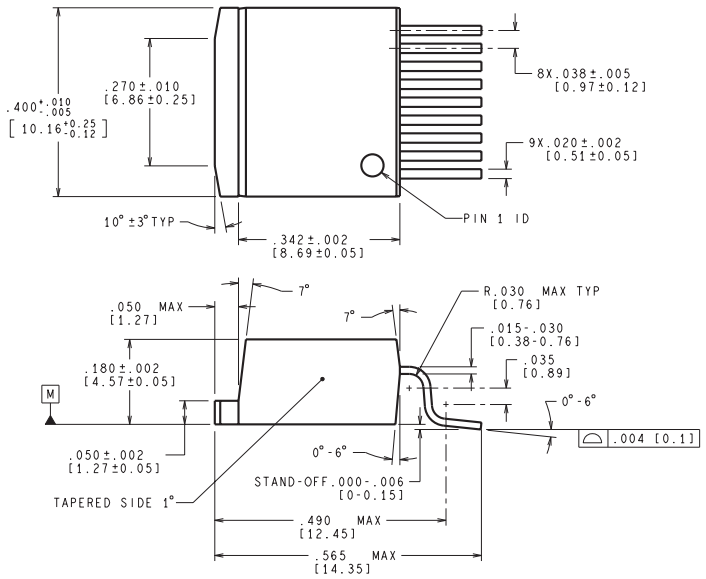
TUBE

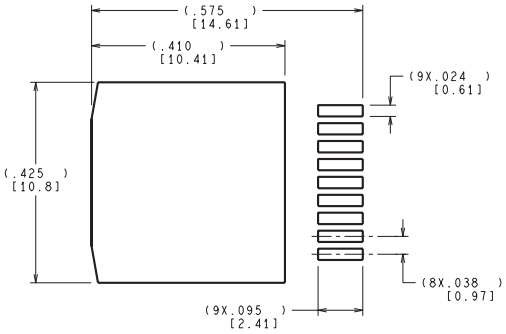


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4940TS/NOPB	KTW	TO-263	9	45	502	25	8204.2	9.19

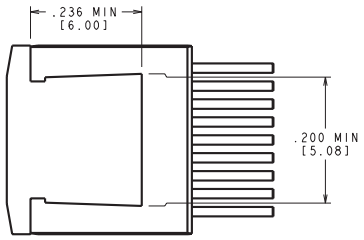
KTW0009A





RECOMMENDED LAND PATTERN

CONTROLLING DIMENSION: INCH
DIMENSIONS IN [ ] ARE MILLIMETERS



BOTTOM SIDE OF PACKAGE

TS9A (Rev B)

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