LMZ14202H 2A， SIMPLE SWITCHER® 电源模块，此模块针对高输出电压应用

查询样品: LMZ14202H

特性

- 集成屏蔽式电感器
- 简单印刷电路板 **(PCB)** 布局布线
- 使用外部软启动和精密使能的灵活启动排序
- 防止涌入电流
- 输入欠压闭锁 **(UVLO)** 和输出短路保护
- **-40°C** 至 **125°C** 的结温范围
- 用于简单装配和制造的单个外露垫和标准引脚分配
- 低输出电压纹波
- 引脚到引脚兼容系列：
  - **LMZ14203H/2H/1H**（**42V** 最大值 **3A**，**2A**，**1A**）
  - **LMZ14203/2/1**（**42V** 最大值 **3A**，**2A**，**1A**）
  - **LMZ12003/2/1**（**20V** 最大值 **3A**，**2A**，**1A**）
- 针对 **Webench®** 电源设计工具完全启用

应用范围

- 中间总线转换至 **12V** 和 **24V** 电源轨
- 时间关键项目
- 空间受限**/**高热量要求应用
- 负输出电压应用

Top View Bottom View

图 **1.** 易于使用的 **7** 引脚封装
PFM 7 引脚封装
10.16 x 13.77 x 4.57mm（**0.4 x 0.542 x 0.18** 英寸）
θ_{JA}**= 16°C/W**，θ_{JC}**= 1.9°C/W**
与无铅 **(RoHS)** 认证标准兼容

电气规范

- 高达 **2A** 输出电流
- 输入电压范围 **6V** 至 **42V**
- 输出电压低至 **5V**
- 效率高达 **97%**

性能优势

- 高效率减少了系统散热
- 低辐射电磁干扰 **(EMI)**（与 **EN 55022 B** 类标准兼容） (1)
- 无需补偿
- 低封装热阻

说明

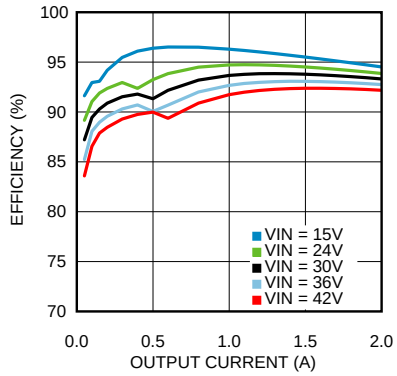
LMZ14202H SIMPLE SWITCHER 电源模块是一款易于使用的降压直流至直流 (DC-DC) 解决方案，此解决方案能够以出色的功率转换效率、线路和负载调节和输出精度驱动高达 2A 的负载。 LMZ14202H 采用创新型封装，此封装可提高热性能并可实现手工或机器焊接。

LMZ14202H 可接受 6V 到 42V 之间的输入电压轨，提供低至 5V 的可调且高精确度输出电压。
LMZ14202H 只需 3 个外部电阻器和 4 个外部电容器即可完成电源解决方案。 LMZ14202H 是一款具有以下保护特性的可靠且稳定耐用的设计：热关断、输入欠压闭锁、输出过压保护、短路保护、输出电流限制并允许启动至一个预偏置输出。 一个单个电阻器将开关频率调节至 1MHz。

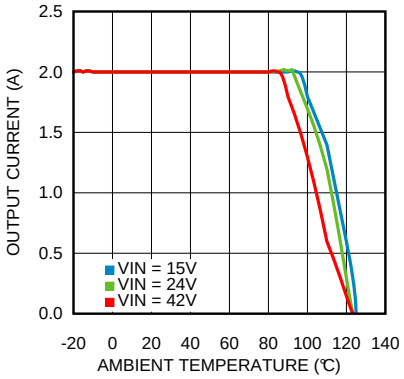
(1) EN 55022:2006，+A1:2007，FCC 部分 15 子部分 B: 2007.

System Performance

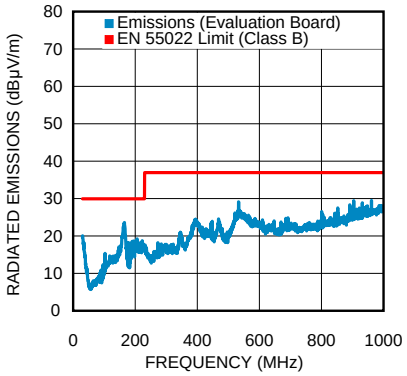
Efficiency V_{OUT} = 12V



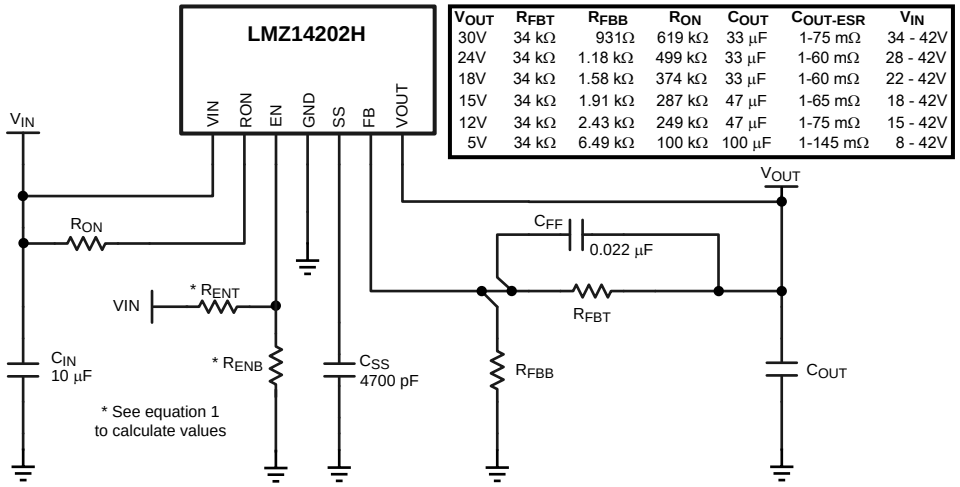
Thermal Derating V_{OUT} = 12V, θ_{JA} = 16°C/W



Radiated Emissions (EN 55022 Class B)



Simplified Application Schematic



V_{OUT}	R_{FBT}	R_{FBB}	R_{ON}	C_{OUT}	$C_{OUT-ESR}$	V_{IN}
30V	34 kΩ	931Ω	619 kΩ	33 µF	1-75 mΩ	34 - 42V
24V	34 kΩ	1.18 kΩ	499 kΩ	33 µF	1-60 mΩ	28 - 42V
18V	34 kΩ	1.58 kΩ	374 kΩ	33 µF	1-60 mΩ	22 - 42V
15V	34 kΩ	1.91 kΩ	287 kΩ	47 µF	1-65 mΩ	18 - 42V
12V	34 kΩ	2.43 kΩ	249 kΩ	47 µF	1-75 mΩ	15 - 42V
5V	34 kΩ	6.49 kΩ	100 kΩ	100 µF	1-145 mΩ	8 - 42V

Connection Diagram

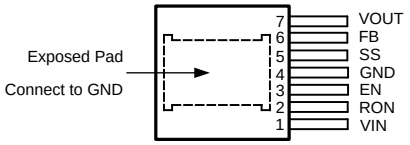


Figure 2. Top View
7-Lead PFM

PIN DESCRIPTIONS

Pin	Name	Description
1	VIN	Supply input — Additional external input capacitance is required between this pin and the exposed pad (EP).
2	RON	On time resistor — An external resistor from V_{IN} to this pin sets the on-time and frequency of the application. Typical values range from 100k to 700k ohms.
3	EN	Enable — Input to the precision enable comparator. Rising threshold is 1.18V.
4	GND	Ground — Reference point for all stated voltages. Must be externally connected to EP.
5	SS	Soft-Start — An internal 8 µA current source charges an external capacitor to produce the soft-start function.
6	FB	Feedback — Internally connected to the regulation, over-voltage, and short-circuit comparators. The regulation reference point is 0.8V at this input pin. Connect the feedback resistor divider between the output and ground to set the output voltage.
7	VOUT	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and the EP.
EP	EP	Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

VIN, RON to GND	-0.3V to 43.5V
EN, FB, SS to GND	-0.3V to 7V
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility(3)	± 2 kV
Peak Reflow Case Temperature (30 sec)	245°C
For soldering specifications, refer to the following document: www.ti.com/lit/snoa549c	

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

Operating Ratings (1)

V_{IN}	6V to 42V
EN	0V to 6.5V
Operation Junction Temperature	−40°C to 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24V, V_{OUT} = 12V, R_{ON} = 249kΩ

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
SYSTEM PARAMETERS						
Enable Control						
V_{EN}	EN threshold trip point	V_{EN} rising	**1.10**	1.18	**1.25**	V
V_{EN-HYS}	EN threshold hysteresis			90		mV
Soft-Start						
I_{SS}	SS source current	V_{SS} = 0V	**8**	10	**15**	µA
I_{SS-DIS}	SS discharge current			-200		µA
Current Limit						
I_{CL}	Current limit threshold	DC average	**2.4**	3.2	**3.95**	A
VIN UVLO						
VIN_{UVLO}	Input UVLO	EN pin floating V_{IN} rising		3.75		V
$VIN_{UVLO-HYST}$	Hysteresis	EN pin floating V_{IN} falling		130		mV
ON/OFF Timer						
t_{ON-MIN}	ON timer minimum pulse width			150		ns
t_{OFF}	OFF timer pulse width			260		ns
Regulation and Over-Voltage Comparator						

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24V, V_{OUT} = 12V, R_{ON} = 249kΩ

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{FB}	In-regulation feedback voltage	V_{IN} = 24V, V_{OUT} = 12V V_{SS} >+ 0.8V T_J = -40°C to 125°C I_{OUT} = 10mA to 2A	**0.782**	0.803	**0.822**	V
		V_{IN} = 24V, V_{OUT} = 12V V_{SS} >+ 0.8V T_J = 25°C I_{OUT} = 10mA to 2A	0.786	0.803	0.818	V
V_{FB}	In-regulation feedback voltage	V_{IN} = 36V, V_{OUT} = 24V V_{SS} >+ 0.8V T_J = -40°C to 125°C I_{OUT} = 10mA to 2A	**0.780**	0.803	**0.824**	V
		V_{IN} = 36V, V_{OUT} = 24V V_{SS} >+ 0.8V T_J = 25°C I_{OUT} = 10mA to 2A	0.787	0.803	0.819	V
V_{FB-OVP}	Feedback over-voltage protection threshold			0.92		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non Switching Input Current	V_{FB}= 0.86V		1		mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0V		25		µA
Thermal Characteristics						
T_{SD}	Thermal Shutdown	Rising		165		°C
$T_{SD-HYST}$	Thermal Shutdown Hysteresis			15		°C
θ_{JA}	Junction to Ambient	4 layer Printed Circuit Board, 7.62cm x 7.62cm (3in x 3in) area, 1 oz Copper, No air flow		16		°C/W
		4 layer Printed Circuit Board, 6.35cm x 6.35cm (2.5in x 2.5in) area, 1 oz Copper, No air flow		18.4		°C/W
θ_{JC}	Junction to Case	No air flow		1.9		°C/W
PERFORMANCE PARAMETERS						
ΔV_{OUT}	Output Voltage Ripple	V_{OUT} = 5V, C_O = 100µF 6.3V X7R		8		mV_{PP}
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 16V to 42V, I_{OUT}= 3A		.01		%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 24V, I_{OUT} = 0A to 2A		1.5		mV/A
η	Efficiency	V_{IN} = 24V V_{OUT} = 12V I_{OUT} = 1A		93		%
η	Efficiency	V_{IN} = 24V V_{OUT} = 12V I_{OUT} = 2A		92		%

Typical Performance Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.

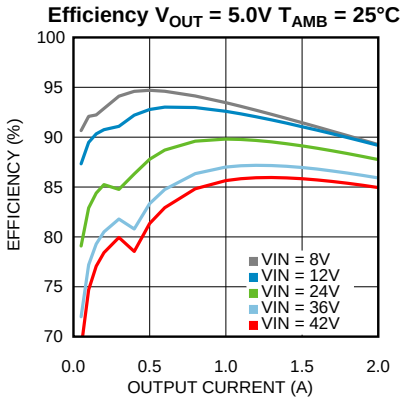


Figure 3.

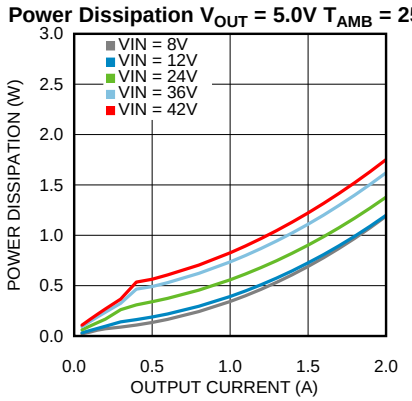


Figure 4.

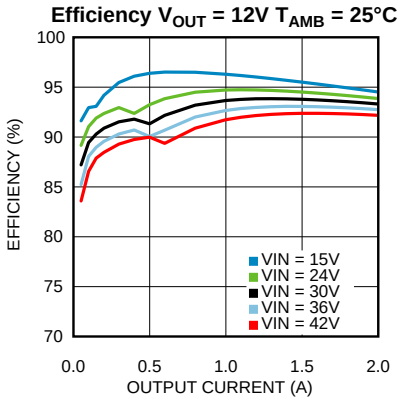


Figure 5.

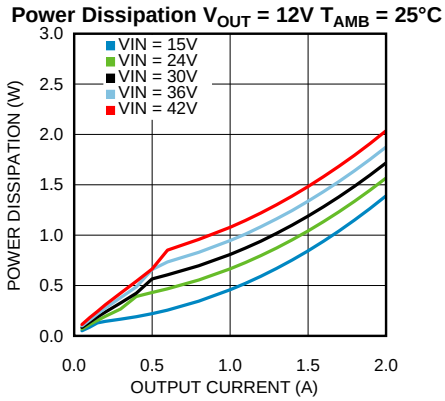


Figure 6.

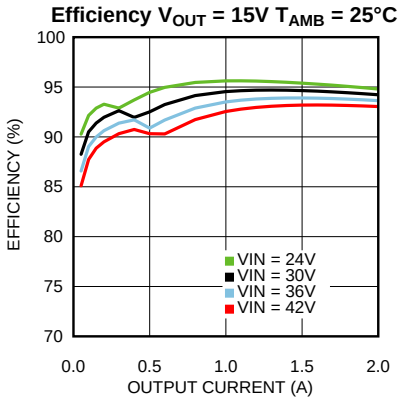


Figure 7.

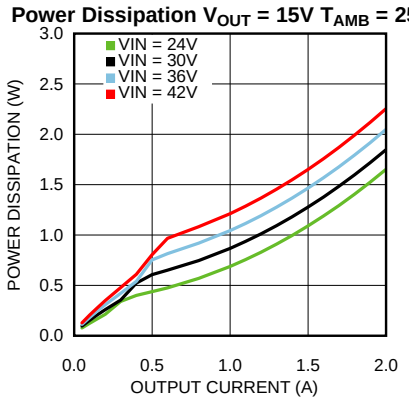
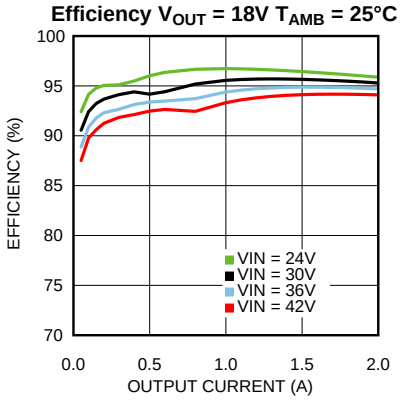


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.



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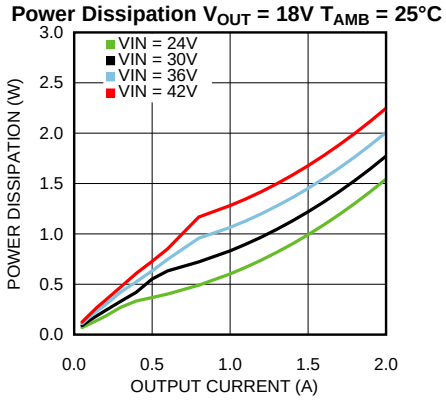


Figure 10.

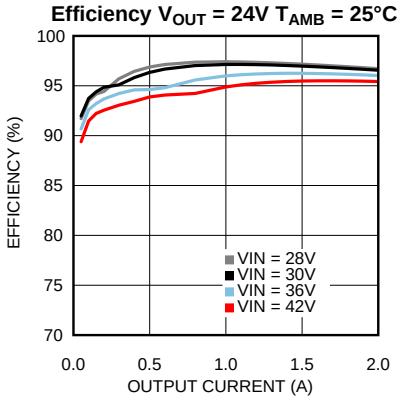


Figure 11.

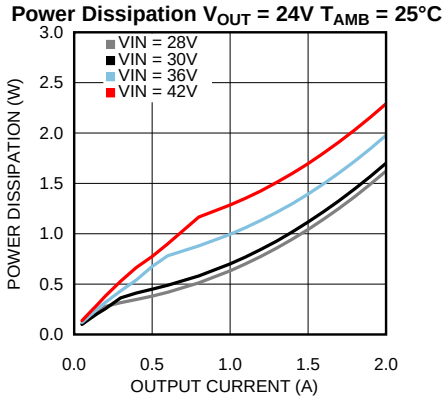
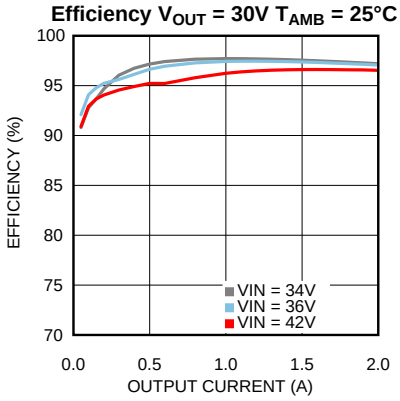


Figure 12.



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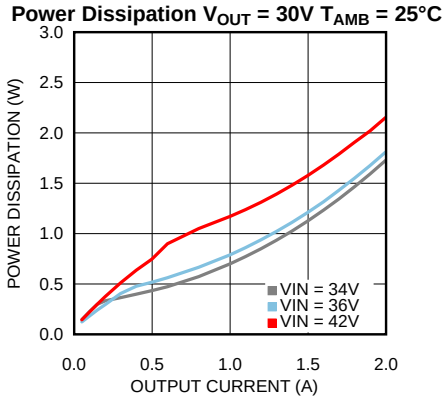


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.

Efficiency V_{OUT} = 5.0V T_{AMB} = 85°C

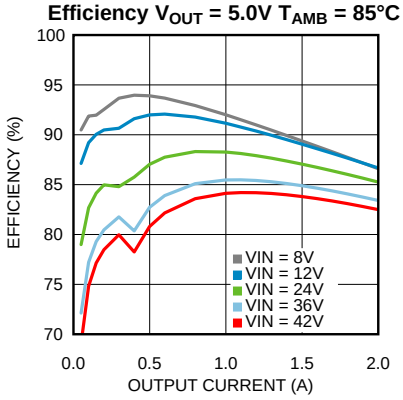


Figure 15.

Power Dissipation V_{OUT} = 5.0V T_{AMB} = 85°C

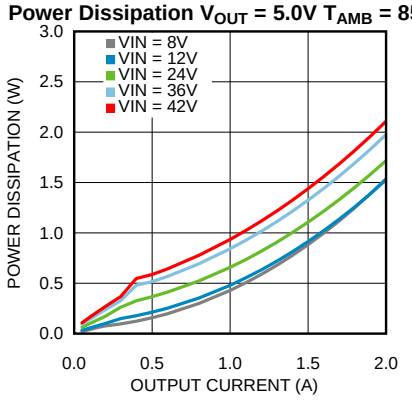


Figure 16.

Efficiency V_{OUT} = 12V T_{AMB} = 85°C

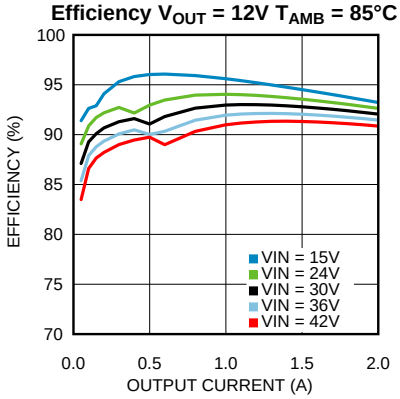


Figure 17.

Power Dissipation V_{OUT} = 12V T_{AMB} = 85°C

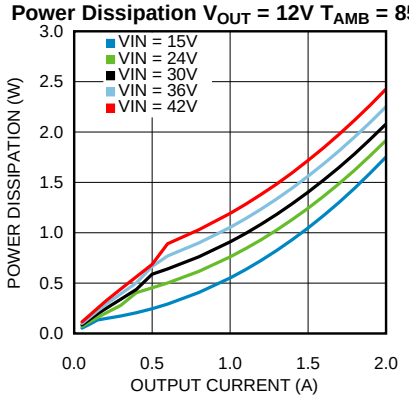


Figure 18.

Efficiency V_{OUT} = 15V T_{AMB} = 85°C

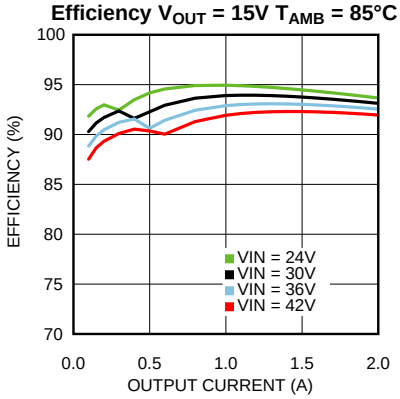


Figure 19.

Power Dissipation V_{OUT} = 15V T_{AMB} = 85°C

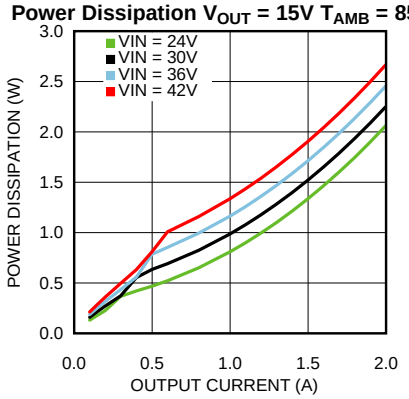


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.

Efficiency V_{OUT} = 18V T_{AMB} = 85°C

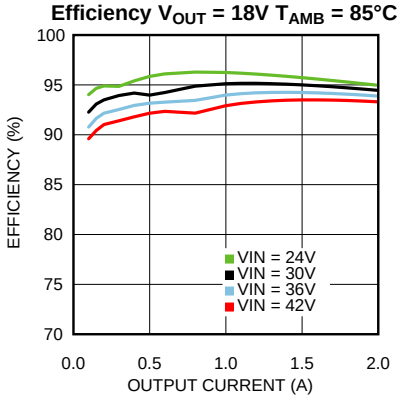


Figure 21.

Power Dissipation V_{OUT} = 18V T_{AMB} = 85°C

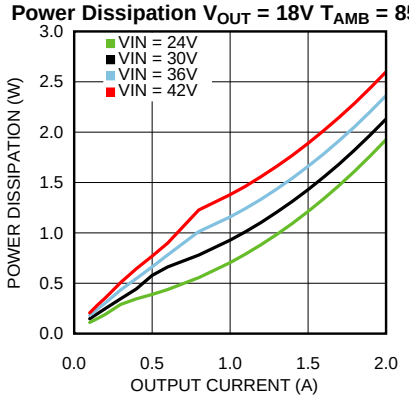


Figure 22.

Efficiency V_{OUT} = 24V T_{AMB} = 85°C

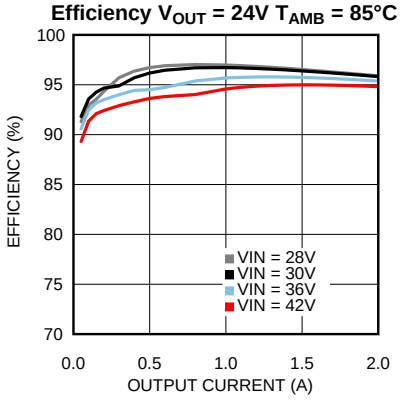


Figure 23.

Power Dissipation V_{OUT} = 24V T_{AMB} = 85°C

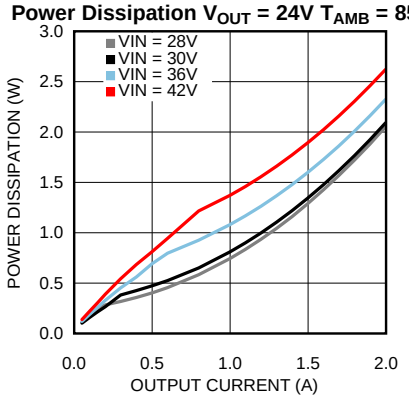


Figure 24.

Efficiency V_{OUT} = 30V T_{AMB} = 85°C

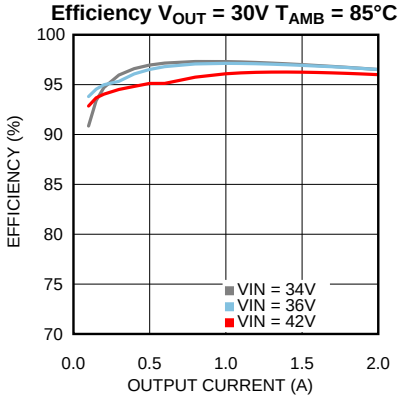


Figure 25.

Power Dissipation V_{OUT} = 30V T_{AMB} = 85°C

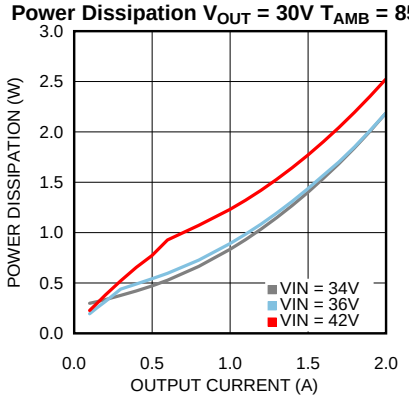


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.

Thermal Derating V_{OUT} = 12V, θ_{JA} = 16°C/W

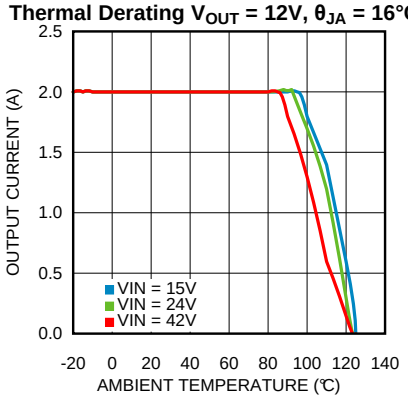


Figure 27.

Thermal Derating V_{OUT} = 12V, θ_{JA} = 20°C/W

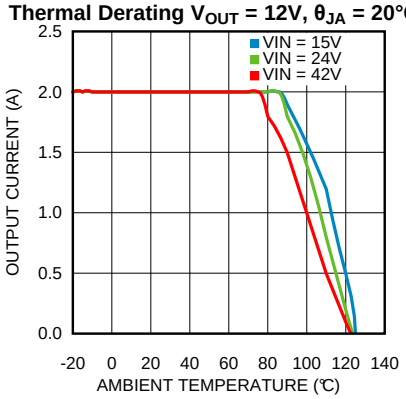


Figure 28.

Thermal Derating V_{OUT} = 24V, θ_{JA} = 16°C/W

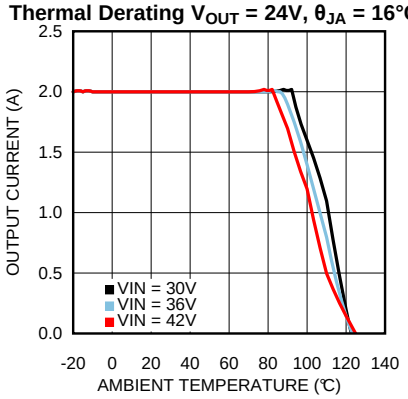


Figure 29.

Thermal Derating V_{OUT} = 24V, θ_{JA} = 20°C/W

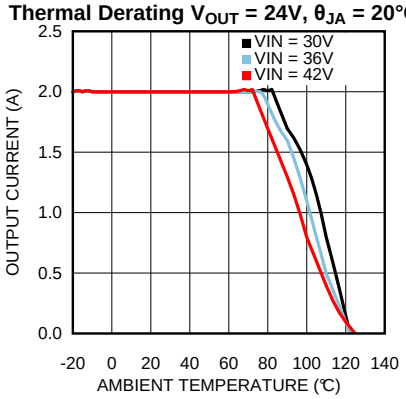


Figure 30.

Thermal Derating V_{OUT} = 30V, θ_{JA} = 16°C/W

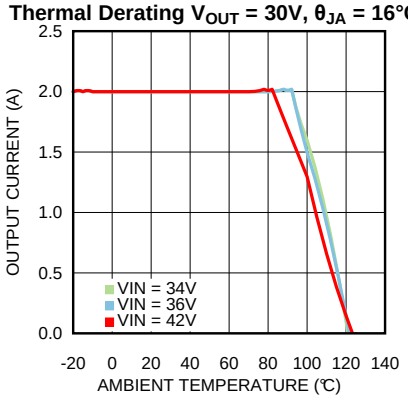


Figure 31.

Thermal Derating V_{OUT} = 30V, θ_{JA} = 20°C/W

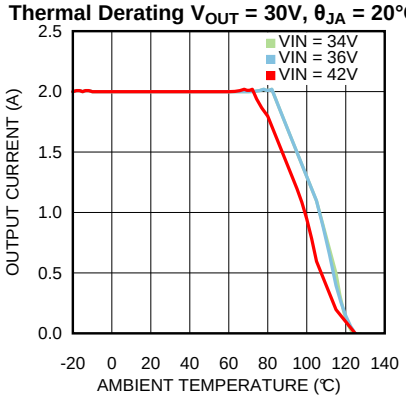


Figure 32.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.

Package Thermal Resistance θ_{JA}
4 Layer Printed Circuit Board with 1oz Copper

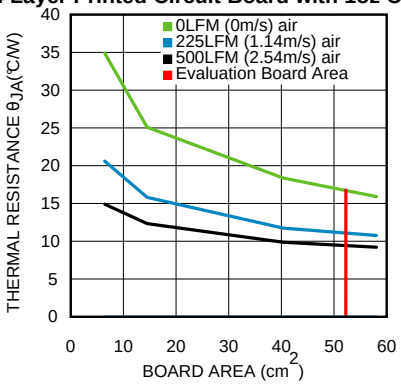


Figure 33.

Line and Load Regulation T_{AMB} = 25°C

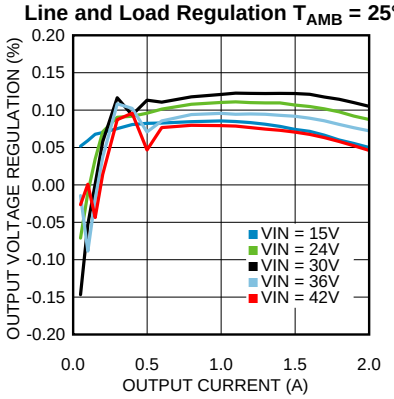


Figure 34.

Output Ripple
V_{IN} = 12V, I_{OUT} = 2A, Ceramic C_{OUT}, BW = 200 MHz

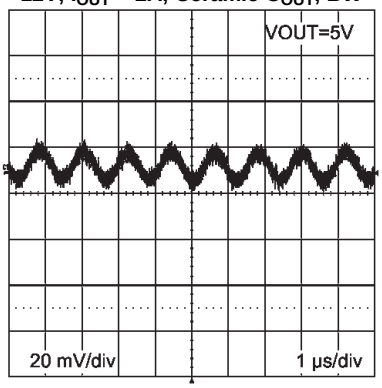


Figure 35.

Output Ripple
V_{IN} = 24V, I_{OUT} = 2A, Polymer Electrolytic C_{OUT}, BW = 200 MHz

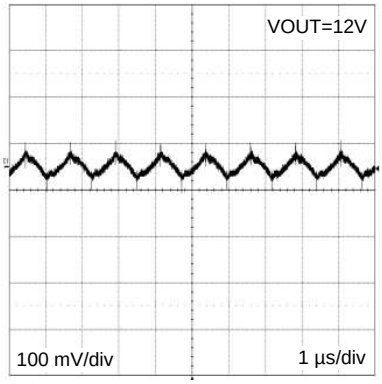


Figure 36.

Load Transient Response V_{IN} = 24V V_{OUT} = 12V
Load Step from 10% to 100%

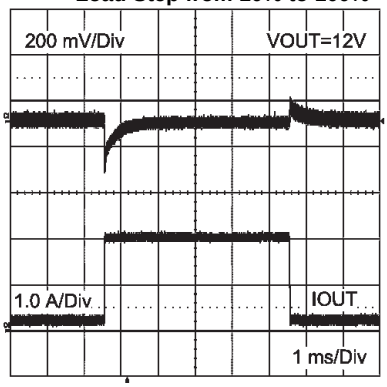


Figure 37.

Load Transient Response V_{IN} = 24V V_{OUT} = 12V
Load Step from 30% to 100%

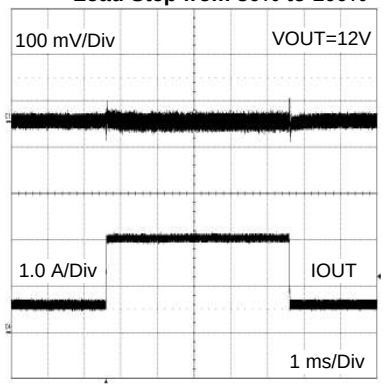


Figure 38.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.

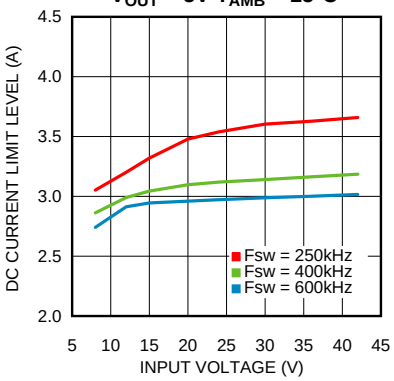


Figure 39.

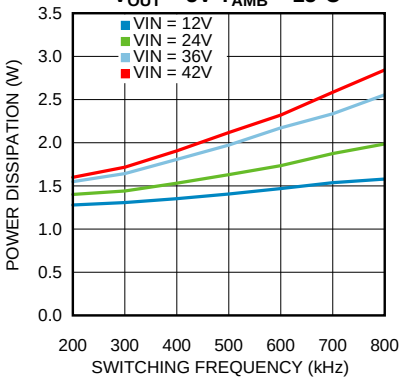


Figure 40.

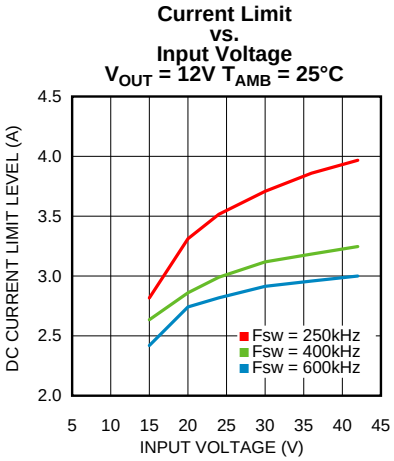


Figure 41.

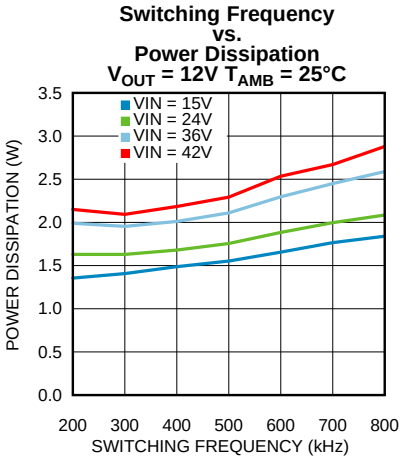


Figure 42.

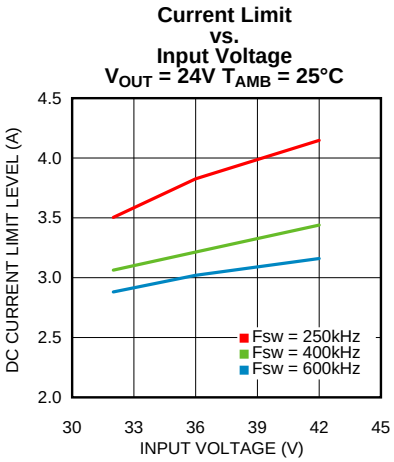


Figure 43.

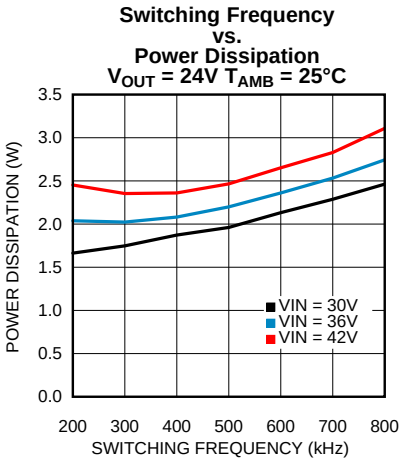


Figure 44.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 47uF; T_{AMB} = 25°C.

Startup
V_{IN} = 24V I_{OUT} = 2A

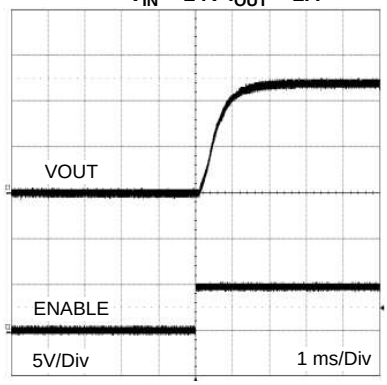


Figure 45.

Radiated EMI of Evaluation Board, V_{OUT} = 12V

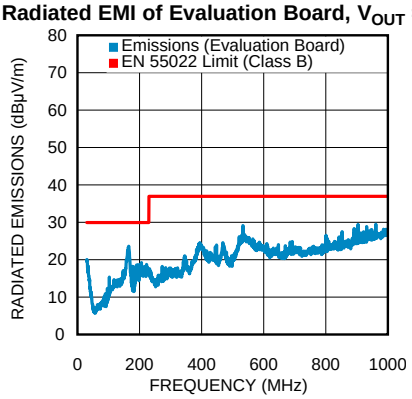


Figure 46.

Conducted EMI, V_{OUT} = 12V
Evaluation Board BOM and 3.3µH 2x10µF LC line filter

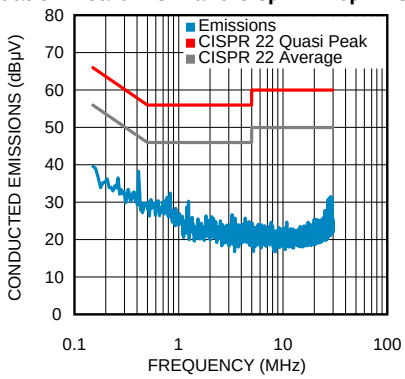
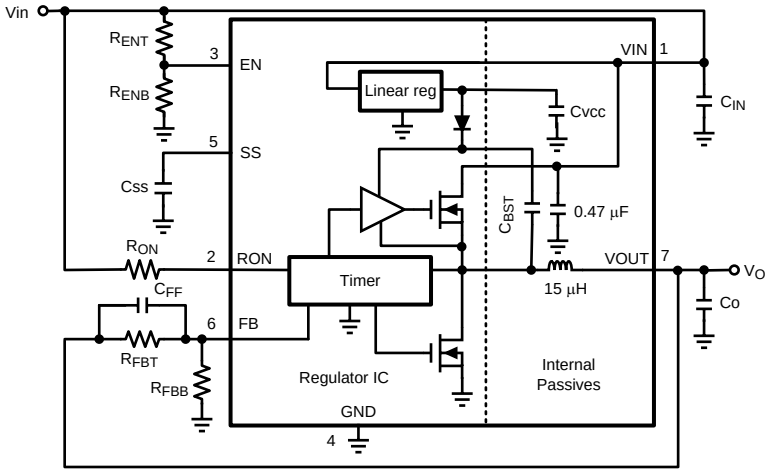


Figure 47.

APPLICATION BLOCK DIAGRAM



COT CONTROL CIRCUIT OVERVIEW

Constant On Time control is based on a comparator and an on-time one shot, with the output voltage feedback compared to an internal 0.8V reference. If the feedback voltage is below the reference, the high-side MOSFET is turned on for a fixed on-time determined by a programming resistor R_{ON}. R_{ON} is connected to V_{IN} such that on-time is reduced with increasing input supply voltage. Following this on-time, the high-side MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the on-time cycle is repeated. Regulation is achieved in this manner.

Design Steps for the LMZ14202H Application

The LMZ14202H is fully supported by Webench® which offers the following:

- Component selection
- Electrical simulation
- Thermal simulation
- Build-it prototype board for a reduction in design time

The following list of steps can be used to manually design the LMZ14202H application.

- Select minimum operating V_{IN} with enable divider resistors
- Program V_O with divider resistor selection
- Program turn-on time with soft-start capacitor selection
- Select C_O
- Select C_{IN}
- Set operating frequency with R_{ON}
- Determine module dissipation
- Layout PCB for required thermal performance

ENABLE DIVIDER, R_{ENT} AND R_{ENB} SELECTION

The enable input provides a precise 1.18V reference threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typ) of hysteresis resulting in a falling threshold of 1.09V. The maximum recommended voltage into the EN pin is 6.5V. For applications where the midpoint of the enable divider exceeds 6.5V, a small zener can be added to limit this voltage.

The function of the R_{ENT} and R_{ENB} divider shown in the Application Block Diagram is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14202H output rail. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\text{-}ENABLE} / 1.18V) - 1 \quad (1)$$

The EN pin is internally pulled up to VIN and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will guarantee smooth startup and will prevent overloading the input supply.

OUTPUT VOLTAGE SELECTION

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8V internal reference. In normal operation an on-time cycle is initiated when the voltage on the FB pin falls below 0.8V. The high-side MOSFET on-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8V. As long as the voltage at FB is above 0.8V, on-time cycles will not occur.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$V_O = 0.8V \times (1 + R_{FBT} / R_{FBB})$ (2)

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$R_{FBT} / R_{FBB} = (V_O / 0.8V) - 1$ (3)

These resistors should be chosen from values in the range of 1 kΩ to 50 kΩ.

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , and R_{ON} is included in the simplified applications schematic.

SOFT-START CAPACITOR, C_{SS}, SELECTION

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turn-on, after all UVLO conditions have been passed, an internal 8uA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady state operation is given by the formula:

$t_{SS} = V_{REF} \times C_{SS} / Iss = 0.8V \times C_{SS} / 8uA$ (4)

This equation can be rearranged as follows:

$C_{SS} = t_{SS} \times 8\ \mu A / 0.8V$ (5)

Use of a 4700pF capacitor results in 0.5ms soft-start duration. This is a recommended value. Note that high values of C_{SS} capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use Equation 18 below to find the DCM-CCM boundary load current for the specific operating condition. If a fast load transient response is desired for steps between DCM and CCM mode the softstart capacitor value should be less than 0.018µF.

As the soft-start input exceeds 0.8V the output of the power stage will be in regulation. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200 µA current sink:

- The enable input being “pulled low”
- Thermal shutdown condition
- Over-current fault
- Internal V_{IN}UVLO

OUTPUT CAPACITOR, C_O, SELECTION

None of the required output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst case RMS current rating of 0.5 x $I_{LR\ P-P}$, as calculated in Equation 19. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Low ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

CAPACITANCE:

Equation 6 provides a good first pass approximation of C_O for load transient requirements:

$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} — V_O) \times V_{OUT\text{-}TRAN})$ (6)

As an example, for 2A load step, V_{IN} = 24V, V_{OUT} = 12V, $V_{OUT\text{-}TRAN}$ = 50mV:

$C_O \geq 2A \times 0.8V \times 15\mu H \times 24V / (4 \times 12V \times (24V — 12V) \times 50mV)$

$C_O \geq 20\mu F$

ESR:

The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the over-voltage protection monitored at the FB pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid over-voltage protection during normal operation. The following equations can be used:

$$ESR_{MAX\text{-}RIPPLE} \leq V_{OUT\text{-}RIPPLE} / I_{LR\ P\text{-}P}$$

where

- $I_{LR\ P\text{-}P}$ is calculated using Equation 19 below (7)

$$ESR_{MAX\text{-}OVP} < (V_{FB\text{-}OVP} - V_{FB}) / (I_{LR\ P\text{-}P} \times A_{FB})$$

where

- A_{FB} is the gain of the feedback network from V_{OUT} to V_{FB} at the switching frequency. (8)

As worst case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1.

The selected capacitor should have sufficient voltage and RMS current rating. The RMS current through the output capacitor is:

$$I(C_{OUT(RMS)}) = I_{LR\ P\text{-}P} / \sqrt{12} \quad (9)$$

INPUT CAPACITOR, C_{IN}, SELECTION

The LMZ14202H module contains an internal 0.47 µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be located as close as possible to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst case input ripple current rating is dictated by Equation 10:

$$I(C_{IN(RMS)}) \cong 1 / 2 \times I_O \times \sqrt{(D / 1\text{-}D)}$$

where

- $D \cong V_O / V_{IN}$ (10)

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$).

Recommended minimum input capacitance is 10uF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain maximum value of input ripple voltage ΔV_{IN} to be maintained then Equation 11 may be used.

$$C_{IN} \geq I_O \times D \times (1\text{–}D) / f_{SW\text{-}CCM} \times \Delta V_{IN} \quad (11)$$

If ΔV_{IN} is 1% of V_{IN} for a 24V input to 12V output application this equals 240 mV and f_{SW} = 400 kHz.

$C_{IN} \geq$ 2A x 12V/24V x (1– 12V/24V) / (400000 x 0.240 V)

$C_{IN} \geq$ 5.2µF

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

ON TIME, R_{ON}, RESISTOR SELECTION

Many designs will begin with a desired switching frequency in mind. As seen in the Typical Performance Characteristics section, the best efficiency is achieved in the 300kHz-400kHz switching frequency range. Equation 12 can be used to calculate the R_{ON} value.

$$f_{SW(CCM)} \cong V_O / (1.3 \times 10^{-10} \times R_{ON}) \quad (12)$$

This can be rearranged as

$$R_{ON} \cong V_O / (1.3 \times 10^{-10} \times f_{SW(CCM)}) \quad (13)$$

The selection of R_{ON} and $f_{SW(CCM)}$ must be confined by limitations in the on-time and off-time for the COT Control Circuit Overview section.

The on-time of the LMZ14202H timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN} \quad (14)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the on-time at maximum V_{IN} is greater than 150 ns. The on-timer has a limiter to ensure a minimum of 150 ns for t_{ON}. This limits the maximum operating frequency, which is governed by Equation 15:

$$f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150 \text{ nsec}) \quad (15)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum on-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geq V_{IN(MAX)} \times 150 \text{ nsec} / (1.3 \times 10^{-10}) \quad (16)$$

If R_{ON} calculated in Equation 13 is less than the minimum value determined in Equation 16 a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.

Additionally, the minimum off-time of 260 ns (typ) limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

Discontinuous Conduction and Continuous Conduction Modes

At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the off-time. Note that during the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next on-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained since conduction and switching losses are reduced with the smaller load and lower switching frequency. Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \cong V_O \times (V_{IN}\text{-}1) \times 15\mu H \times 1.18 \times 10^{20} \times I_O / (V_{IN} - V_O) \times R_{ON}^2 \quad (17)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using Equation 12 above.

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O \times (V_{IN} - V_O) / (2 \times 15\mu H \times f_{SW(CCM)} \times V_{IN}) \quad (18)$$

The inductor internal to the module is 15µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\ P\text{-}P} = V_O \times (V_{IN} - V_O) / (15\mu H \times f_{SW} \times V_{IN})$$

where

- V_{IN} is the maximum input voltage and f_{SW} is determined from Equation 12. (19)

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

POWER DISSIPATION AND BOARD THERMAL REQUIREMENTS

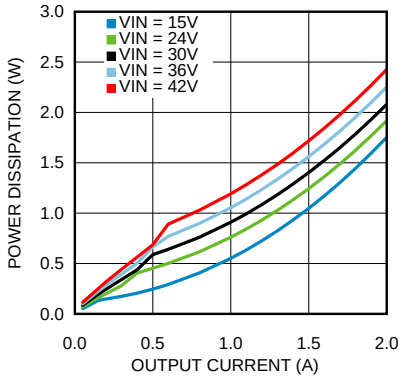
For a design case of V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 2A, T_{AMB} (MAX) = 85°C , and $T_{JUNCTION}$ = 125°C, the device must see a maximum junction-to-ambient thermal resistance of:

$$\theta_{JA\text{-}MAX} < (T_{J\text{-}MAX} - T_{AMB(MAX)}) / P_D$$

This $\theta_{JA\text{-}MAX}$ will ensure that the junction temperature of the regulator does not exceed $T_{J\text{-}MAX}$ in the particular application ambient temperature.

To calculate the required θ_{JA-MAX} we need to get an estimate for the power losses in the IC. The following graph is taken form the Typical Performance Characteristics section and shows the power dissipation of the LMZ14202H for V_{OUT} = 12V at 85°C T_{AMB}.

Figure 48. Power Dissipation V_{OUT} = 12V T_{AMB} = 85°C



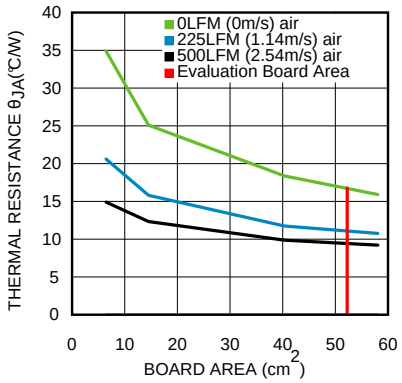
Using the 85°C T_{AMB} power dissipation data P_D for V_{IN} = 24V and V_{OUT} = 12V is estimated to be 1.8W. The necessary θ_{JA-MAX} can now be calculated.

θ_{JA-MAX} < (125°C - 85°C) / 1.8W

θ_{JA-MAX} < 22.2°C/W

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to the following Package Thermal Resistance graph. This graph is taken from the Typical Performance Characteristics section and shows how the θ_{JA} varies with the PCB area.

Figure 49. Package Thermal Resistance θ_{JA} 4 Layer Printed Circuit Board with 1oz Copper

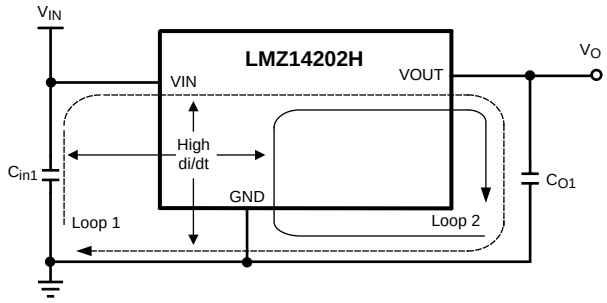


For θ_{JA-MAX}< 22.2°C/W and only natural convection (i.e. no air flow), the PCB area will have to be at least 30cm^2. This corresponds to a square board with approximately 5.5cm x 5.5cm (2.17in x 2.17in) copper area, 4 layers, and 1oz copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

For more guidelines and insight on PCB copper area, thermal vias placement, and general thermal design practices please refer to Application Note AN-2020 (http://www.ti.com/lit/an/snva419b/snva419b.pdf).

PC BOARD LAYOUT GUIDELINES

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.



1. Minimize area of switched current loops.

From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ14202H. Therefore place C_{IN1} as close as possible to the LMZ14202H VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. Have a single point ground.

The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. Minimize trace length to the FB pin.

Both feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the LMZ14202H to minimize noise pickup.

4. Make input and output bus connections as wide as possible.

This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 6 via array with minimum via diameter of 10mils (254 µm) thermal vias spaced 59mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

Additional Features

OUTPUT OVER-VOLTAGE COMPARATOR

The voltage at FB is compared to a 0.92V internal reference. If FB rises above 0.92V the on-time is immediately terminated. This condition is known as over-voltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET on-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

CURRENT LIMIT

Current limit detection is carried out during the off-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds I_{CL} the current limit comparator disables the start of the next on-time period. The next switching cycle will occur only if the FB input is less than 0.8V and the inductor current has decreased below I_{CL}. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds I_{CL}, further on-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer off-time. It should also be noted that DC current limit varies with duty cycle, switching frequency, and temperature.

THERMAL PROTECTION

The junction temperature of the LMZ14202H should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145 °C (typ Hyst = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

ZERO COIL CURRENT DETECTION

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

PRE-BIASED STARTUP

The LMZ14202H will properly start up into a pre-biased output. This is startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The pre-bias level of the output voltage must be less than the input UVLO set point. This will prevent the output pre-bias from enabling the regulator through the high side MOSFET body diode.

REVISION HISTORY

Changes from Revision C (February 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ14202HTZ/NOPB	ACTIVE	TO-PMOD	NDW	7	250	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ	Samples
LMZ14202HTZE/NOPB	ACTIVE	TO-PMOD	NDW	7	45	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ	Samples
LMZ14202HTZX/NOPB	ACTIVE	TO-PMOD	NDW	7	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

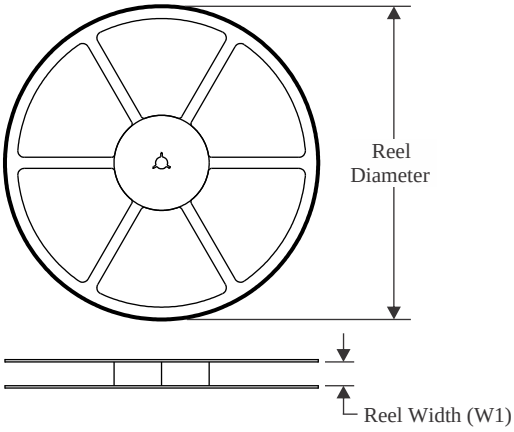
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

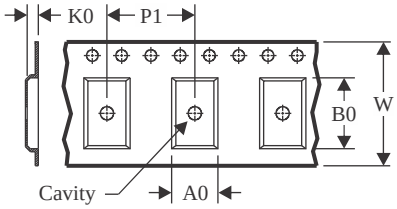
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

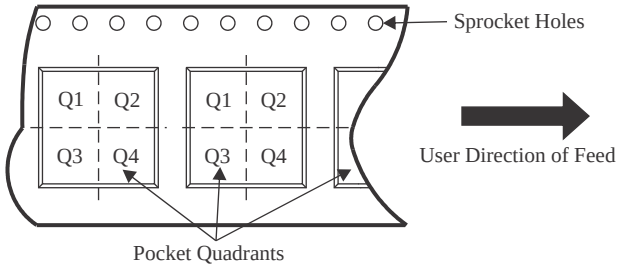


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

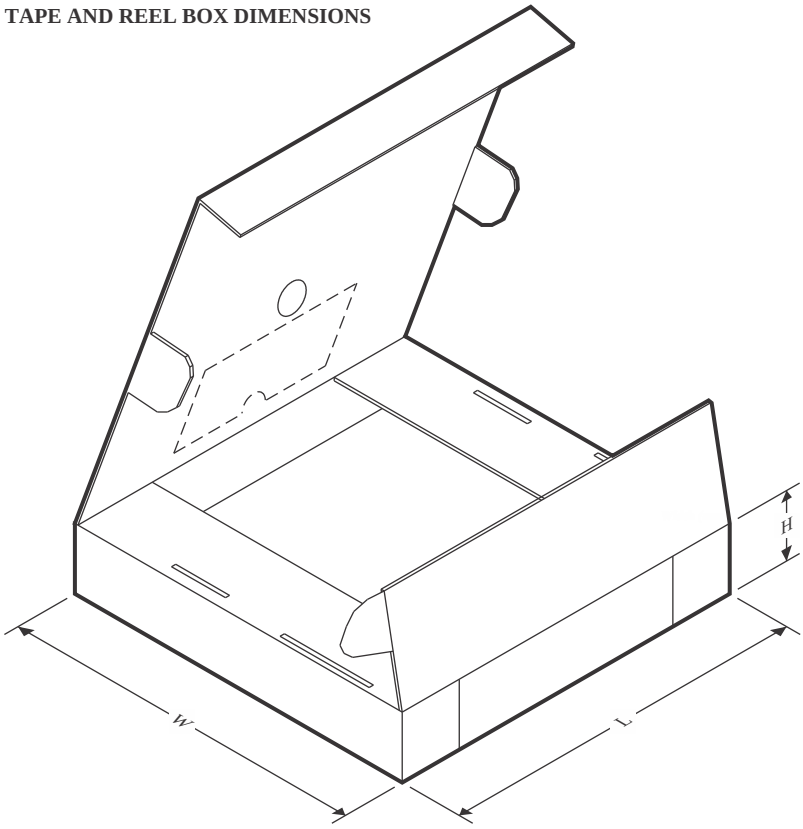
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ14202HTZ/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ14202HTZX/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

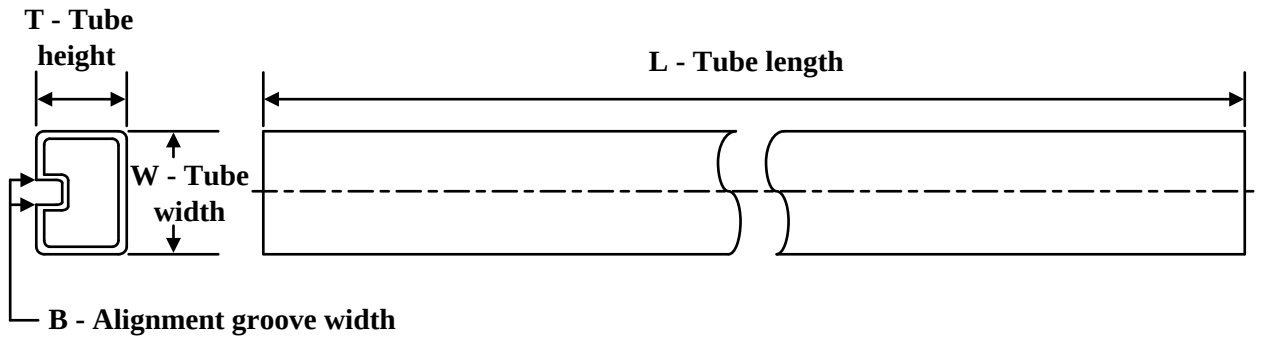
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ14202HTZ/NOPB	TO-PMOD	NDW	7	250	367.0	367.0	45.0
LMZ14202HTZX/NOPB	TO-PMOD	NDW	7	500	367.0	367.0	45.0

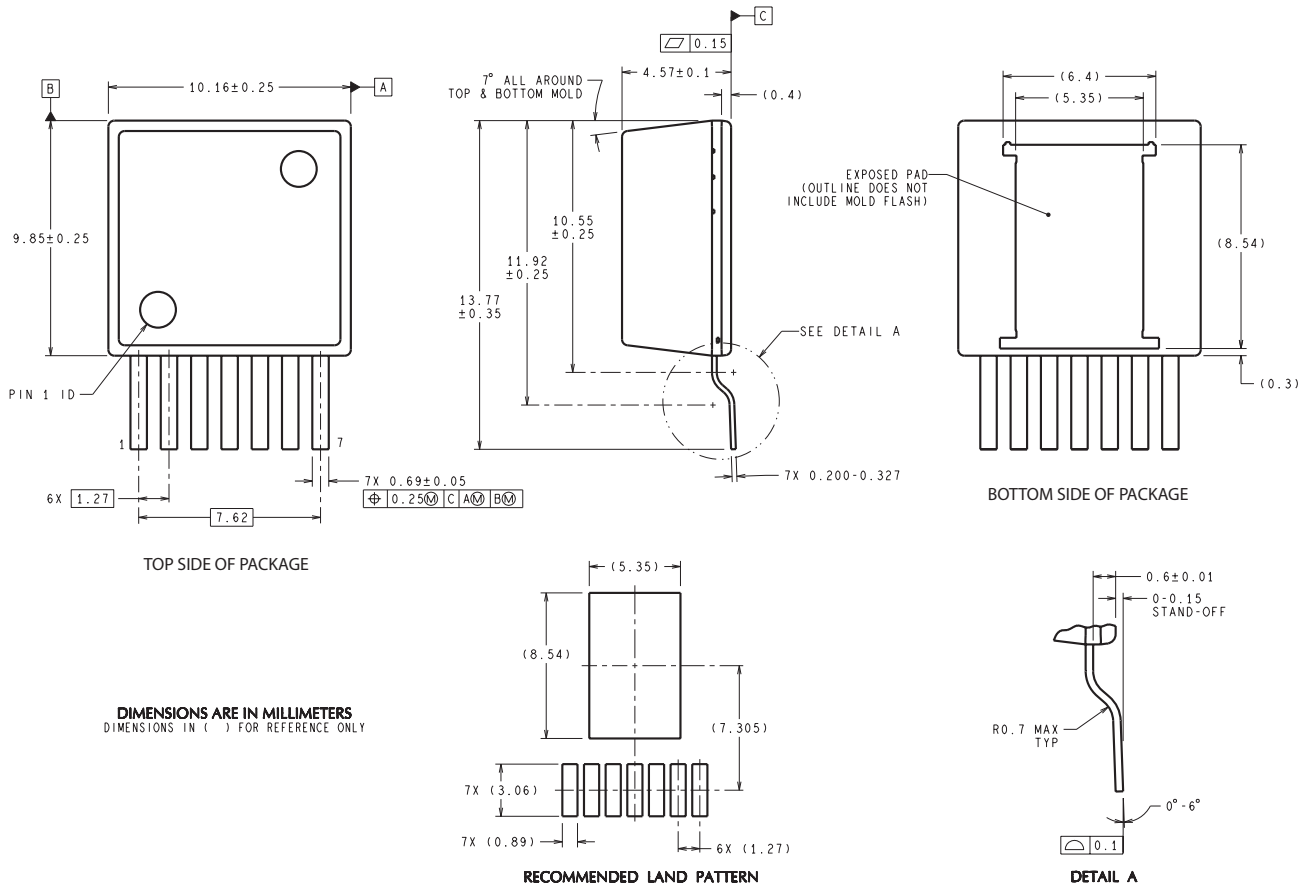
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMZ14202HTZE/NOPB	NDW	TO-PMOD	7	45	502	17	6700	8.4

NDW0007A



TZA07A (Rev D)

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