

CSD13306W 12V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低导通电阻
- 低 Q_g 和 Q_{gd}
- 1mm x 1.5mm 小尺寸封装
- 低高度（高度为 0.62mm）
- 无铅
- 符合 RoHS 环保标准
- 无卤素

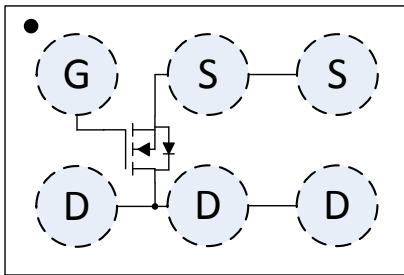
2 应用范围

- 电池管理
- 负载开关
- 电池保护

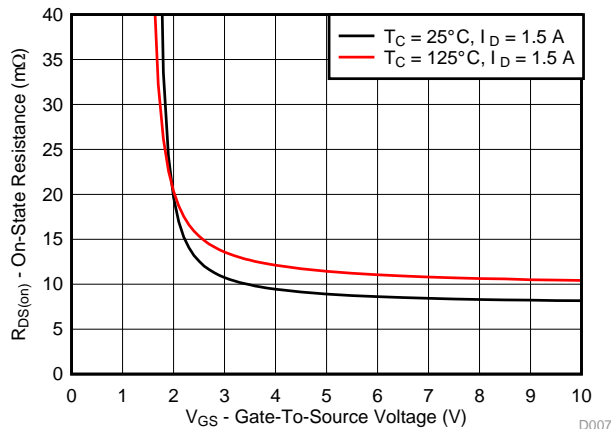
3 说明

这款 8.8mΩ、12V N 通道器件设计用于在超薄且具有出色散热特性的 1.5 mm × 1mm 小外形封装内提供最低的导通电阻和栅极电荷。

顶视图



$R_{DS(on)}$ 与 V_{GS} 间的关系



D007

产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	12		V
Q_g	栅极电荷总量 (4.5V)	8.6		nC
Q_{gd}	栅极电荷 (栅极到漏极)	3.0		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 2.5\text{V}$	12.9	mΩ
		$V_{GS} = 4.5\text{V}$	8.8	mΩ
$V_{GS(th)}$	电压阈值	1.0		V

订购信息⁽¹⁾

器件	数量	介质	封装	出货
CSD13306W	3000	7 英寸卷带	1.0mm x 1.5mm 晶圆级封装	卷带封装
CSD13306WT	250	7 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

最大绝对额定值

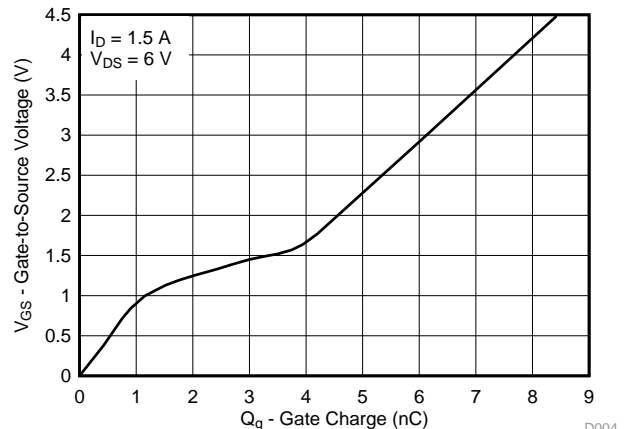
$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	12	V
V_{GS}	栅源电压	±10	V
I_D	持续漏极电流 ⁽¹⁾	3.5	A
I_{DM}	脉冲漏极电流 ⁽²⁾	44	A
P_D	功率耗散 ⁽³⁾	1.9	W
T_{stg}	储存温度范围	-55 至 150	°C
T_J	工作结温范围		

(1) 器件在 105°C 温度下运行

(2) $R_{\theta JA} = 230^\circ\text{C/W}$ (覆铜面积最小时的典型值)，脉宽 ≤ 100μs，占空比 ≤ 1%

(3) $R_{\theta JA} = 65^\circ\text{C/W}$ (覆铜面积最大时的典型值)

栅极电荷



D004



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4 修订历史记录

日期	修订版本	注释
2015 年 3 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise stated

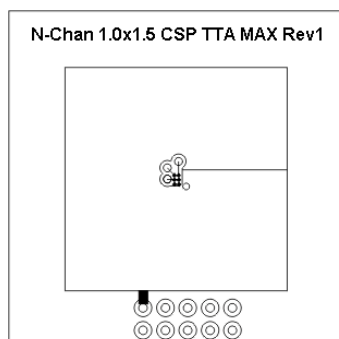
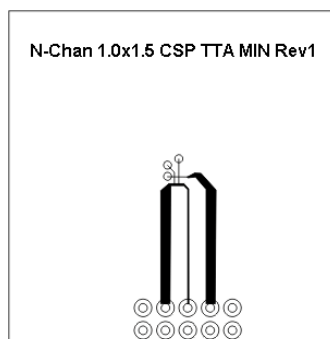
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	12			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 9.6\text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 10\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.7	1.0	1.3	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}, I_D = 1.5\text{ A}$		12.9	15.5	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 1.5\text{ A}$		8.8	10.2	m Ω
g_{fs}	Transconductance	$V_{DS} = 1.2\text{ V}, I_D = 1.5\text{ A}$		15		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 6\text{ V}, f = 1\text{ MHz}$		1050	1370	pF
C_{OSS}	Output Capacitance			324	421	pF
C_{RSS}	Reverse Transfer Capacitance			226	294	pF
R_g	Gate Resistance		4.2	8.4		Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 6\text{ V}, I_D = 1.5\text{ A}$		8.6	11.2	nC
Q_{gd}	Gate Charge Gate-to-Drain			3.0		nC
Q_{gs}	Gate Charge Gate-to-Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.2		nC
Q_{OSS}	Output Charge	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$		3.3		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 1.5\text{ A}$ $R_G = 4\ \Omega$		7		ns
t_r	Rise Time			11		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			8		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	$I_S = 1.5\text{ A}, V_{GS} = 0\text{ V}$		0.7	1.0	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 6\text{ V}, I_F = 1.5\text{ A}, di/dt = 200\text{ A}/\mu\text{s}$		14.8		nC
t_{rr}	Reverse Recovery Time			23		ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ unless otherwise stated

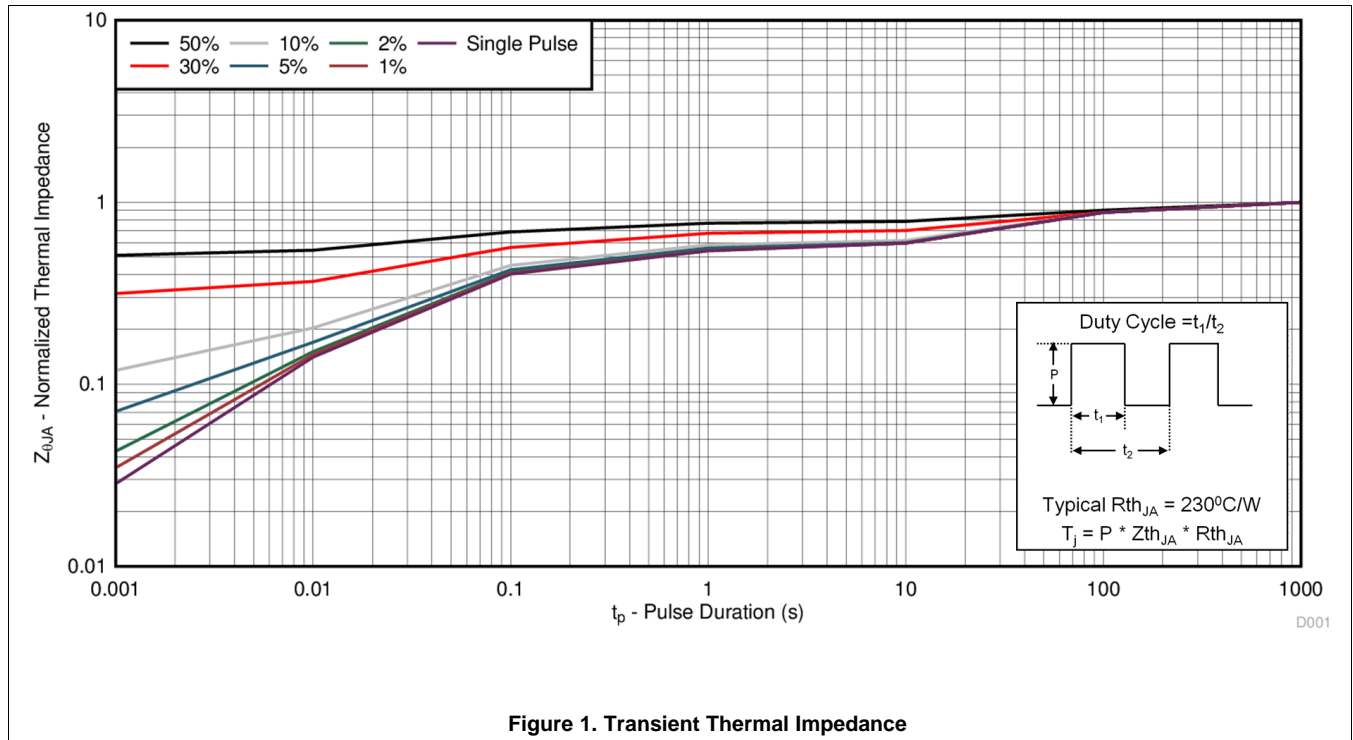
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾		230		$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance ⁽²⁾		65		

(1) Device mounted on FR4 material with minimum Cu mounting area

(2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

Typ $R_{\theta JA} = 65^\circ\text{C}/\text{W}$
when mounted on
1 inch² of 2 oz. Cu.

Typ $R_{\theta JA} = 230^\circ\text{C}/\text{W}$
when mounted on
minimum pad area of
2 oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

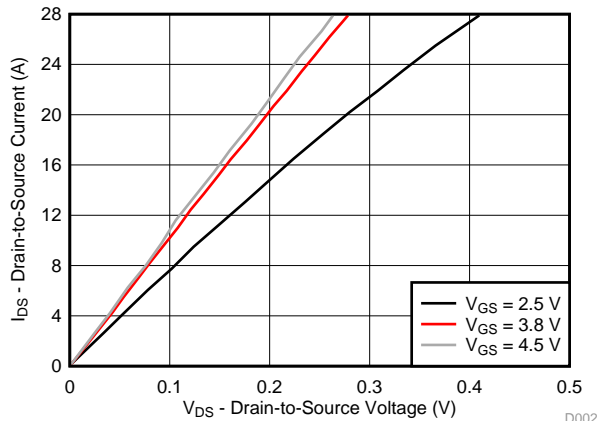


Figure 2. Saturation Characteristics

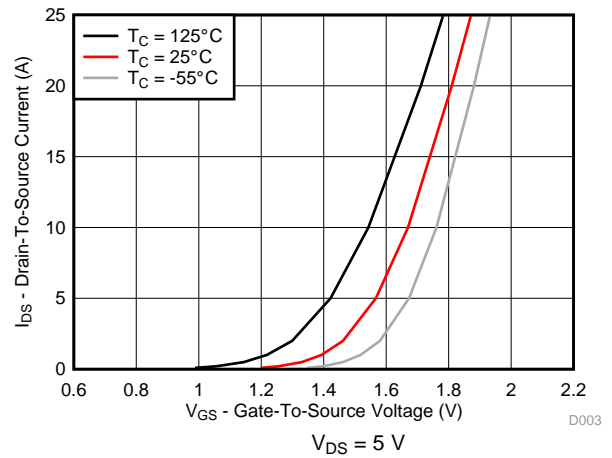


Figure 3. Transfer Characteristics

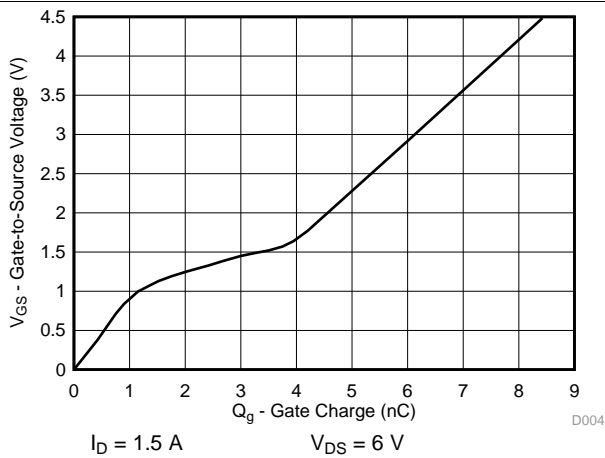


Figure 4. Gate Charge

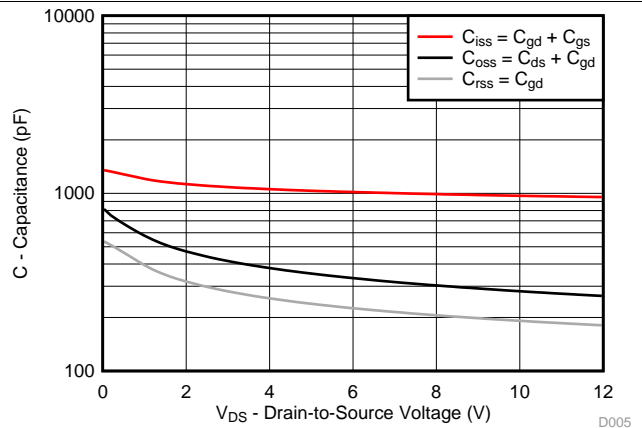


Figure 5. Capacitance

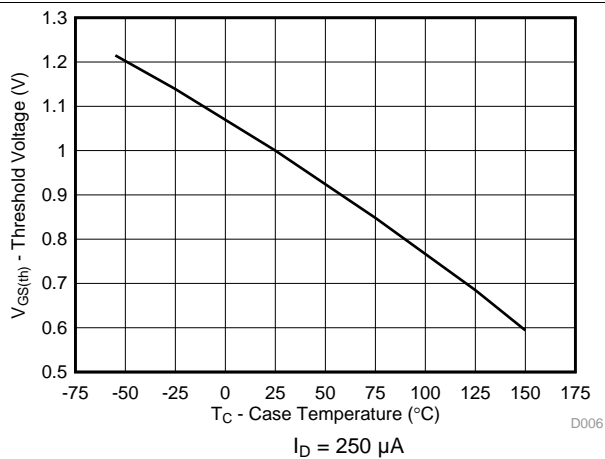


Figure 6. Threshold Voltage vs Temperature

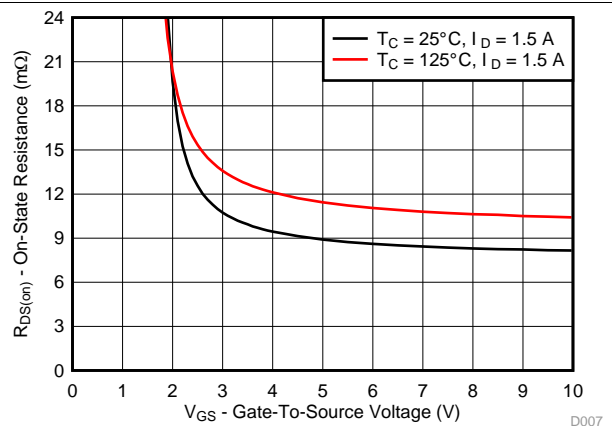
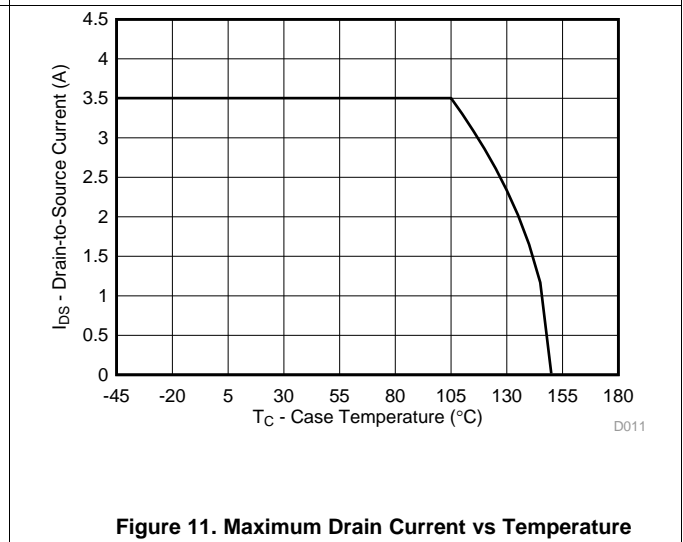
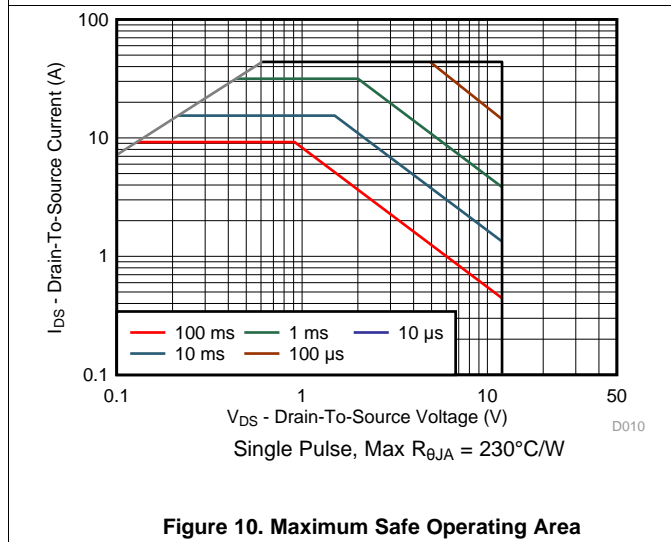
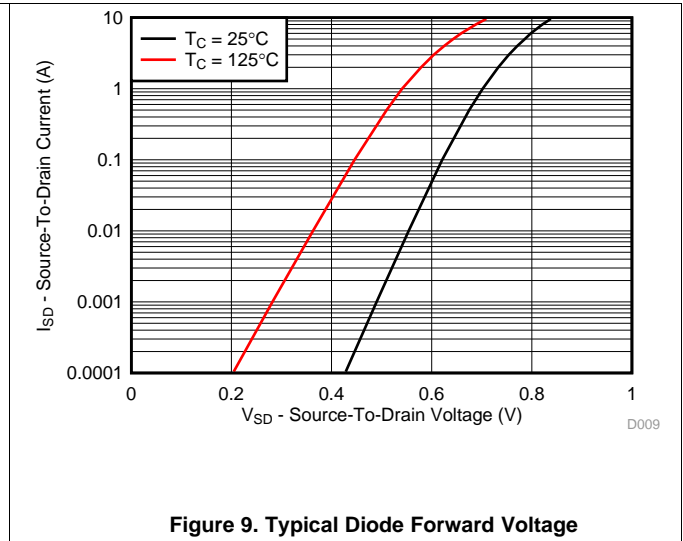
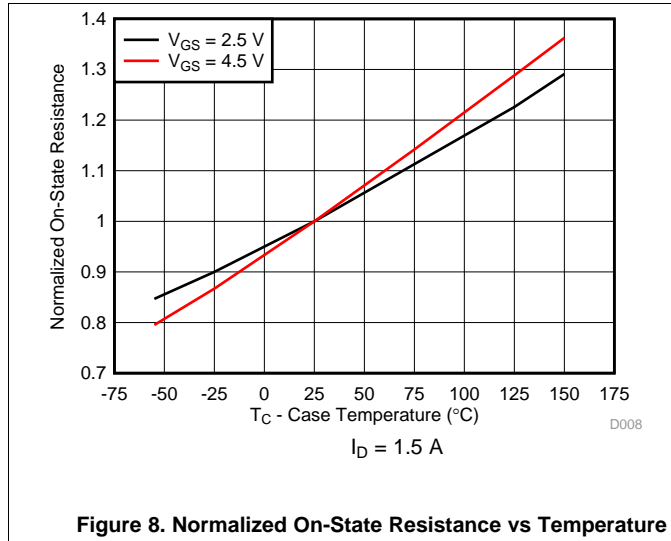


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

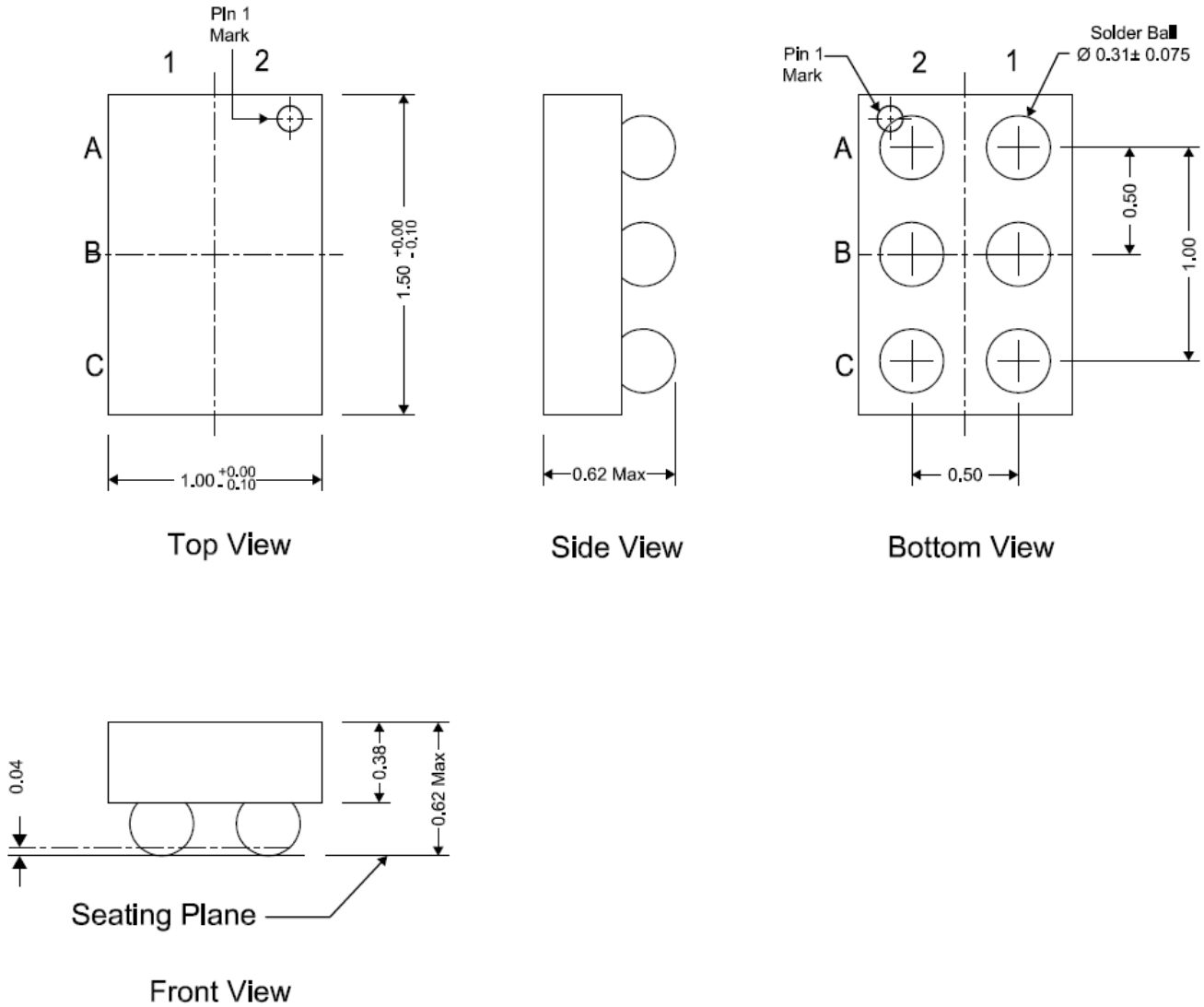
[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 CSD13306W 封装尺寸

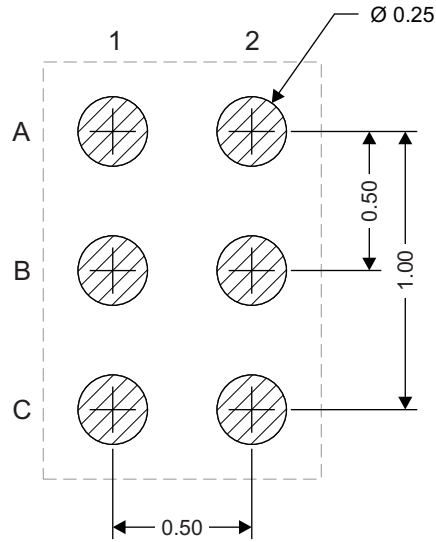


NOTE: 全部尺寸单位为 mm (除非另外注明)

引脚分配

位置	名称
C2, B2	源极
A2	栅极
A1, B1, C1	漏极

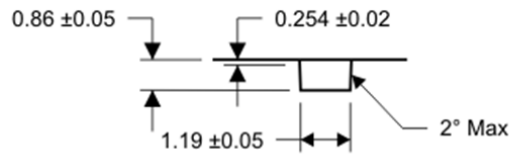
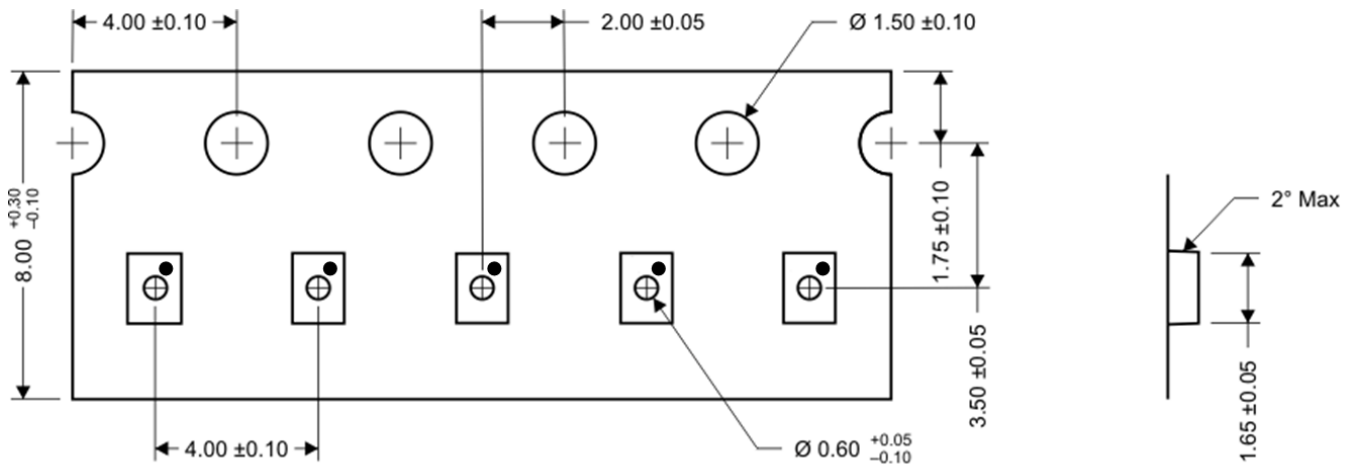
焊盘布局建议



M0158-01

NOTE: 全部尺寸单位为 mm (除非另外注明)

7.2 卷带信息



M0159-01

NOTE: 全部尺寸单位为 mm (除非另外注明)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13306W	ACTIVE	DSBGA	YZC	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		13306	Samples
CSD13306WT	ACTIVE	DSBGA	YZC	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	13306	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

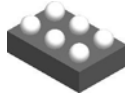
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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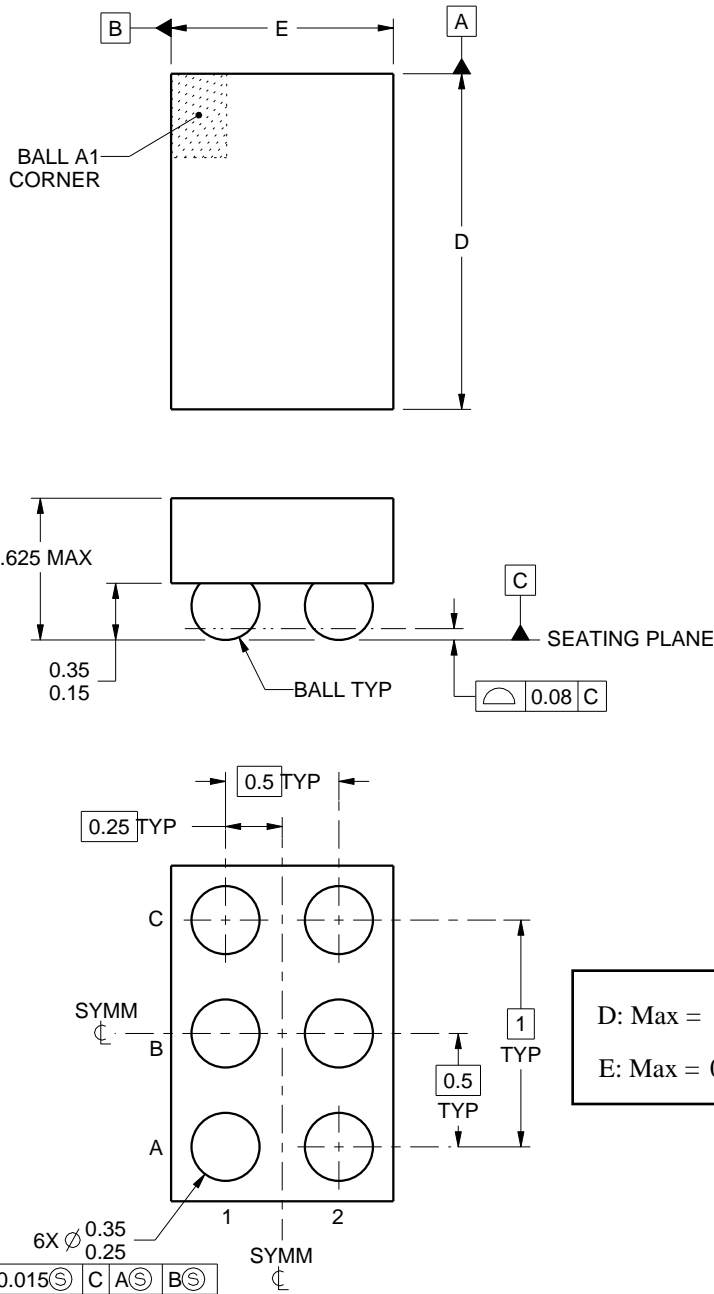
YZC0006



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.49 mm, Min = 1.43 mm
 E: Max = 0.996 mm, Min = 0.936 mm

4219522/A 02/2015

NOTES:

NanoFree is a trademark of Texas Instruments.

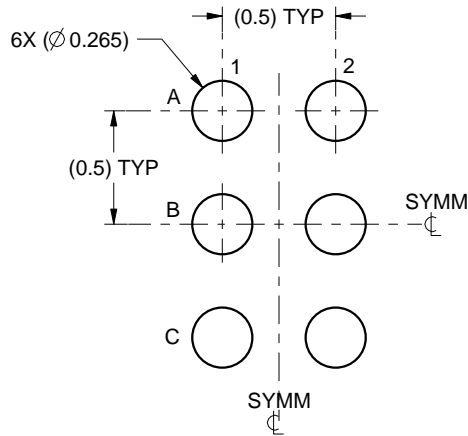
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

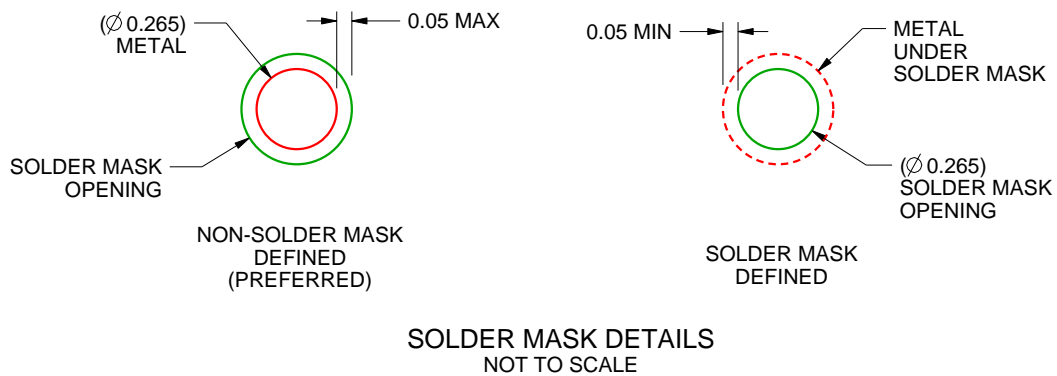
YZC0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

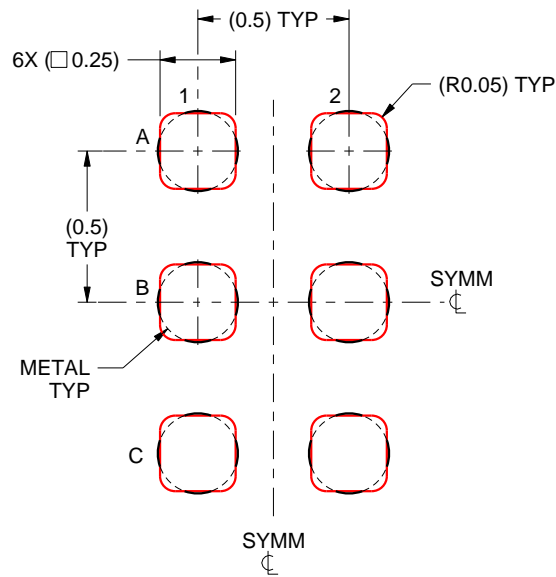
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZC0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

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