LM8850 High-Performance, Step-Up DC-DC Converter for High-Power Applications in Mobile Devices

Check for Samples: LM8850

FEATURES

- 6µA typ. Quiescent Current
- V_{OUT} = 3.6V to 5.7V (max V_O = 5.7V)
- Operates from a Single Lithium Ion Cell (2.3V to 5.5V)
- 8 User-selectable Output Voltages via I^2C
- High-speed 3.4 MHz I^2C-compatible Interface
- Up to 1.0A Maximum Load Current Capability
- 4 Levels of Current Limiting
- Auto-mode Operation and Forced PWM
- 2.5 MHz Switching Drequency (typ.)
- ±2.5% DC Output Voltage Precision
- 1.0 µH Inductor (2520 Case Size)
- 4.7 µF Input and Output Capacitors (0603 case size)
- PGOOD Signal
- True Shutdown Isolation
- Output Over-voltage Protection
- Internal Active Voltage Balancing for Supercapacitors
- DSBGA 9-bump Package
  - (1.58 mm x 1.62 mm x 0.35 mm)(0.5 mm pitch)

APPLICATIONS

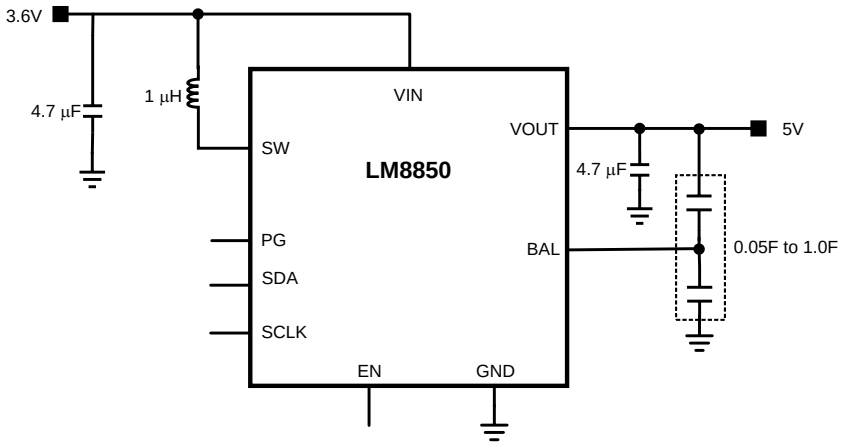
- Flash LED
- Mobile Phones
- WiMAX
- USB
- Audio Amplifier

DESCRIPTION

LM8850 is a step-up DC-DC converter optimized for use with a supercapacitor to protect a battery from power surges and enable new high power applications in mobile device architectures. The device creates an ideal rail from 3.6V to 5.7V boosting from a single Li-Ion cell with an input voltage range of 2.3V to 5.5V; Target V_{OUT} must be at least 10% higher than V_{IN}.

An I^2C interface controlling multiple output voltage settings, input current limits, and load currents up to 1A provides superior user flexibility. The LM8850 operates in Auto mode, where the converter is in PFM mode at light loads and switches to PWM mode at heavy loads. Hysteretic PFM extends the battery life by reduction of the quiescent current to 6µA (typ.) during light load and standby conditions. Synchronous operation provides true shutdown isolation and improves its efficiency at medium-to-full load conditions.

Typical Application Circuit



DESCRIPTION (CONTINUED)

High-switching frequency enables smaller passive components. Internal compensation is used for a broader range of inductor and output capacitor values to meet system demand and achieve small system solution size.

LM8850 is available in a 9-bump ultra-thin DSBGA package. Only four external surface-mount components, a 1.0 µH inductor, a 4.7 µF for input capacitor, 4.7 µF for output capacitor and 0.05F-1.0F supercapacitor for energy storage are required.

Connection Diagram

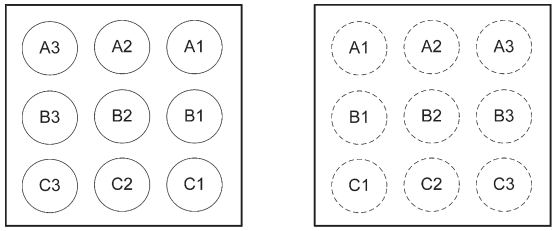


Figure 1. 9-Bump Ultra-Thin DSBGA Package
See Package Number YPD0009

PIN DESCRIPTIONS

Pin #	Name	Description
A1	VIN	Power Supply Input. Connect to input filter capacitor (See Typical Application Circuit)
A2	SW	Switching node. Connection to the internal NFET switch and PFET synchronous rectifier
A3	GND	Ground Pin
B1	SDA	I^2C data (Use a 2kΩ pull-up resistor)
B2	PG	Power Good indicator
B3	VOUT	Output pin.
C1	SCLK	I^2C Clock (Use a 2kΩ pull-up resistor)
C2	EN	Enable pin. The device is in shutdown when voltage to this pin is <0.4V and enabled when >1.2V. Do not leave this pin floating.
C3	BAL	Balancing pin for active voltage balancing of supercapacitor

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VIN Pin to GND		−0.2V to 6.5V
EN, PG, SDA, SCLK pins to GND		−0.2V to 6.0V
VOUT to GND		(GND−0.2V) to 6.5V
SW pin to GND		−0.2V to 6.5V
BAL to GND		−0.2V to VOUT
Junction Temperature (T_{J-MAX})		+150°C
Storage Temperature Range		−65°C to +150°C
Continuous Power Dissipation(3)		Internally Limited
Maximum Lead Temperature (Soldering, 10 sec.)		260°C
ESD Rating(4)	Human Body Model	2kV
	Machine Model	200V
	Charged Device Model	500V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 140°C (typ.).
(4) The Human Body Model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883–3015.7.

Operating Ratings(1)(2)

Input Voltage Range	2.3V to 5.5V
Recommended Load Current	0mA to 1.0A
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range(3)	−40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction-to-ambient thermal resistance of the part/package (θ_{JA}) in the application, as given by the following equation: $T_{A-MAX} = T_{J-MAX} - (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) (DSBGA)(1)	70°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.

Electrical Characteristics (1)(2)(3)(4)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the operating junction temperature range (−40°C ≤ T_J = T_A ≤ +85°C). Unless otherwise noted, specifications apply to the LM8850 open loop Typical Application Circuit with V_{IN} = EN = 3.6V.

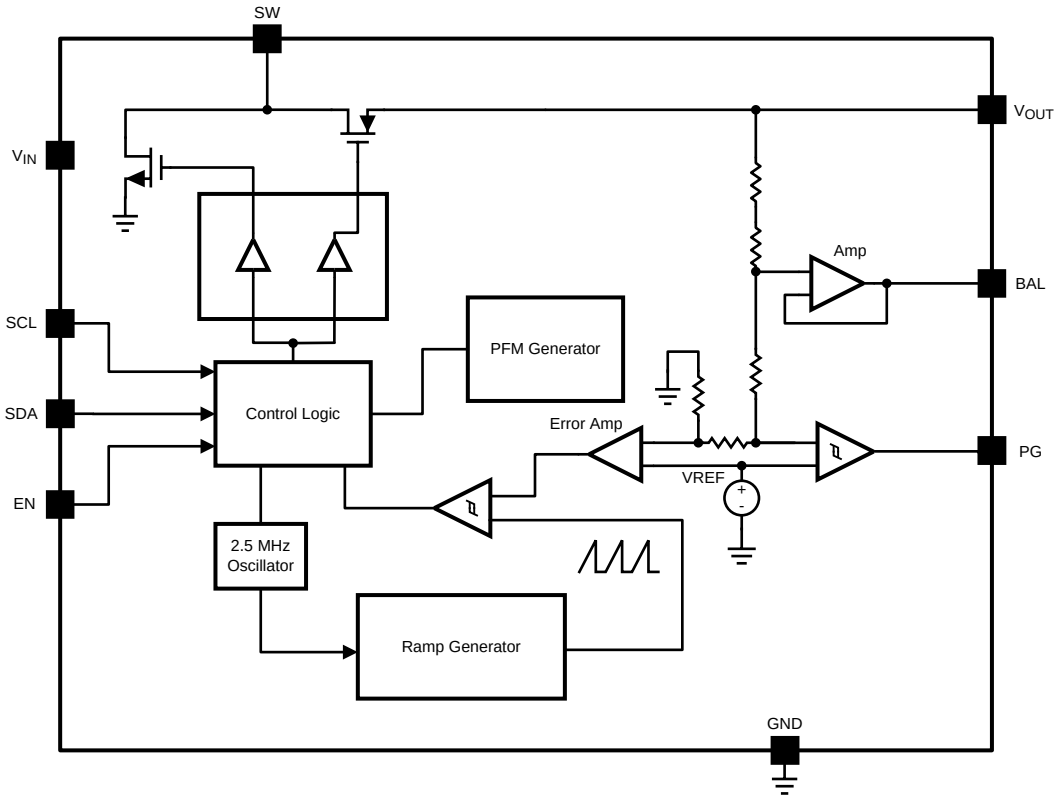
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage	I_{OUT} = 0mA, V_{OUT} = 5V	**-2.5**		**+2.5**	%
V_{OUT}	Output Voltage Range Register 0	VSEL bits = 0 0 0		3.6		V
		VSEL bits = 0 0 1		3.9		
		VSEL bits = 0 1 0		4.2		
		VSEL bits = 0 1 1		4.5		
	Output Voltage Range Register 1	VSEL bits = 1 0 0		4.7		
		VSEL bits = 1 0 1		5.0		
		VSEL bits = 1 1 0		5.3		
		VSEL bits = 1 1 1		5.7		
I_{SHDN}	Shutdown Supply Current			0.4	**3**	µA
I_{Q_PFM}	Quiescent Current in PFM Mode			6	**10**	
I_{Q_PWM}	Quiescent Current in PWM Mode			330	**500**	
$R_{DSON\ (NFET)}$	Pin-Pin Resistance for Sync NFET	V_{IN} = V_{GS} = 3.6V		200		mΩ
$R_{DSON\ (PFET)}$	Pin-Pin Resistance for PFET	V_{IN} = V_{GS} = 5.0V		215		
I_{LIM}	Switch Peak Current Limit	ISEL bits = 111 VIN = 4.5V	**1350**	1500	**1650**	mA
		ISEL bits = 101 VIN = 4.5V	**923**	1025	**1128**	
		ISEL bits = 011 VIN = 4.5V	**666**	740	**814**	
		ISEL bits = 001 VIN = 4.5V	**477**	530	**583**	
T_{ON}	Turn on Time	T_{ON} = 00		5		secs.
		T_{ON} = 01		7.5		
		T_{ON} = 10		10		
		T_{ON} = 11		12.5		
I_{EN}	Pin Input current	EN		0.01	1	µA
F_{OSC}	Internal Oscillator Frequency		**2.25**	2.5	**2.75**	MHz
V_{IH}	Logic High Input		**1.2**			V
V_{IL}	Logic Low Input				**0.4**	
V_{OH}	Logic Output High		**1.2**			
V_{OL}	Logic Input High				**0.4**	

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) The parameters in the electrical characteristic table are tested under open loop conditions at V_{IN} = 3.6V unless otherwise specified. For performance over the input voltage range and closed loop condition, refer to the datasheet curves.
(4) Open-loop Electrical Characteristics taken without supercapacitor.

Table 1. Dissipation Rating Table

θ_{JA}	T_A ≤ 25°C Power Rating	T_A ≤ 60°C Power Rating	T_A ≤ 85°C Power Rating
70°C/W	1500 mW	980 mW	600 mW

Block Diagram



Typical Performance Characteristics

Unless otherwise noted: V_{OUT} = 5.0V, T_A = 25°C, Supercapacitor = TDK EDLC272020–501–2F-50).

I_q Shutdown

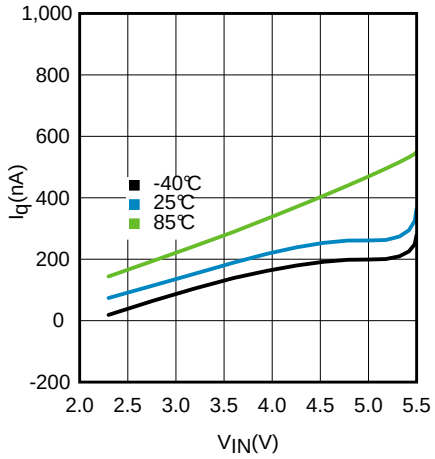


Figure 2.

I_q, PFM, No Load

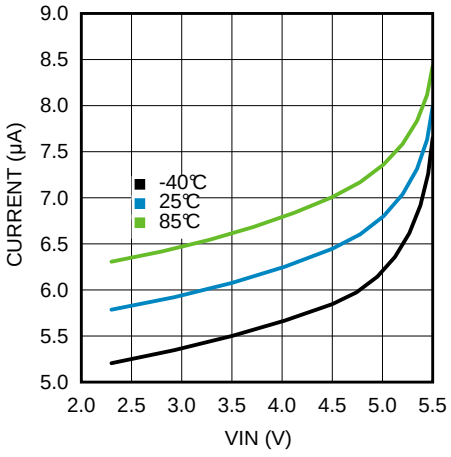


Figure 3.

I_q, PWM

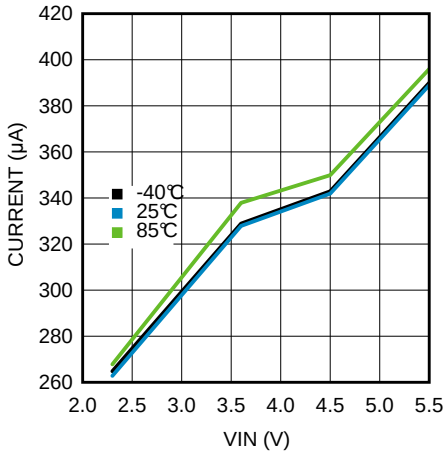


Figure 4.

Efficiency, V_{OUT} = 5V, PWM Mode, 25°C

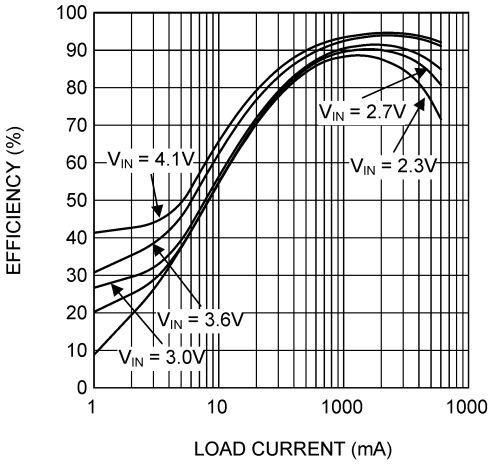


Figure 5.

Efficiency Room temp, 100 mV PFM ripple

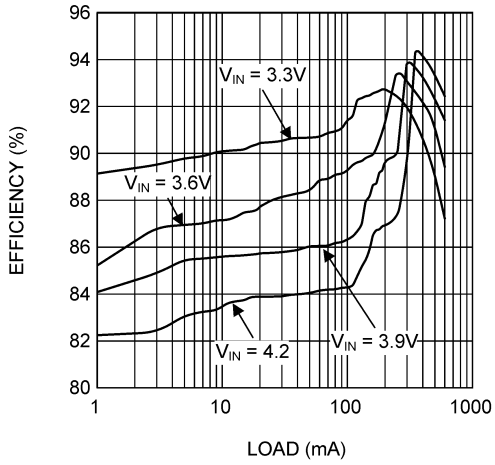


Figure 6.

Efficiency over PFM ripple, V_{IN} = 3.9V, Room Temp

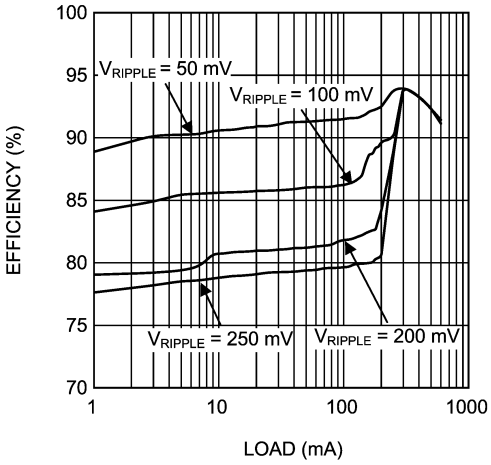


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise noted: V_{OUT} = 5.0V, T_A = 25°C, Supercapacitor = TDK EDLC272020–501–2F-50).

Line Regulation, V_{OUT} 5V
V_{IN} = 3.6V, 100 mV Ripple, Auto Mode

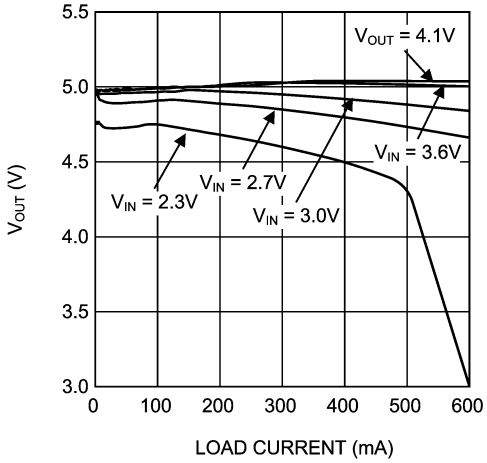


Figure 8.

Load Regulation, V_{OUT} 5V,
V_{IN} = 3.6V, 100 mV Ripple, Auto Mode

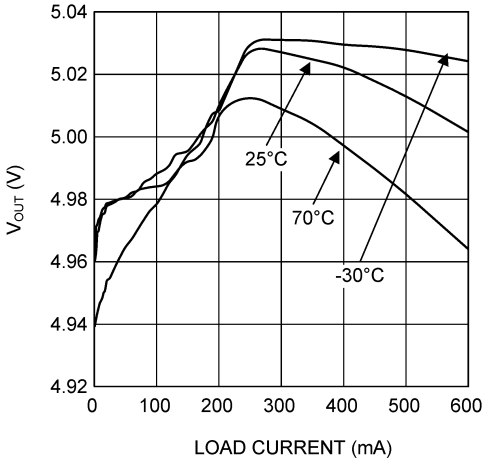


Figure 9.

Line Regulation, V_{OUT} 5V,
250 mA Load, 100 mV Ripple, Auto Mode

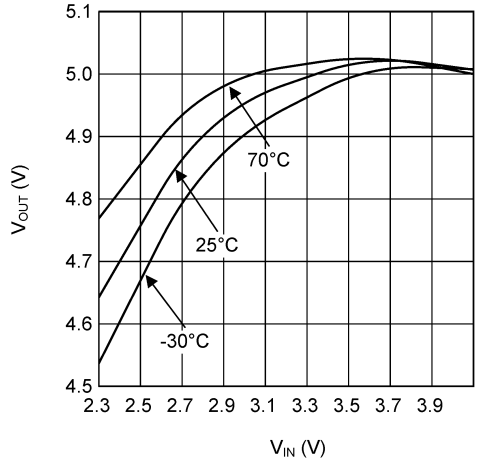


Figure 10.

Osc Freq Error Normalized to 3.6V

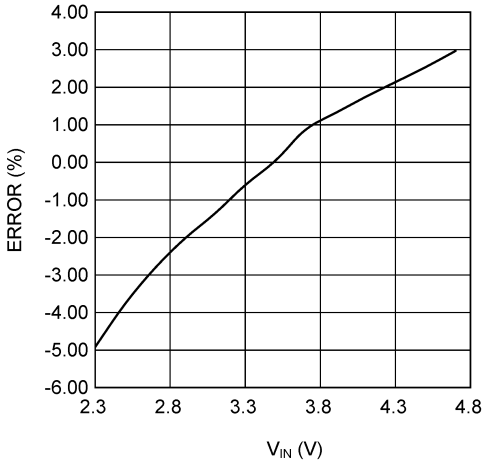


Figure 11.

Startup V_{IN} 2.7V, V_{OUT} 5.3V,
5sec Delay, Room Temp

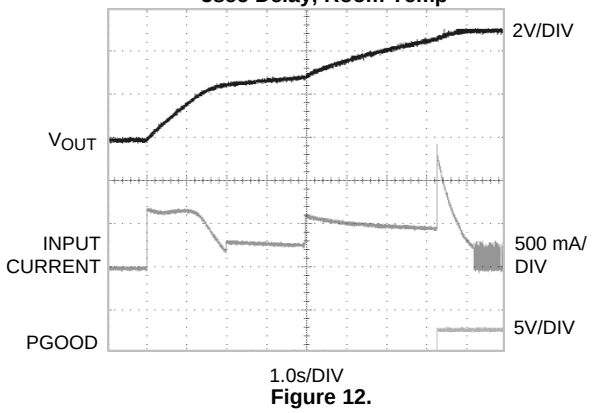


Figure 12.

Startup V_{IN} 3.6V, V_{OUT} 5.0V,
5sec Delay, Room Temp

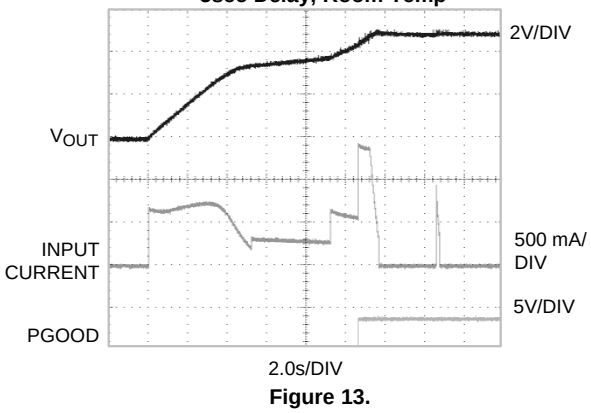


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise noted: V_{OUT} = 5.0V, T_A = 25°C, Supercapacitor = TDK EDLC272020–501–2F-50).

Input Current and V_{OUT}, 1.5A Current Limit

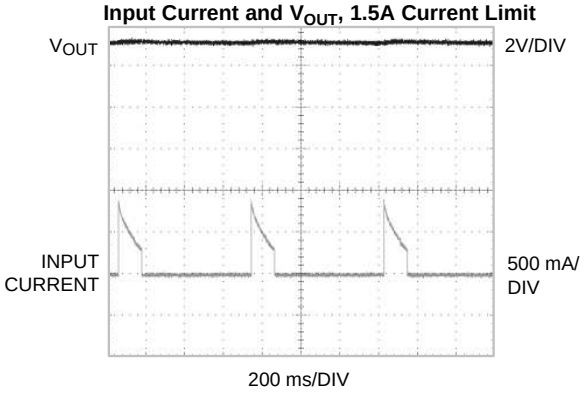


Figure 14.

Input Current and V_{OUT}, 500 mA Current Limit

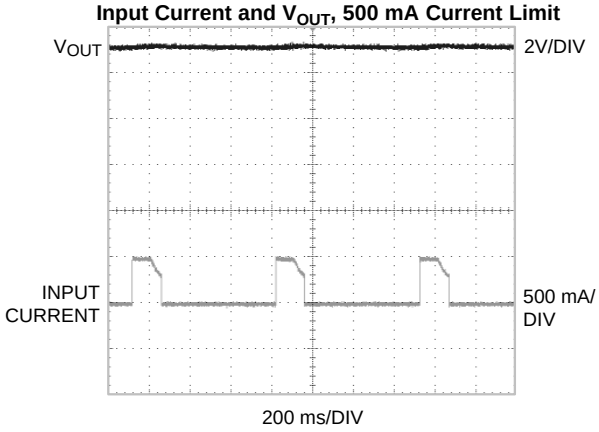


Figure 15.

Line Transient
V_{IN} 2.7V - 3.6V, I_{LOAD} = 600 mA

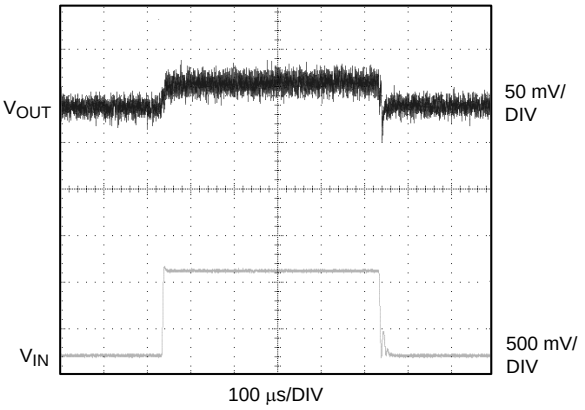


Figure 16.

Line Transient
V_{IN} 3.6V - 4.2V, I_{LOAD} = 600 mA

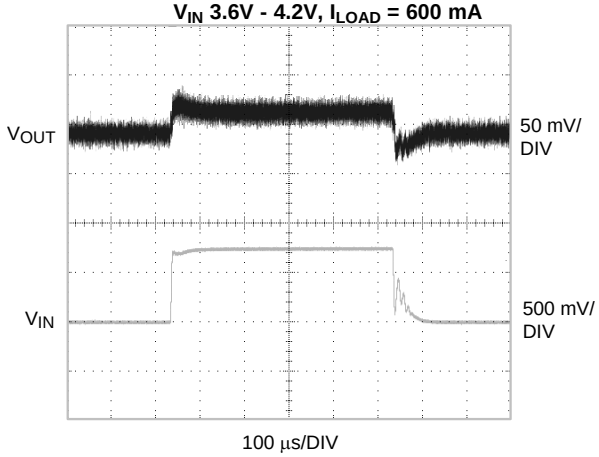


Figure 17.

Load Transient
V_{IN} = 2.7V, V_{OUT} 5.0V, I_{LOAD} 0-1000 mA

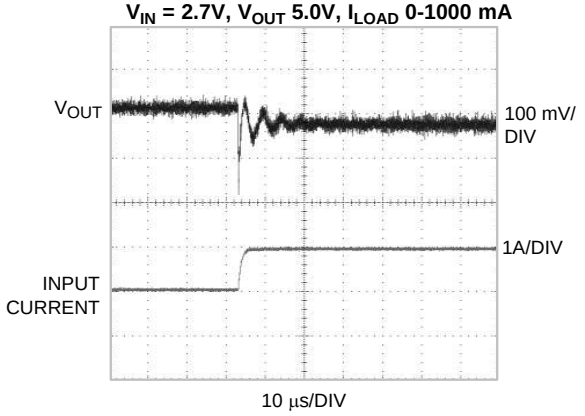


Figure 18.

Load Transient
V_{IN} = 2.7V, V_{OUT} 5.0V, I_{LOAD} 1000-0 mA

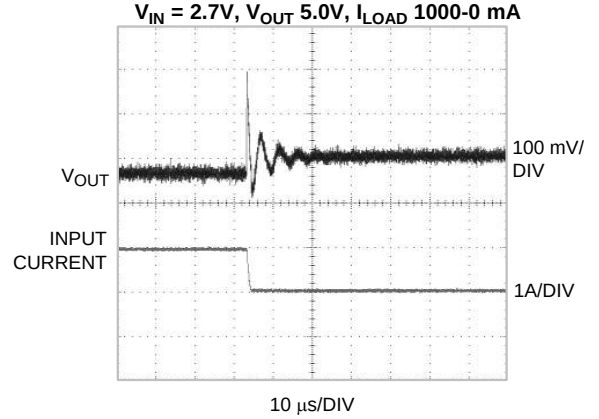


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise noted: V_{OUT} = 5.0V, T_A = 25°C, Supercapacitor = TDK EDLC272020–501–2F-50).

Load Transient
V_{IN} = 3.6V, V_{OUT} 5.0V, I_{LOAD} 200-800 mA

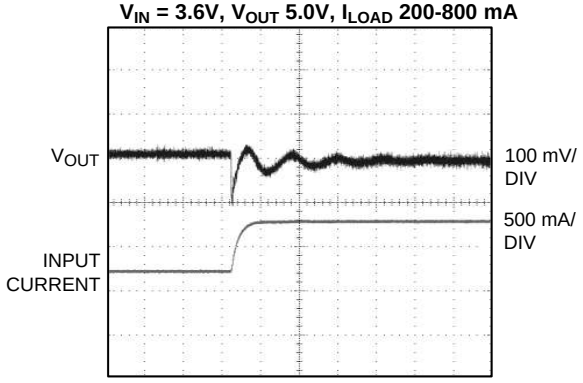


Figure 20.

Load Transient
V_{IN} = 3.6V, V_{OUT} 5.0V, I_{LOAD} 800-200 mA

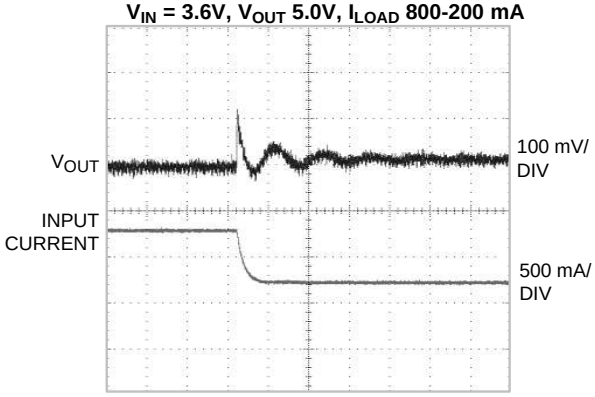


Figure 21.

Load Transient
V_{IN} = 4.2V, V_{OUT} 5.0V, I_{LOAD} 0-200 mA

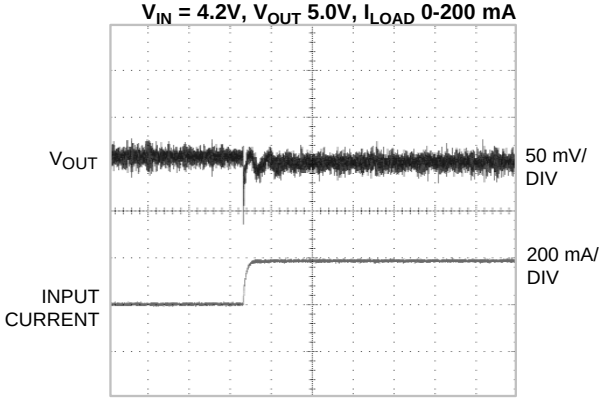


Figure 22.

Load Transient
V_{IN} = 4.2V, V_{OUT} 5.0V, I_{LOAD}200-0mA

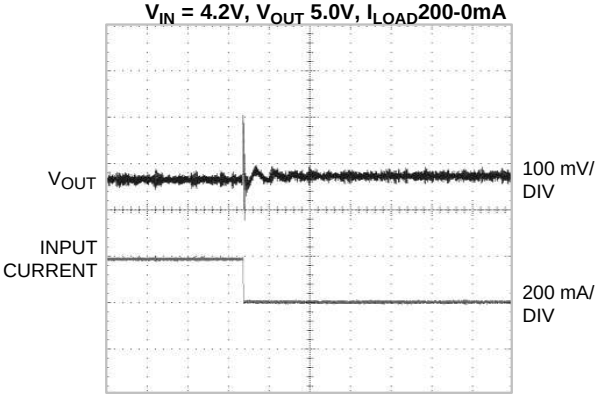


Figure 23.

OPERATION DESCRIPTION

LM8850 FUNCTIONALITY

The LM8850, a high-efficiency, step-up DC-DC switching boost converter, delivers a constant voltage from a stable DC input voltage source. Using a voltage mode architecture with synchronous rectification, the LM8850 has the ability to deliver up to 600 mA of load current, depending on the input voltage, output voltage, ambient temperature, and the inductor chosen.

There are three modes of operation depending on the current required - PWM (Pulse Width Modulation), PFM (Pulse Frequency Modulation), and shutdown. The device operates in PWM mode at load currents of approximately 200 mA or higher. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_q = 6µA typ). Shutdown mode turns off the voltage regulation and offers the lowest current consumption ($I_{SHUTDOWN}$ = 0.4 µA typ).

Once enabled, the LM8850 charges the supercapacitor utilizing all of the default settings in the registers. The I^2C must be used to change the default settings and this can only be done with the LM8850 enabled. Once a register is written to, the changes will transition immediately. Every time the EN pin transitions from VIL to VIH, registers 0 and 1 are reset to their defaults settings and any settings need to be rewritten into the appropriate registers.

AUTO MODE

The LM8850 utilizes AUTO mode to reduce the amount of energy required to maintain the regulated output voltage under light load conditions. The transition from Auto mode to PWM mode varies depending on input voltage and output voltage. For an output voltage of 5.0V and an input voltage of 3.6V, the transition will occur around 225 mA.

Auto mode can only be used with a supercapacitor. If no supercapacitor is being used in the circuit, Auto-Mode must be disabled via I^2C.

V_{RIPPLE}

The ripple voltage used in Auto-Mode is programmable via I^2C. The ripple voltage can be set to 50, 100, 200 and 250 mV. The larger the ripple voltage, the more constant energy will be supplied by the supercapacitor. The regulator will remain asleep until the effective energy to reduce the supercapacitor's voltage by the ripple value has been used by the load.

POWER GOOD

The Power Good signal is both an output and a read only register bit. The Power Good signal will have a V_{OH} value if the V_{OUT} is greater than 85% of its programmed value. This is a typical value for 5.0V and 3.6V V_{IN}. The typical value will vary based on input and output voltage.

PROGRAMMABLE V_{OUT}

The output voltage of the LM8850 can be programmed via I^2C to any of 8 different values: 3.6, 3.9, 4.2, 4.5, 4.7, 5.0, 5.3, and 5.7V. The only requirement is that the input voltage must remain 10% below the desired output voltage for it to remain in regulation. The output voltage can be changed while the part is enabled and regulating. The transition time will depend on load conditions.

TURN-ON TIME

The LM8850 has four programmable turn time values, 5, 7.5, 10, and 12.5 seconds. During the turn on time, the LM8850 is ramping to the output voltage while limiting the inrush current which charges the supercapacitor.

BALANCING CIRCUIT

The LM8850 has an internal balancing circuit that helps maintain voltage balance between the two capacitors within the super capacitor. The BAL pin regulates a voltage of VOUT/ 2 between the two capacitors. If one capacitor is overcharged or less charged, the LM8850 will use the balancing circuit to correct this charge inbalance. The balancing circuit can be turned off/on via the I^2C registers (BALMODE – Control Reg01, bit 3). The balancing circuit also has the ability to stay ON even after the LM8850 is shutting down (BAL – Control Reg00, bit 4).

I²C Interface

Control of LM8850 is done via I²C compatible interface. This includes switch over from AUTO to PWM mode, adjustment of current limit, output voltage, PFM Hysteresis voltage, and start-up time. The I²C interface can also switch the active voltage balance circuit ON during shutdown. Additionally, there is a flag bit that reads back PGOOD condition.

I²C SIGNALS

In I²C-compatible mode, the SCL pin is used for the I²C clock and the SDA pin is used for the I²C data. Both these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistors are determined by the capacitance of the bus. See I²C specification from Philips for further details. Signal timing specifications are according to the I²C bus specification. Maximum frequency is 400 kHz or 3.4 MHz if in High-Speed Mode.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

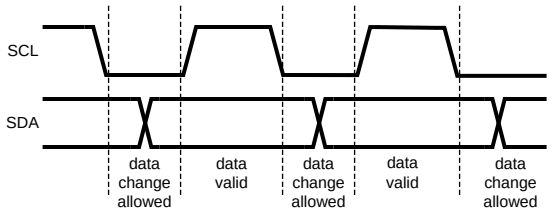


Figure 24. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

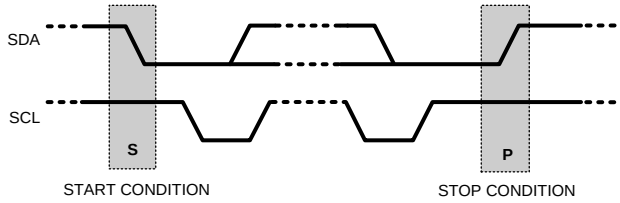


Figure 25. START and STOP Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. All clock pulses are generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the ninth clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM8850 address is 0x60. the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

Chip address: 60h

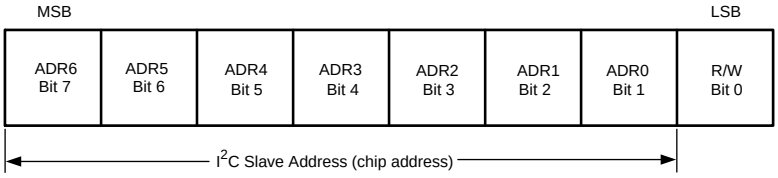


Figure 26. I²C Chip Address

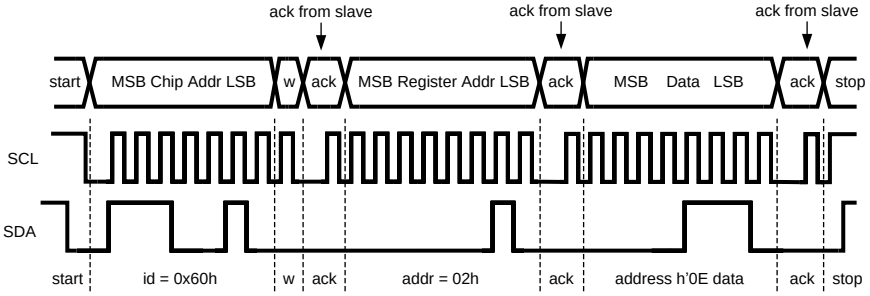


Figure 27. I²C Write Cycle

- w = write (SDA = “0”)
- r = read (SDA = “1)
- ack = acknowledge (SDA pulled down by either master or slave)
- rs = repeated start
- id = chip address

When a READ function is to be accomplished, a WRITE function must precede the READ function as shown in the Read Cycle waveform.

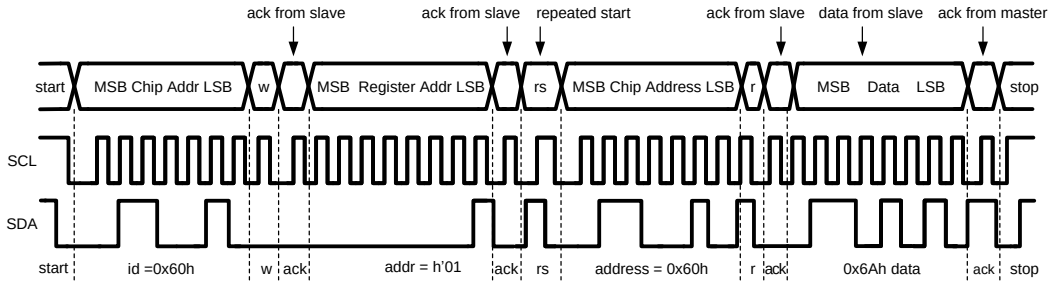


Figure 28. I²C Read Cycle

HIGH-SPEED, 3.4 MHZ MODE

High-speed mode is entered by:

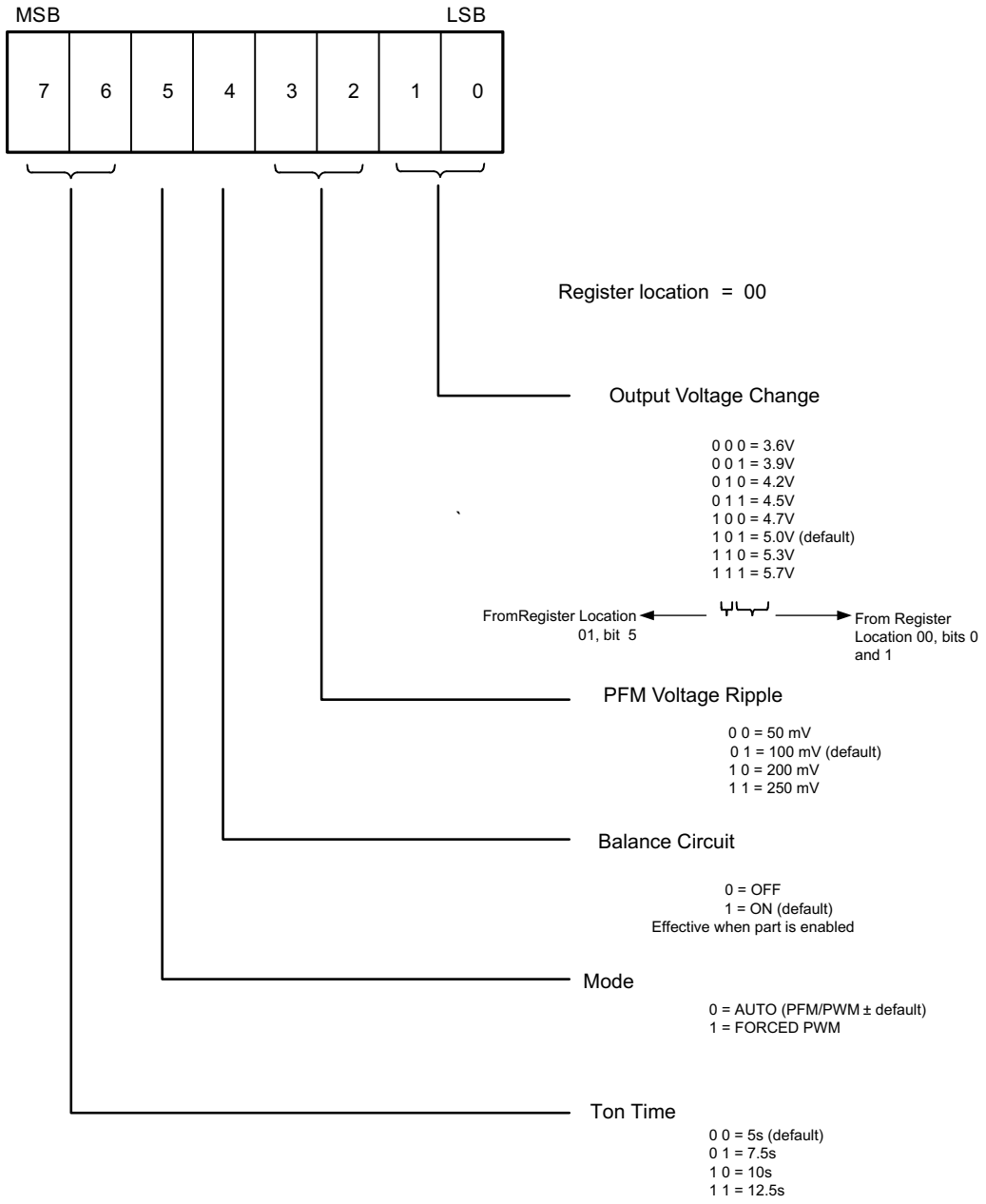
1. Start condition;
2. Chip Address: 0000 1XXXX (X = don't care);
3. Wait a clock for the acknowledge;
4. Now everything is in HS mode...do a repeated start (do NOT do a “stop” then a “start” because a “stop” kicks the part out of HS mode);
5. Send read or writes in HS mode. (Remember to use “repeated starts” between commands.); then
6. When you are done with the last command send a “stop” condition to put the part back into regular 400 kHz mode.

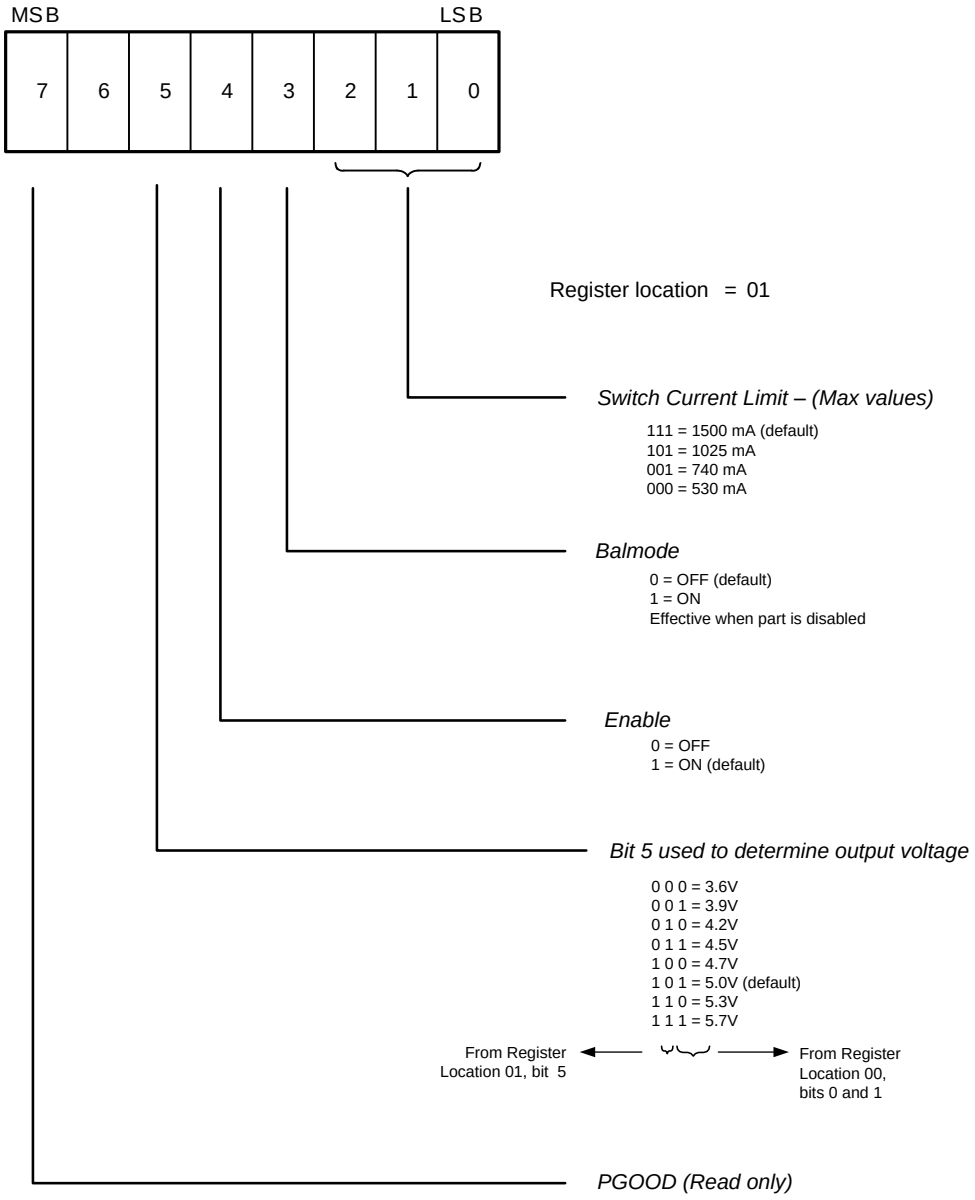
I²C-COMPATIBLE CHIP ADDRESS

The device address for LM8850 is 60 (HEX).

Table 2. Register Information and Details

Register name	Location	Type	Register
CONTROL	0	R/W	Control Register 1
CONTROL	1	R/W	Control Register 2





REVISION HISTORY

Changes from Revision B (May 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM8850URE/NOPB	ACTIVE	DSBGA	YPD	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SK	Samples
LM8850URX/NOPB	ACTIVE	DSBGA	YPD	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

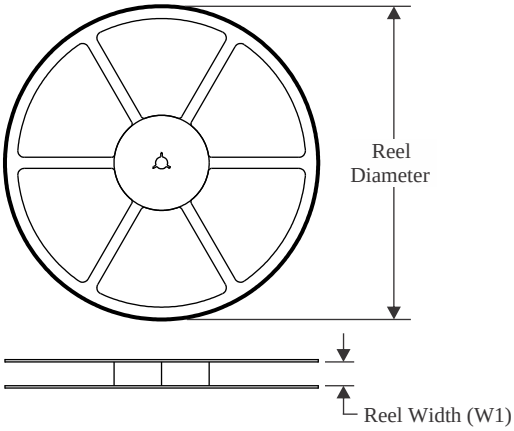
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

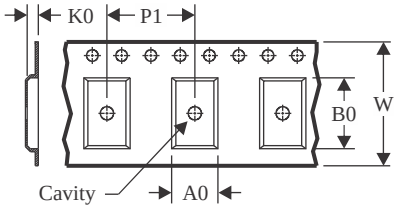
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

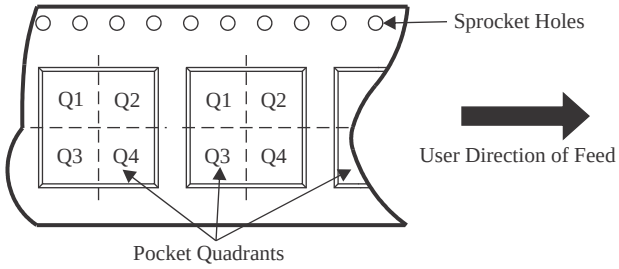


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

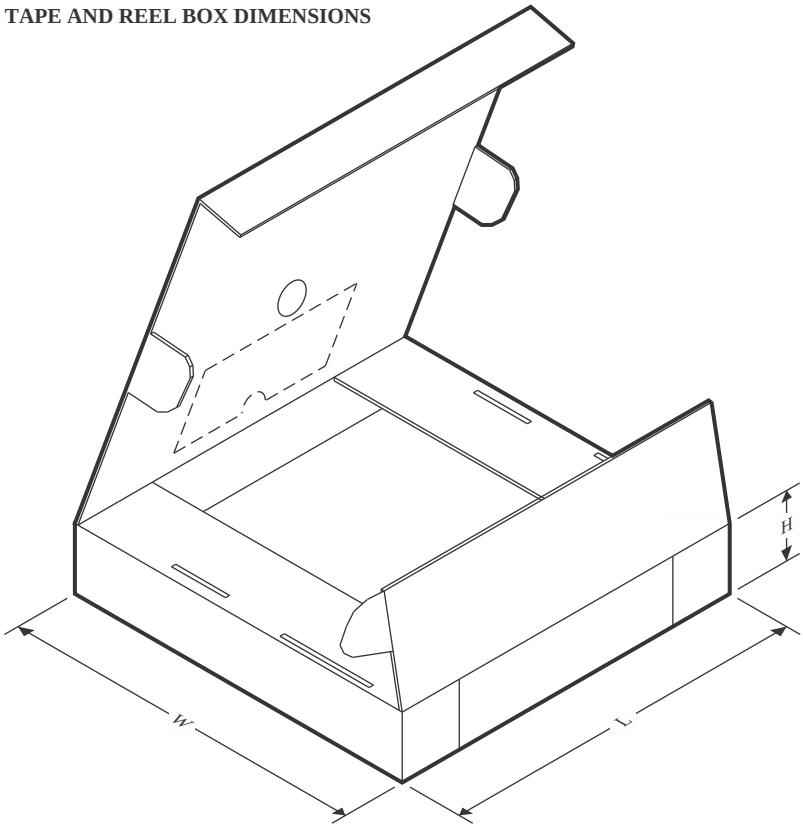
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8850URE/NOPB	DSBGA	YPD	9	250	178.0	8.4	1.7	1.75	0.56	4.0	8.0	Q1
LM8850URX/NOPB	DSBGA	YPD	9	3000	178.0	8.4	1.7	1.75	0.56	4.0	8.0	Q1

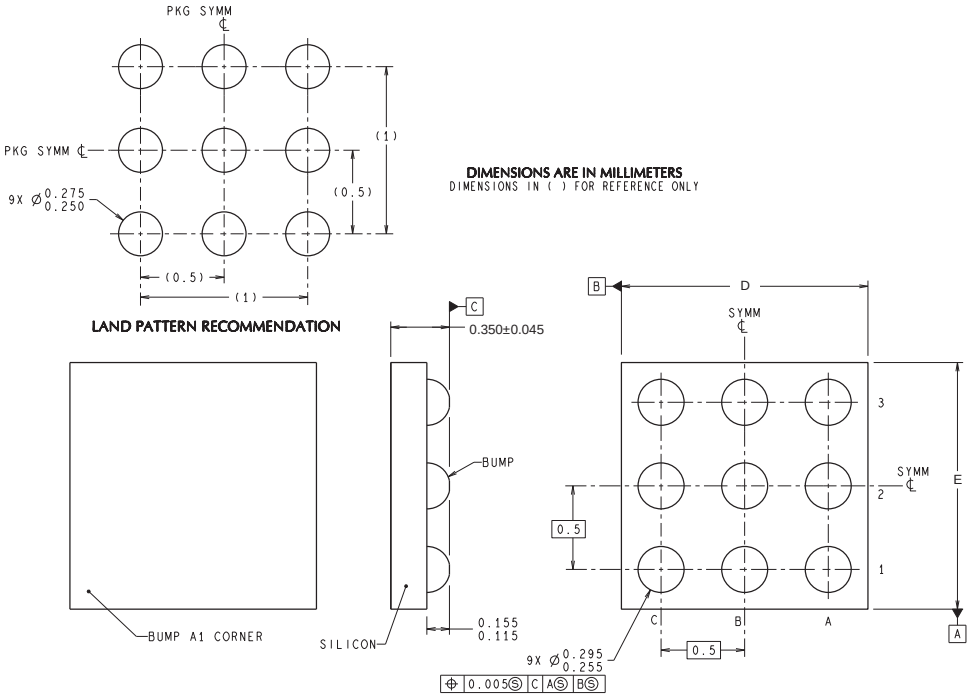
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8850URE/NOPB	DSBGA	YPD	9	250	208.0	191.0	35.0
LM8850URX/NOPB	DSBGA	YPD	9	3000	208.0	191.0	35.0

YPD0009



URA09XXX (Rev A)

D: Max = 1.635 mm, Min =1.574 mm

E: Max = 1.594 mm, Min =1.534 mm

4215145/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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