HD3SS460 4 x 6 通道 USB Type-C™交替模式 MUX

1 特性

- 提供面向 USB Type-C™ 生态系统的 MUX 解决方案，其中包括交替模式 (AM)
- 提供多种通道选择选项，其中包括 USBSS、双通道 AM 和四通道 AM
- 与 5 Gbps USB3.1 第 1 代和包含 5.4 Gbps DisplayPort 1.2a 的 AM 兼容
- 与源设备/主机和接收设备/设备应用 兼容
- 针对低速 SBU 引脚提供交叉点 MUX
- 双向“复用/解复用”差动开关
- 支持 0V 至 2V 共模电压
- 功耗较低，关断电流和工作电流分别为 1μA 和 0.6mA
- 单电源电压 VCC：3.3V±10%
- 工业温度范围：–40°C 至 85°C

2 应用

- 可换向 USB Type-C™ 生态系统
- 平板电脑、笔记本电脑、监视器、电话
- USB 主机和设备
- 扩展坞

3 说明

HD3SS460 是一款高速双向无源开关，可采用复用或解复用两种配置。该器件可通过负载点 (POL) 控制引脚进行切换，从而适应连接器换向。该器件还可通过 AMSEL 控制引脚来实现双通道数据/双通道视频与所有四通道视频的复用。

该器件还针对低速引脚提供了交叉点 MUX，可满足可换向连接器实现的需求。

HD3SS460 是一款通用模拟差分无源开关，适用于所有高速接口 应用， 前提条件是该应用在 0V 至 2V 共模电压范围内发生偏置并且具有幅值高达 1800 mVpp 的差分信令。该器件采用自适应跟踪，可确保信道在整个共模电压范围内保持不变。

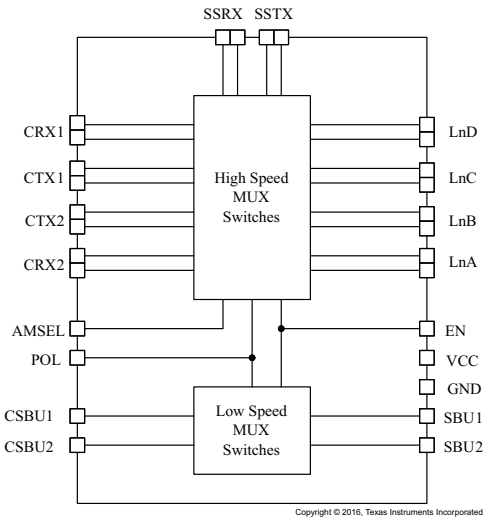
该器件具有出色的动态特性，可在信号眼图衰减最小的情况下实现高速转换，并且附加抖动极少。该器件在工作模式下的功耗 < 2mW，关断模式下的功耗 < 5μW（可通过 EN 引脚切换模式）。

器件信息(1)

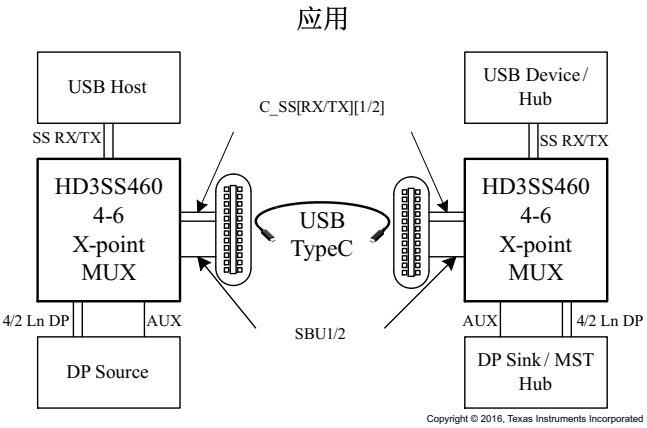
器件型号	封装	封装尺寸（标称值）
HD3SS460	QFN (RHR) (28)	3.50mm x 5.50mm
HD3SS460I		
HD3SS460	QFN (RNH) (30)	2.50mm x 4.50mm
HD3SS460I		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



应用



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (December 2016) to Revision D — **Page**

- Deleted R187 from Figure 16 ... 21
- Deleted R187 from Figure 19. ... 23

Changes from Revision B (June 2016) to Revision C — **Page**

- 已将 QFN (RNH) (30) 添加至*器件信息表* ... 1
- Added the RNH package option to the *Device Comparison Table* table ... 4
- Added the RNH package option to the *Pin Configuration and Functions* section ... 5
- Changed the Description of pins LnBn, p, LnCn, p, LnDn, p, SSTXn, p, and SSRXn, p From: positive, negative To: negative, positive in the *Pin Functions* table ... 5
- Changed the Supply voltage MIN value From: 3.0 V To: 2.7 V in the *Recommended Operating Conditions* table ... 6
- Added the RNH package option to the *Thermal Information* table ... 6
- Changed V_{IH} to include a separate line entry for POL pin in the *Electrical Characteristics* table ... 7

Changes from Revision A (March 2015) to Revision B — **Page**

- Changed text and Figure 3, Figure 4 in the USB SS and DP as Alternate Mode section for clarity. ... 14
- Added Figure 5 ... 15
- Added Figure 6 ... 16
- Deleted Table *Pin Assignments for DP Source Pins and DP Sink Pins* in the *Detailed Design Procedure* section ... 17
- Added Table 2, Table 3, Table 4, and Table 5 ... 17
- Added Figure 8 through Figure 13 ... 17
- Changed image for Figure 16 ... 21
- Changed image for Figure 19. ... 23

Changes from Original (January 2015) to Revision A **Page**

- Added full data sheet specification complement 6

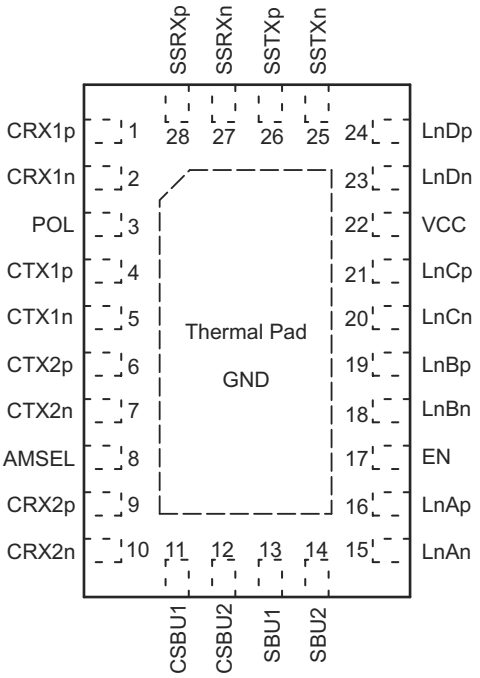
5 Device Comparison Table(1)

OPERATING TEMPERATURE (°C)	PART NUMBER	PINS	TOP-SIDE MARKING
0 to 70	HD3SS460RHR	28	3SS460
–40 to 85	HD3SS460IRHR	28	3SS460I
0 to 70	HD3SS460RNH	30	460RNH
–40 to 85	HD3SS460IRNH	30	460IRNH

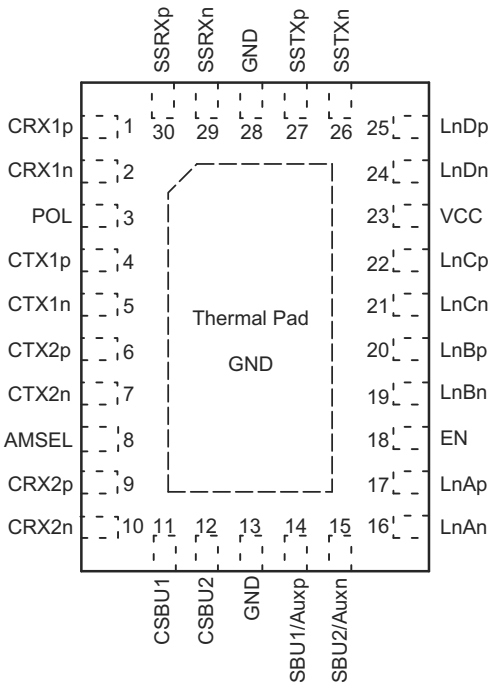
(1) For all available packages, see the orderable addendum at the end of the data sheet. Package drawings, thermal data, and symbolization are available at www.ti.com/packaging

6 Pin Configuration and Functions

RHR Package With Thermal Pad
(28-Pin WQFN)
Top View



RNH Package With Thermal Pad
(30-Pin WQFN)
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	RHR NO.	RNH NO.		
VCC	22	23	P	Power
GND	PAD	13, 28, PAD	G	Ground
POL	3	3	Input	Provides MUX control (Table 1)
AMSEL	8	8	3-Level Input	Provides MUX configurations (Table 1)
EN	17	18	3-Level Input	Enable signal; also provides MUX control (Table 1)
CRX1p, n	1, 2	1, 2	I/O	High Speed Signal Port CRX1 positive, negative
CTX1p, n	4, 5	4, 5	I/O	High Speed Signal Port CTX1 positive, negative
CTX2p, n	6, 7	6, 7	I/O	High Speed Signal Port CTX2 positive, negative
CRX2p, n	9, 10	9, 10	I/O	High Speed Signal Port CRX2 positive, negative
LnAn, p	15, 16	16, 17	I/O	High Speed Signal Port LnA positive, negative
LnBn, p	18, 19	19, 20	I/O	High Speed Signal Port LnB negative, positive
LnCn, p	20, 21	21, 22	I/O	High Speed Signal Port LnC negative, positive
LnDn, p	23, 24	24, 25	I/O	High Speed Signal Port LnD negative, positive
SSTXn, p	25, 26	26, 27	I/O	High Speed Signal Port SSTX negative, positive
SSRXn, p	27, 28	29, 30	I/O	High Speed Signal Port SSRX negative, positive
CSBU1, 2	11, 12	11, 12	I/O	Low Speed Signal Port CSBU 1, 2
SBU1, 2	13, 14	14, 15	I/O	Low Speed Signal Port SBU 1, 2

(1) High speed data ports (CRX[1/2][p/n], Ln[A-D][p,n], and SS[T/R]X[p/n]) incorporate 20kΩ pull down resistors that are switched in when a port is not selected and switched out when the port is selected.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply Voltage, VCC	–0.5	4	V
Differential High Speed I/O Voltages, C[R/T]X[1/2][p/n], Ln[A-D][p/n], SS[R/T]X[p/n]	–0.5	2.5	V
Low Speed I/O Voltages, CSBU[1/2], SBU[1/2]	–0.5	4	V
Control signal voltages, POL, AMSEL, EN	–0.5	4	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
T_A	Operating free air temperature	HD3SS460	0	25	70	°C
		HD3SS460I	–40	25	85	
V_{CM}	High speed port common mode voltage		0		2	V
V_{IN}	Low Speed signal voltage		0		VCC	
Vdiff	High speed port differential voltage		0		1.8	Vpp

7.4 Thermal Information

THERMAL METRIC (1)		HD3SS460		UNIT
		QFN (RNH)	QFN (RHR)	
		30 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.6	44.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.5	34.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.3	24.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.8	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

typical values for all parameters are at V_{DD} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low voltage, control pins POL, AMSEL, EN		–0.1		0.4	V
V_{IH}	Input high voltage, control pins AMSEL, EN		V_{CC} –0.4		V_{CC} +0.1	V
	Input high voltage, control pins POL		1.7		V_{CC} +0.1	V
V_{IM}	Input mid-level voltage, control pins AMSEL, EN		$V_{CC}/2$ –0.3	$V_{CC}/2$	$V_{CC}/2$ +0.3	V
$I_{LK-DIFF-ACTIVE}$	Leakage current on active differential IO pins, VCC = 3.6 V, pin at 0 or 2.4 V.				1	µA
$I_{LK-DIFF-INACTIVE}$	Leakage current on inactive differential IO pins, VCC = 3.6V, pin at 2.4 V.				150	µA
I_{IH}	Input high current, control pins POL, AMSEL, EN and signal pins CSBU1/2, SBU1/2				1	µA
I_{IL}	Input low current, control pins POL, AMSEL, EN and signal pins CSBU1/2, SBU1/2				1	µA
I_{IM}	Input mid-level current, control pins AMSEL, EN				1	µA
I_{OFF}	Device shutdown current			1	5	µA
I_{DD}	Device active current, EN=H or M			0.6	0.9	mA
$R_{ON(HS)}$	Switch ON resistance for high speed differential signals	V_{CC} = 3.3 V, V_{CM} = 0-2 V, I_O = - 8 mA		8	14	Ω
$R_{ON(LS)}$	Switch ON resistance for low speed signals	V_{CC} = 3.3 V, V_{CM} = 0-2 V, I_O = - 8 mA		12		Ω
$R_{FLAT(ON,HS)}$	High speed differential signals' ON resistance flatness for a channel	($R_{ON(MAX)}$ – $R_{ON(MIN)}$) over V_{CM} range V_{CC} = 3.3 V, V_{CM} = 0-2 V, I_O = - 8 mA			1.5	Ω
$C_{ON(HS)}$	High speed differential signals' input capacitance				1	pF

7.6 High Speed Port Performance Parameters

under recommended operating conditions; R_{LOAD}, R_{SC} = 50 Ω (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
RL	Differential return loss	100 Mhz SS Paths		–23		dB
		2.5 Ghz SS Paths		–9		
		100 MHz AM Paths		–23		
		2. 7GHz AM Paths		–13		
IL	Differential insertion loss	100 Mhz SS Paths		–0.7		
		2.5 Ghz SS Paths		–1.6		
		100 MHz AM Paths		–0.7		
		2.7 GHz AM Paths		–1.4		
OI	Differential off isolation	100 Mhz		–50		
		2.5 Ghz		–26		
		2.7 GHz		–25		
Xtalk	Differential cross talk, Between CRX1/2 and CTX1/2	100 Mhz		–80		
		2.5 Ghz		–30		
		2.7 Ghz		–28		
	Differential cross talk, Between CRX1 and CRX2 or CTX1 and CTX2	100 Mhz		–50		
		2.5 Ghz		–26		
		2.7 Ghz		–25		
BW_{SS}	Differential –3 dB BW SS Paths			4.2		GHz
BW_{AM}	Differential –3 dB BW AM Paths			5.4		
BW_{SBU}	Low-speed switch –3 dB BW			500		MHz

7.7 High Speed Signal Path Switching Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	R_{SC} and R_{LOAD} = 50 Ω, Figure 2			100	ps
$t_{SK(O)}$	Inter-Pair output skew (CH-CH)				50	
$t_{SK(b-b)}$	Intra-Pair output skew (bit-bit)				5	
t_{ON}	Control signals POL, AMSEL and EN (H/M toggle) to switch ON time	R_{SC} and R_{LOAD} = 50 Ω, Figure 1			3	µs
t_{OFF}	Control signals POL, AMSEL and EN (H/M toggle) to switch OFF time				1	

Timing Diagrams

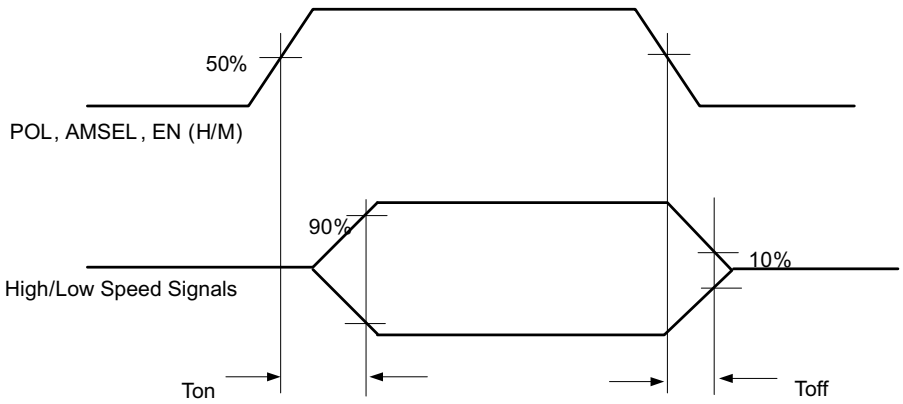
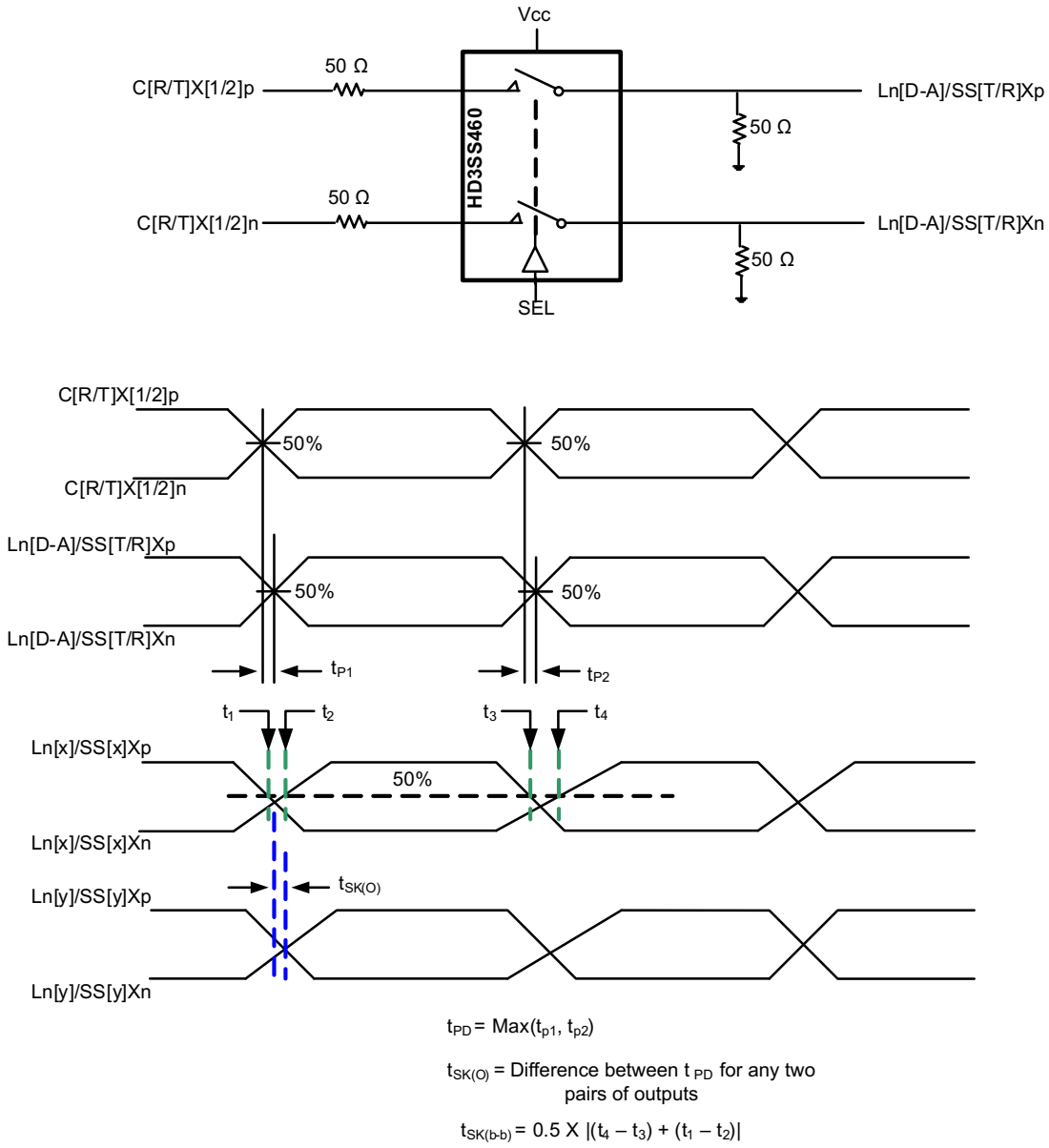


Figure 1. Switch ON/OFF Time



t_{PD} = Max(t_{p1}, t_{p2})

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs

$t_{SK(b\text{-}b)}$ = 0.5 X |(t_4 – t_3) + (t_1 – t_2)|

Figure 2. Propagation Delay and Skew

8 Detailed Description

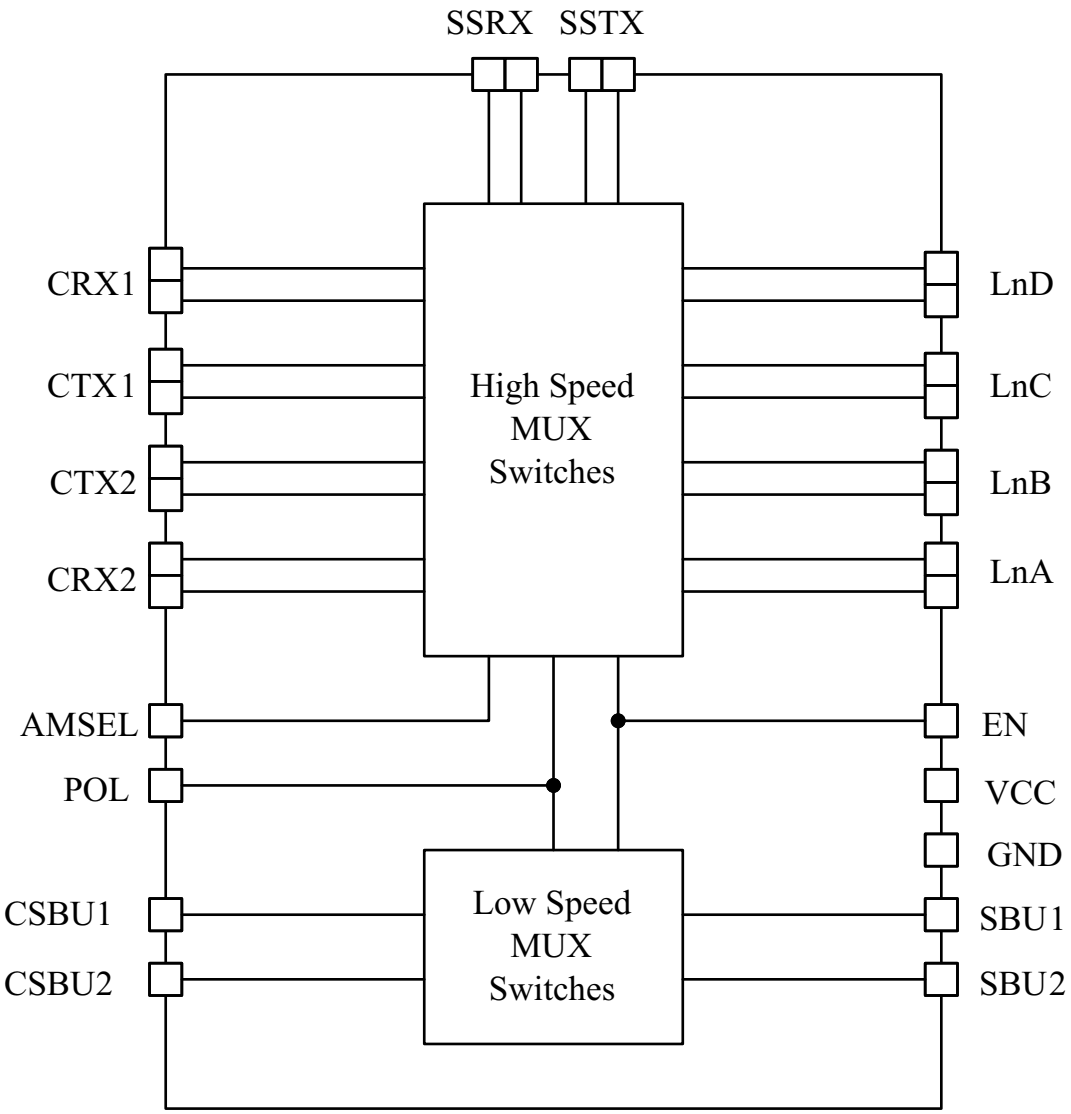
8.1 Overview

The HD3SS460 is a high-speed bi-directional passive 4-6 cross-point switch in mux or demux configurations. Based on control pin POL the device provides switching to accommodate USB Type-C plug flipping. The device provides multiple signal switching options that allow system implementation flexibility.

The HD3SS460 is a generic analog, differential passive switch that can work for any high speed interface applications as long as it is biased at a common mode voltage range of 0-2 V and has differential signaling with differential amplitude up to 1800 mVpp. It employs an adaptive tracking that ensures the channel remains unchanged for entire common mode voltage range

Excellent dynamic characteristics of the device allow high speed switching with minimum attenuation to the signal eye diagram with very little added jitter.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 High Speed Differential Signal Switching

Based on control pin AMSEL the device provides muxing options of:

1. 1 port (RX and TX) USB3.1 SS data / 2Ch video (or any other Alternate Mode data)
2. All 4Ch video (or any other Alternate Mode data)
3. 1 port (RX and TX) USB3.1 SS data
4. 1 port (RX and TX) USB3.1 SS data / 2Ch video (or any other Alternate Mode data) with option of choosing video from two different source/sink
5. 1 port (RX and TX) USB3.1 SS data / 2Ch video (or any other Alternate Mode data) with option of choosing video 2 Ln Video or 1 Ln Video from two different source/sink

8.3.2 Low Speed SBU Signal Switching

The device also provides cross point muxing for low speed SBU signals as needed in USB Type-C flippable connector implementation. The device provides the option to choose the USB only implementation where SBU ports are in tri-state.

8.3.3 Output Enable and Power Savings

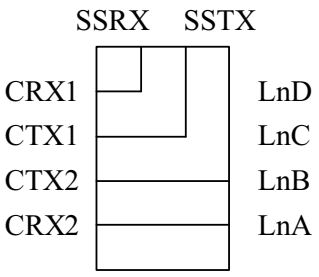
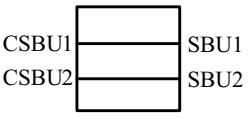
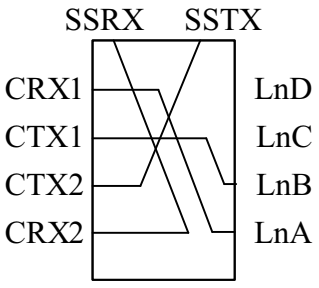
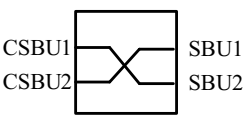
The HD3SS460 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes very little current to save the maximum power. To enter standby mode, the EN control pin is pulled low and must remain low. For active/normal operation, the EN control pin should be pulled high to VDD through a resistor or dynamically controlled to switch between H or M.

HD3SS460 consumes <2 mW of power when operational and <5 µW in shutdown mode, exercisable by the EN pin.

8.4 Device Functional Modes

8.4.1 Device High Speed Switch Control Modes

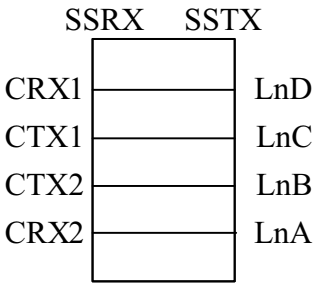
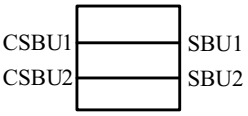
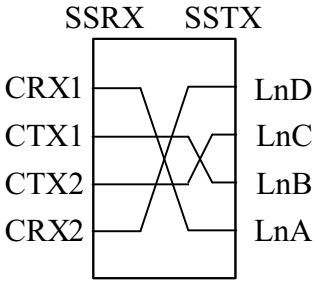
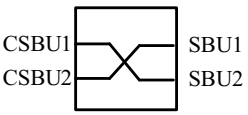
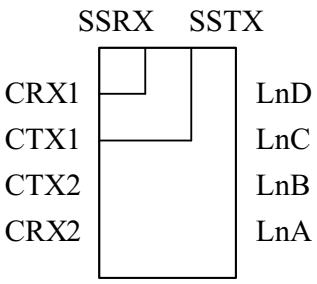
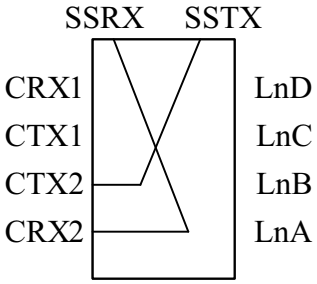
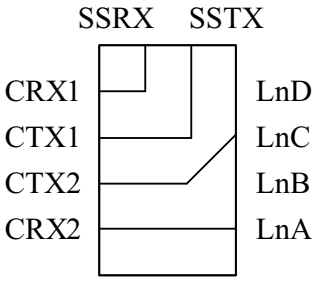
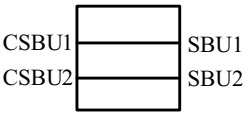
Table 1. MUX Control for High Speed and Low Speed SBU Channels

POL	AMSEL	EN	CONFIGURATIONS	HIGH SPEED SIGNAL FLOW(1)	SBU SIGNAL FLOW
L	L	H	2CH USBSS + 2CH AM (Normal)		
H	L	H	2CH USBSS + 2CH AM (Flipped)		

(1) All positive signals connect to positive and negative to negative

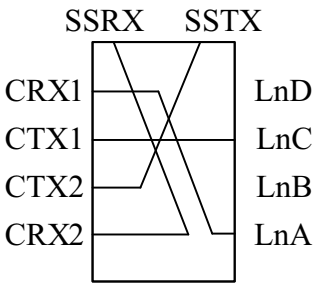
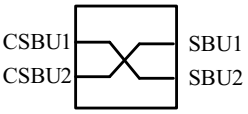
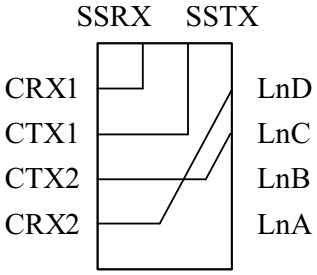
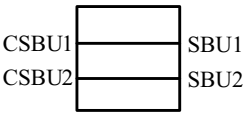
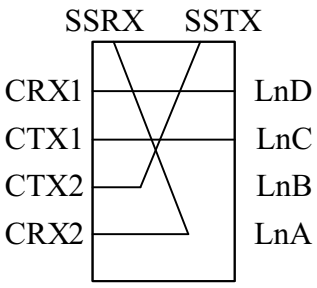
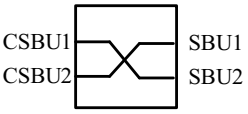
Device Functional Modes (continued)

Table 1. MUX Control for High Speed and Low Speed SBU Channels (continued)

POL	AMSEL	EN	CONFIGURATIONS	HIGH SPEED SIGNAL FLOW(1)	SBU SIGNAL FLOW
L	H	H	4CH AM (Normal)		
H	H	H	4CH AM (Flipped)		
L	M	H	2CH USBSS (Normal)		All Low Speed SBU Ports HighZ
H	M	H	2CH USBSS (Flipped)		All Low Speed SBU Ports HighZ
L	M	M	2CH USBSS + 2CH AM (Normal)		

Device Functional Modes (continued)

Table 1. MUX Control for High Speed and Low Speed SBU Channels (continued)

POL	AMSEL	EN	CONFIGURATIONS	HIGH SPEED SIGNAL FLOW(1)	SBU SIGNAL FLOW
H	M	M	2CH USBSS + 2CH AM (Flipped)		
L	L	M	2CH USBSS + 2CH AM from alternate GPU (Normal)		
H	L	M	2CH USBSS + 2CH AM from alternate GPU (Flipped)		
L	H	M	Reserved	Reserved	Reserved
H	H	M	Reserved	Reserved	Reserved
X	X	L	All High Speed Ports HighZ	All High Speed Ports HighZ	All Low Speed SBU Ports HighZ

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

HD3SS460 can be utilized for a wide range of muxing needs. This is general purpose passive cross-point switch. The channels have independent adaptive common mode tracking allowing flexibility. As long as recommended electrical use conditions are met the device can be used number of ways as described in Table 1.

NOTE

HD3SS460 does not provide common mode biasing for the channel. Therefore it is required that the device is biased from either side for all active channels.

9.2 USB SS and DP as Alternate Mode

HD3SS460 can be used USB Type-C ecosystem with DP as alternate mode in two distinct application configurations – one is for DP Source/USB Host, the other one for the DP Sink/USB Device/Dock. Figure 3 and Figure 4 illustrate typical application block diagrams for these two cases. Detail schematics are illustrated in Detailed Design Procedure section. Other applications and or use cases possible where these examples can be used as general guidelines.

Figure 3 and Figure 4 depict the AC coupling capacitor placement examples. TI recommends placing the capacitors as shown in the illustrations for the backward compatibility and interoperability purposes as some of the existing USB systems may present Vcm, exceeding the typical range of 0–2 V on SS differential pairs.

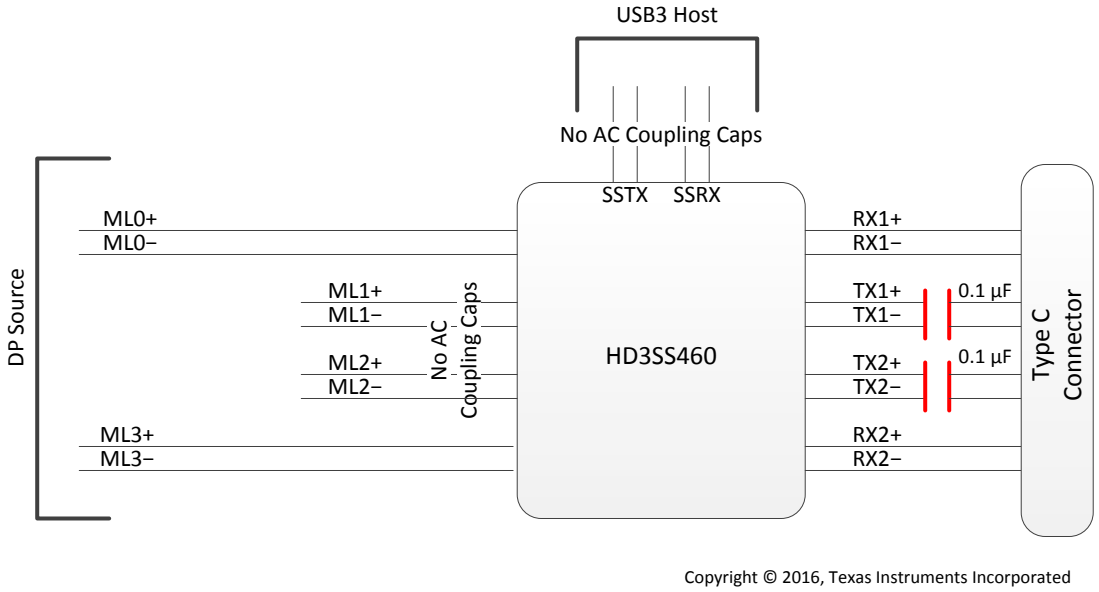


Figure 3. Block Diagram for a Type C Interface Using DP as Alternate Mode – Source/Host

USB SS and DP as Alternate Mode (continued)

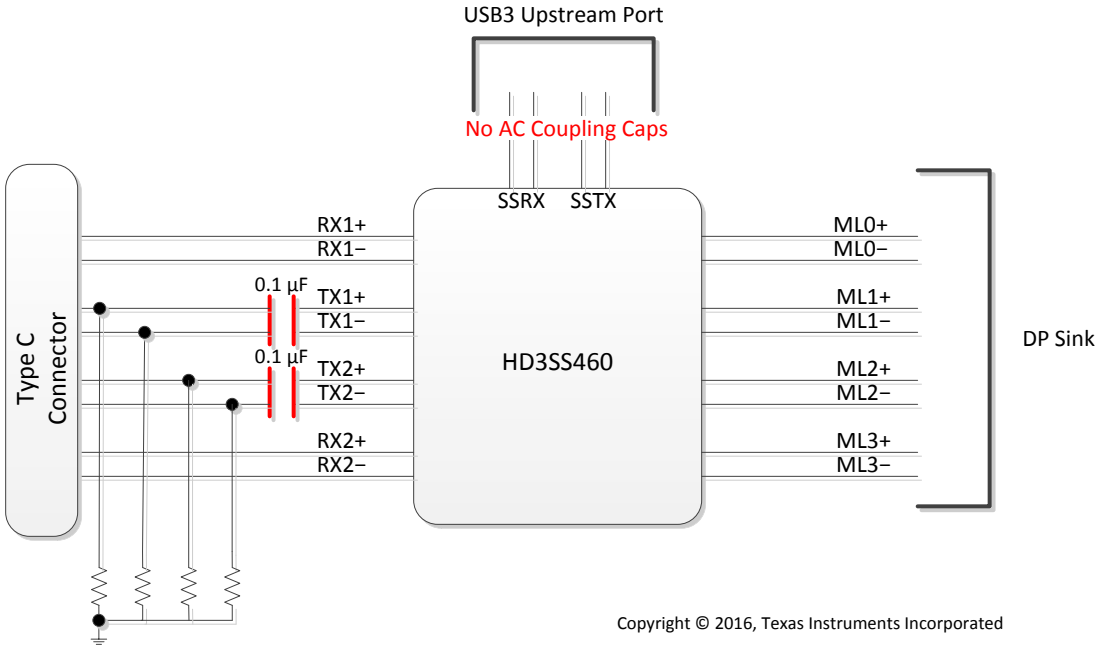


Figure 4. Diagram for a Type C Interface Using DP as Alternate Mode – Sink/Device/Dock

Figure 5 and Figure 6 depict the AC coupling capacitor recommendations in case the upstream or downstream port connected internally to the HD3SS460 presents Vcm greater than 2 V.

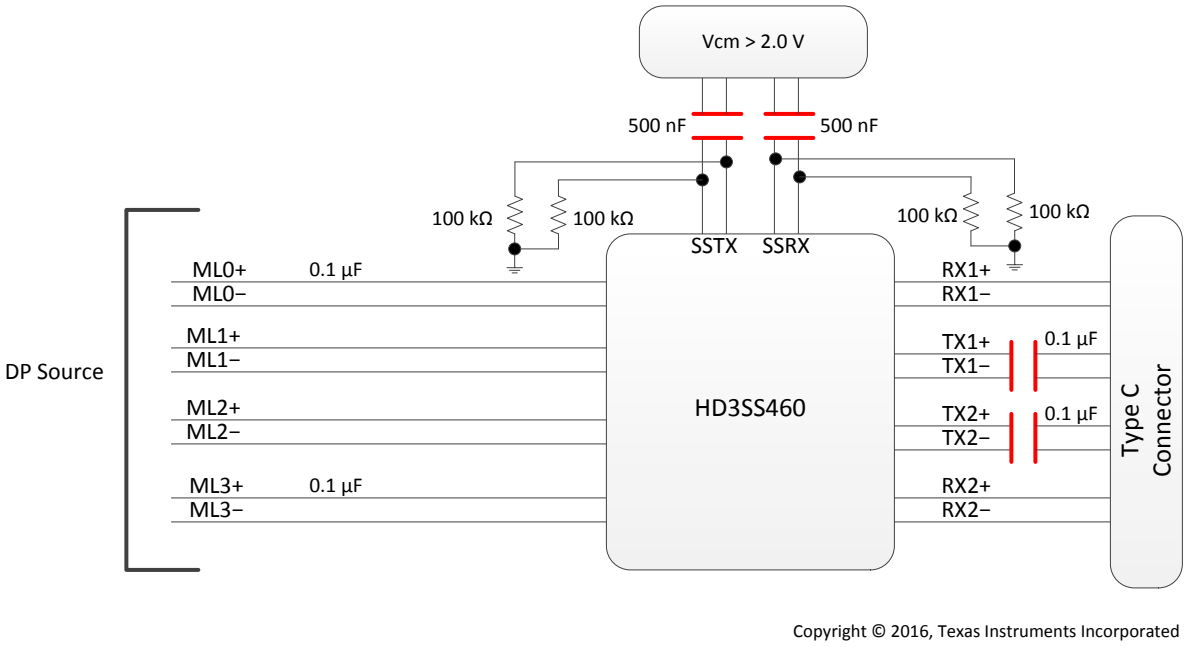


Figure 5. HD3SS460 USB Host (DP Source with SS USB Vcm)

USB SS and DP as Alternate Mode (continued)

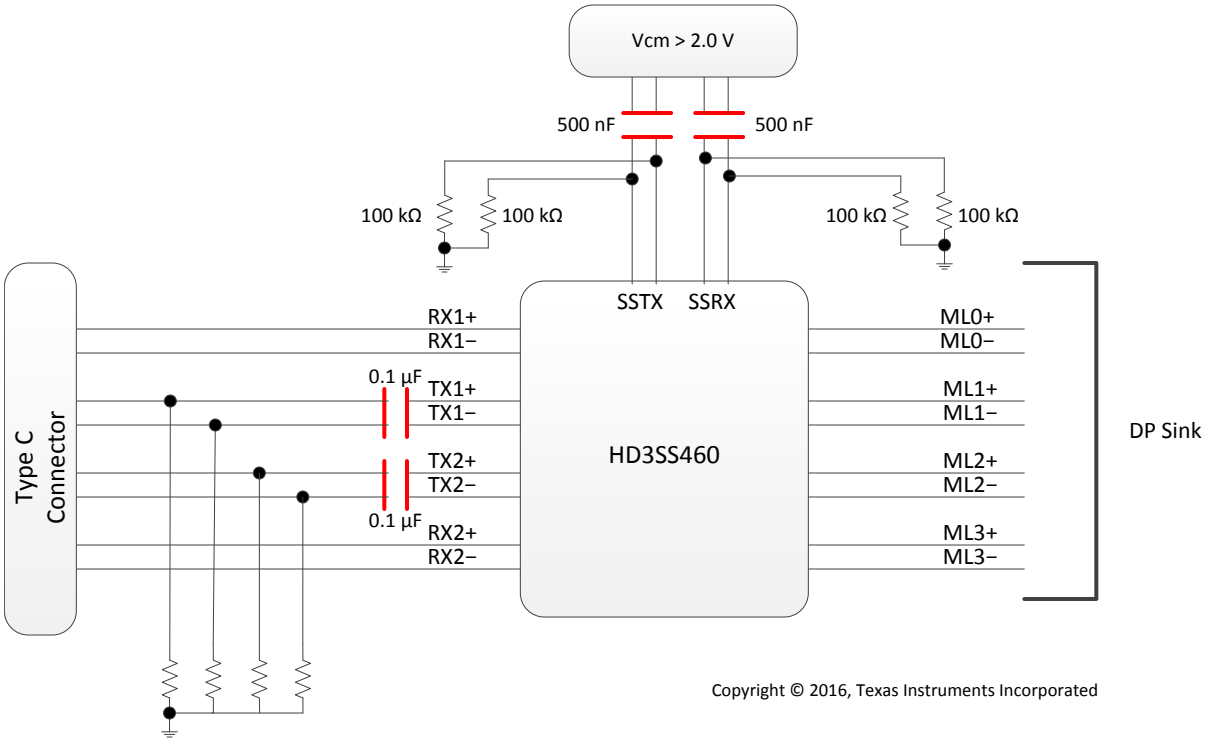


Figure 6. HD3SS460 USB Upstream (DP Sink Implementation Example)

9.2.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUES
VCC	3.3 V
Decoupling capacitors	0.1 µF
AC Capacitors	75-200nF (100nF shown) USBSS TX p and n lines require AC capacotprs. Alternate mode signals may or may not require AC capacitors
Control pins	Controls pins can be dynamically controlled or pin-strapped. The POL signal is controlled by CC logic in the Type-C ecosystem.

9.2.2 Detailed Design Procedure

The reference schematics shown in this document are based upon the pin assignment defined in the Alternate mode over Type C specification as shown in Figure 7 below.

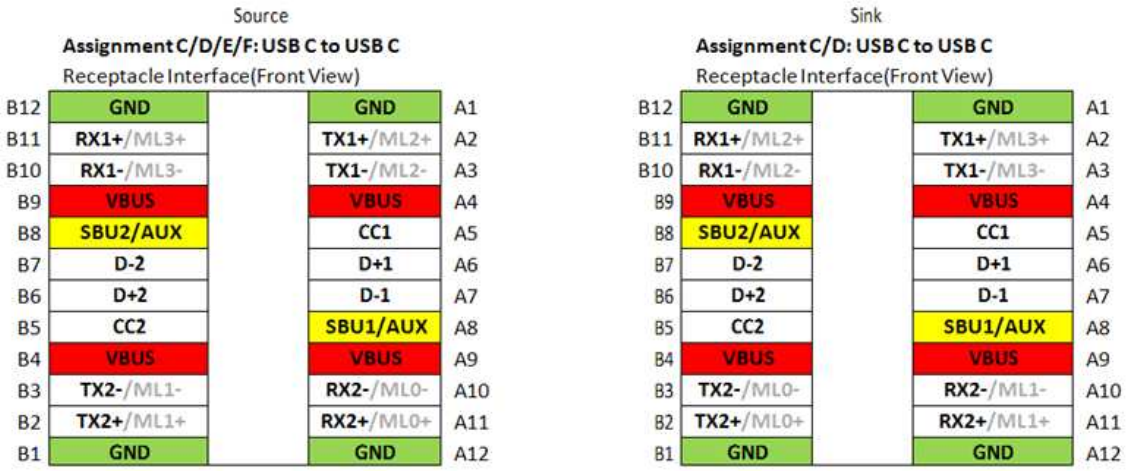


Figure 7. Pin Assignment – Alternate Mode Over Type C

Table 2 represents the example pin mapping to HD3SS460 for the DP Source pin assignments C, D, E and F, DP Sink pin assignments C and D.

Table 2. SOURCE Pin Assignment Option C and E (AMSEL = H, EN = H)

RECEPTACLE PIN NUMBER	460 PIN MAPPING TO TYPE C CONNECTOR	460 PIN MAPPING TO DP SOURCE (GPU)	
		POL = L	POL = H
A11/10	CRX2	LnA(ML0)	LnD(ML3)
A2/3	CTX1	LnC(ML2)	LnB(ML1)
B11/10	CRX1	LnD(ML3)	LnA(ML0)
B2/3	CTX2	LnB(ML1)	LnC(ML2)
A8	CSBU1	SBU1(AUXP)	SBU2(AUXN)
B8	CSBU2	SBU2(AUXN)	SBU1(AUXP)

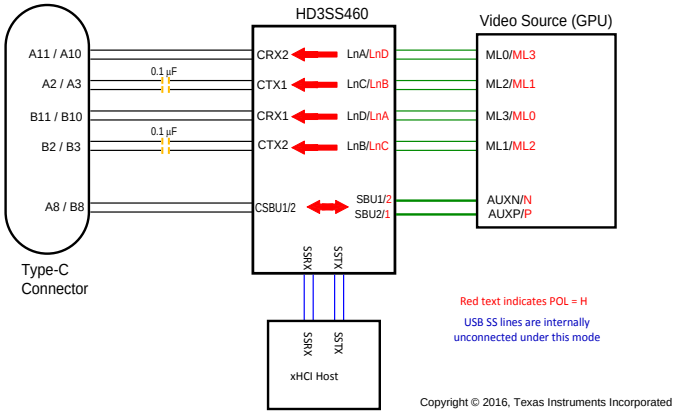


Figure 8. SOURCE Pin Assignment Option C and E (AMSEL = H, EN = H)

Table 3. SOURCE Pin Assignment Option D and F (AMSEL = L, EN = H)

RECEPTACLE PIN NUMBER	460 PIN MAPPING TO TYPE C CONNECTOR	460 PIN MAPPING TO DP SOURCE (GPU)	
		POL = L	POL = H
A11/10	CRX2	LnA(ML0)	SSRX
A2/3	CTX1	SSTX	LnB(ML1)
B11/10	CRX1	SSRX	LnA(ML0)
B2/3	CTX2	LnB(ML1)	SSTX
A8	CSBU1	SBU1(AUXP)	SBU2(AUXN)
B8	CSBU2	SBU2(AUXN)	SBU1(AUXP)

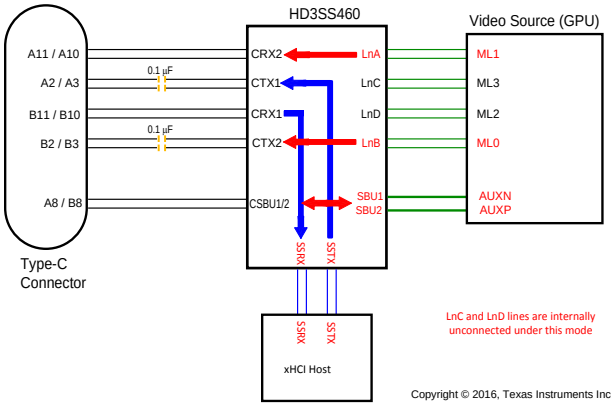


Figure 9. SOURCE Pin Assignment Option D and F (AMSEL = L, EN = H, POL = L)

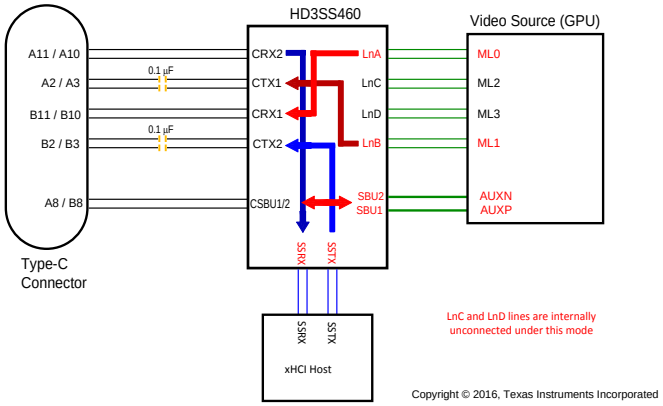


Figure 10. SOURCE Pin Assignment Option D and F (AMSEL = L, EN = H, POL = H)

Table 4. SINK Pin Assignment Option C (AMSEL = H, EN = H)

RECEPTACLE PIN NUMBER	460 PIN MAPPING TO TYPE C CONNECTOR	460 PIN MAPPING TO DP SOURCE (GPU)	
		POL = L	POL = H
A11/10	CRX2	LnA(ML1)	LnD(ML2)
A2/3	CTX1	LnC(ML3)	LnB(ML0)
B11/10	CRX1	LnD(ML2)	LnA(ML1)
B2/3	CTX2	LnB(ML0)	LnC(ML3)
A8	CSBU1	SBU1(AUXN)	SBU2(AUXP)
B8	CSBU2	SBU2(AUXP)	SBU1(AUXN)

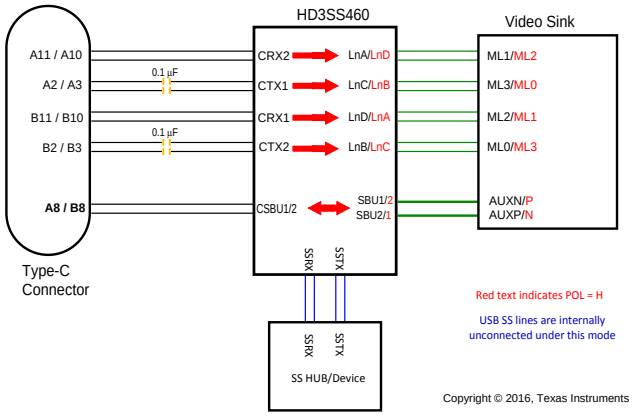


Figure 11. SINK Pin Assignment Option C (AMSEL = H, EN = H)

Table 5. SINK Pin Assignment Option D (AMSEL = L, EN = H)

RECEPTACLE PIN NUMBER	460 PIN MAPPING TO TYPE C CONNECTOR	460 PIN MAPPING TO DP SOURCE (GPU)	
		POL = L	POL = H
A11/10	CRX2	LnA(ML1)	SSRX
A2/3	CTX1	SSTX	LnB(ML0)
B11/10	CRX1	SSRX	LnA(ML1)
B2/3	CTX2	LnB(ML0)	SSTX
A8	CSBU1	SBU1(AUXN)	SBU2(AUXP)
B8	CSBU2	SBU2(AUXP)	SBU1(AUXN)

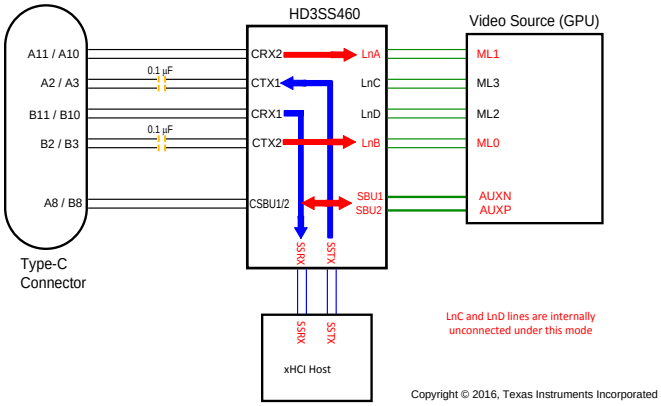


Figure 12. SINK Pin Assignment Option D (AMSEL = L, EN = H, POL=L)

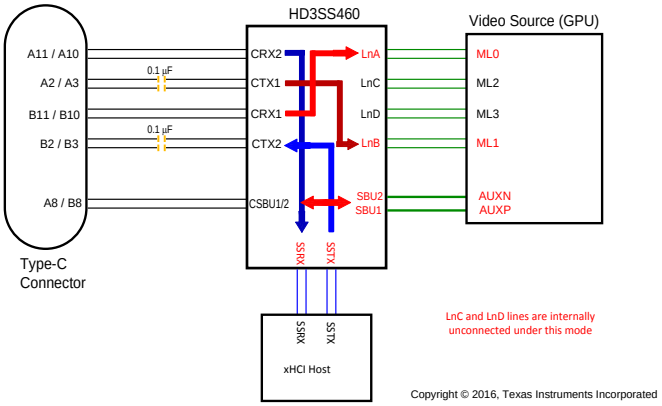


Figure 13. SINK Pin Assignment Option D (AMSEL = L, EN = H, POL=H)

Schematic diagrams Figure 14, Figure 15, and Figure 16 show the DP Source/USB Host implementation; and, Figure 17, Figure 18, and Figure 19 show the DP Sink/USB Device/HUSB Hub/Dock implementation, respectively.

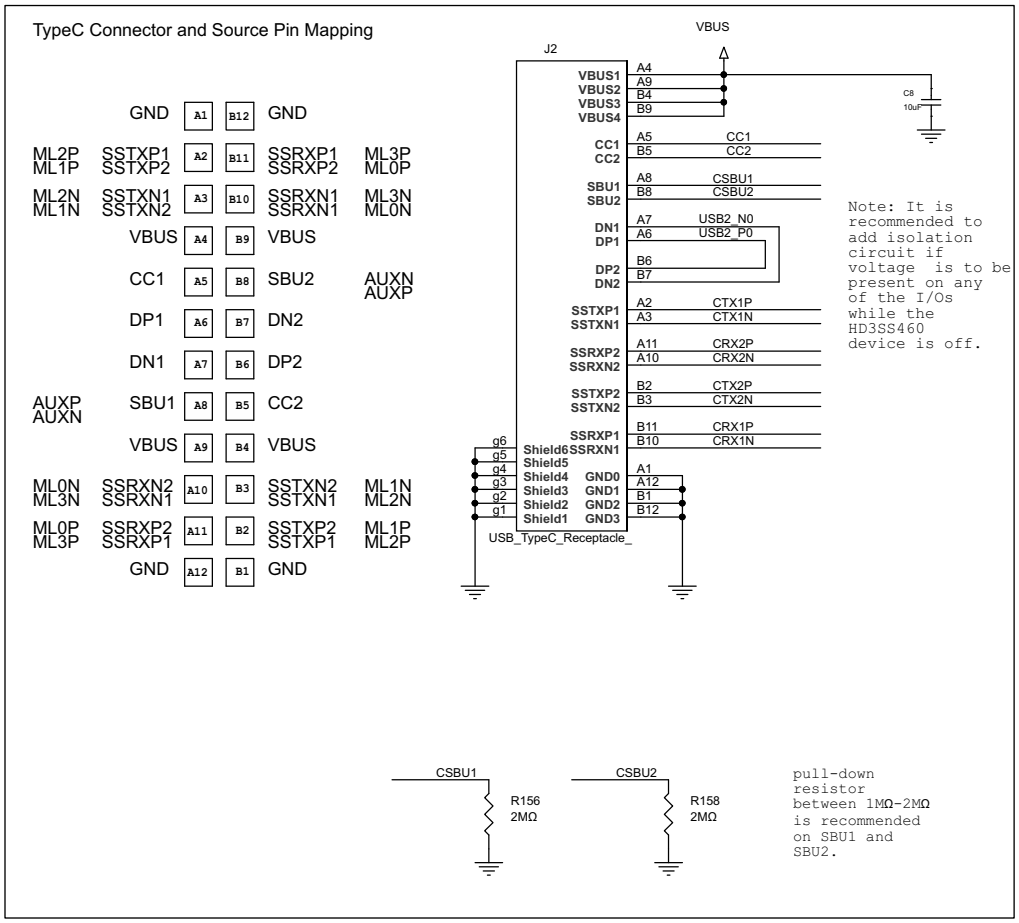


Figure 14. Schematic Implementations for DP Source/ USB Host (1 of 3)

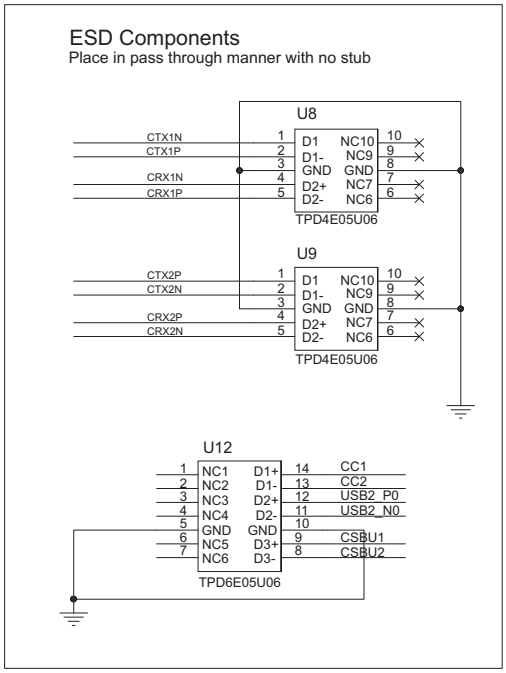


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Figure 15. Schematic Implementations for DP Source/ USB Host (2 of 3)

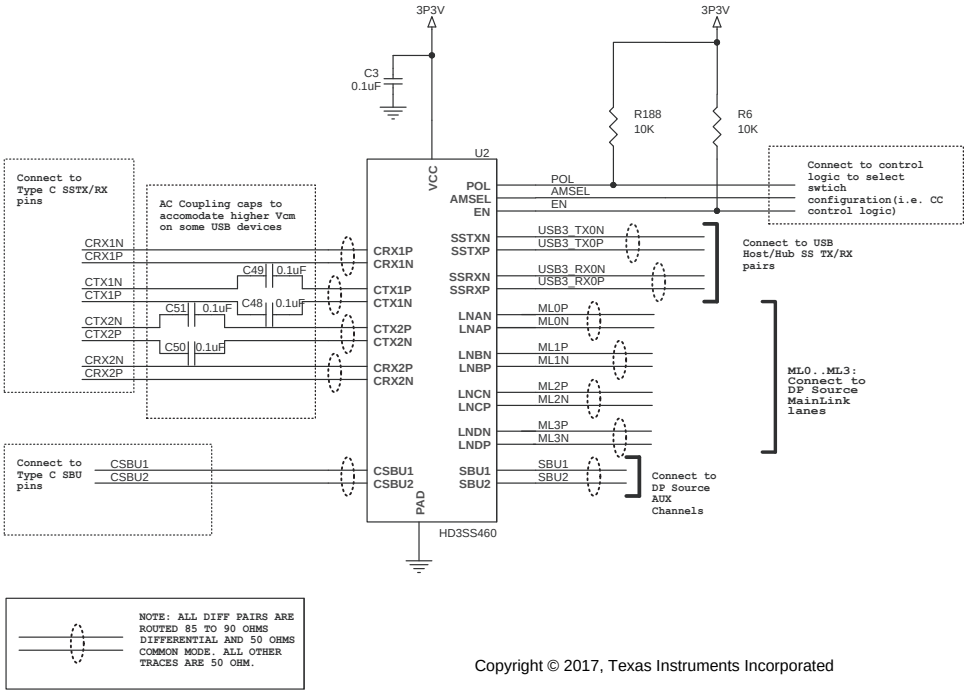

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Figure 16. Schematic Implementations for DP Source/ USB Host (3 of 3)

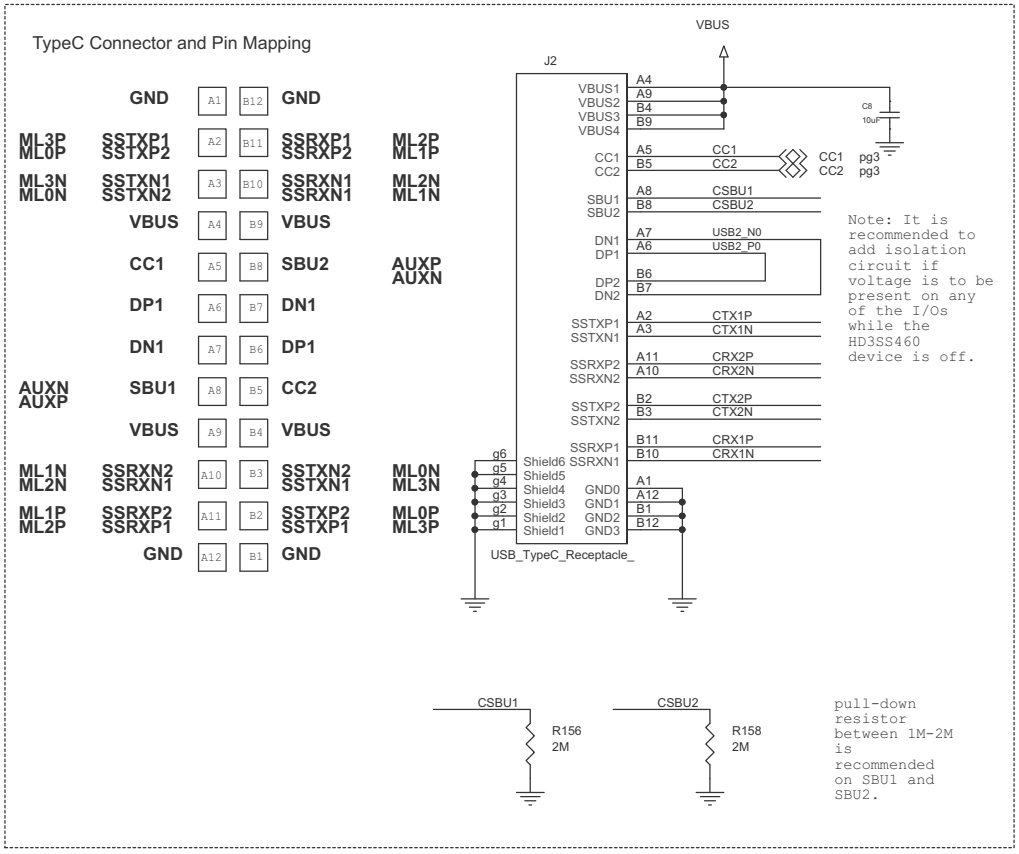


Figure 17. Schematic Implementations for DP Sink/ USB Device/HUB/Dock (1 of 3)

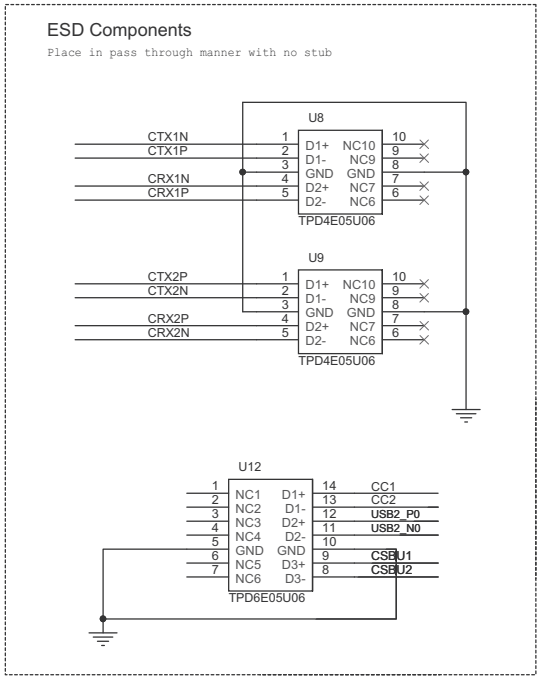


Figure 18. Schematic Implementations for DP Sink/ USB Device/HUB/Dock (2 of 3)

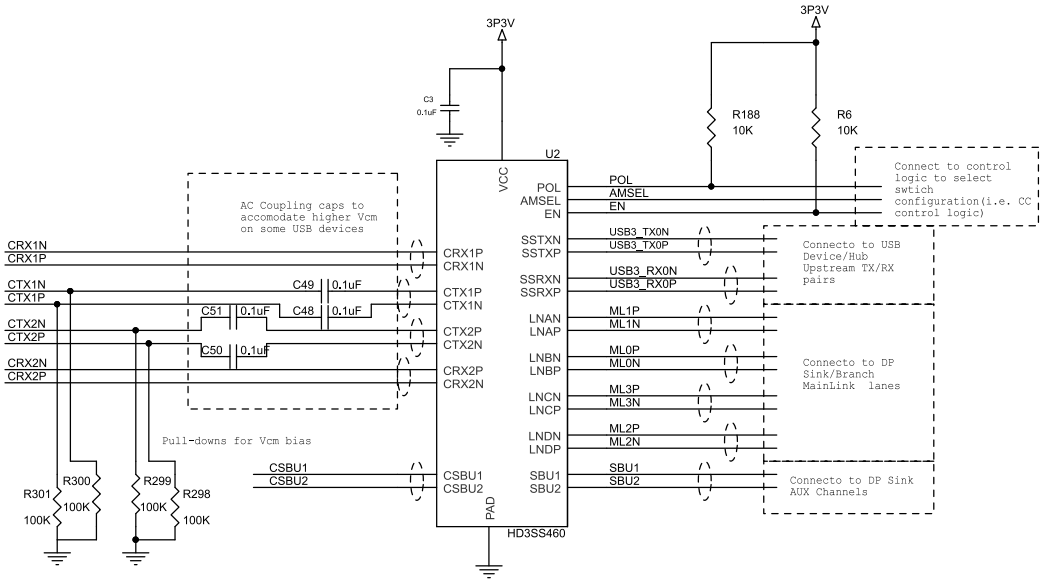


Figure 19. Schematic Implementations for DP Sink/ USB Device/HUB/Dock (3 of 3)

10 Power Supply Recommendations

There is no power supply sequence required for HD3SS460. However it is recommended that EN is asserted low after device supply VCC is stable and within specification. It is also recommended that ample decoupling capacitors are placed at the device V_{CC} near the pin.

11 Layout

11.1 Layout Guidelines

High performance layout practices are paramount for board layout for high speed signals to ensure good signal integrity. Even minor imperfection can cause impedance mismatch resulting reflection. Special care is warranted for traces, connections to device, and connectors.

11.1.1 Critical Routing

The high speed differential signals must be routed with great care to minimize signal quality degradation between the connector and the source or sink of the high speed signals by following the guidelines provided in this document. Depending on the configuration schemes, the speed of each differential pair can reach a maximum speed of 5.4 Gbps. These signals are to be routed first before other signals with highest priority.

- Each differential pair should be routed together with controlled differential impedance of 85 to 90-Ω and 50-Ω common mode impedance. Keep away from other high speed signals. The number of vias should be kept to minimum. Each pair should be separated from adjacent pairs by at least 3 times the signal trace width. Route all differential pairs on the same group of layers (Outer layers or inner layers) if not on the same layer. No 90 degree turns on any of the differential pairs. If bends are used on high speed differential pairs, the angle of the bend should be greater than 135 degrees.
- Length matching:
  - Keep high speed differential pairs lengths within 5 mil of each other to keep the intra-pair skew minimum.
  - The inter-pair matching of the differential pairs is not as critical as intra-pair matching. The SSTX and SSRX pairs do not have to match while they need to be routed as short as possible.
- Keep high speed differential pair traces adjacent to ground plane.
- Do not route differential pairs over any plane split
- ESD components on the high speed differential lanes should be placed nearest to the connector in a pass through manner without stubs on the differential path. In order to control impedance for transmission lines, a solid ground plane should be placed next to the high- speed signal layer. This also provides an excellent low-inductance path for the return current flow.
  - Placement recommendation would be: Connector – ESD Components --- HD3SS460
- For ease of routing, the P and N connection of the USB3.1 differential pairs to the HD3SS460 pins can be swapped as long as the corresponding pairs are swapped on the other end of the switch The example is shown in the reference EVM schematics section of this document. The P/N can be swapped on USB 3.1 connection of the switch for ease of routing purposes.

11.1.2 General Routing/Placement Rules

- Route all high-speed signals first on un-routed PCB: SSTXP/N, SSRXT/N, LNAP/N, LNB P/N, LNC P/N, LND P/N, CTX*P/N. The stub on USB2 D+ and D- pairs should not exceed 3.5mm.
- Follow 20H rule (H is the distance to reference plane) for separation of the high-speed trace from the edge of the plane
- Minimize parallelism of high speed clocks and other periodic signal traces to high speed lines
- All differential pairs should be routed on the top or bottom layer (microstrip traces) if possible or on the same group of layers. Vias should only be used in the breakout region of the device to route from the top to bottom layer when necessary. Avoid using vias in the main region of the board at all cost. Use a ground reference via next to signal via. Distance between ground reference via and signal need to be calculated to have similar impedance as traces.
- All differential signals should not be routed over plane split. Changing signal layers is preferable to crossing plane splits.
- Use of and proper placement of stitching caps when split plane crossing is unavoidable to account for high-frequency return current path
- Route differential traces over a continuous plane with no interruptions.
- Do not route differential traces under power connectors or other interface connectors, crystals, oscillators, or any magnetic source.
- Route traces away from etching areas like pads, vias, and other signal traces. Try to maintain a 20 mil keep-out distance where possible.

Layout Guidelines (continued)

- Decoupling capacitors should be placed next to each power terminal on the HD3SS460. Care should be taken to minimize the stub length of the trace connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling capacitors.
- Place vias as close as possible to the decoupling capacitor solder pad.
- Widen VCC/GND planes to reduce effect of static and dynamic IR drop.
- The VBUS traces/planes must be wide enough to carry maximum of 2 A current.

11.2 Layout Example

Figure 20, Figure 21, and Figure 22 illustrate some guidelines for layout. Actual layout should be optimized for various factors such as board geometry, connector type, and application.

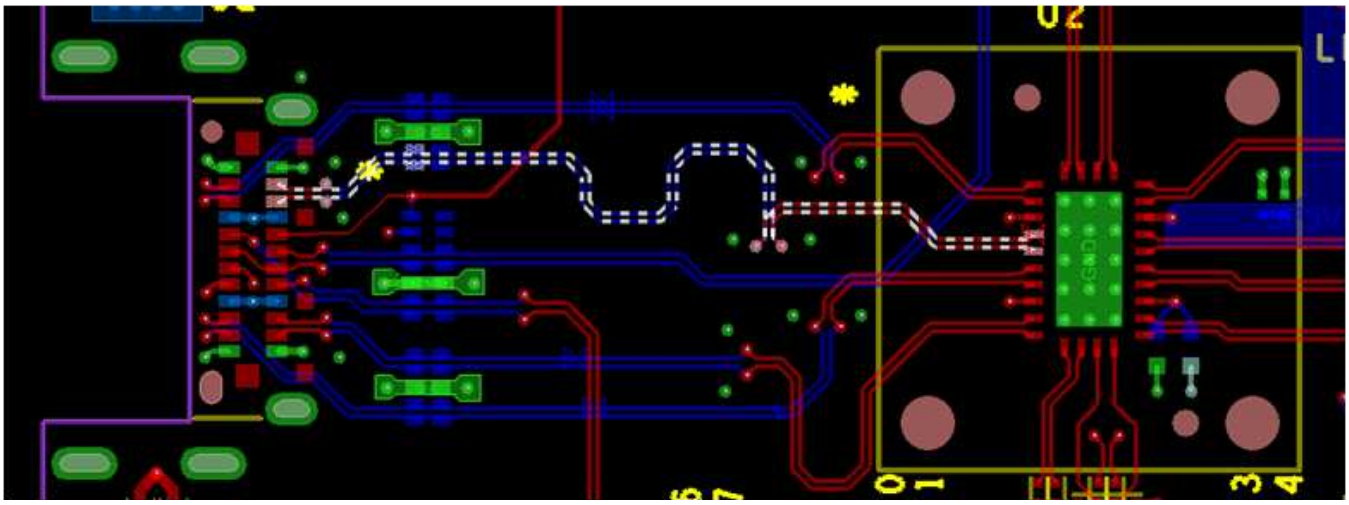


Figure 20. USB Type C Connector to HD3SS460 Signal Routing

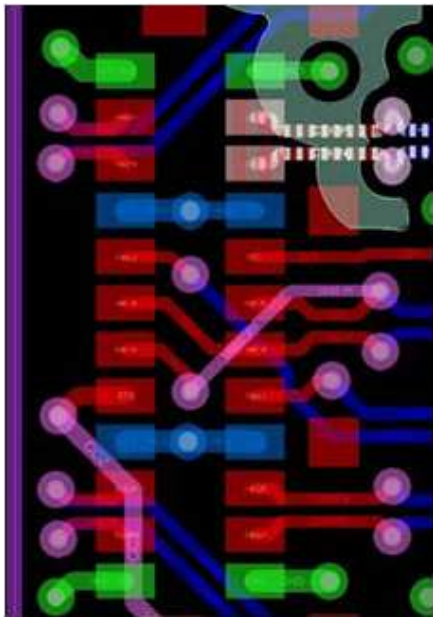


Figure 21. Dual SMT Mid-Mount Type C Connector Layout Example Zoom-in

Layout Example (continued)

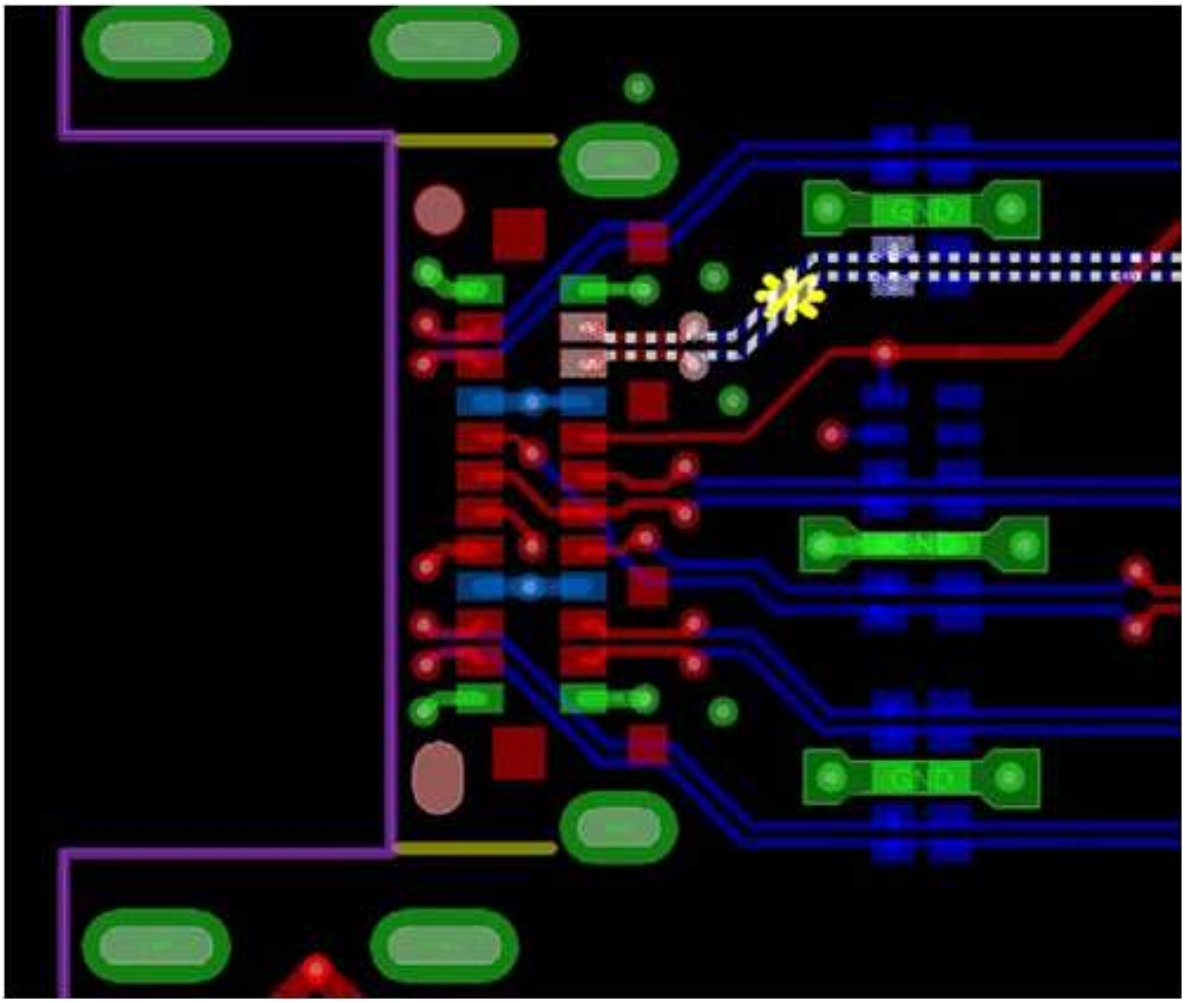


Figure 22. Dual-row SMT Mid-mount Type C with ESD Components

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请访问 www.ti.com.cn 您器件对应的产品文件夹。点击右上角的*提醒我 (Alert me)* 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.
USB Type-C is a trademark of USB-IF, Inc..
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS460IRHRR	ACTIVE	WQFN	RHR	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3SS460I	Samples
HD3SS460IRHRT	ACTIVE	WQFN	RHR	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3SS460I	Samples
HD3SS460IRNHR	ACTIVE	WQFN	RNH	30	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	460IRNH	Samples
HD3SS460IRNHT	ACTIVE	WQFN	RNH	30	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	460IRNH	Samples
HD3SS460RHRR	ACTIVE	WQFN	RHR	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	3SS460	Samples
HD3SS460RHRT	ACTIVE	WQFN	RHR	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	3SS460	Samples
HD3SS460RNHR	ACTIVE	WQFN	RNH	30	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	460RNH	Samples
HD3SS460RNHT	ACTIVE	WQFN	RNH	30	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	460RNH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

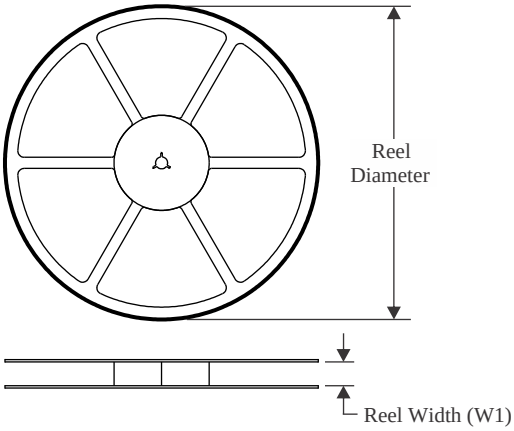
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

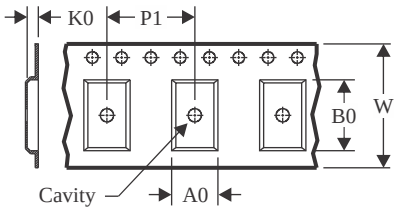
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

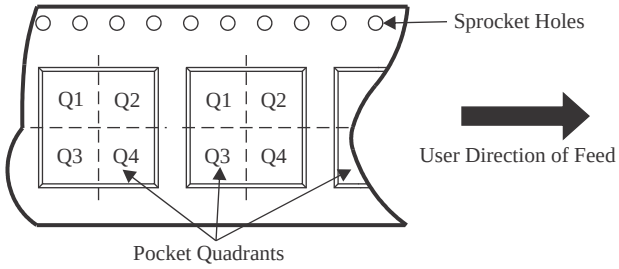


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

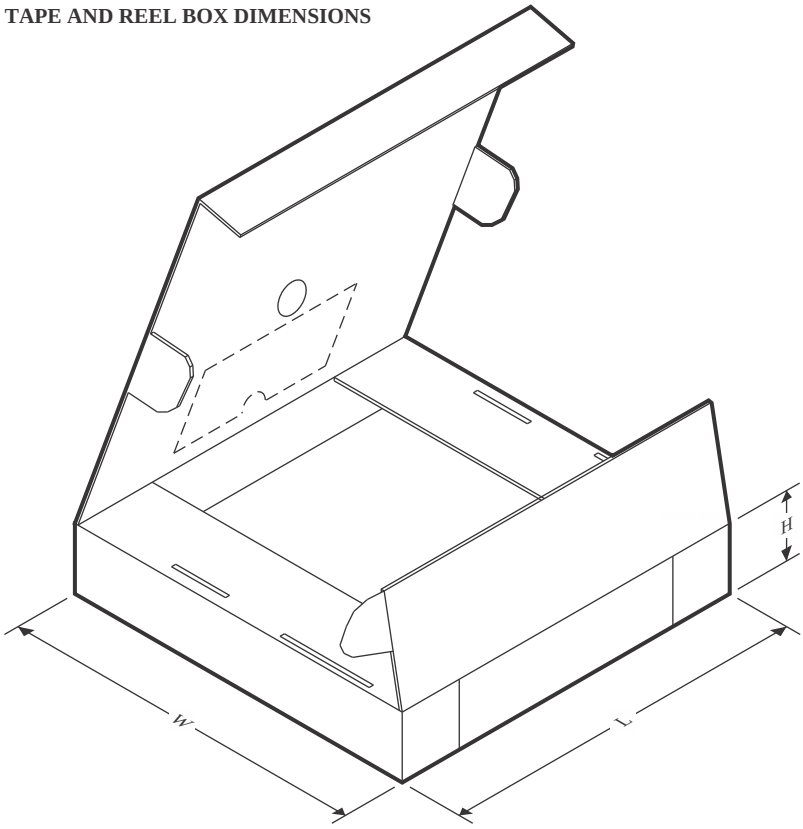
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS460IRHRR	WQFN	RHR	28	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
HD3SS460IRHRT	WQFN	RHR	28	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
HD3SS460IRNHR	WQFN	RNH	30	3000	330.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS460IRNHT	WQFN	RNH	30	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS460RHRR	WQFN	RHR	28	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
HD3SS460RHRT	WQFN	RHR	28	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
HD3SS460RNHR	WQFN	RNH	30	3000	330.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS460RNHT	WQFN	RNH	30	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS460IRHRR	WQFN	RHR	28	3000	367.0	367.0	35.0
HD3SS460IRHRT	WQFN	RHR	28	250	210.0	185.0	35.0
HD3SS460IRNHR	WQFN	RNH	30	3000	367.0	367.0	35.0
HD3SS460IRNHT	WQFN	RNH	30	250	210.0	185.0	35.0
HD3SS460RHRR	WQFN	RHR	28	3000	367.0	367.0	35.0
HD3SS460RHRT	WQFN	RHR	28	250	210.0	185.0	35.0
HD3SS460RNHR	WQFN	RNH	30	3000	367.0	367.0	35.0
HD3SS460RNHT	WQFN	RNH	30	250	210.0	185.0	35.0

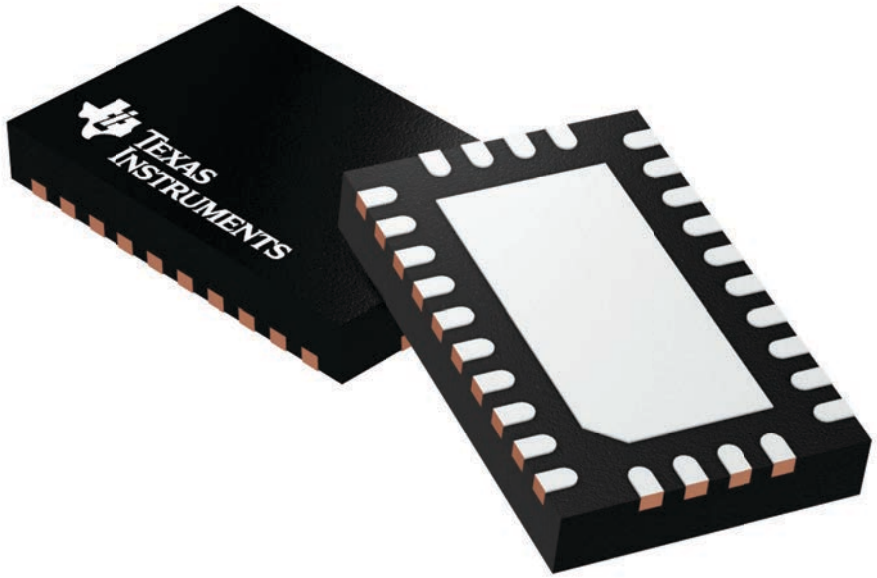
GENERIC PACKAGE VIEW

RHR 28

WQFN - 0.8 mm max height

3.5 x 5.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

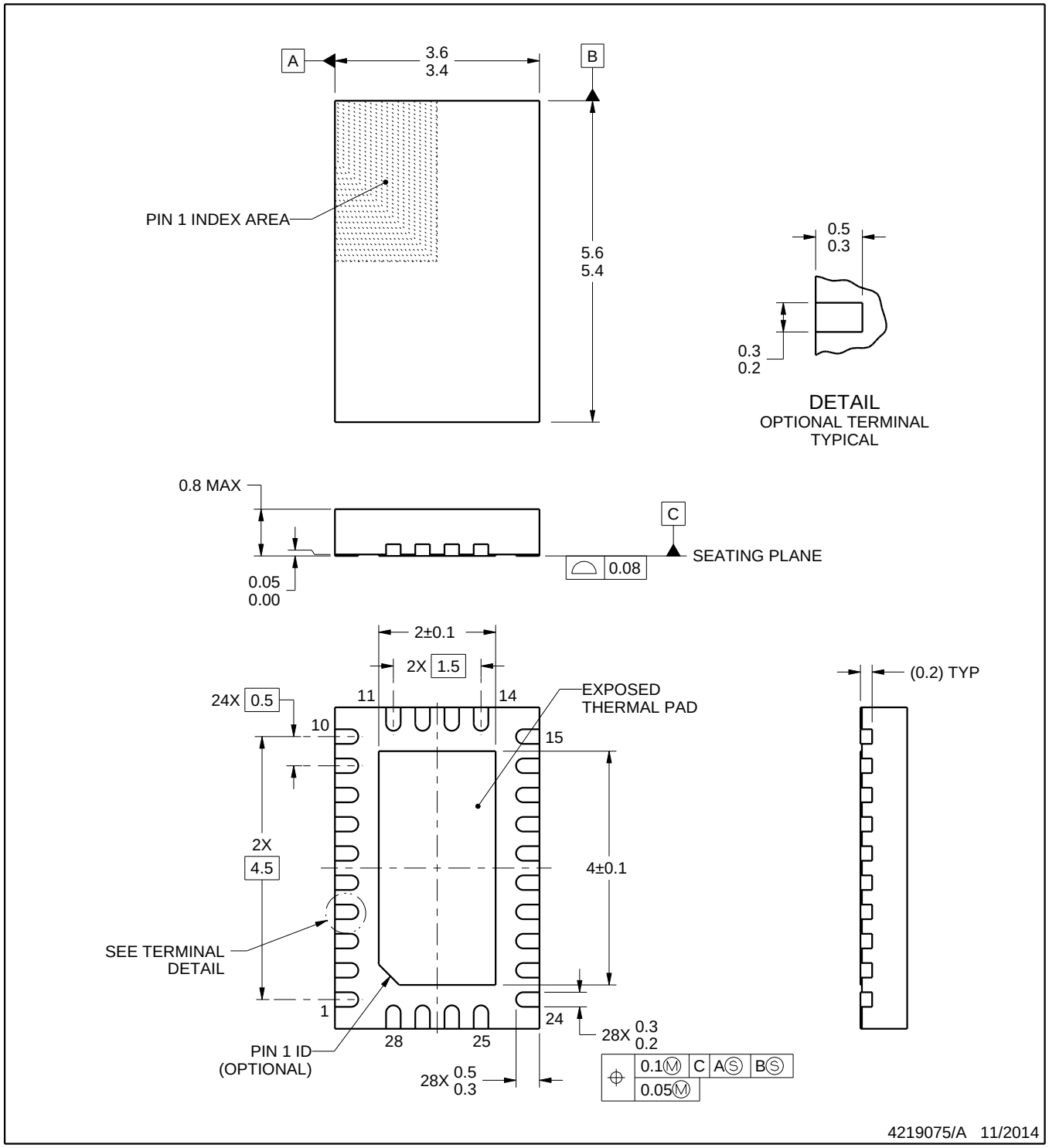
4210249/B

PACKAGE OUTLINE

RHR0028A

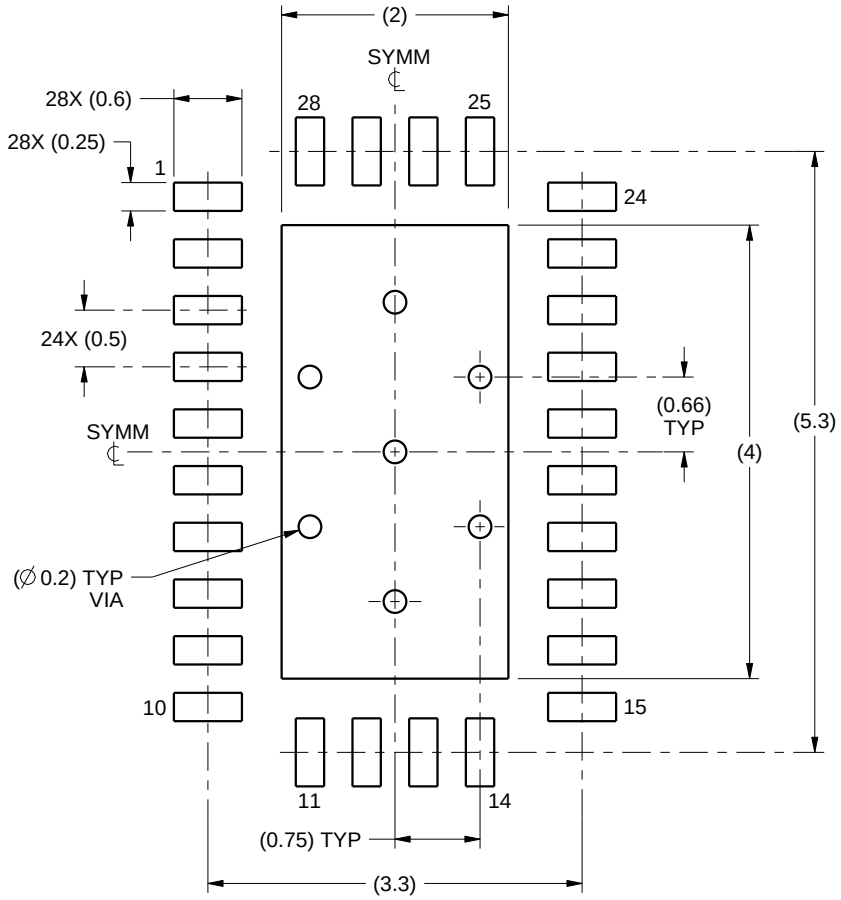
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

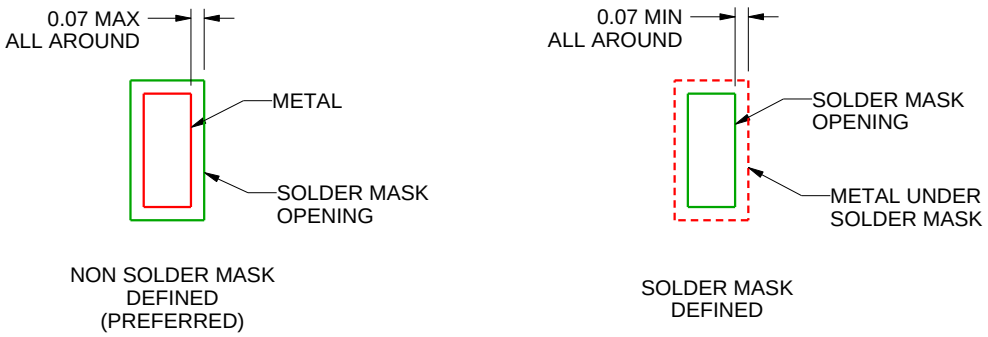


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

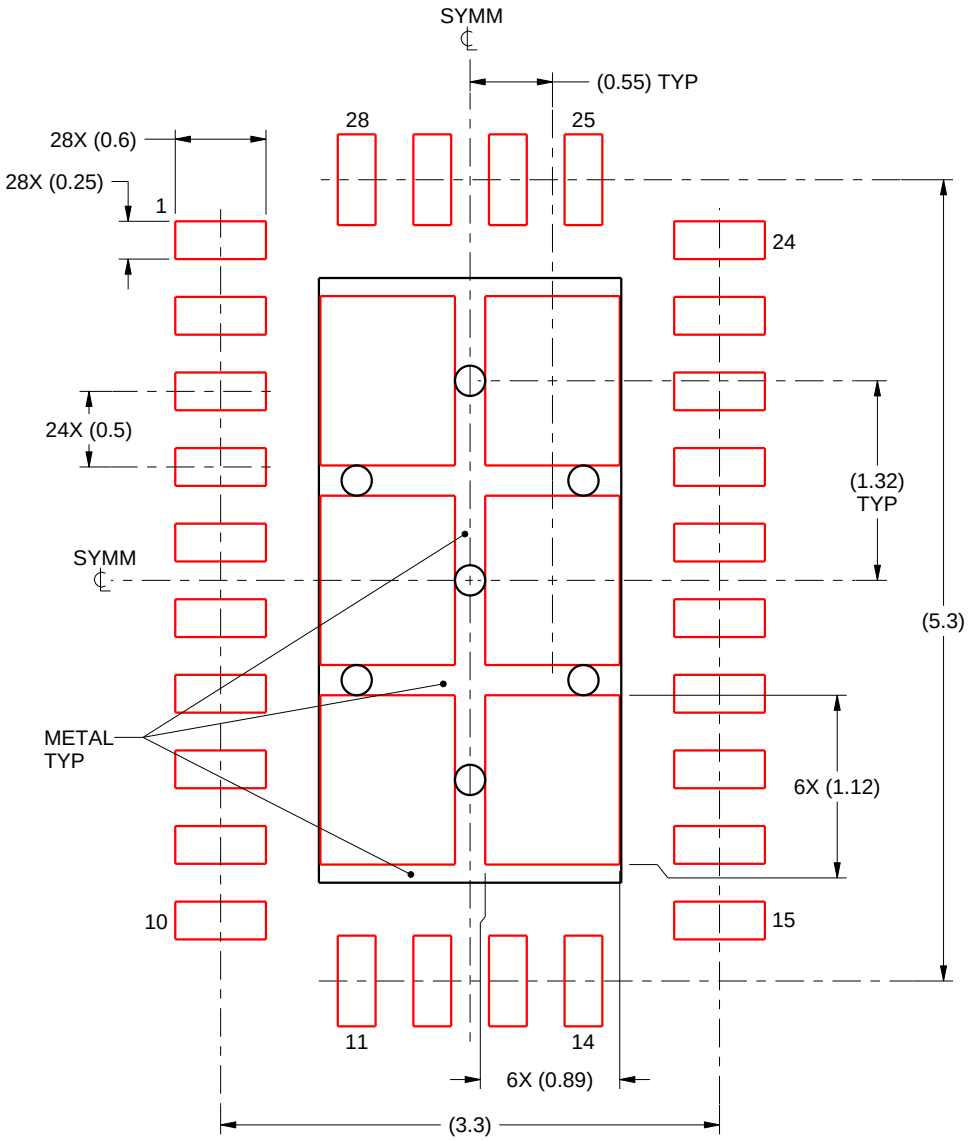


SOLDER MASK DETAILS

4219075/A 11/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219075/A 11/2014

NOTES: (continued)

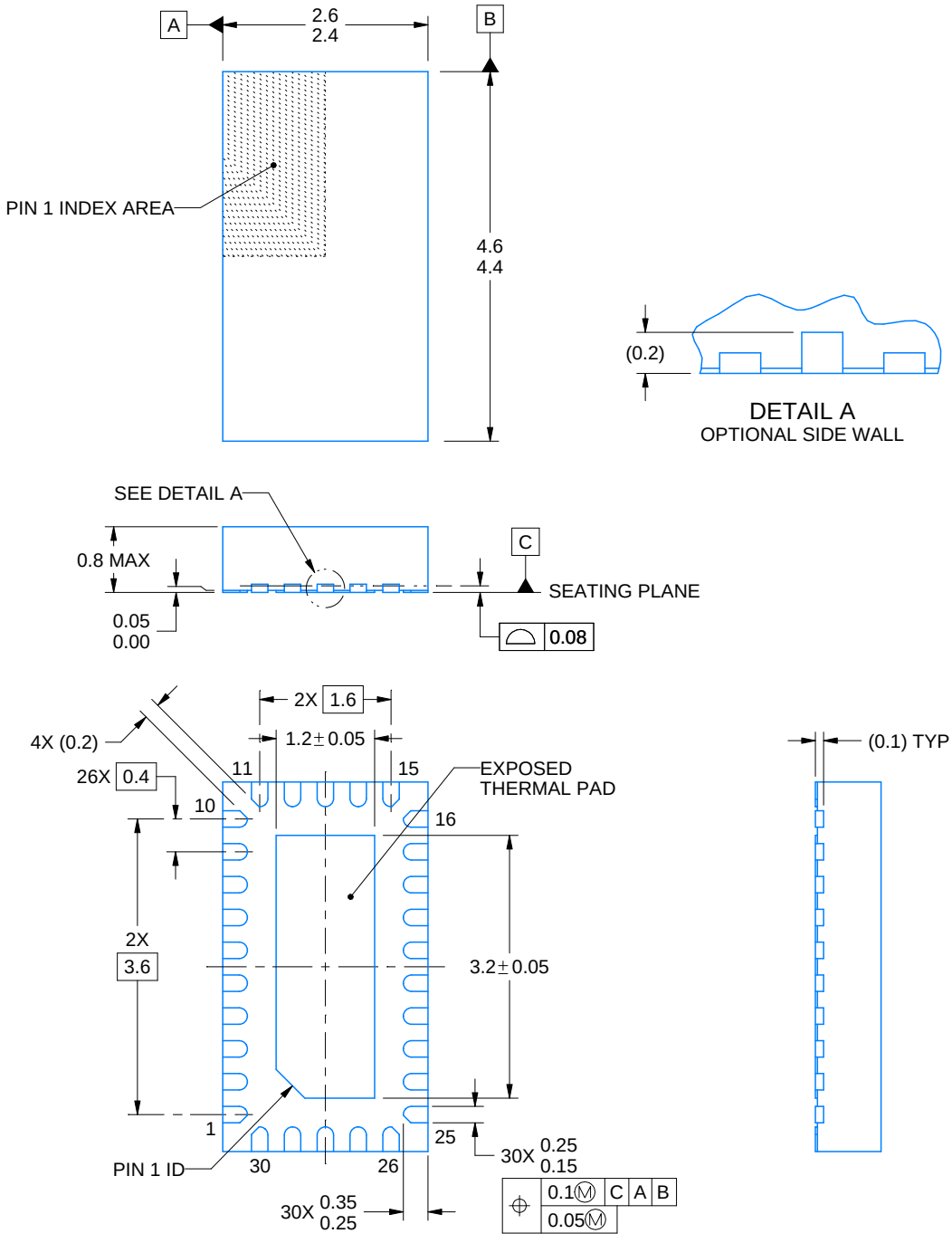
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RNH0030A

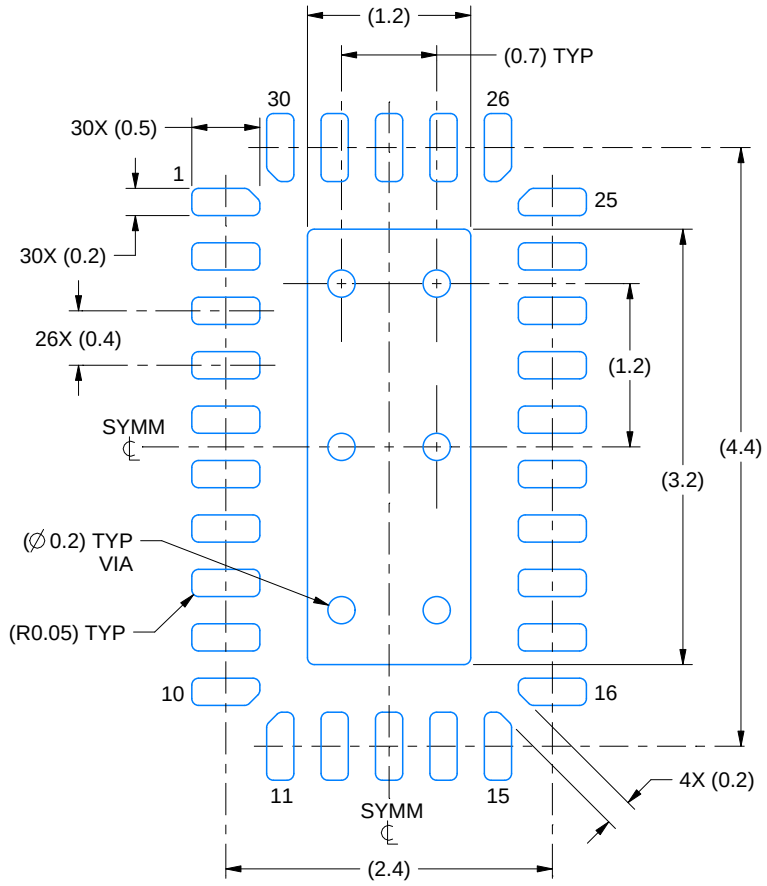
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

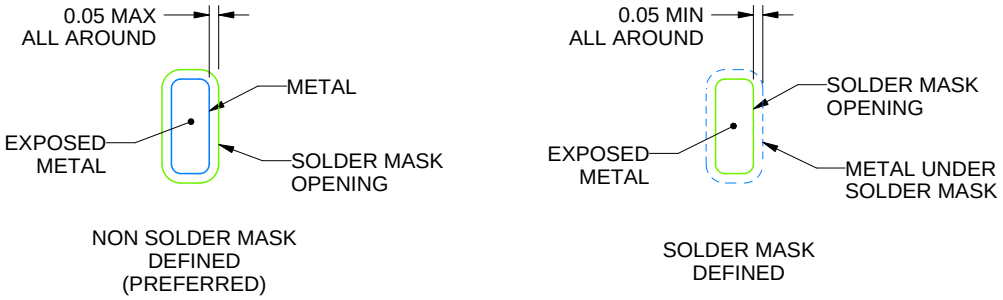


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

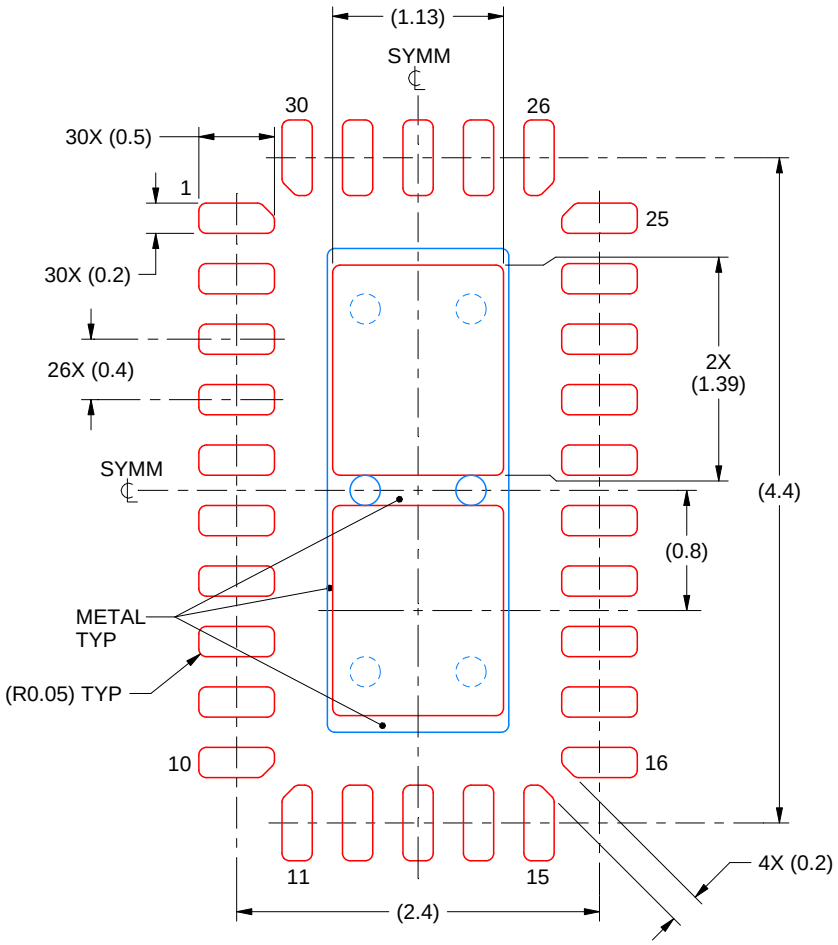


SOLDER MASK DETAILS

4221819/B 10/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4221819/B 10/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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