

## CDx4HC4075 三路 3 输入或门

### 1 特性

- 缓冲输入
- 宽工作电压范围：2V 至 6V
- 宽工作温度范围：-55°C 至 +125°C
- 支持多达 10 个 LSTTL 负载的扇出
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗

### 2 应用

- 通过更少的输入来监控误差信号
- 将低电平有效使能信号进行结合

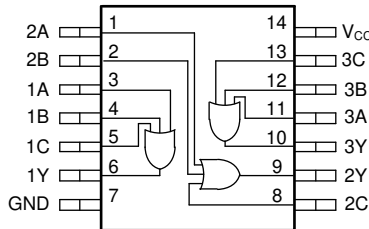
### 3 说明

该器件包含三个独立的 3 输入或门。每个逻辑门以正逻辑执行布尔函数  $Y = A + B + C$ 。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
CD74HC4075M	SOIC (14)	8.70mm × 3.90mm
CD74HC4075E	PDIP (14)	19.30mm × 6.40mm
CD74HC4075NS	SO (14)	10.20mm × 5.30mm
CD74HC4075PW	TSSOP (14)	5.00mm × 4.40mm
CD54HC4075F	CDIP (14)	21.30mm × 7.60mm
CD54HC4075FK	LCCC (20)	8.90mm × 8.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能引脚分配

## Table of Contents

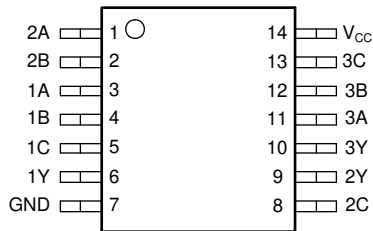
<b>1 特性</b> .....	1	8.2 Functional Block Diagram.....	8
<b>2 应用</b> .....	1	8.3 Feature Description.....	8
<b>3 说明</b> .....	1	8.4 Device Functional Modes.....	9
<b>4 Revision History</b> .....	2	<b>9 Application and Implementation</b> .....	10
<b>5 Pin Configuration and Functions</b> .....	3	9.1 Application Information.....	10
Pin Functions.....	3	9.2 Typical Application.....	10
<b>6 Specifications</b> .....	4	<b>10 Power Supply Recommendations</b> .....	12
6.1 Absolute Maximum Ratings.....	4	<b>11 Layout</b> .....	13
6.2 ESD Ratings.....	4	11.1 Layout Guidelines.....	13
6.3 Recommended Operating Conditions.....	4	11.2 Layout Example.....	13
6.4 Thermal Information.....	5	<b>12 Device and Documentation Support</b> .....	14
6.5 Electrical Characteristics.....	5	12.1 Documentation Support.....	14
6.6 Switching Characteristics.....	5	12.2 支持资源.....	14
6.7 Operating Characteristics.....	6	12.3 Trademarks.....	14
6.8 Typical Characteristics.....	6	12.4 静电放电警告.....	14
<b>7 Parameter Measurement Information</b> .....	7	12.5 术语表.....	14
<b>8 Detailed Description</b> .....	8	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	14
8.1 Overview.....	8		

## 4 Revision History

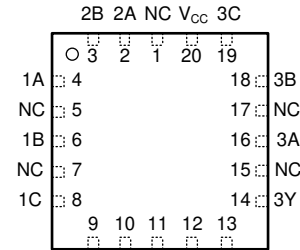
注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision G (June 2006) to Revision H (June 2021)</b>	<b>Page</b>
• 更新至全新的数据表标准.....	1
• 将 HCT 器件移至单独的数据表 (SCHS408).....	1
• $R_{\theta JA}$ increased for the D (86 to 133.6 °C/W), PW (133 to 151.7 °C/W), and NS (76 to 122.6 °C/W) packages and decreased for the N package (80 to 61.3 °C/W).....	5

## 5 Pin Configuration and Functions



**D, N, NS, PW, or J Package**  
**14-Pin SOIC, PDIP, SO, TSSOP, or CDIP**  
**Top View**



**FK Package**  
**20-Pin LCCC**  
**Top View**

## Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D, N, NS, PW, or J	FK		
2A	1	2	Input	Channel 2, Input A
2B	2	3	Input	Channel 2, Input B
1A	3	4	Input	Channel 1, Input A
1B	4	6	Input	Channel 1, Input B
1C	5	8	Input	Channel 1, Input C
1Y	6	9	Output	Channel 1, Output Y
GND	7	10	—	Ground
2C	8	12	Input	Channel 2, Input C
2Y	9	13	Output	Channel 2, Output Y
3Y	10	14	Output	Channel 3, Output Y
3A	11	16	Input	Channel 3, Input A
3B	12	18	Input	Channel 3, Input B
3C	13	19	Input	Channel 3, Input C
V <sub>CC</sub>	14	20	—	Positive Supply
NC		1, 5, 7, 11, 15, 17	—	Not internally connected

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	- 0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < - 0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < - 0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA
T <sub>J</sub>	Junction temperature <sup>(3)</sup>	Plastic package		150 °C
		Hermetic package or die		175 °C
	Lead temperature (soldering 10s)	SOIC - lead tips only		300 °C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

### 6.2 ESD Ratings

		VALUE	UNIT
<b>CD74HC4075 IN D (SOIC) AND N (PDIP) PACKAGES</b>			
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000 V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 4.5 V		1.35	
		V <sub>CC</sub> = 6 V		1.8	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
t <sub>t</sub>	Input transition time	V <sub>CC</sub> = 2 V		1000	ns
		V <sub>CC</sub> = 4.5 V		500	
		V <sub>CC</sub> = 6 V		400	
T <sub>A</sub>	Operating free-air temperature	CD74HC4075		- 55	125 °C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD74HC4075				UNIT
		PW (TSSOP)	N (PDIP)	D (SOIC)	NS (SOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	61.3	133.6	122.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	49.0	89.0	81.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	41.0	89.5	83.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	25.2	28.7	45.5	45.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	94.1	40.8	89.1	83.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT
			25°C			- 40°C to 85°C			- 55°C to 125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2 V	1.9		1.9		1.9		V	
				4.5 V	4.4		4.4					
				6 V	5.9		5.9					
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -4 \text{ mA}$	4.5 V	3.98		3.84		3.7		V	
				6 V	5.48		5.34		5.2			
				6 V	5.48		5.34		5.2			
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2 V	0.1		0.1		0.1		V	
				4.5 V	0.1		0.1		0.1			
				6 V	0.1		0.1		0.1			
			$I_{OL} = 4 \text{ mA}$	4.5 V	0.26		0.33		0.4			
$I_{OL} = 5.2 \text{ mA}$	6 V	0.26		0.33		0.4						
$I_I$	Input leakage current	$V_I = V_{CC}$ or 0	6 V	$\pm 0.1$		$\pm 1$		$\pm 1$		$\mu\text{A}$		
$I_{CC}$	Supply current	$V_I = V_{CC}$ or 0	$I_O = 0$	6 V	2		20		40		$\mu\text{A}$	
$C_i$	Input capacitance		5 V	10		10		10		pF		

## 6.6 Switching Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT
					25°C			- 40°C to 85°C			- 55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{pd}$	Propagation delay	A, B, or C	Y	$C_L = 50 \text{ pF}$	2 V	100		125		150		ns		
					4.5 V	20		25		30				
					6 V	17		21		26				
		A, B, or C	Y	$C_L = 15 \text{ pF}$	5 V	8								

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT
					25°C			- 40°C to 85°C			- 55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_t$	Transition-time	Y	$C_L = 50\text{ pF}$	2 V	75			95			110			ns
				4.5 V	15			19			22			
				6 V	13			16			19			

### 6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance per gate No load	2 V to 6 V		26		pF

### 6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$

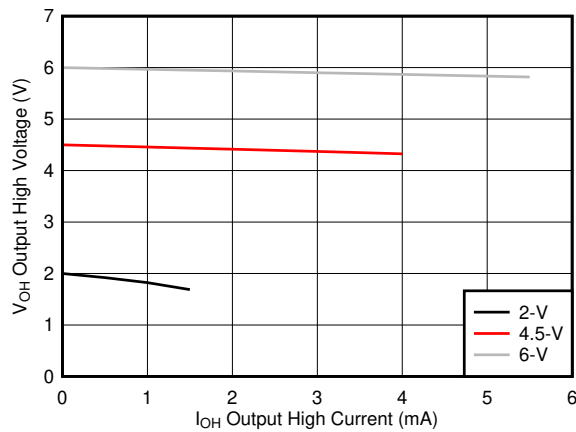


图 6-1. Typical output voltage in the high state ( $V_{OH}$ )

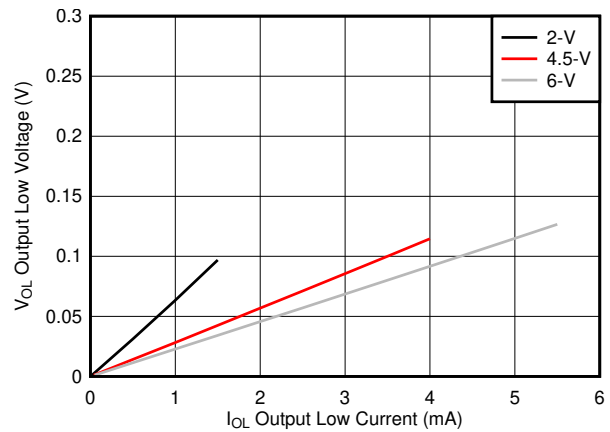
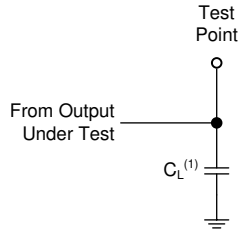


图 6-2. Typical output voltage in the low state ( $V_{OL}$ )

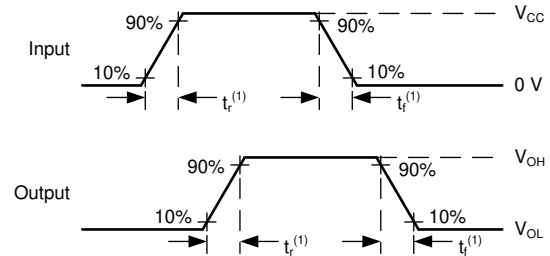
## 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .
- The outputs are measured one at a time, with one input transition per measurement.



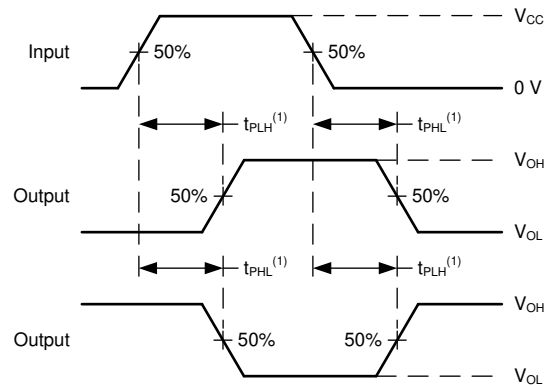
A.  $C_L = 50 \text{ pF}$  and includes probe and jig capacitance.

图 7-1. Load Circuit



A.  $t_t$  is the greater of  $t_r$  and  $t_f$ .

图 7-2. Voltage Waveforms Transition Times



A. The maximum between  $t_{PLH}$  and  $t_{PHL}$  is used for  $t_{pd}$ .

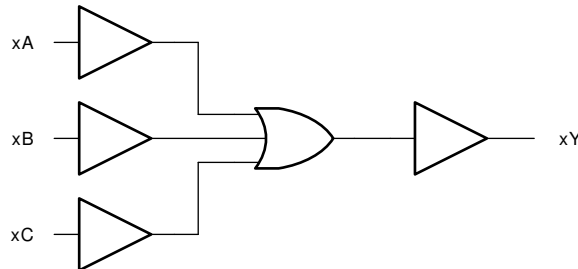
图 7-3. Voltage Waveforms Propagation Delays

## 8 Detailed Description

### 8.1 Overview

This device contains three independent 3-input OR gates. Each gate performs the Boolean function  $Y = A + B + C$  in positive logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [§ 6.1](#) must be followed at all times.

The CD74HC4075 can drive a load with a total capacitance less than or equal to the maximum load listed in the [§ 6.6](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [§ 6.1](#).

#### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [§ 6.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [§ 6.1](#), and the maximum input leakage current, given in the [§ 6.5](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the [§ 6.3](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.



### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 图 8-1.

**CAUTION**

Voltages beyond the values specified in the 节 6.1 table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.4 Device Functional Modes

表 8-1. Function Table

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

In this application, one 3-input OR gates is used to combine overhear signals to control a fan as shown in [图 9-1](#). The other two gates can be used for another application in the system, or the inputs can be grounded and the channels left unused.

This device is used to directly control the Enable pin of a fan driver. The fan driver requires only one input signal to be HIGH before being enabled, and should be disabled in the event that all signals go LOW. The 4-input OR gate function combines the four individual overhear signals into a single active-high enable signal.

### 9.2 Typical Application

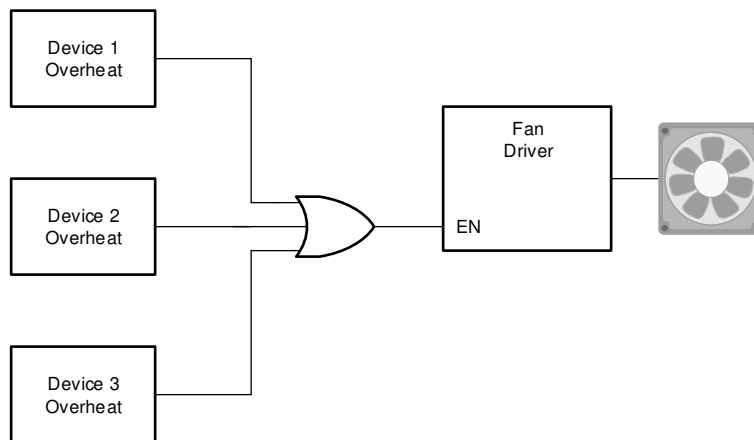


图 9-1. Typical application schematic

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [节 6.3](#). The supply voltage sets the device's electrical characteristics as described in the [节 6.5](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HC4075 plus the maximum supply current,  $I_{CC}$ , listed in the [节 6.5](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or  $V_{CC}$  listed in the [节 6.1](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_J(\text{max})$  listed in the [节 6.1](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [节 6.1](#). These limits are provided to prevent damage to the device.

### 9.2.1.2 Input Considerations

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HC4075, as specified in the [§ 6.5](#), and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The CD74HC4075 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [§ 6.3](#).

Refer to the [§ 8.3](#) for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the [§ 6.5](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [§ 6.5](#).

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to [§ 8.3](#) for additional information regarding the outputs for this device.

## 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the [§ 11](#).
2. Ensure the capacitive load at the output is  $\leq 70$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HC4075 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the [§ 6.1](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

## 9.2.3 Application Curves

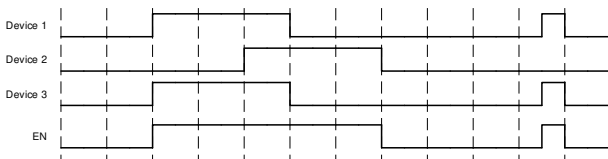


图 9-2. Typical application timing diagram

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [# 6.3](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [图 11-1](#).

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

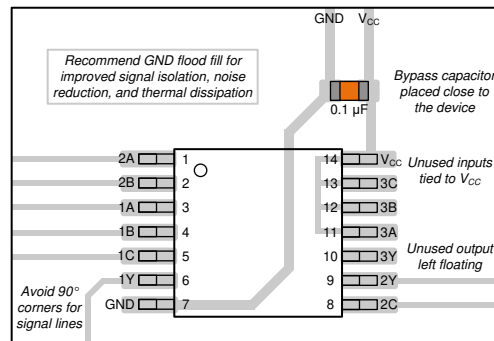


图 11-1. Example layout for the CD74HC4075

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

### 12.2 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87722012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87722012A CD54HC4075FK	<a href="#">Samples</a>
5962-8772201CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8772201CA CD54HC4075F3A	<a href="#">Samples</a>
CD54HC4075F3A	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8772201CA CD54HC4075F3A	<a href="#">Samples</a>
CD54HC4075FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87722012A CD54HC4075FK	<a href="#">Samples</a>
CD74HC4075E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4075E	<a href="#">Samples</a>
CD74HC4075EE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4075E	<a href="#">Samples</a>
CD74HC4075M	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4075M	<a href="#">Samples</a>
CD74HC4075M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HC4075M	<a href="#">Samples</a>
CD74HC4075MT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4075M	<a href="#">Samples</a>
CD74HC4075NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4075M	<a href="#">Samples</a>
CD74HC4075PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4075	<a href="#">Samples</a>
CD74HC4075PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HJ4075	<a href="#">Samples</a>
CD74HC4075PWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4075	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF CD54HC4075, CD74HC4075 :**

● Catalog : [CD74HC4075](#)

● Military : [CD54HC4075](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4075M96	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HC4075M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4075MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4075NSR	SO	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD74HC4075PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
CD74HC4075PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4075PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4075M96	SOIC	D	14	2500	366.0	364.0	50.0
CD74HC4075M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC4075MT	SOIC	D	14	250	210.0	185.0	35.0
CD74HC4075NSR	SO	NS	14	2000	356.0	356.0	35.0
CD74HC4075PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
CD74HC4075PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
CD74HC4075PWT	TSSOP	PW	14	250	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-87722012A	FK	LCCC	20	1	506.98	12.06	2030	NA
CD54HC4075FK	FK	LCCC	20	1	506.98	12.06	2030	NA
CD74HC4075E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4075E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4075EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4075EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4075M	D	SOIC	14	50	506.6	8	3940	4.32
CD74HC4075PW	PW	TSSOP	14	90	530	10.2	3600	3.5

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\diamond$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.



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