# AM26LS31x 四路差动线路驱动器

## 1 特性

- 符合或超出 ANSI TIA/EIA-422-B 和 ITU 的要求
- 采用 5V 单电源供电
- TTL 兼容
- 互补输出
- 断电时具有高输出阻抗
- 互补输出使能输入
- 可用的已通过 MIL-PRF-38535 认证的选项 (M)：除非另有说明，否则所有参数均经过测试。对于所有其他产品，生产流程不一定包含对所有参数的测试。

## 2 应用

- 电机编码器
- 现场发送器：压力传感器和温度传感器
- 军用和航空电子成像
- 采用 Modbus 的温度传感器或控制器

## 3 说明
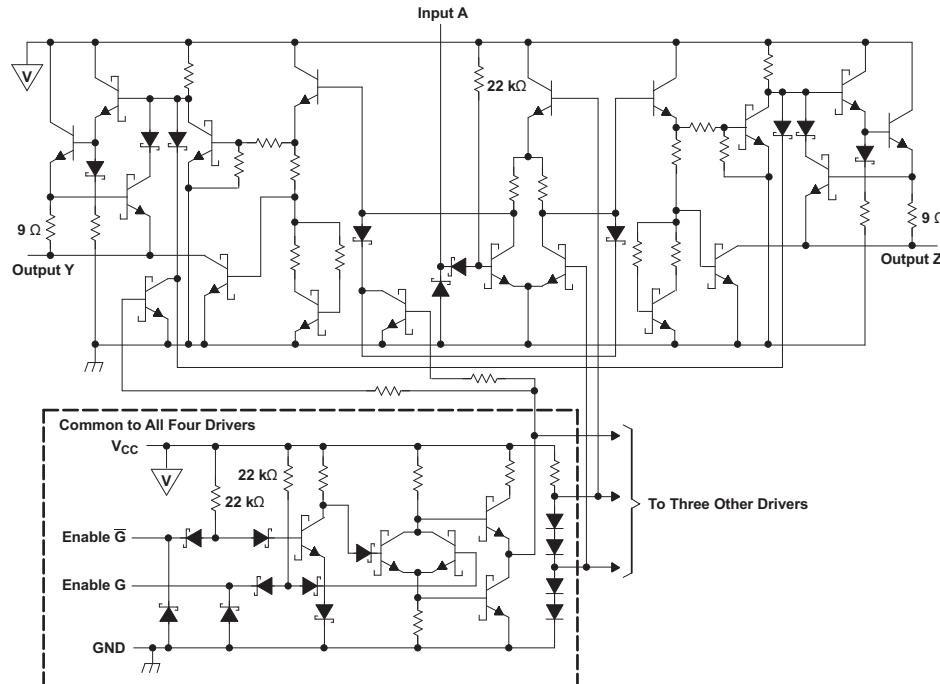
AM26LS31 系列器件是四路互补输出线路驱动器，可满足 ANSI TIA/EIA-422-B 和 ITU（原 CCITT）建议 V.11 的要求。三态输出可提供用于驱动双绞线或平行双线传输线路等平衡线路的高电流，并在断电情况下处于高阻抗状态。四个驱动器均具有使能功能，该功能提供了两种可选输入：高电平有效使能和低电平有效使能（G、$\overline{\text{G}}$）输入。低功耗肖特基电路可在不牺牲速度的情况下降低功耗。

### 器件信息[1]

| 器件编号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| AM26LS31MFK | LCCC (20) | 8.89mm x 8.89mm |
| AM26LS31MJ | CDIP (16) | 19.60mm × 6.92mm |
| AM26LS31MW | CFP (16) | 10.30mm × 6.73mm |
| AM26LS31CD | SOIC (16) | 9.90mm x 3.91mm |
| AM26LS31CDB | SSOP (16) | 6.20mm × 5.30mm |
| AM26LS31CN | PDIP (16) | 19.30mm x 6.35mm |
| AM26LS31xNS | SO (16) | 10.30mm × 5.30mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

原理图（每个驱动器）



All resistor values are nominal.

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## 目录

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision K (July 2016) to Revision L**         **Page**

**Changes from Revision J (January 2014) to Revision K**         **Page**
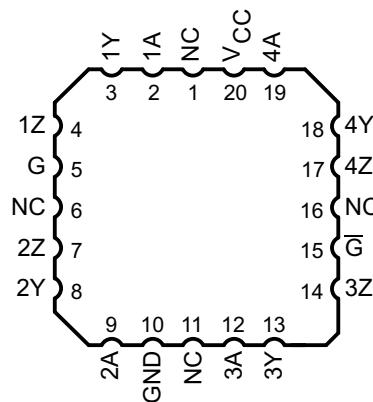
**Changes from Revision I (February 2006) to Revision J**         **Page**

# 5 Pin Configuration and Functions

**D, DB, N , NS, J, or W Package**
**SOIC, SSOP, PDIP, SO, CDIP, or CFP**
**Top View**

```
1A   [ 1      16 ]  V_CC
1Y   [ 2      15 ]  4A
1Z   [ 3      14 ]  4Y
G    [ 4      13 ]  4Z
2Z   [ 5      12 ]  G̅
2Y   [ 6      11 ]  3Z
2A   [ 7      10 ]  3Y
GND  [ 8       9 ]  3A
```

**FK Package**
**20-Pin LCCC**
**Top View**

```
            1Y  1A  NC  V_CC 4A
             3   2   1   20  19
1Z   4                        18  4Y
G    5                        17  4Z
NC   6                        16  NC
2Z   7                        15  G̅
2Y   8                        14  3Z
             9   10  11  12  13
            2A  GND  NC  3A  3Y
```

## Pin Functions

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, SSOP, PDIP, SO, CDIP, or CFP | LCCC | | |
| 1A | 1 | 2 | I | Logic Data Input to RS422 Driver number 1 |
| 1Y | 2 | 3 | O | RS-422 Data Line (Driver 1) |
| 1Z | 3 | 4 | O | RS-422 Data Line (Driver 1) |
| G | 4 | 5 | I | Driver Enable (active high) |
| G̅ | 12 | 15 | I | Driver Enable (active Low) |
| 2A | 7 | 9 | I | Logic Data Input to RS422 Driver number 2 |
| 2Y | 6 | 8 | O | RS-422 Data Line (Driver 2) |
| 2Z | 5 | 7 | O | RS-422 Data Line (Driver 2) |
| 3A | 9 | 12 | I | Logic Data Input to RS422 Driver number 3 |
| 3Y | 10 | 13 | O | RS-422 Data Line (Driver 3) |
| 3Z | 11 | 14 | O | RS-422 Data Line (Driver 3) |
| 4A | 15 | 19 | I | Logic Data Input to RS422 Driver number 4 |
| 4Y | 14 | 18 | O | RS-422 Data Line (Driver 4) |
| 4Z | 13 | 17 | O | RS-422 Data Line (Driver 4) |
| VCC | 16 | 20 | – | Power Input. Connect to 5-V Power Source. |
| GND | 8 | 10 | – | Device Ground Pin |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

|       |                                               |           | MIN | MAX | UNIT |
|-------|-----------------------------------------------|-----------|-----|-----|------|
| $V_{CC}$ | Supply voltage[2]                          |           |     | 7   | V    |
| $V_I$ | Input voltage                                 |           |     | 7   | V    |
|       | Output off-state voltage                      |           |     | 5.5 | V    |
|       | Lead temperature 1,6 mm (1/16 in) from case for 10 s |    |     | 260 | °C   |
|       | Lead temperature 1,6 mm (1/16 in) from case for 60 s | J package | | 300 | °C   |
| $T_{stg}$ | Storage temperature                       |           | −65 | 150 | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential output voltage $V_{OD}$, are with respect to network GND.

## 6.2 ESD Ratings

|           |                        |                                                              | VALUE | UNIT |
|-----------|------------------------|--------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]        | ±2000 | V    |
|           |                        | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

|          |                              |           | MIN  | NOM | MAX  | UNIT |
|----------|------------------------------|-----------|------|-----|------|------|
| $V_{CC}$ | Supply voltage               | AM26LS31C | 4.75 | 5   | 5.25 | V    |
|          |                              | AM26LS31M | 4.5  | 5   | 5.5  |      |
| $V_{IH}$ | High-level input voltage     |           | 2    |     |      | V    |
| $V_{IL}$ | Low-level input voltage      |           |      |     | 0.8  | V    |
| $I_{OH}$ | High-level output current    |           |      |     | −20  | mA   |
| $I_{OL}$ | Low-level output current     |           |      |     | 20   | mA   |
| $T_A$    | Operating free-air temperature | AM26LS31C | 0  |     | 70   | °C   |
|          |                              | AM26LS31I | −40  |     | 85   |      |
|          |                              | AM26LS31M | −55  |     | 125  |      |

## 6.4 Thermal Information

|                   | THERMAL METRIC[1]                          | AM26LS31x | | | | UNIT |
|-------------------|--------------------------------------------|-----------|-----------|-----------|-----------|------|
|                   |                                            | D (SOIC)  | DB (SSOP) | N (PDIP)  | NS (SO)   |      |
|                   |                                            | 16 PINS   | 16 PINS   | 16 PINS   | 16 PINS   |      |
| $R_{\theta JA}$   | Junction-to-ambient thermal resistance[2]  | 73        | 82        | 67        | 64        | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 38.1    | –         | –         | 32.6      | °C/W |
| $R_{\theta JB}$   | Junction-to-board thermal resistance       | 34.7      | –         | –         | 36.8      | °C/W |
| $\psi_{JT}$       | Junction-to-top characterization parameter | 7.1       | –         | –         | 4.2       | °C/W |
| $\psi_{JB}$       | Junction-to-board characterization parameter | 34.4    | –         | –         | 36.5      | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1]

| | PARAMETER | TEST CONDITIONS | | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $I_{OH}$ = −20 mA | | 2.5 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $I_{OL}$ = 20 mA | | | | 0.5 | V |
| $I_{OZ}$ | Off-state (high-impedance-state) output current | $V_{CC}$ = MIN, | $V_O$ = 0.5 V | | | −20 | μA |
| | | | $V_O$ = 2.5 V | | | 20 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.36 | mA |
| $I_{OS}$ | Short-circuit output current[3] | $V_{CC}$ = MAX | | −30 | | −150 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, all outputs disabled | | | 32 | 80 | mA |

(1) For C-suffix devices, $V_{CC}$ min = 4.75 V and $V_{CC}$ max = 5.25 V. For M-suffix devices, $V_{CC}$ min = 4.5 V and $V_{CC}$ max = 5.5 V.
(2) All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
(3) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

## 6.6 Switching Characteristics – AM26LS31

$T_A$ = 25°C, $V_{CC}$ = 5 V (see Figure 11)
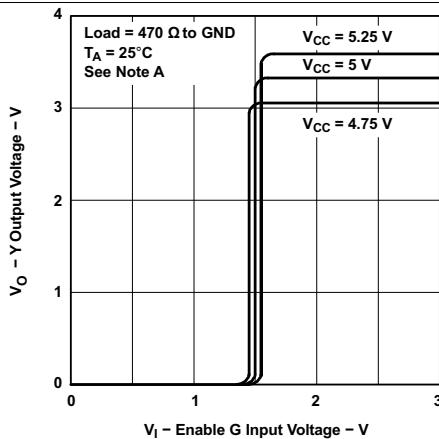
| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 30 pF, S1 and S2 open | | | 14 | 20 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 14 | 20 | |
| $t_{PZH}$ | Output enable time to high level | $C_L$ = 30 pF | $R_L$ = 75 Ω | | 25 | 40 | ns |
| $t_{PZL}$ | Output enable time to low level | | $R_L$ = 180 Ω | | 37 | 45 | |
| $t_{PHZ}$ | Output disable time from high level | $C_L$ = 10 pF, S1 and S2 closed | | | 21 | 30 | ns |
| $t_{PLZ}$ | Output disable time from low level | | | | 23 | 35 | |
| $t_{SKEW}$ | Output-to-output skew | $C_L$ = 30 pF, S1 and S2 open | | | 1 | 6 | ns |

## 6.7 Switching Characteristics – AM26LS31M

$T_A$ = 25°C, $V_{CC}$ = 5 V (see Figure 11)
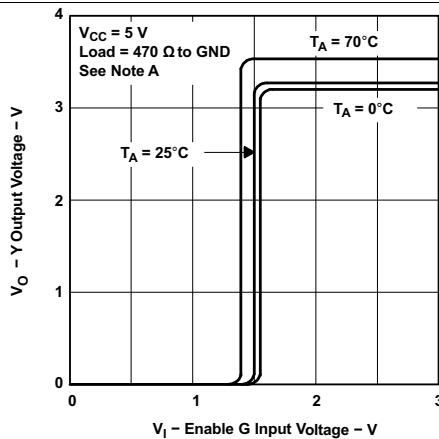
| | PARAMETER | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 30 pF, S1 and S2 open | | | 30 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 30 | |
| $t_{PZH}$ | Output enable time to high level | $C_L$ = 30 pF | $R_L$ = 75 Ω | | 60 | ns |
| $t_{PZL}$ | Output enable time to low level | | $R_L$ = 180 Ω | | 68 | |
| $t_{PHZ}$ | Output disable time from high level | $C_L$ = 10 pF, S1 and S2 closed | | | 45 | ns |
| $t_{PLZ}$ | Output disable time from low level | | | | 53 | |
| $t_{SKEW}$ | Output-to-output skew | $C_L$ = 30 pF, S1 and S2 open | | | 9 | ns |

## 6.8 Typical Characteristics
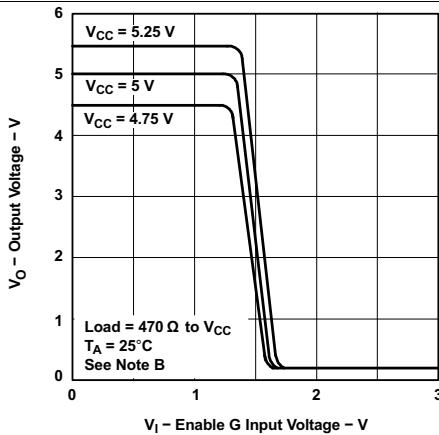


A. The A input is connected to $V_{CC}$ during testing of the Y outputs and to ground during testing of the Z outputs.

**Figure 1. Output Voltage vs Enable G Input Voltage**
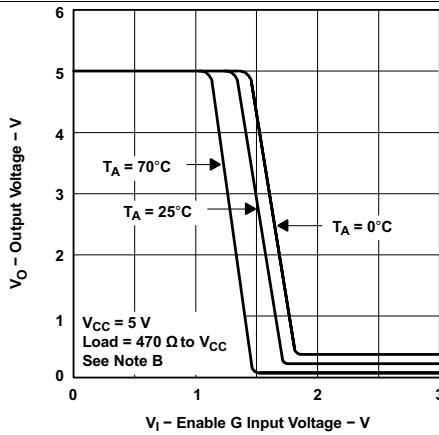


A. The A input is connected to $V_{CC}$ during testing of the Y outputs and to ground during testing of the Z outputs.

**Figure 2. Output Voltage vs Enable G Input Voltage**
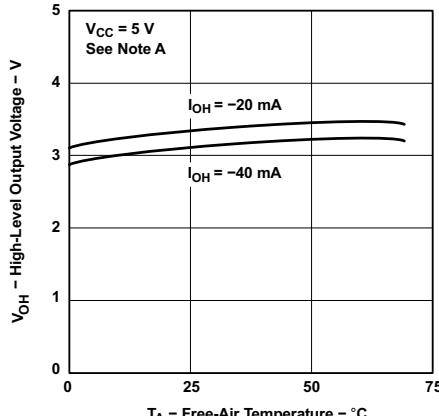


B. The A input is connected to ground during testing of the Y outputs and to $V_{CC}$ during testing of the Z outputs.

**Figure 3. Output Voltage vs Enable G Input Voltage**
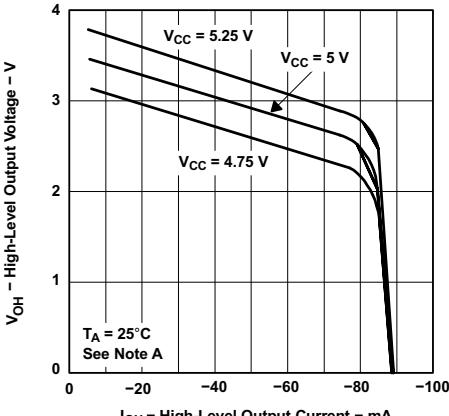


B. The A input is connected to ground during testing of the Y outputs and to $V_{CC}$ during testing of the Z outputs.

**Figure 4. Output Voltage vs Enable G Input Voltage**



A. The A input is connected to $V_{CC}$ during testing of the Y outputs and to ground during testing of the Z outputs.
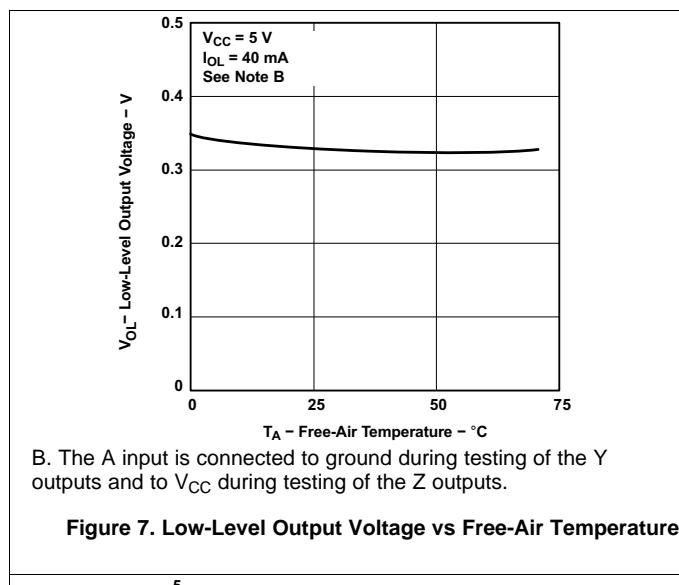
**Figure 5. High-Level Output Voltage vs Free-Air Temperature**
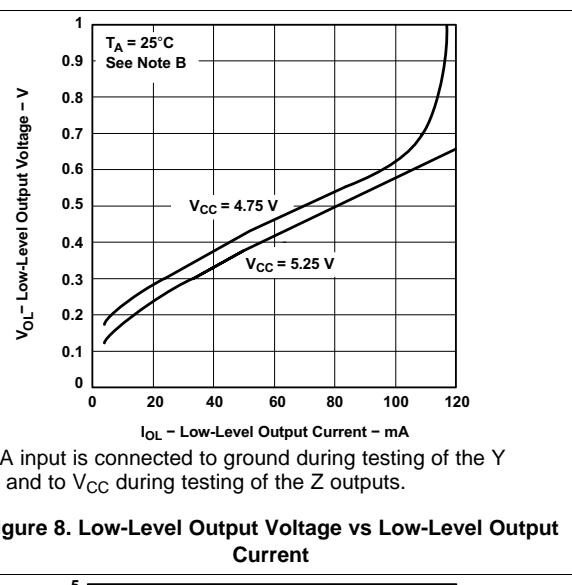


A. The A input is connected to $V_{CC}$ during testing of the Y outputs and to ground during testing of the Z outputs.

**Figure 6. High-Level Output Voltage vs High-Level Output Current**
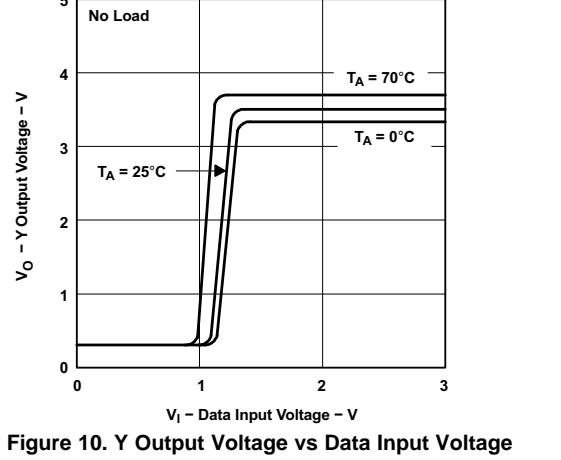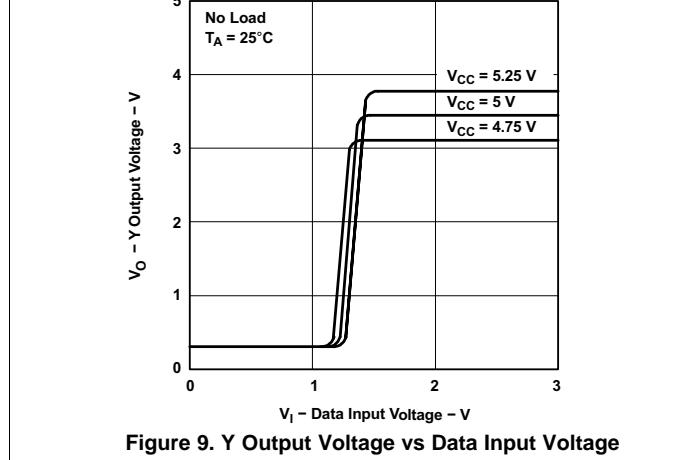
## Typical Characteristics (continued)
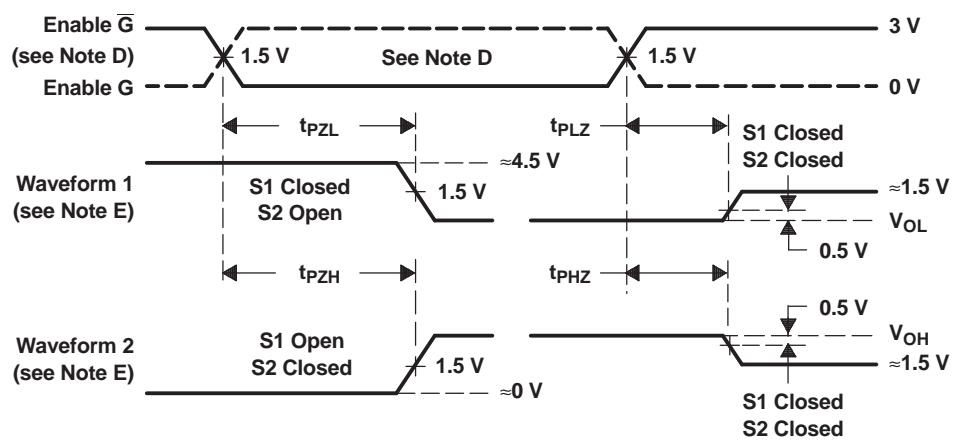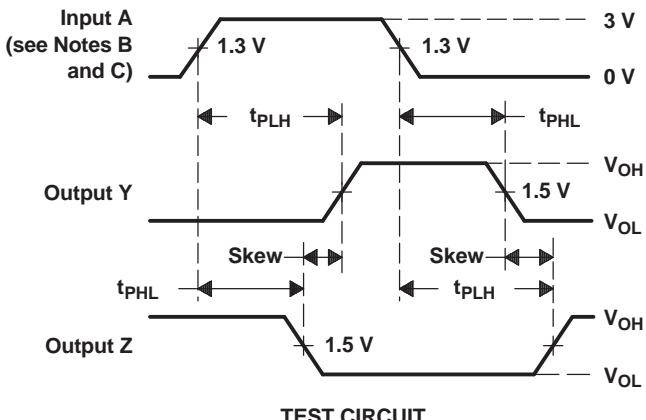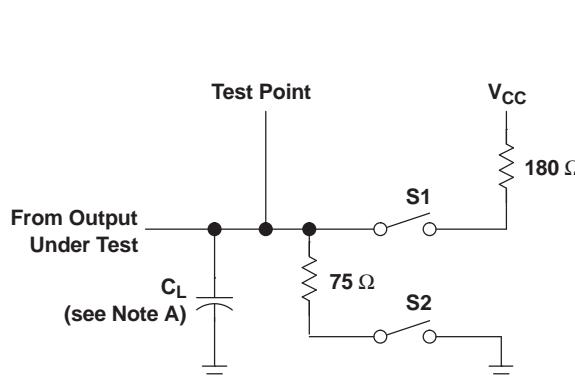


B. The A input is connected to ground during testing of the Y outputs and to $V_{CC}$ during testing of the Z outputs.

**Figure 7. Low-Level Output Voltage vs Free-Air Temperature**



B. The A input is connected to ground during testing of the Y outputs and to $V_{CC}$ during testing of the Z outputs.

**Figure 8. Low-Level Output Voltage vs Low-Level Output Current**



**Figure 9. Y Output Voltage vs Data Input Voltage**



**Figure 10. Y Output Voltage vs Data Input Voltage**

# 7 Parameter Measurement Information



PROPAGATION DELAY TIMES AND SKEW

TEST CIRCUIT

ENABLE AND DISABLE TIME WAVEFORMS

NOTES:  A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ ≈ 50 Ω, $t_r$ ≤ 15 ns, $t_f$ ≤ 6 ns.
C. When measuring propagation delay times and skew, switches S1 and S2 are open.
D. Each enable is tested separately.
E. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

**Figure 11. Test Circuit and Voltage Waveforms**

# 8 Detailed Description
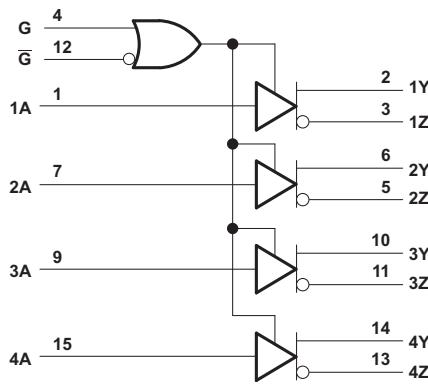
## 8.1 Overview

The AM26LS31x differential bus transmitter is a monolithic integrated circuit designed for unidirectional data communication on transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The AM26LS31x has a four 3-state differential line drivers that operate from a single 5-V power supply. The driver also integrates active-high and active-low enables for precise device control.

The driver is designed to handle loads of a minimum of ±30 mA of sink or source current. The driver features positive- and negative-current limiting for protection from line fault conditions.

## 8.2 Functional Block Diagram



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## 8.3 Feature Description

### 8.3.1 Complementary Output-Enable Inputs

The AM26LS31x can be configured using the G and $\overline{G}$ logic inputs to control transmitter outputs. Setting either G to a logic HIGH or $\overline{G}$ to an logic LOW enables the transmitter outputs. If G is set to logic LOW and $\overline{G}$ is set to logic HIGH, the transmitter outputs are disabled. See Table 1 for a complete truth table.

### 8.3.2 High Output Impedance in Power-Off Conditions

When the AM26LS31x transmitter outputs are disabled using G and $\overline{G}$, the outputs are set to a high impedance state.

### 8.3.3 Complementary Outputs

The AM26LS31x is the driver half of a pair of devices, with the AM26LS32 being the complementary receiver. TI recommends using these devices together for optimal performance, but any RS-422 compliant receive must ensure proper RS-422 communication and logic level translation.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the AM26LS31.

**Table 1. Function Table[1]**
**(Each Driver)**

| INPUT A | ENABLES | | OUTPUTS | |
|---|---|---|---|---|
| | **G** | **$\overline{G}$** | **Y** | **Z** |
| H | H | X | H | L |
| L | H | X | L | H |
| H | X | L | H | L |
| L | X | L | L | H |
| X | L | H | Z | Z |

(1)  H = high level, L = low level,
X = irrelevant,
Z = high impedance (off)

# 9 Application and Implementation
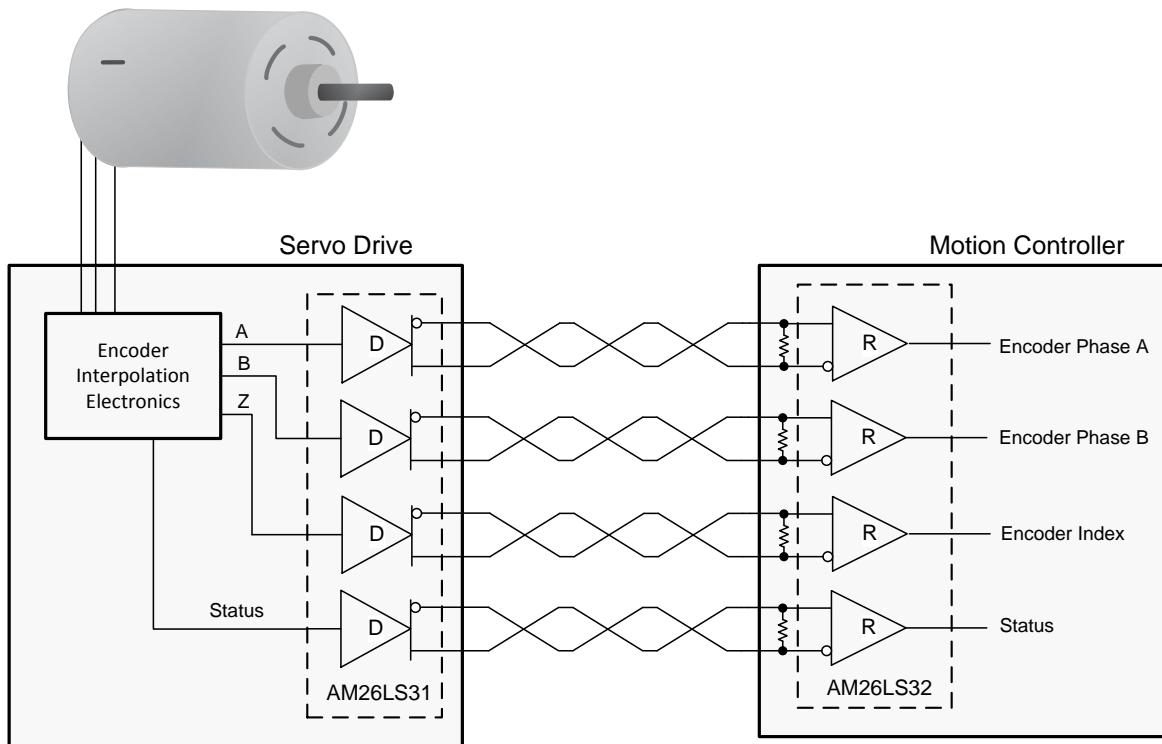
## 9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and, indirectly, RS-485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100-$\Omega$, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LS31 and AM26LS32C, respectively, were tested at room temperature with a 5-V supply voltage. Two plots per termination technique are shown. In each plot, the top waveform is the driver input and the bottom waveform is the receiver output. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable; the second plot shows input waveforms to the receiver at the far end of the cable.

## 9.2 Typical Application



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**Figure 12. Encoder Application**

## Typical Application  (continued)

### 9.2.1  Design Requirements

This example requires the following:
- 5-V power source
- RS-485 bus operating at 10 Mbps or less
- Connector that ensures the correct polarity for port pins
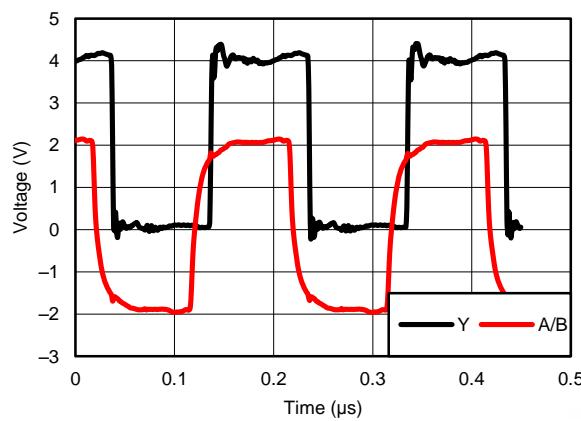
### 9.2.2  Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line.

If desired, add external fail-safe biasing to ensure 200 mV on the A-B port, if the drive is in high impedance state (see *Failsafe in RS-485 data buses*).

### 9.2.3  Application Curve



**Figure 13.  Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable)**

# 10 Power Supply Recommendations

Place a 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.
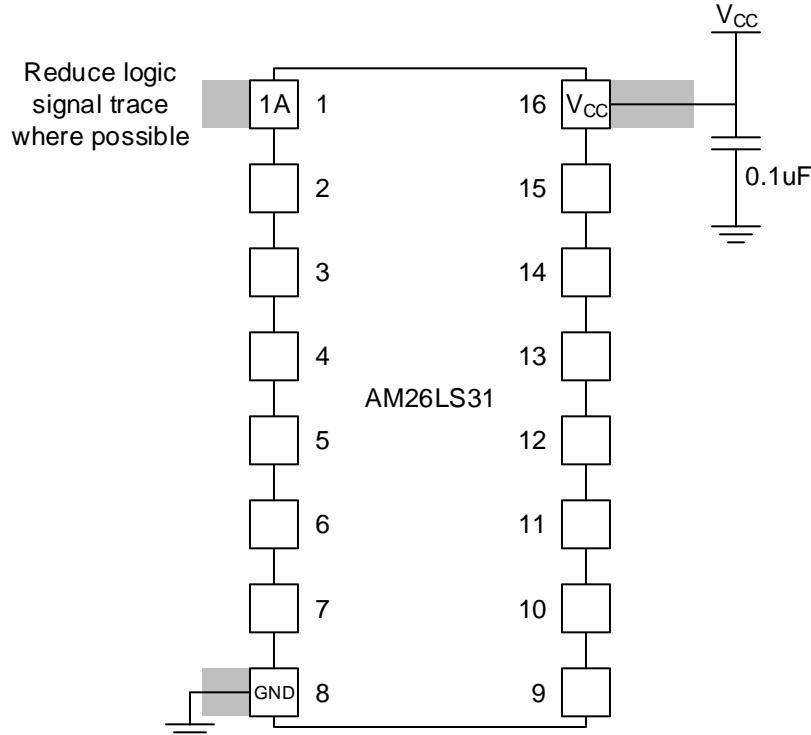
# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can often propagate into analog circuitry through the power supply of the circuit. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

## 11.2 Layout Example



**Figure 14. Layout Recommendation**

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档：

  *《RS-485 数据总线中的失效防护》* (SLYT080)

### 12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

**表 2. 相关链接**

| 器件 | 产品文件夹 | 样片与购买 | 技术文档 | 工具与软件 | 支持和社区 |
|---|---|---|---|---|---|
| AM26LS31 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| AM26LS31C | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| AM26LS31I | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| AM26LS31M | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

### 12.3 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 *《使用条款》*。

**TI E2E™ 在线社区** *TI 的工程师对工程师 (E2E) 社区。*此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持**   *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.7 术语表

SLYZ022 — *TI 术语表*。
  这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-7802301M2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7802301M2A AM26LS31 MFKB | Samples |
| 5962-7802301MEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7802301ME A AM26LS31MJB | Samples |
| 5962-7802301MFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7802301MF A AM26LS31MWB | Samples |
| 5962-7802301Q2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | | 5962-7802301Q2A AM26LS31M | Samples |
| AM26LS31CD | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AM26LS31C | Samples |
| AM26LS31CDBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SA31C | Samples |
| AM26LS31CDE4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AM26LS31C | Samples |
| AM26LS31CDG4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AM26LS31C | Samples |
| AM26LS31CDR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AM26LS31C | Samples |
| AM26LS31CDRE4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AM26LS31C | Samples |
| AM26LS31CDRG4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AM26LS31C | Samples |
| AM26LS31CN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | AM26LS31CN | Samples |
| AM26LS31CNSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 26LS31 | Samples |
| AM26LS31INSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 26LS31 | Samples |
| AM26LS31MFKB | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7802301M2A AM26LS31 MFKB | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AM26LS31MJB | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7802301MEA AM26LS31MJB | Samples |
| AM26LS31MWB | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7802301MFA AM26LS31MWB | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**PACKAGE OPTION ADDENDUM**
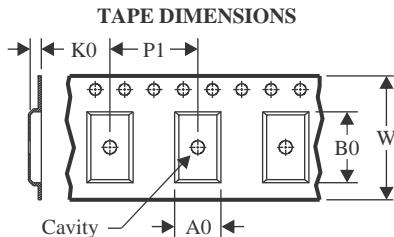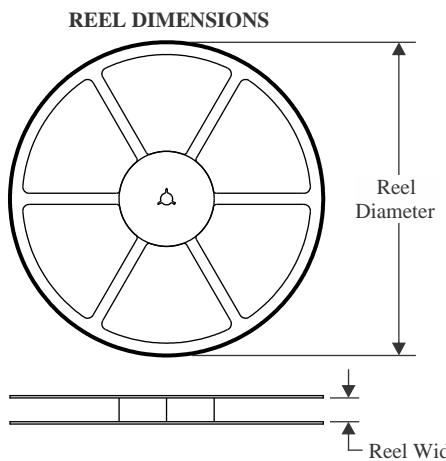
**OTHER QUALIFIED VERSIONS OF AM26LS31, AM26LS31M :**

● Catalog : AM26LS31

● Military : AM26LS31M

NOTE: Qualified Version Definitions:
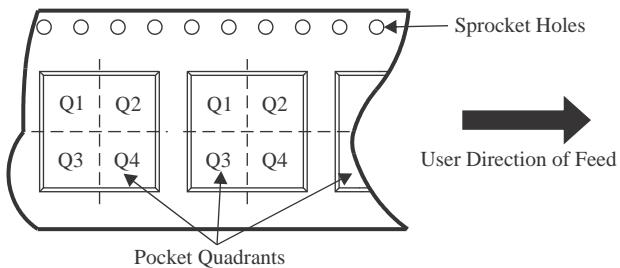
  ● Catalog - TI's standard catalog product

  ● Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**
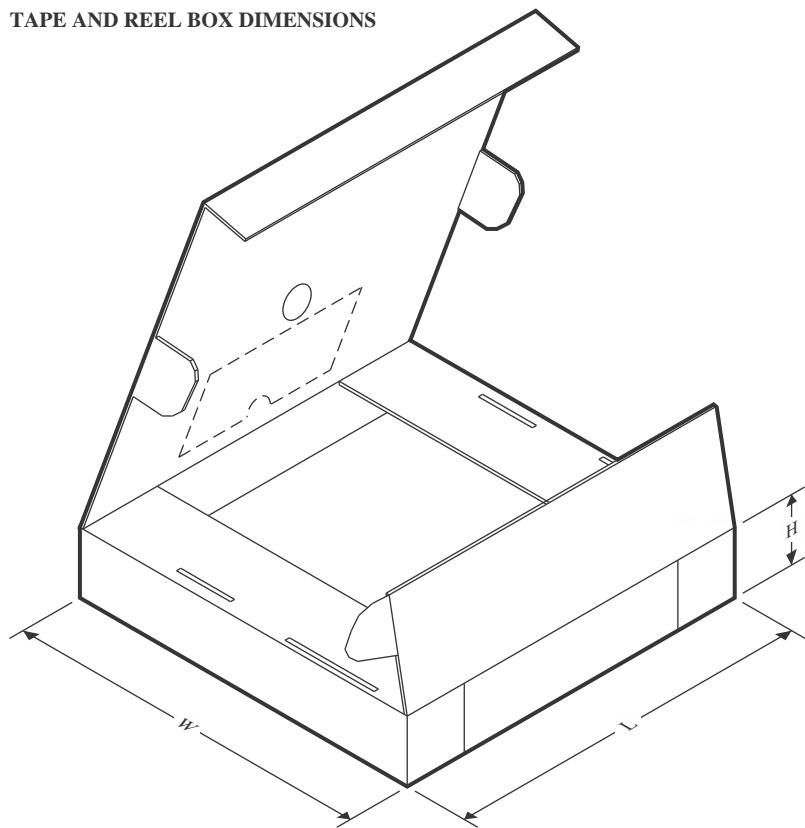
**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
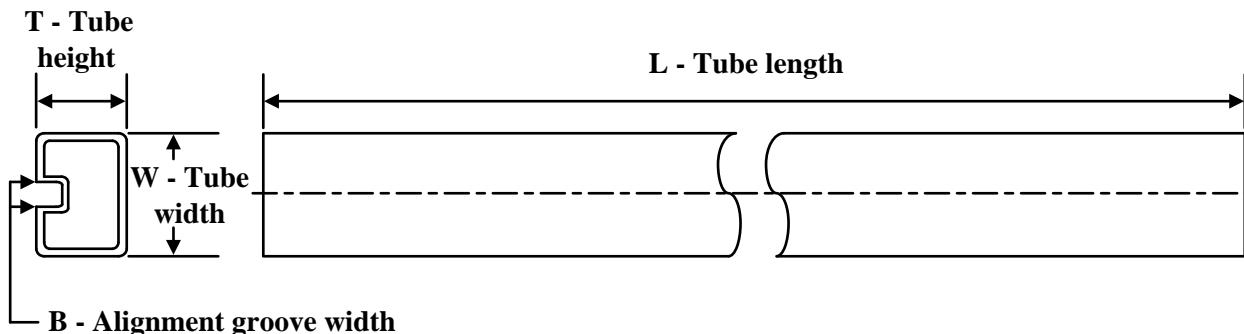


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AM26LS31CDBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| AM26LS31CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LS31CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LS31CDRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LS31CDRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LS31CNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| AM26LS31INSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|------|-------------|------------|-------------|
| AM26LS31CDBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| AM26LS31CDR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| AM26LS31CDR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| AM26LS31CDRG4 | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| AM26LS31CDRG4 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| AM26LS31CNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| AM26LS31INSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE



**T - Tube height**

**W - Tube width**

**L - Tube length**

**B - Alignment groove width**
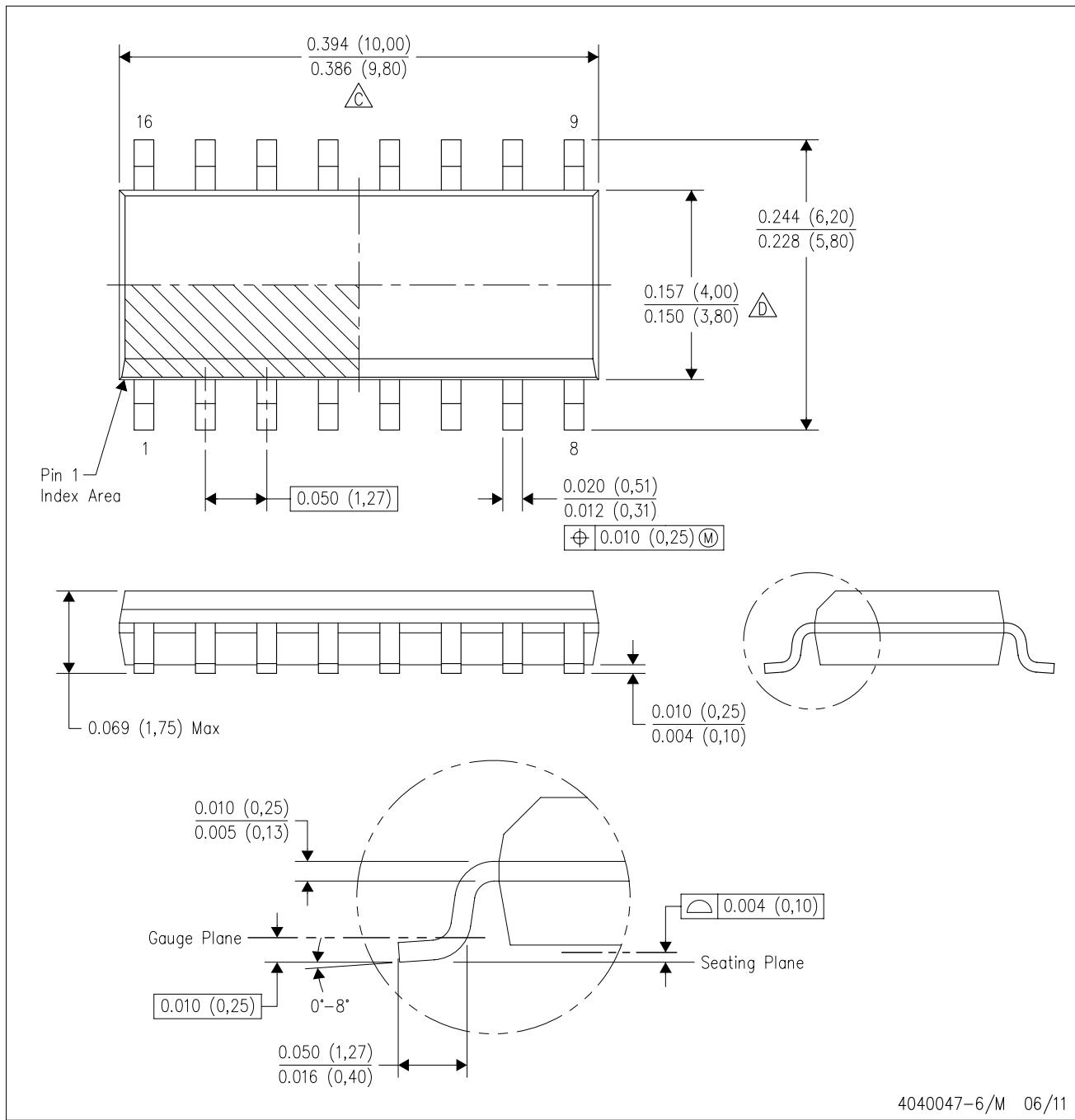
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-7802301M2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 5962-7802301MFA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| 5962-7802301Q2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| AM26LS31CD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| AM26LS31CD | D | SOIC | 16 | 40 | 506.6 | 8 | 3940 | 4.32 |
| AM26LS31CDE4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| AM26LS31CDE4 | D | SOIC | 16 | 40 | 506.6 | 8 | 3940 | 4.32 |
| AM26LS31CDG4 | D | SOIC | 16 | 40 | 506.6 | 8 | 3940 | 4.32 |
| AM26LS31CDG4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| AM26LS31CN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| AM26LS31MFKB | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| AM26LS31MWB | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |

D (R−PDSO−G16)                                    PLASTIC SMALL OUTLINE



0.394 (10,00)
0.386 (9,80)
C

16                                                9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)     D

1                                                8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)          0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES:    A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
          D.   Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AC.

TEXAS
INSTRUMENTS
www.ti.com
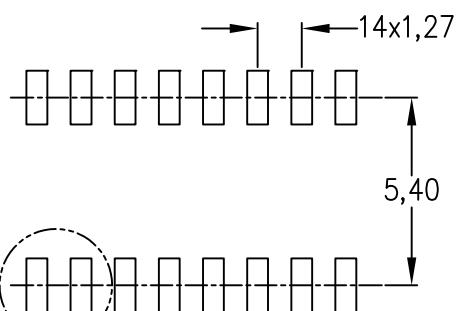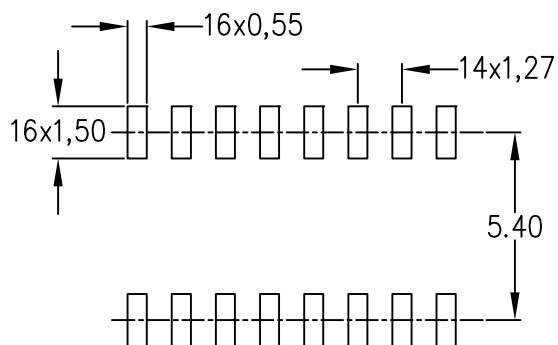
D (R−PDSO−G16)                    PLASTIC SMALL OUTLINE
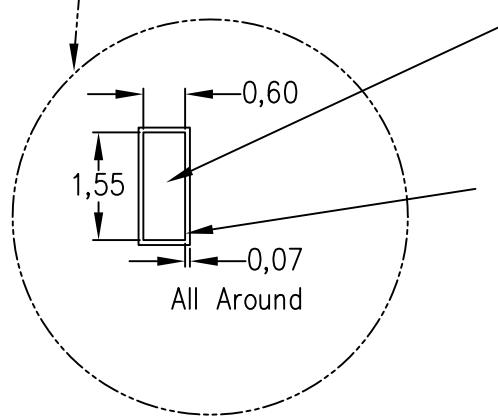
Example Board Layout
(Note C)

Stencil Openings
(Note D)

←14x1,27

16x0,55

←14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←0,60

1,55

Example
Solder Mask Opening
(See Note E)

←0,07

All Around
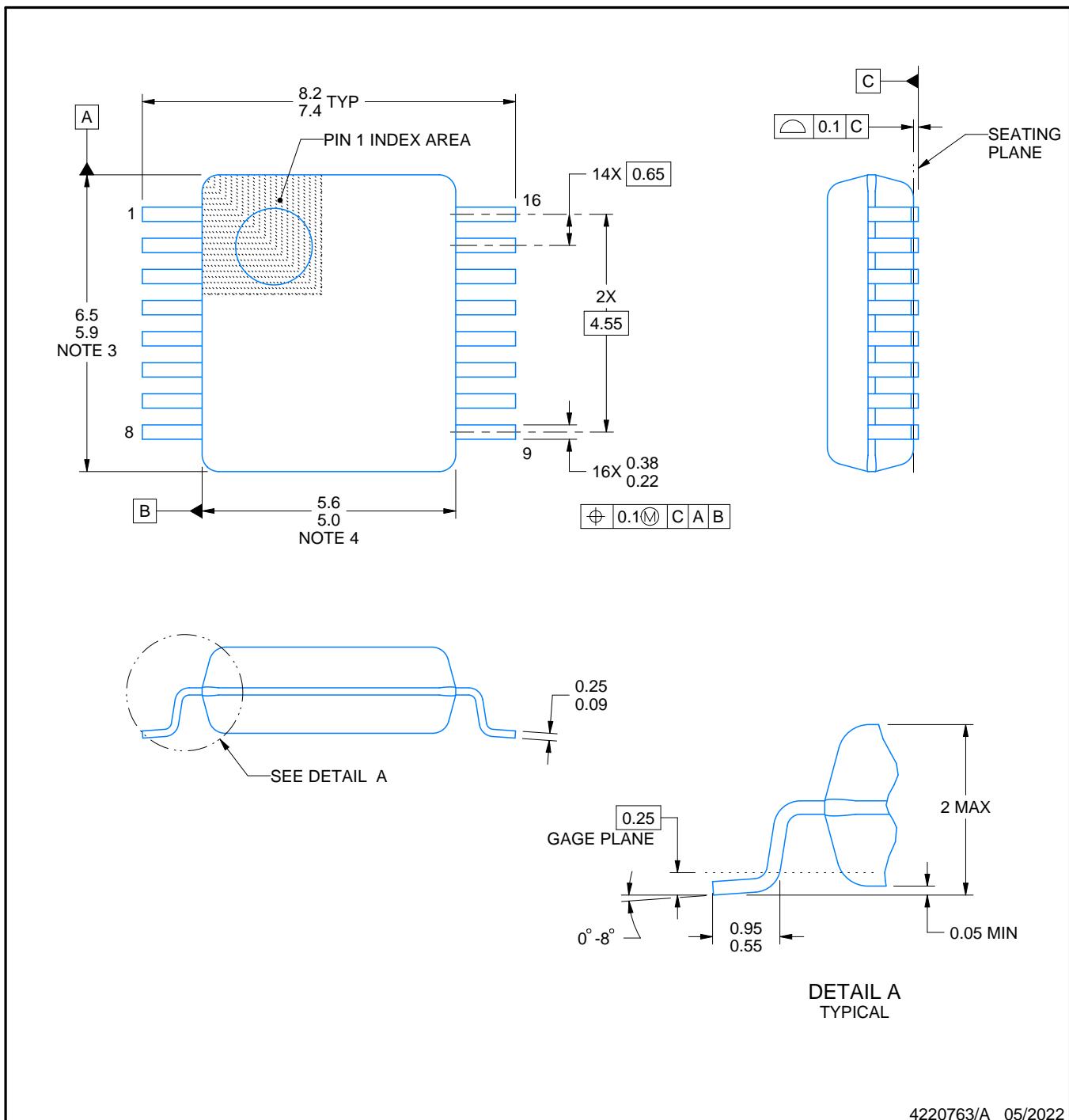
4211283−4/E  08/12

NOTES:    A.  All linear dimensions are in millimeters.
          B.  This drawing is subject to change without notice.
          C.  Publication IPC−7351 is recommended for alternate designs.
          D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

2X 4.55

6.5 / 5.9 NOTE 3

1

8

9

16X 0.38 / 0.22

B

5.6 / 5.0 NOTE 4

⊕ 0.1 Ⓜ C A B

C

⌒ 0.1 C

SEATING PLANE

SEE DETAIL A

0.25 / 0.09

0.25

GAGE PLANE

0° -8°

0.95 / 0.55

2 MAX

0.05 MIN

**DETAIL A**
TYPICAL

4220763/A  05/2022

NOTES:
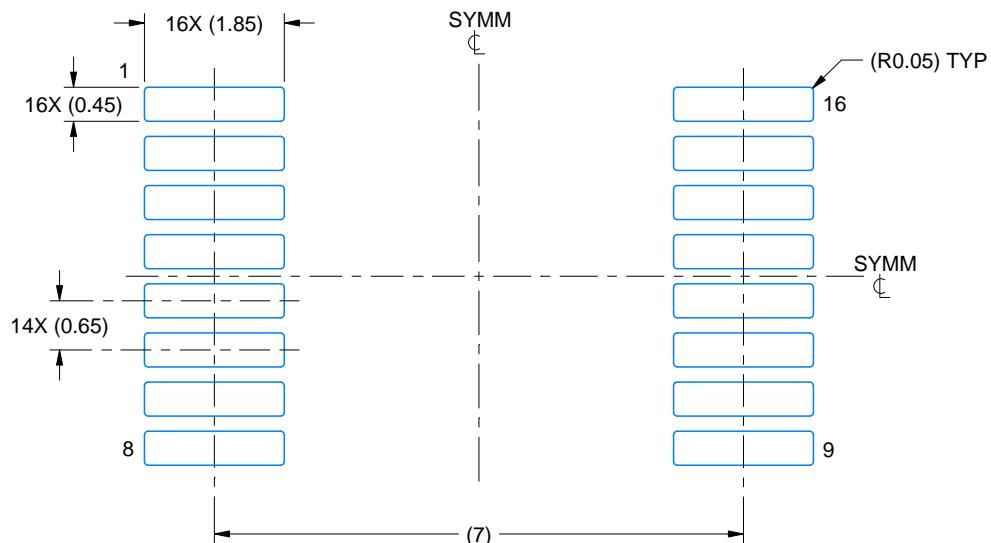
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

16X (1.85)

16X (0.45)

14X (0.65)

1

8

16

9

SYMM

SYMM

(R0.05) TYP

(7)
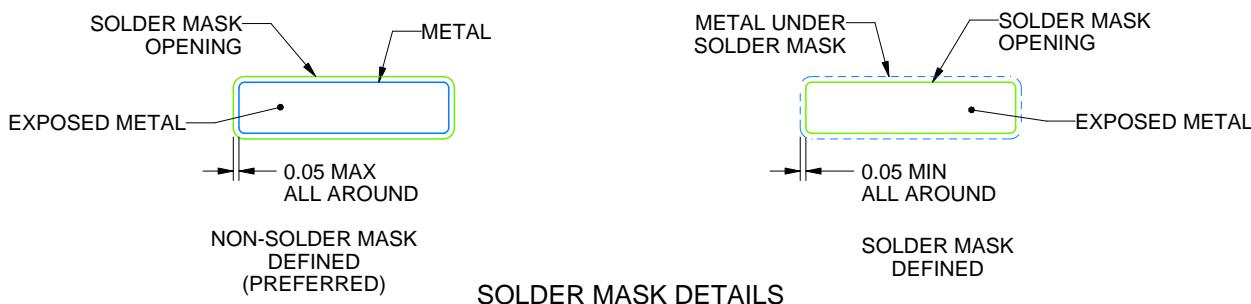
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220763/A   05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A   05/2022

NOTES: (continued)
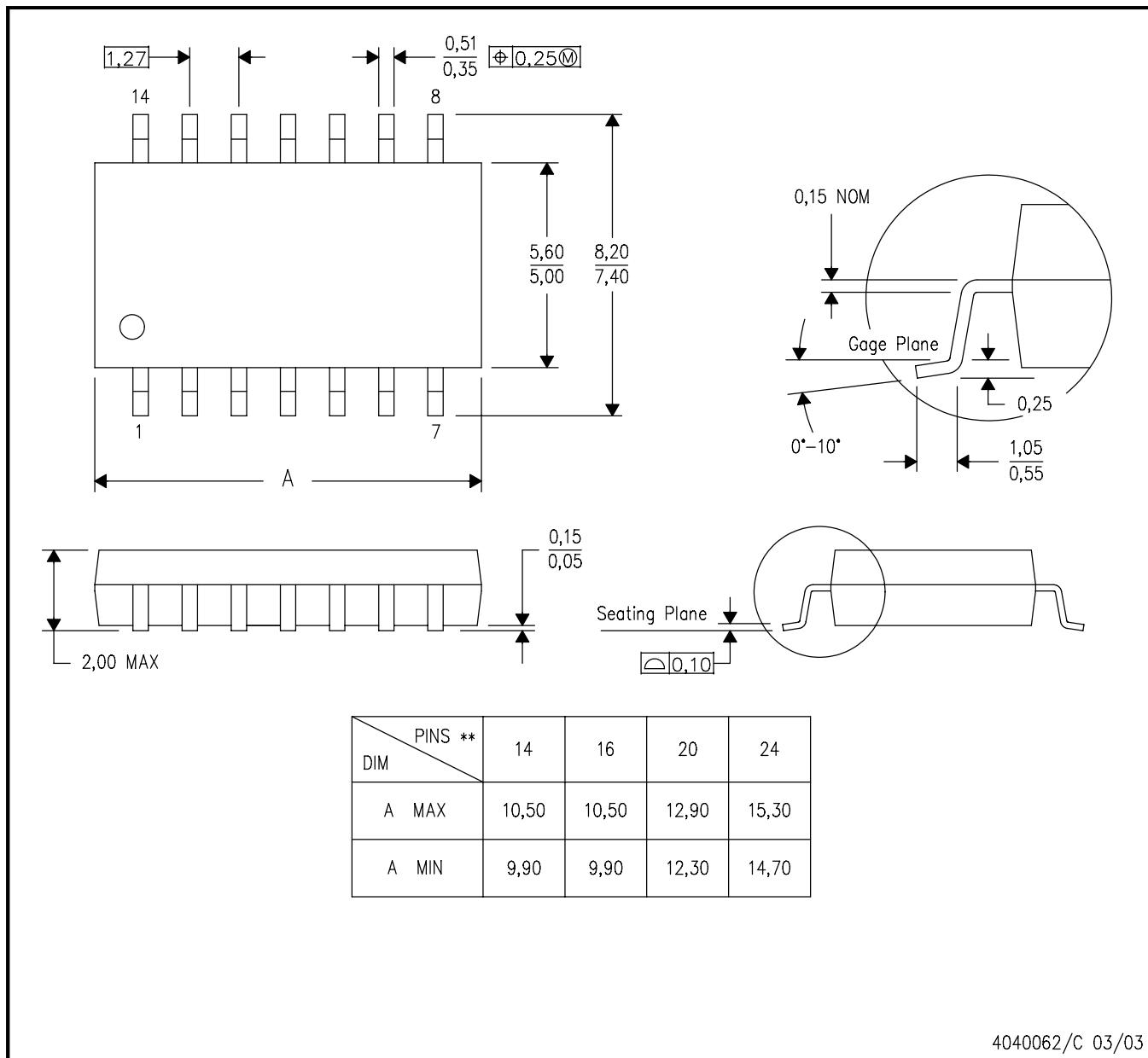
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA
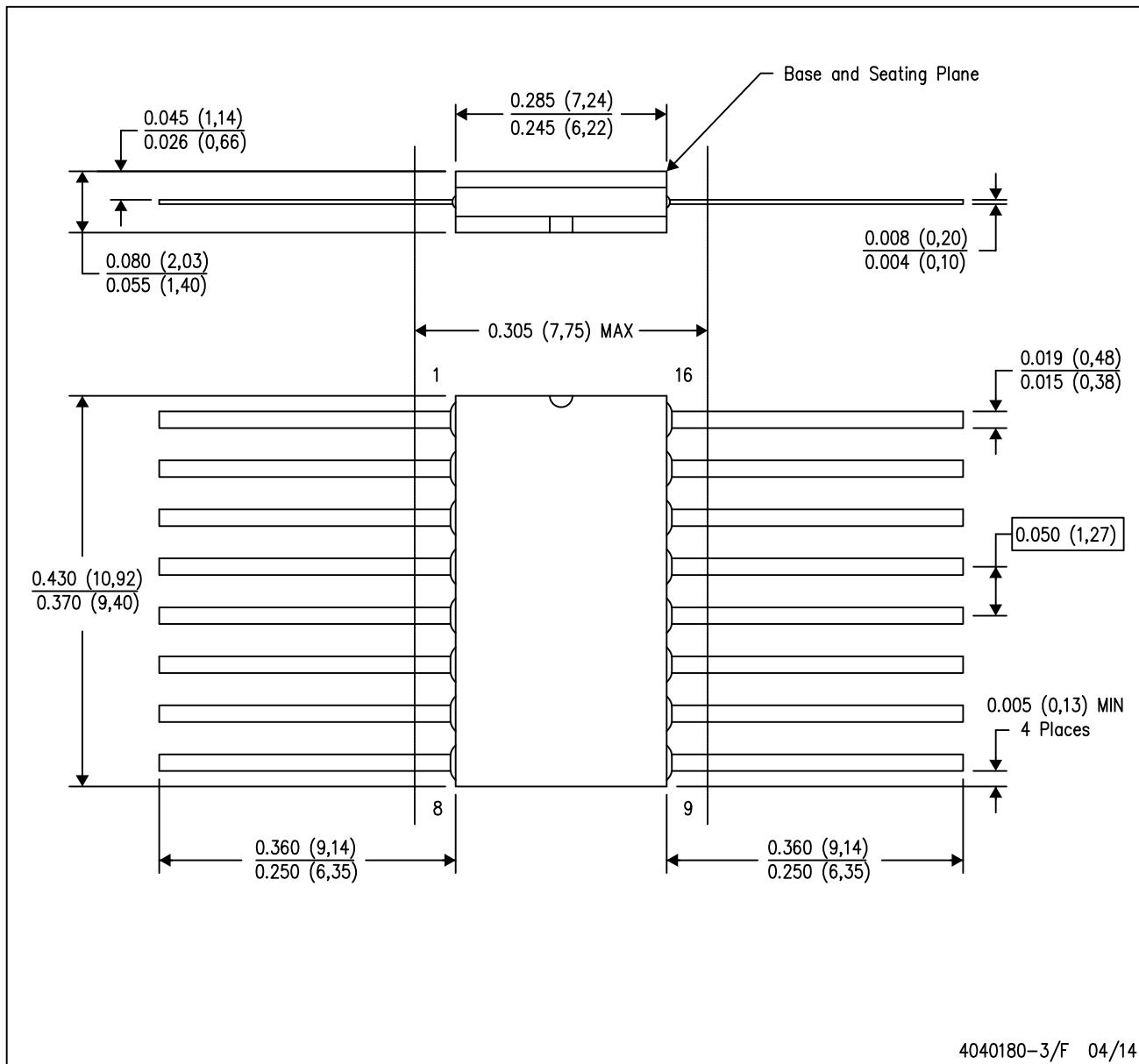
| PINS **<br>DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A   MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A   MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

TEXAS
INSTRUMENTS
www.ti.com

W (R−GDFP−F16)                                      CERAMIC DUAL FLATPACK
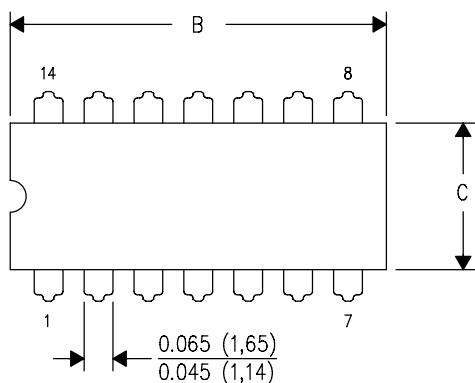
Base and Seating Plane

0.285 (7,24)
0.245 (6,22)

0.045 (1,14)
0.026 (0,66)

0.008 (0,20)
0.004 (0,10)

0.080 (2,03)
0.055 (1,40)

0.305 (7,75) MAX

1                16

0.019 (0,48)
0.015 (0,38)

0.430 (10,92)
0.370 (9,40)

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8                 9

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180−3/F   04/14

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
         C.  This package can be hermetically sealed with a ceramic lid using glass frit.
         D.  Index point is provided on cap for terminal identification only.
         E.  Falls within MIL STD 1835 GDFP2−F16
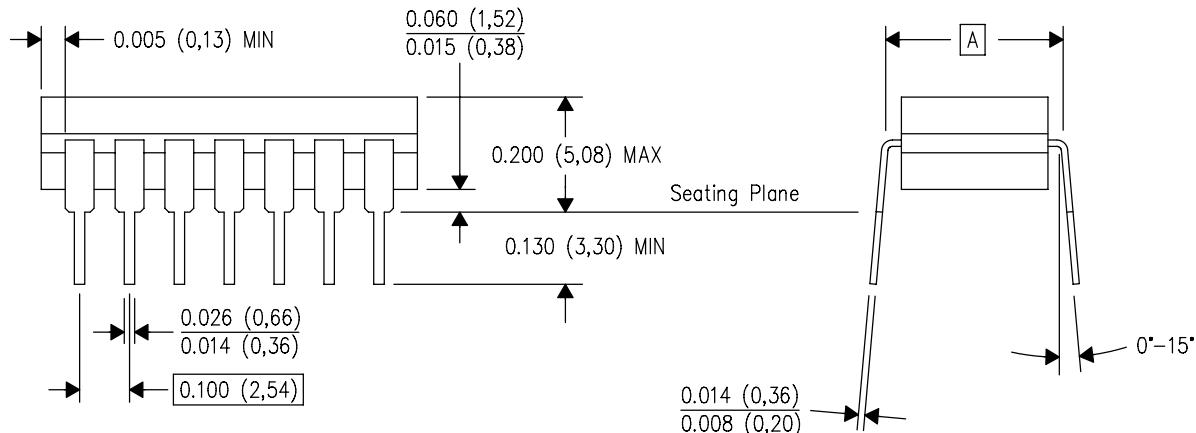
J (R−GDIP−T\*\*)                                    CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN



| DIM ⟍ PINS \*\* | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14                    8

1                    7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)
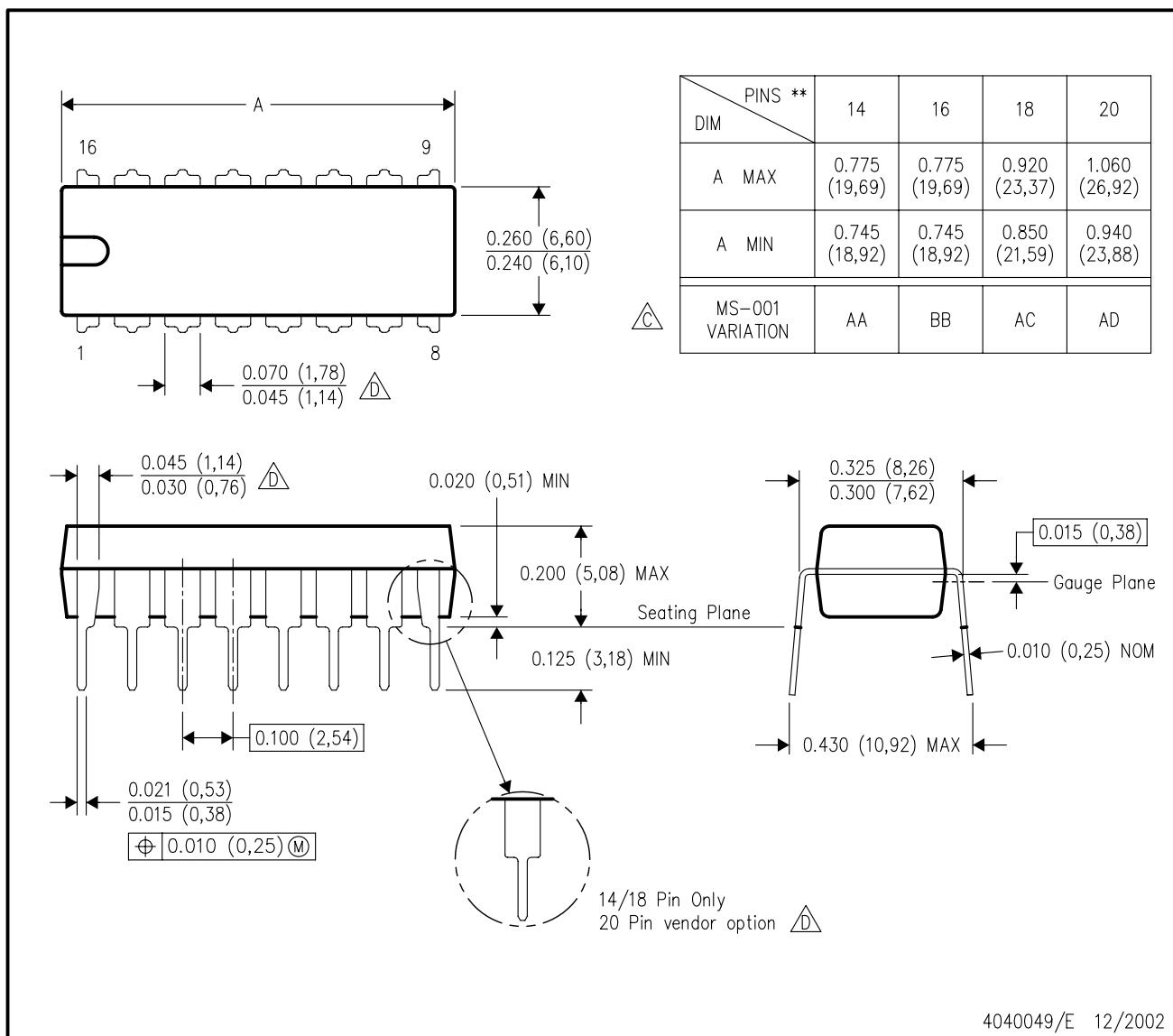
4040083/F 03/03

NOTES:    A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.
          C.  This package is hermetically sealed with a ceramic lid using glass frit.
          D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.  Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

## N (R−PDIP−T**)                    PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A    MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A    MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | AA | BB | AC | AD |

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E  12/2002

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D.  The 20 pin end lead shoulder width is a vendor option, either half or full width.

8.2
7.4 TYP

A

PIN 1 ID
AREA

1

16

14X 1.27

10.4
10.0
NOTE 3

2X
8.89

8

9

B

5.4
5.2
NOTE 4

16X 0.51
0.35

⊕ 0.25Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.00 MAX

SEE DETAIL A

0.15 TYP

GAGE PLANE

0.25

0.3
0.1

0° - 10°

1.05
0.55

(1.25)

DETAIL A
TYPICAL
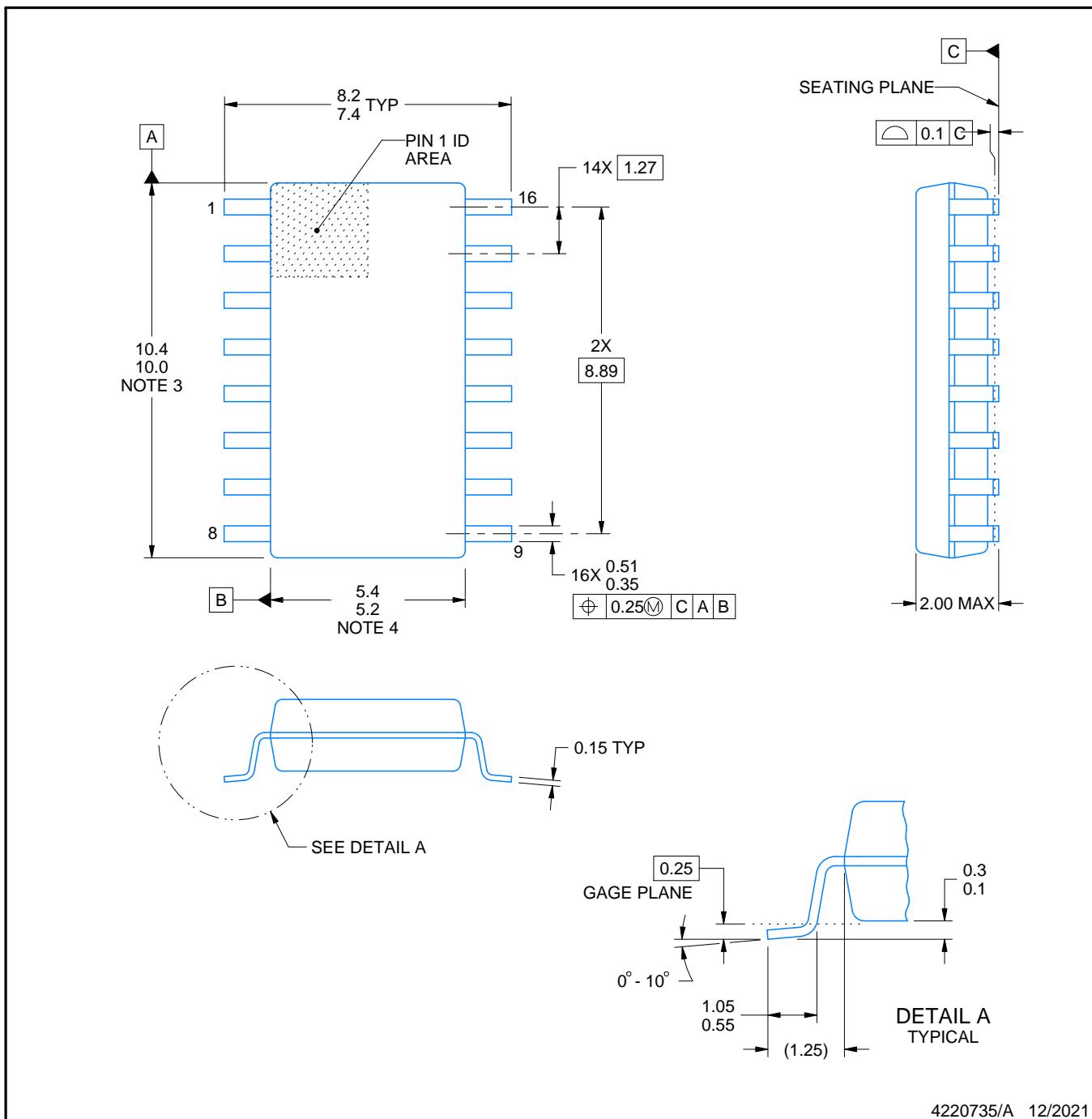
4220735/A   12/2021

NOTES:
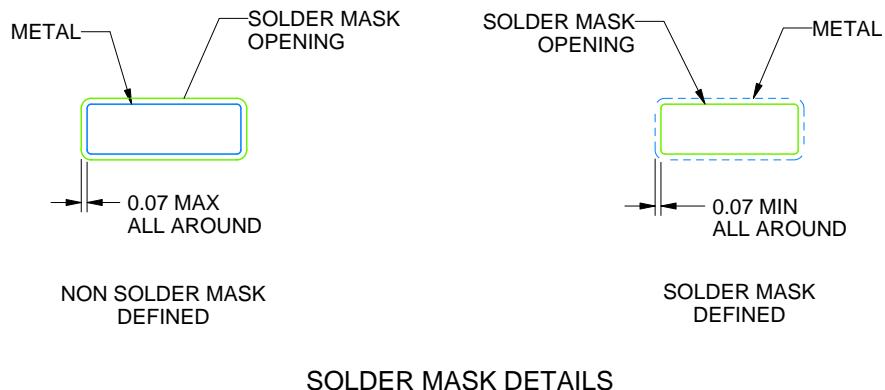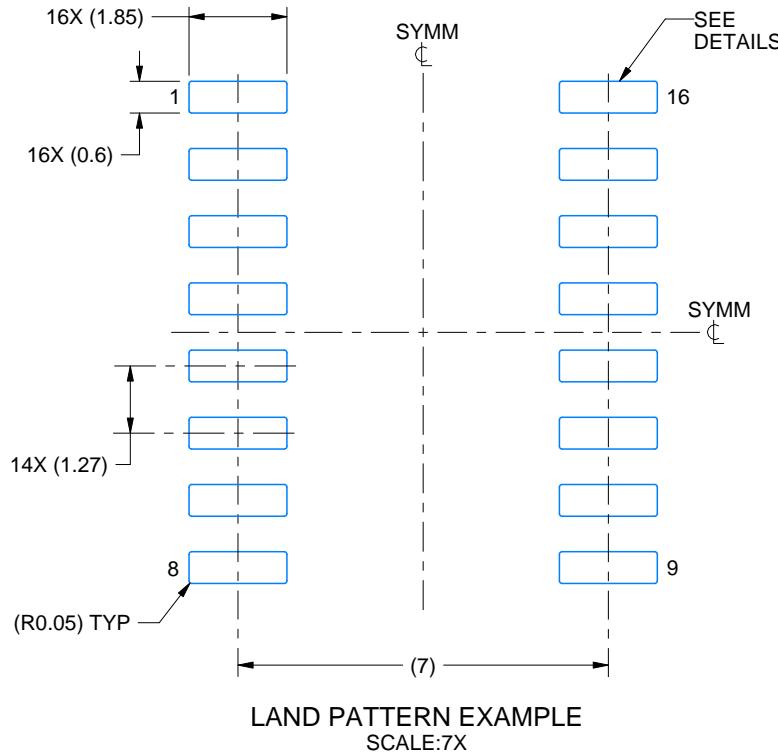
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

16X (1.85)

SYMM

SEE
DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

SYMM

1

16X (0.6)

16

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)
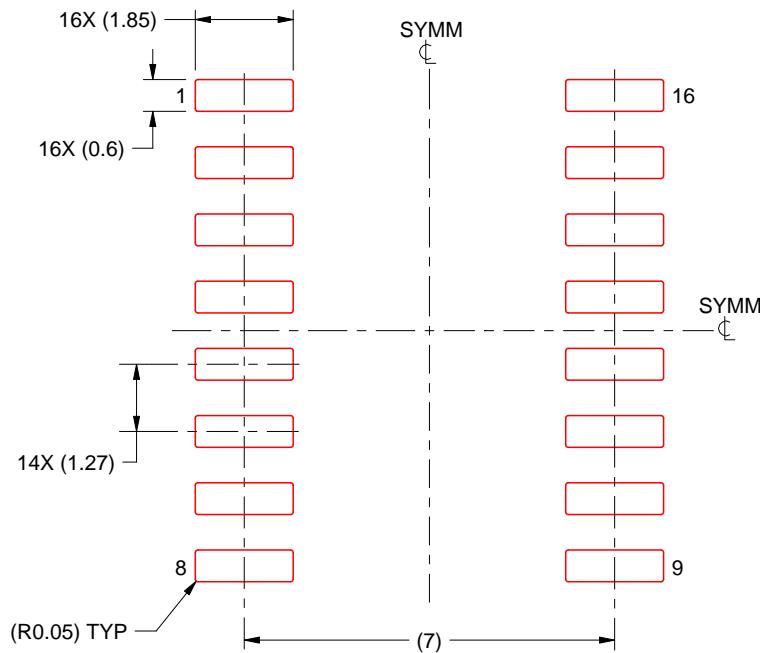
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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