SN74ALVCH162344
1-BIT TO 4-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS

SCES085I−AUGUST 1996−REVISED OCTOBER 2004

FEATURES

- **Member of the Texas Instruments Widebus™ Family**

- **Operates From 1.65 V to 3.6 V**

- **Max t_{pd} of 4.4 ns at 3.3 V**

- **±12-mA Output Drive at 3.3 V**

- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**

- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DESCRIPTION/ORDERING INFORMATION

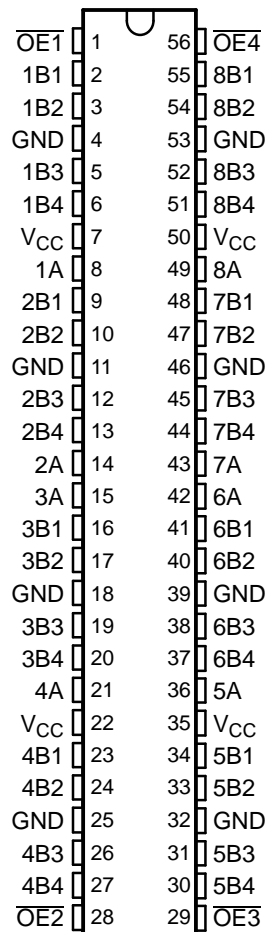This 1-bit to 4-bit address driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162344 is used in applications in which four separate memory locations must be addressed by a single address.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, the output-enable ($\overline{OE}$) inputs should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

$\overline{OE1}$	1	56	$\overline{OE4}$
1B1	2	55	8B1
1B2	3	54	8B2
GND	4	53	GND
1B3	5	52	8B3
1B4	6	51	8B4
V_{CC}	7	50	V_{CC}
1A	8	49	8A
2B1	9	48	7B1
2B2	10	47	7B2
GND	11	46	GND
2B3	12	45	7B3
2B4	13	44	7B4
2A	14	43	7A
3A	15	42	6A
3B1	16	41	6B1
3B2	17	40	6B2
GND	18	39	GND
3B3	19	38	6B3
3B4	20	37	6B4
4A	21	36	5A
V_{CC}	22	35	V_{CC}
4B1	23	34	5B1
4B2	24	33	5B2
GND	25	32	GND
4B3	26	31	5B3
4B4	27	30	5B4
$\overline{OE2}$	28	29	$\overline{OE3}$

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH162344DL	ALVCH162344
		Tape and reel	SN74ALVCH162344DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH162344GR	ALVCH162344
	TVSOP - DGV	Tape and reel	SN74ALVCH162344VR	VH2344

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

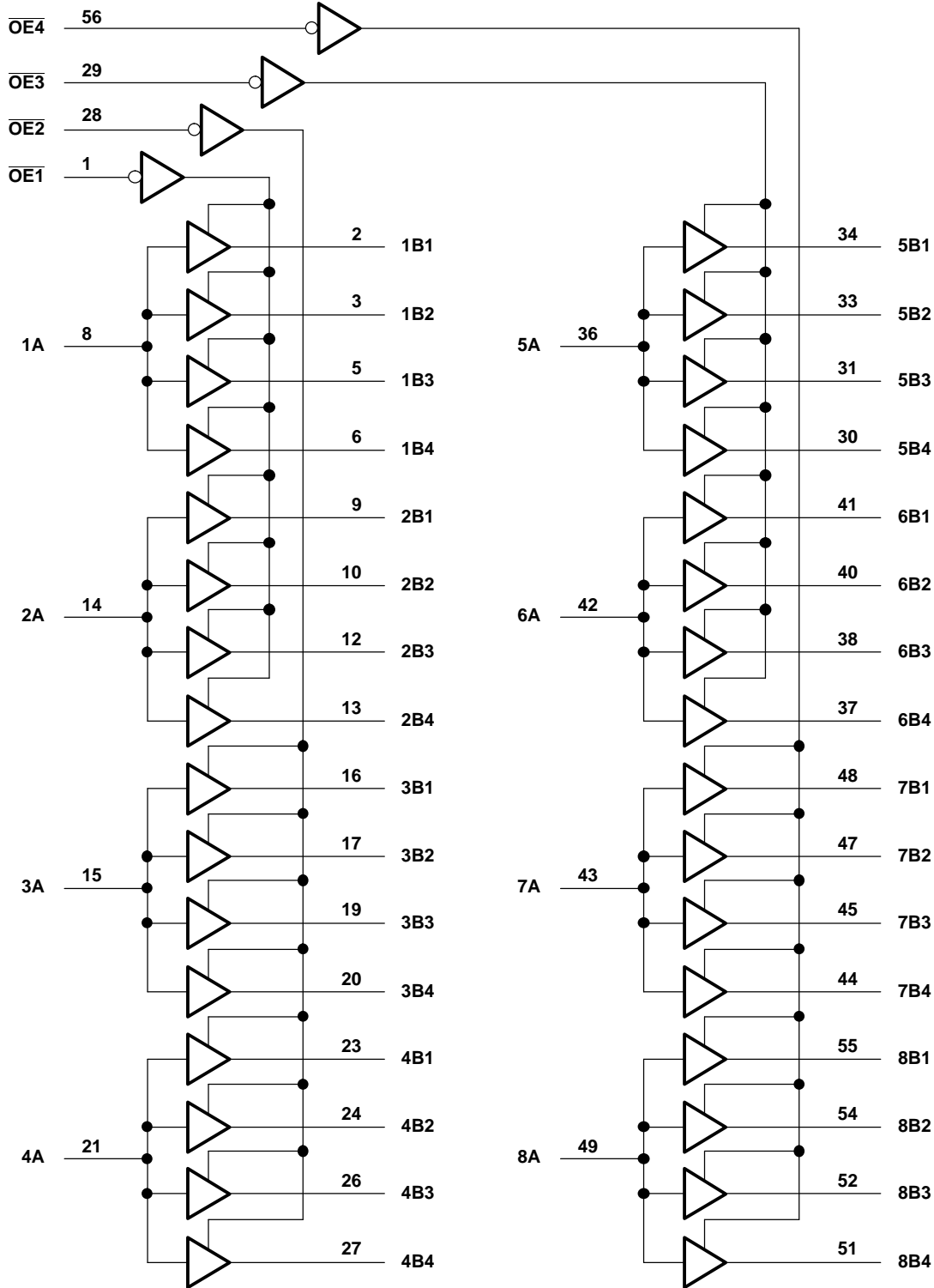Widebus is a trademark of Texas Instruments.

SN74ALVCH162344
1-BIT TO 4-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS

SCES085I−AUGUST 1996−REVISED OCTOBER 2004

**TEXAS
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A-TO-B FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Bn
L	H	H
L	L	L
H	X	Z

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SN74ALVCH162344
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WITH 3-STATE OUTPUTS
SCES085I−AUGUST 1996−REVISED OCTOBER 2004

LOGIC DIAGRAM (POSITIVE LOGIC)

SN74ALVCH162344
1-BIT TO 4-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS

SCES085I−AUGUST 1996−REVISED OCTOBER 2004

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range[2]		-0.5	4.6	V
V_O	Output voltage range[2][3]		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DGG package		64	°C/W
		DGV package		48	
		DL package		56	
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		-2	mA
		V_{CC} = 2.3 V		-6	
		V_{CC} = 2.7 V		-8	
		V_{CC} = 3 V		-12	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		2	mA
		V_{CC} = 2.3 V		6	
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}		I_{OH} = -100 µA	1.65 V to 3.6 V	V_{CC} - 0.2			V
		I_{OH} = -2 mA	1.65 V	1.2			
		I_{OH} = -4 mA	2.3 V	1.9			
		I_{OH} = -6 mA	2.3 V	1.7			
			3 V	2.4			
		I_{OH} = -8 mA	2.7 V	2			
		I_{OH} = -12 mA	3 V	2			
V_{OL}		I_{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I_{OL} = 2 mA	1.65 V			0.45	
		I_{OL} = 4 mA	2.3 V			0.4	
		I_{OL} = 6 mA	2.3 V			0.55	
			3 V			0.55	
		I_{OL} = 8 mA	2.7 V			0.6	
		I_{OL} = 12 mA	3 V			0.8	
I_I		V_I = V_{CC} or GND	3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.58 V	1.65 V	25			µA
		V_I = 1.07 V	1.65 V	-25			
		V_I = 0.7 V	2.3 V	45			
		V_I = 1.7 V	2.3 V	-45			
		V_I = 0.8 V	3 V	75			
		V_I = 2 V	3 V	-75			
		V_I = 0 to 3.6 V[2]	3.6 V			±500	
I_{OZ}		V_O = V_{CC} or GND	3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V		2.5		pF
	Data inputs				3.5		
C_o	Outputs	V_O = V_{CC} or GND	3.3 V		4		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	[1]	1	4.9		5.1	1.4	4.4	ns
t_{en}	$\overline{OE}$	B	[1]	1	6.4		6.6	1.2	5.7	ns
t_{dis}	$\overline{OE}$	B	[1]	1	5.4		4.7	1.2	4.5	ns
$t_{sk(o)}$[2]									0.35	ns
$t_{sk(o)}$[3]									0.5	ns

(1) This information was not available at the time of publication.
(2) Skew between outputs of the same bank and same package (same transition)
(3) Skew between outputs of all banks of same package (A1−A8 tied together)

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OPERATING CHARACTERISTICS

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 0 pF, f = 10 MHz	(1)	68	82	pF
	Outputs disabled		(1)	12	14	

(1) This information was not available at the time of publication.

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V $\pm$ 0.15 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	2 $\times$ V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	2 $\times$ V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
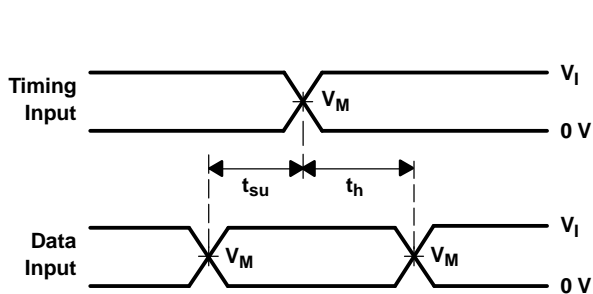
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATION
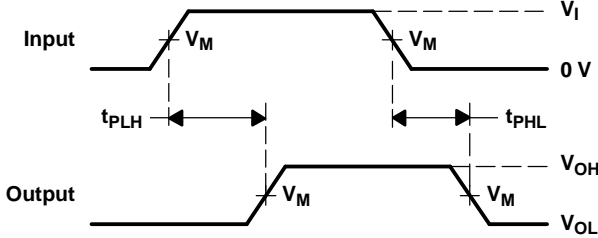
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
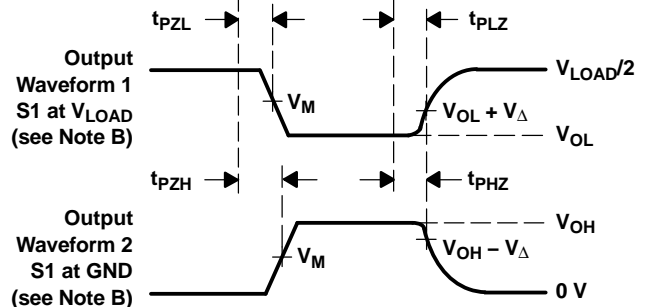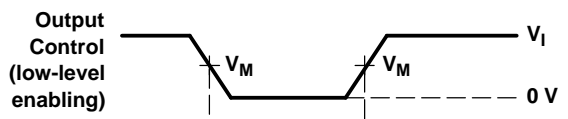
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVCH162344DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162344	Samples
SN74ALVCH162344GR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162344	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH162344GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH162344GR	TSSOP	DGG	56	2000	367.0	367.0	45.0

PACKAGE MATERIALS INFORMATION

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALVCH162344DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

56   29

0.420 (10,67)
0.395 (10,03)

0.299 (7,59)
0.291 (7,39)

1   28

0.730 (18,54)
0.720 (18,29)

0.010 (0,25)
0.005 (0,13)

Gage Plane

0°−8°

0.010 (0,25)

0.040 (1,02)
0.020 (0,51)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−4/F 05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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8.3 TYP
7.9

PIN 1 ID
AREA

A

1

54X [0.5]

56

14.1
13.9
NOTE 3

2X
[13.5]

28

B

6.2
6.0

29

56X [0.27]
[0.17]

⊕ | 0.08 Ⓜ | C | A Ⓢ | B Ⓢ

C

SEATING PLANE

⌓ | 0.1 | C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL
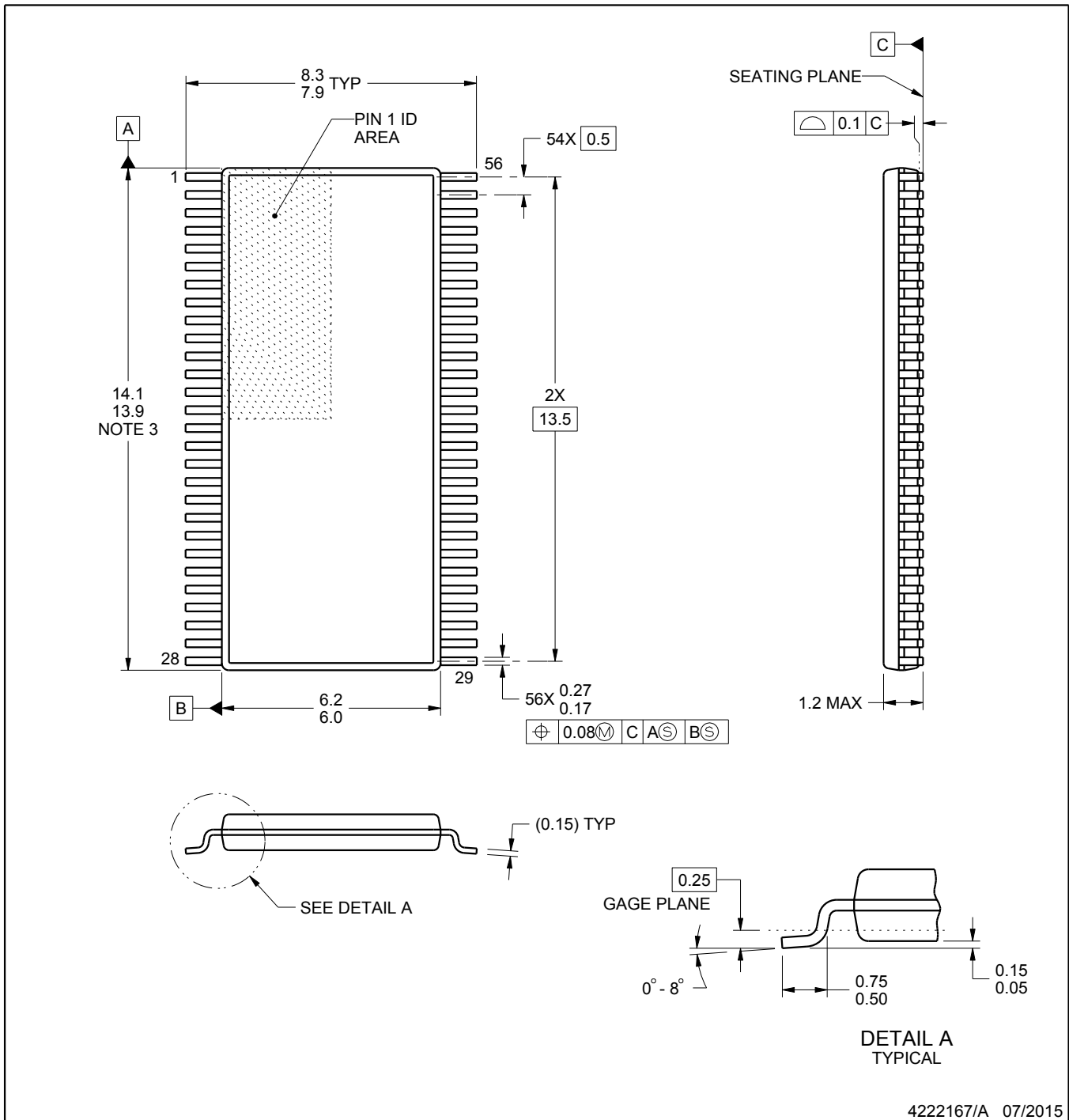
4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

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56X (1.5)

1

56X (0.3)

54X (0.5)

(R0.05)
TYP

SYMM

56

SYMM

28

29

(7.5)
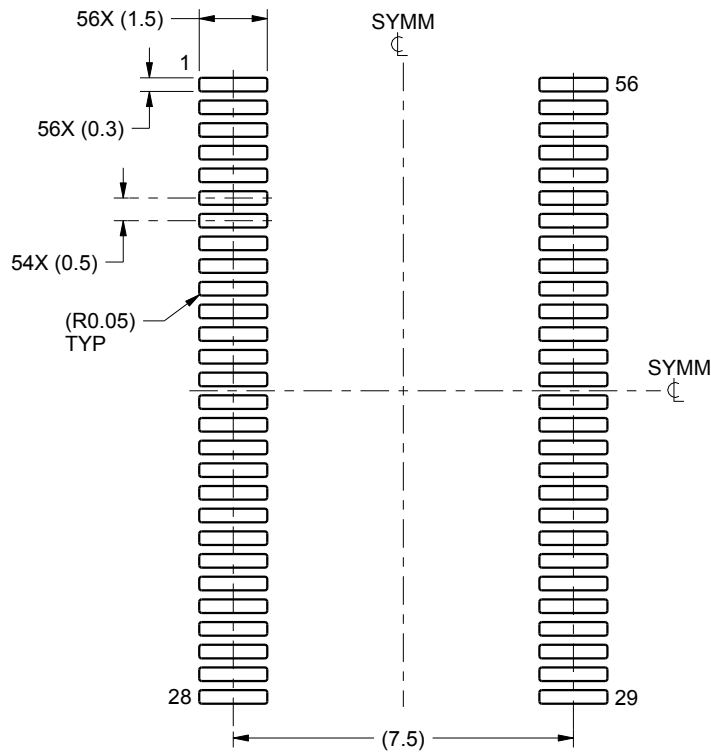
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222167/A   07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DGG0056A

56X (1.5)
1
56X (0.3)
54X (0.5)
(R0.05) TYP
SYMM
56
SYMM
28
29
(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A   07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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