Low-Power, Wideband, Voltage-Feedback OPERATIONAL AMPLIFIER with Disable

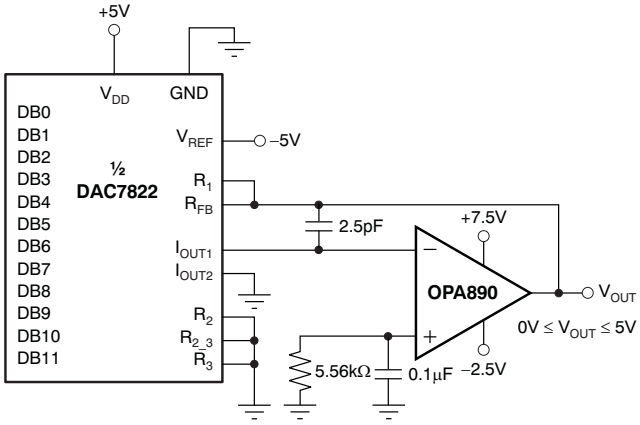
Check for Samples: OPA890

FEATURES

- **FLEXIBLE SUPPLY RANGE:**
  +3V to +12V Single Supply
  ±1.5V to ±6V Dual Supplies
- **UNITY-GAIN STABLE**
- **WIDEBAND +5V OPERATION: 115MHz (G = +2V/V)**
- **OUTPUT VOLTAGE SWING: ±4V**
- **HIGH SLEW RATE: 500V/µs**
- **LOW QUIESCENT CURRENT: 1.1mA**
- **LOW DISABLE CURRENT: 30µA**

APPLICATIONS

- **VIDEO LINE DRIVING**
- **xDSL LINE DRIVERS/RECEIVERS**
- **HIGH-SPEED IMAGING CHANNELS**
- **ADC BUFFERS**
- **PORTABLE INSTRUMENTS**
- **TRANSIMPEDANCE AMPLIFIERS**
- **ACTIVE FILTERS**



Multiplying DAC Transimpedance Amplifier

DESCRIPTION

The OPA890 represents a major step forward in unity-gain stable, voltage-feedback op amps. A new internal architecture provides slew rate and full-power bandwidth previously found only in wideband, current-feedback op amps. These capabilities provide exceptional full power bandwidth. Using a single +5V supply, the OPA890 can deliver a 1V to 4V output swing with over 35mA drive current and 220MHz bandwidth. This combination of features makes the OPA890 an ideal RGB line driver or single-supply analog-to-digital converter (ADC) input driver.

The low 1.1mA supply current of the OPA890 is precisely trimmed at +25°C. This trim, along with low temperature drift, ensures lower maximum supply current than competing products. System power may be reduced further using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, operates the OPA890 normally. If pulled LOW, the OPA890 supply current drops to less than 30µA while the output goes into a high-impedance state.

RELATED OPERATIONAL AMPLIFIER PRODUCTS

DESCRIPTION	SINGLES	DUALS	TRIPLES
Low-Power Voltage-Feedback with Disable	—	OPA2890	—
Voltage-Feedback Amplifier with Disable (1800V/µs)	OPA690	OPA2690	OPA3690
Current-Feedback Amplifier with Disable (2100V/µs)	OPA691	OPA2691	OPA3691
Fixed Gain	OPA692	—	OPA3692

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA890	SO-8	D	–40°C to +85°C	OPA890	OPA890ID	Rail, 75
					OPA890IDR	Tape and Reel, 2500
OPA890	SOT23-6	DBV	–40°C to +85°C	BRI	OPA890IDBVT	Tape and Reel, 250
					OPA890IDBVR	Tape and Reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

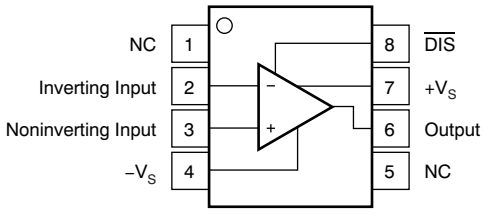
Over operating free-air temperature range (unless otherwise noted).

		OPA890	UNIT
Power Supply		±6.5	V
Internal Power Dissipation		See Thermal Characteristics	
Input Voltage Range		$\pm V_S$	V
Storage Temperature Range		–65 to +125	°C
Maximum Junction Temperature (T_J)		+150	°C
Maximum Junction Temperature, Continuous Operation, Long-Term Reliability		+140	°C
ESD Rating:	Human Body Model (HBM)	2000	V
	Charge Device Model (CDM)	1500	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

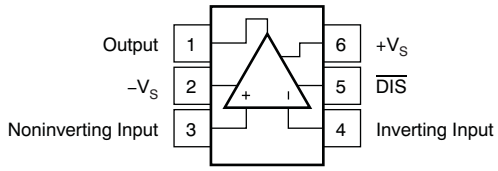
PIN CONFIGURATIONS

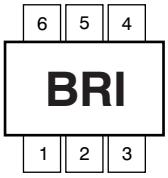
TOP VIEW SO



NC = No Connection

TOP VIEW SOT23





Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at +25°C.
At R_F = 750Ω, G = +2V/V, and R_L = 100Ω, unless otherwise noted.

		OPA890ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1V/V, V_O = 100mV$_{PP}$, R_F = 0Ω	260				MHz	typ	C
	G = +2V/V, V_O = 100mV$_{PP}$	115	75	65	60	MHz	min	B
	G = +10V/V, V_O = 100mV$_{PP}$	13	9	8	7.5	MHz	min	B
Gain Bandwidth Product	G > +20V/V	130	100	90	85	MHz	min	B
Bandwidth for 0.1dB Flatness	G = +2V/V, V_O = 100mV$_{PP}$	20				MHz	typ	C
Peaking at a Gain of +1V/V	V_O < 100mV$_{PP}$	1				dB	typ	C
Large-Signal Bandwidth	G = +2V/V, V_O = 2V$_{PP}$	170				MHz	typ	C
Slew Rate	G = +2V/V, V_O = 2V Step	500	325	300	275	V/µs	min	B
Rise-and-Fall Time	0.2V Step	3.5				ns	typ	C
Settling Time to 0.02%	G = +1V/V, V_O = 2V Step	16				ns	typ	C
Settling Time to 0.1%		10				ns	typ	C
Harmonic Distortion	G = +2V/V, f = 1MHz, V_O = 2V$_{PP}$							
2nd-Harmonic	R_L = 200Ω	–88	–78	–76	–75	dBc	max	B
	R_L ≥ 500Ω	–102	–84	–82	–80	dBc	max	B
3rd-Harmonic	R_L = 200Ω	–89	–84	–81	–80	dBc	max	B
	R_L ≥ 500Ω	–94	–90	–87	–86	dBc	max	B
Input Voltage Noise	f > 100kHz	8	9	10	11	nV/√Hz	max	B
Input Current Noise	f > 100kHz	1	1.3	1.7	1.9	pA/√Hz	max	B
Differential Gain	G = +2V/V, V_O = 1.4V$_{PP}$, R_L = 150Ω	0.05				%	typ	C
Differential Phase	G = +2V/V, V_O = 1.4V$_{PP}$, R_L = 150Ω	0.03				°	typ	C
DC PERFORMANCE[4]								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V, R_L = 100Ω	62	**57**	56	54	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±1	**±5**	±5.7	±6	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±15	±15	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	±0.1	**±1.6**	±1.8	±2	µA	max	A
Average Input Bias Current Drift	V_{CM} = 0V			±5	±6	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±70	**±350**	±450	±500	nA	max	A
Average Input Offset Current Drift	V_{CM} = 0V			±2.5	±2.5	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)[5]		±3.9	**±3.7**	±3.6	±3.5	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V, Input-Referred	67	**61**	58	57	dB	min	A
Input Impedance								
Differential	V_{CM} = 0V	190 || 0.6				kΩ || pF	typ	C
Common-Mode	V_{CM} = 0V	3.2 || 0.9				MΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	No Load	±4.0	**±3.9**	±3.8	±3.7	V	min	A
	R_L = 100Ω	±3.5	**±3.1**	±3.05	±2.9	V	min	A
Output Current, Sourcing, Sinking	V_O = 0V	±40	**±35**	±33	±30	mA	min	A
Peak Output Current	Output Shorted to Ground	±75				mA	typ	C
Closed-Loop Output Impedance	G = +2V/V, f = 100kHz	0.04				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +2°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at +25°C.

At R_F = 750Ω, G = +2V/V, and R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA890ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]			
DISABLE	Disable LOW							
Power-Down Supply Current (+V_S)	V_{DIS} = 0	30	**55**	60	75	µA	max	A
Disable Time	V_{IN} = 1V_{DC}	7				µs	typ	C
Enable Time	V_{IN} = 1V_{DC}	200				ns	typ	C
Off Isolation	G = +2V/V, f = 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Enable Voltage		3.0	**3.2**	3.4	3.8	V	min	A
Disable Voltage		1.4	**1.1**	1.0	0.8	V	max	A
Control Pin Input Bias Current (V_{DIS})	V_{DIS} = 0V, Each Channel	15	**30**	35	40	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Minimum Operating Voltage		±1.5				V	typ	C
Maximum Operating Voltage			**±6.0**	±6.0	±6.0	V	max	A
Maximum Quiescent Current	V_S = ±5V	1.1	**1.2**	1.22	1.25	mA	max	A
Minimum Quiescent Current	V_S = ±5V	1.1	**1.05**	1.02	1	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	+V_S = 4.5V to 5.5V	74	**66**	62	60	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}	Junction-to-Ambient							
D SO-8		105				°C/W	typ	C
DBV SOT23-6		110				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at +25°C.
At R_F = 750Ω, G = +2V/V, and R_L = 100Ω, unless otherwise noted.

		OPA890ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(2)	0°C to +70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1V/V, V_O = 100mV$_{PP}$, R_F = 0Ω	220				MHz	typ	C
	G = +2V/V, V_O = 100mV$_{PP}$	105	70	60	55	MHz	min	B
	G = +10V/V, V_O = 100mV$_{PP}$	12	8	6.8	6.3	MHz	min	B
Gain Bandwidth Product	G > +20V/V	125	90	75	70	MHz	min	B
Bandwidth for 0.1dB Flatness	G = +2V/V, V_O = 100mV$_{PP}$	16				MHz	typ	C
Peaking at a Gain of +1V/V	V_O < 100mV$_{PP}$	2				dB	typ	C
Large-Signal Bandwidth	G = +2V/V, V_O = 2V$_{PP}$	130				MHz	typ	C
Slew Rate	G = +2V/V, V_O = 2V Step	350	250	200	175	V/µs	min	B
Rise-and-Fall Time	0.2V Step	3.8				ns	typ	C
Settling Time to 0.02%	G = +1V/V, V_O = 2V Step	18				ns	typ	C
Settling Time to 0.1%		12				ns	typ	C
Harmonic Distortion	G = +2V/V, f = 1MHz, V_O = 2V$_{PP}$							
2nd-Harmonic	R_L = 200Ω	–85	–76	-73	-72	dBc	max	B
	R_L ≥ 500Ω	–90	–78	–74	–73	dBc	max	B
3rd-Harmonic	R_L = 200Ω	–85	–81	–79	–78	dBc	max	B
	R_L ≥ 500Ω	–87	–84	–82	–81	dBc	max	B
Input Voltage Noise	f > 100kHz	8.1	9.1	10.1	11.1	nV/√Hz	max	B
Input Current Noise	f > 100kHz	1.1	1.4	1.7	2.0	pA/√Hz	max	B
Differential Gain	G = +2V/V, V_O = 1.4V$_{PP}$, R_L = 150Ω	0.06				%	typ	C
Differential Phase	G = +2V/V, V_O = 1.4V$_{PP}$, R_L = 150Ω	0.04				°	typ	C
Channel-to-Channel Crosstalk	f = 5MHz, Input-Referred	–68				dB	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = V_S/2, R_L = 100Ω	60	**55**	54	52	dB	min	A
Input Offset Voltage	V_{CM} = V_S/2	±1	**±5**	±5.7	±6	mV	max	A
Average Offset Voltage Drift	V_{CM} = V_S/2			±15	±15	µV/°C	max	B
Input Bias Current	V_{CM} = V_S/2	±0.1	**±1.7**	±1.9	±2.1	µA	max	A
Average Input Bias Current Drift	V_{CM} = V_S/2			±5	±6	nA/°C	max	B
Input Offset Current	V_{CM} = V_S/2	±70	**±400**	±500	±550	nA	max	A
Average Input Offset Current Drift	V_{CM} = V_S/2			±2.5	±2.5	nA/°C	max	B
INPUT								
Most Positive Input Voltage(5)		+4	**+3.7**	+3.65	+3.6	V	min	A
Least Positive Input Voltage(5)		+1	**+1.3**	+1.3	+1.4	V	max	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = V_S/2, Input-Referred	65	**59**	56	55	dB	min	A
Input Impedance								
Differential	V_{CM} = V_S/2	190 || 0.6				kΩ || pF	typ	C
Common-Mode	V_{CM} = V_S/2	3.2 || 0.9				MΩ || pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	+4.0	**+3.9**	+3.85	+3.8	V	min	A
	R_L = 100Ω	+3.9	**+3.75**	+3.7	+3.65	V	min	A
Least Positive Output Voltage	No Load	+1.0	**+1.1**	+1.15	+1.2	V	max	A
	R_L = 100Ω	+1.1	**+1.35**	+1.4	+1.45	V	max	A
Output Current: Sourcing, Sinking	V_O = V_S/2	±35	**±30**	±28	±25	mA	min	A
Short-Circuit Output Current	Output Shorted to Ground	±65				mA	typ	C
Closed-Loop Output Impedance	G = +2V/V, f = 100kHz	0.04				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +2°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at +25°C.

At R_F = 750Ω, G = +2V/V, and R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA890ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]			
DISABLE	Disable LOW							
Power-Down Supply Current (+V_S)	V_{DIS} = 0V, both channels	18	**45**	50	65	µA	max	A
Disable Time	V_{OUT} = 1V_{DC}	7				ns	typ	C
Enable Time	V_{OUT} = 1V_{DC}	200				ns	typ	C
Off Isolation	G = +2V/V, f = 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Enable Voltage		3.0	**3.2**	3.4	3.8	V	min	A
Disable Voltage		1.4	**1.1**	1.0	0.8	V	max	A
Control Pin Input Bias Current (V_{DIS})	V_{DIS} = 0V, Each Channel	15	**30**	35	40	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		+5				V	typ	C
Minimum Operating Voltage		+3				V	typ	C
Maximum Operating Voltage			**+12**	+12	+12	V	max	A
Maximum Quiescent Current	V_S = +5V	1.06	**1.18**	1.20	1.25	mA	max	A
Minimum Quiescent Current	V_S = +5V	1.06	**0.92**	0.90	0.87	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	+V_S = 4.5V to 5.5V	65				dB	typ	C
THERMAL CHARACTERISTICS								
Specified Operating Range		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}	Junction-to-Ambient							
D SO-8		105				°C/W	typ	C
DBV SOT23-6		110				°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

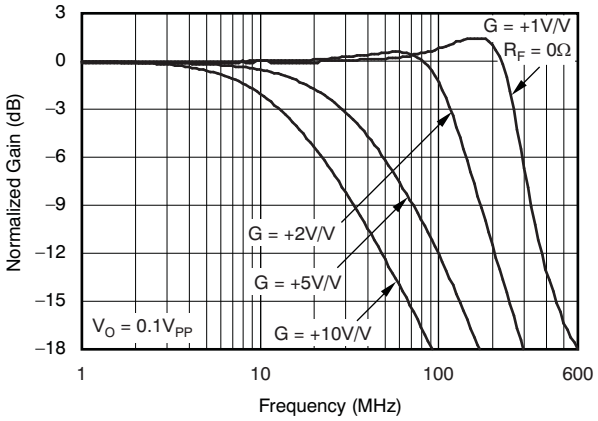


Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

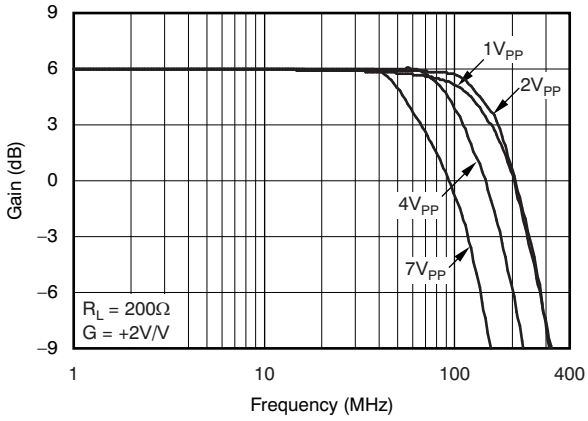


Figure 2.

SMALL-SIGNAL PULSE RESPONSE

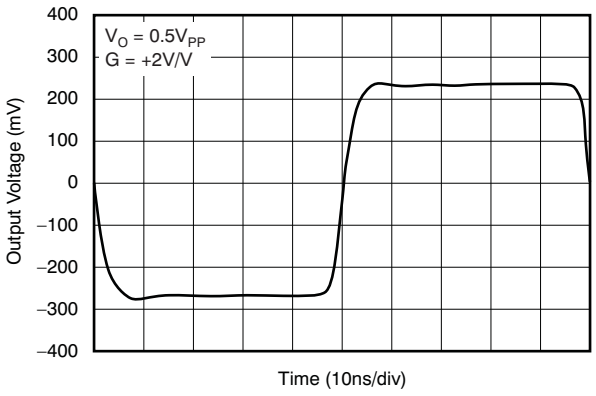


Figure 3.

LARGE-SIGNAL PULSE RESPONSE

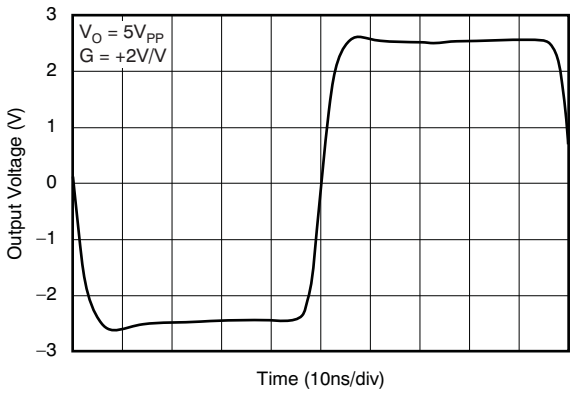


Figure 4.

VIDEO DIFFERENTIAL GAIN/DIFFERENTIAL PHASE

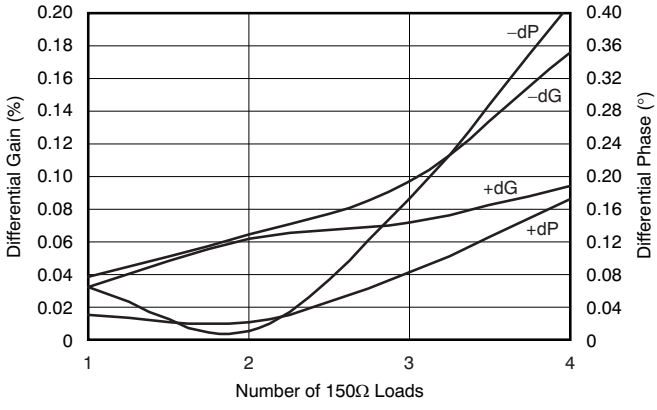


Figure 5.

DISABLE FEEDTHROUGH

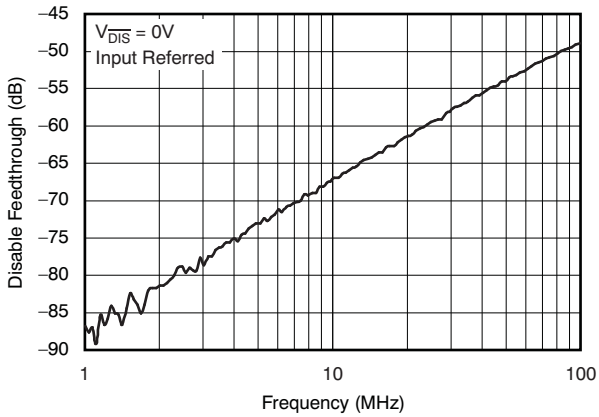


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

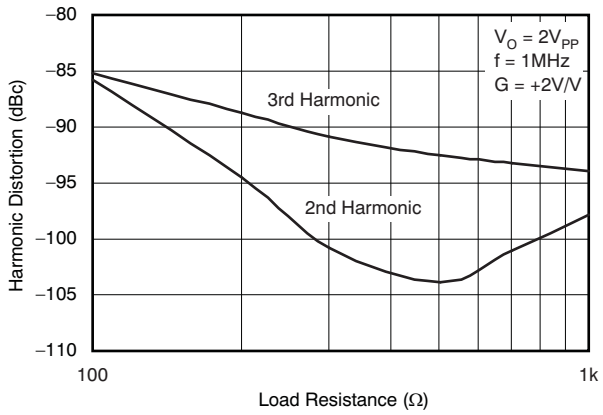


Figure 7.

1MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

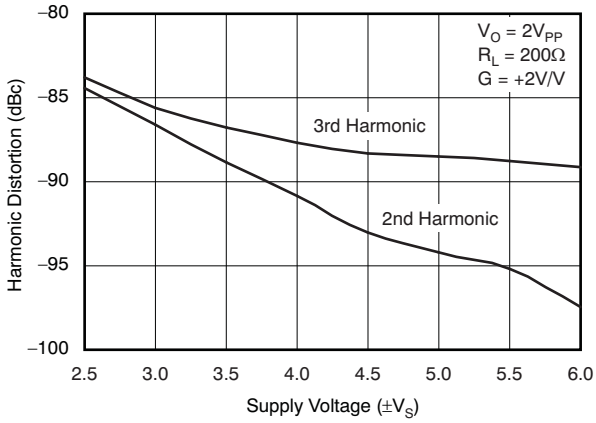


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

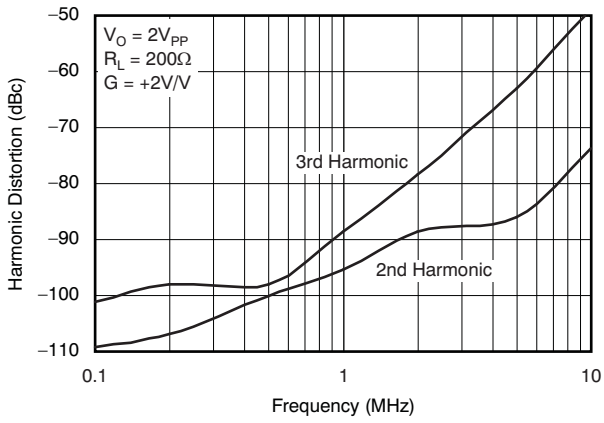


Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

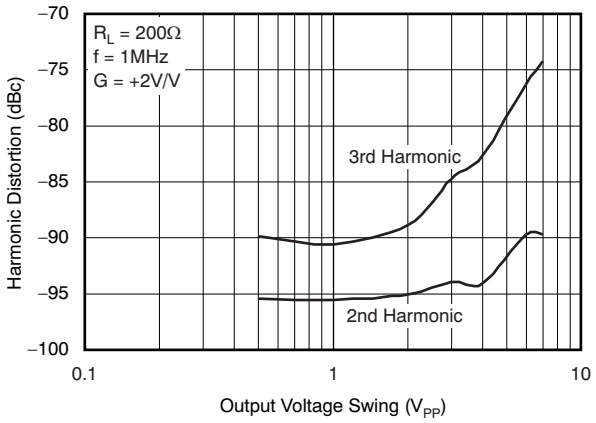


Figure 10.

HARMONIC DISTORTION vs NONINVERTING GAIN

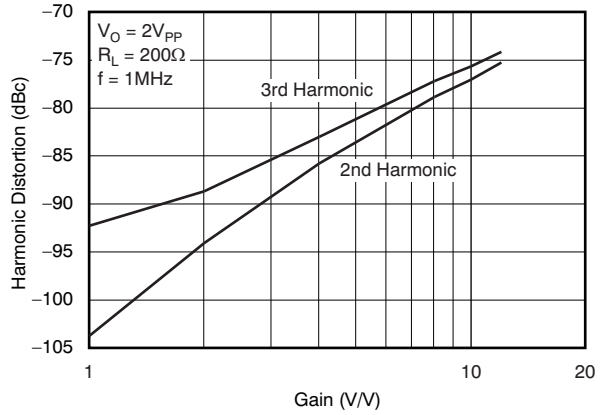


Figure 11.

HARMONIC DISTORTION vs INVERTING GAIN

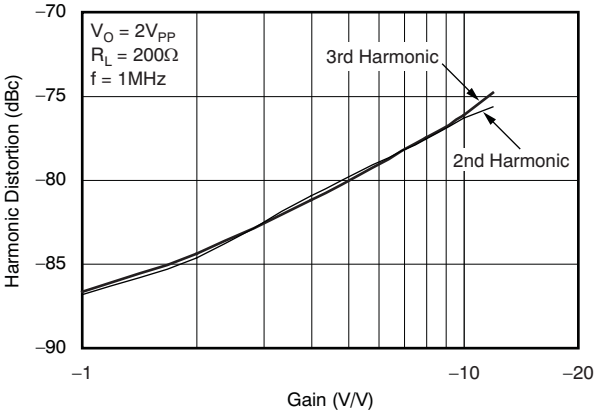


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted.

LOW-FREQUENCY INVERTING HARMONIC DISTORTION

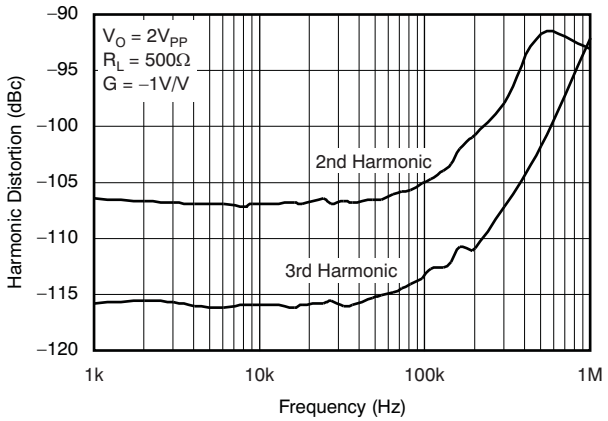


Figure 13.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

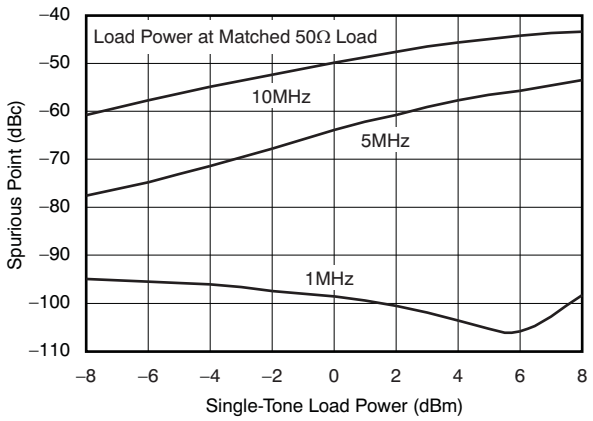


Figure 14.

RECOMMENDED R_S vs CAPACITIVE LOAD

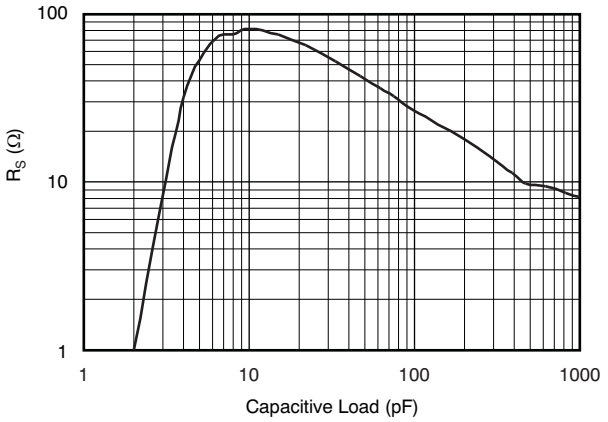


Figure 15.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

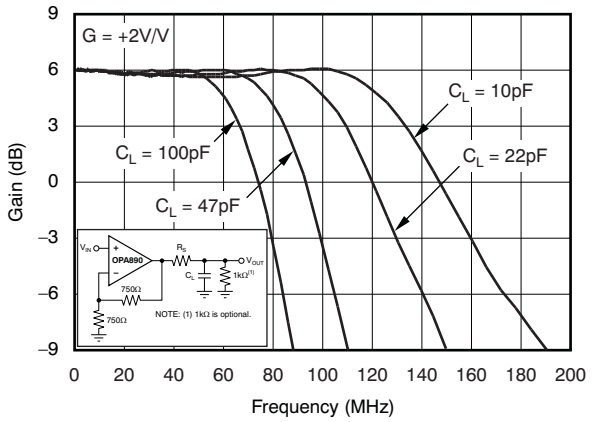


Figure 16.

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY

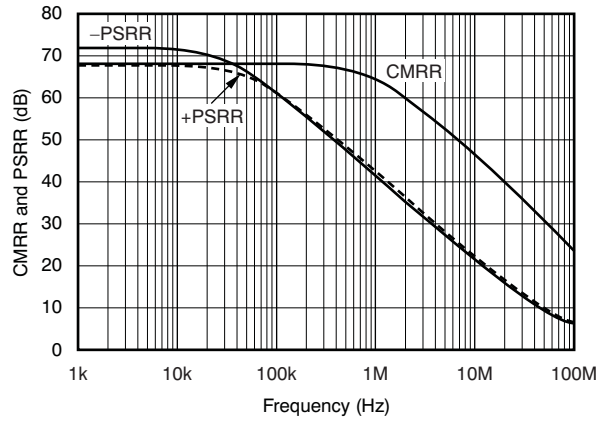


Figure 17.

INPUT VOLTAGE AND CURRENT NOISE

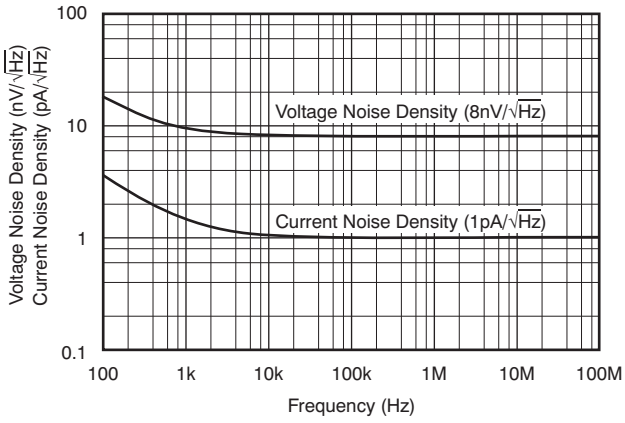


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

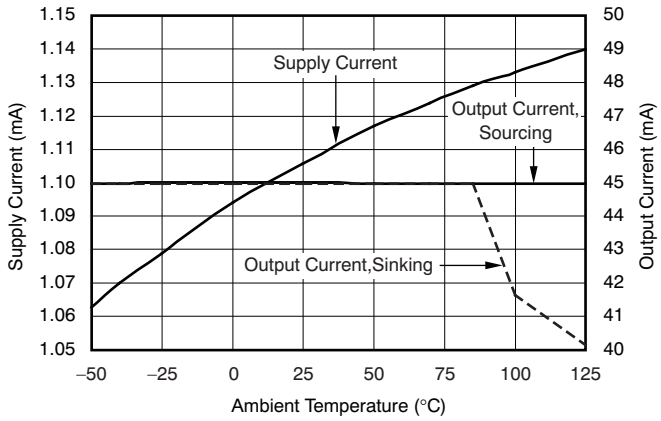


Figure 19.

TYPICAL DC DRIFT vs TEMPERATURE

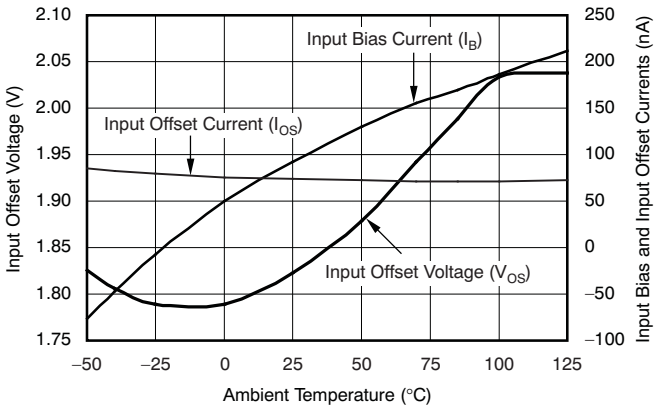


Figure 20.

LARGE-SIGNAL DISABLE/ENABLE RESPONSE

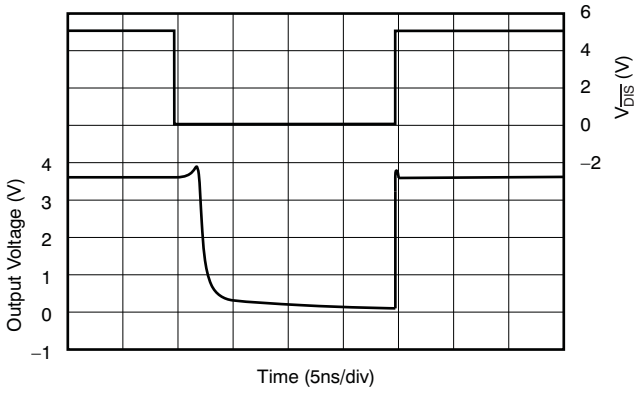


Figure 21.

NONINVERTING OVERDRIVE RECOVERY

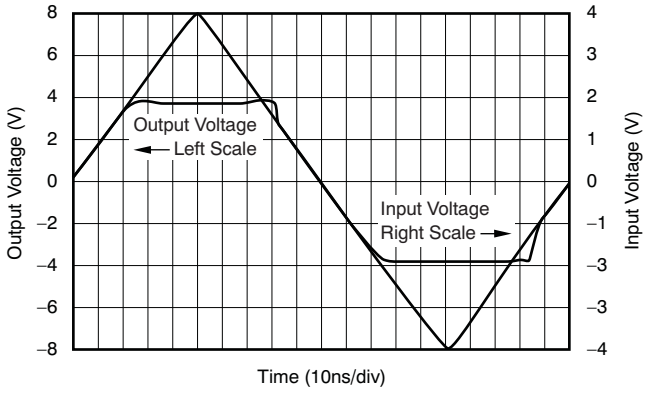


Figure 22.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

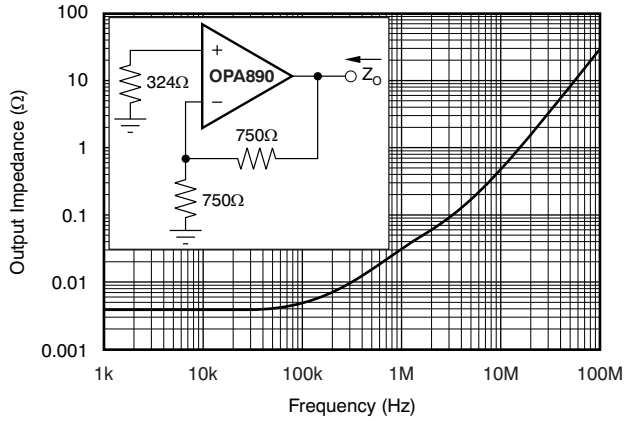


Figure 23.

OPEN-LOOP GAIN AND PHASE

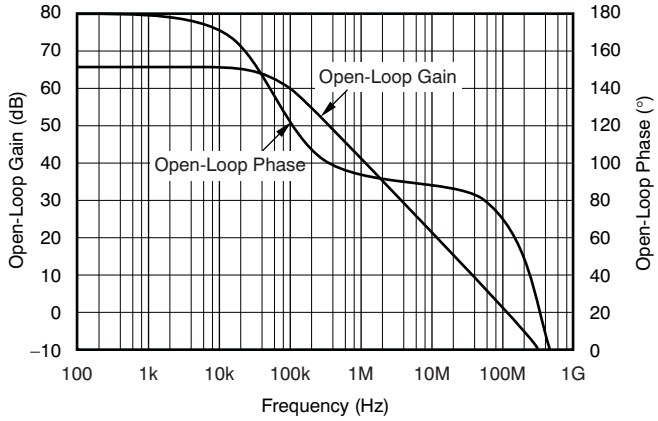


Figure 24.

TYPICAL CHARACTERISTICS: V_S = ±5V, Differential

At T_A = +25°C, Differential Gain = +2V/V, R_F = 750Ω, and R_L = 400Ω, unless otherwise noted.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

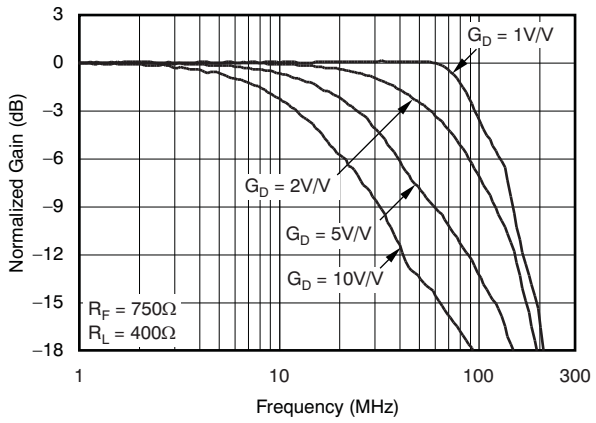


Figure 25.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

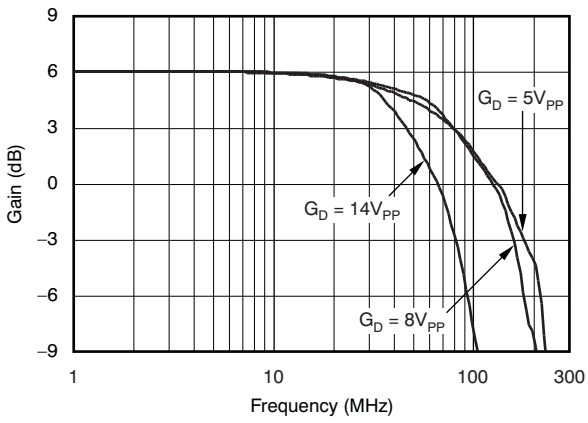


Figure 26.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

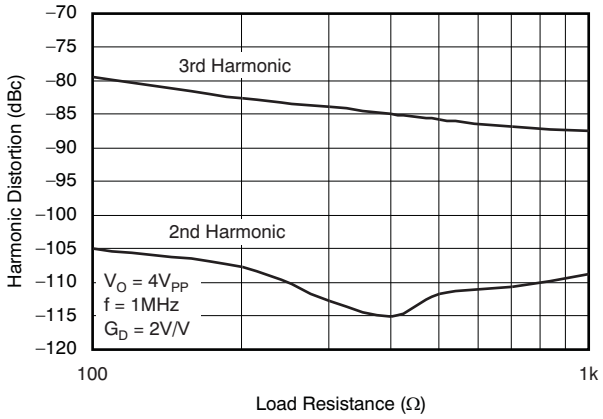


Figure 27.

DIFFERENTIAL DISTORTION vs FREQUENCY

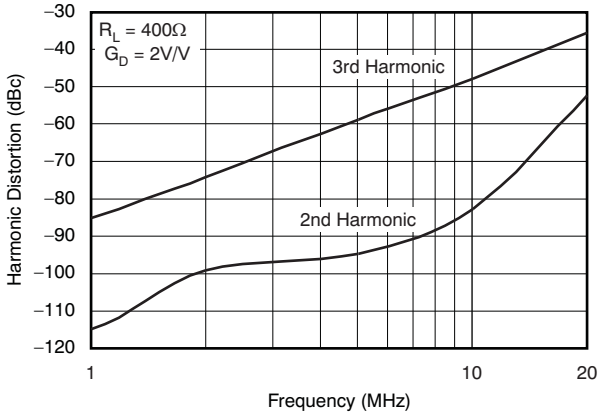


Figure 28.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

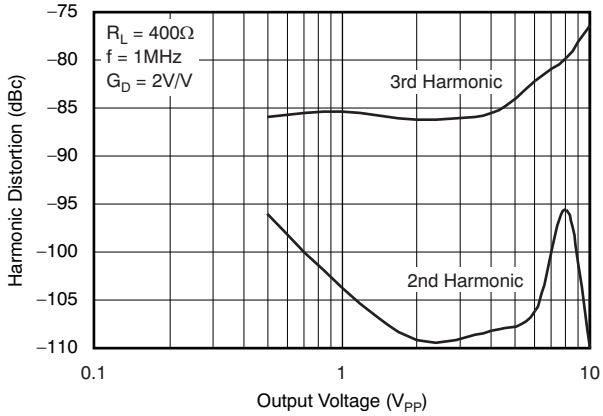


Figure 29.

TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

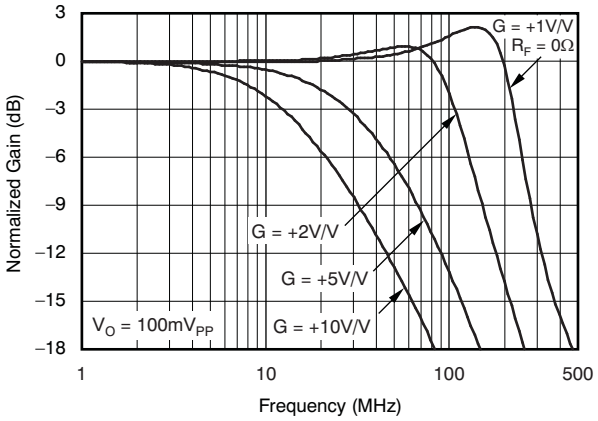


Figure 30.

LARGE-SIGNAL FREQUENCY RESPONSE

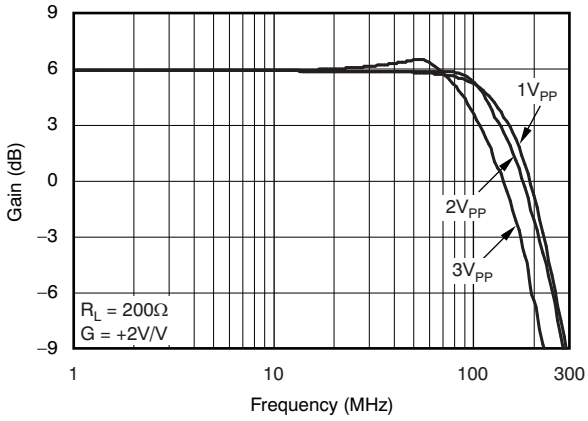


Figure 31.

SMALL-SIGNAL PULSE RESPONSE

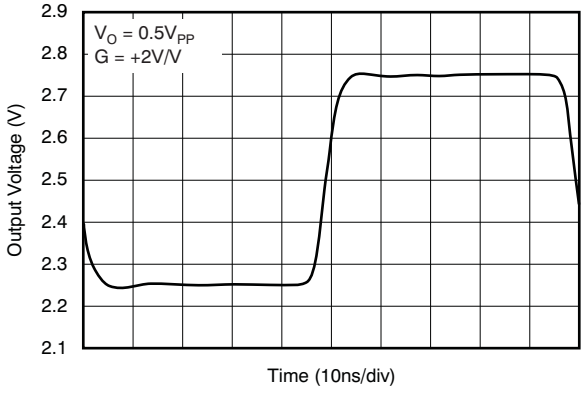


Figure 32.

LARGE-SIGNAL PULSE RESPONSE

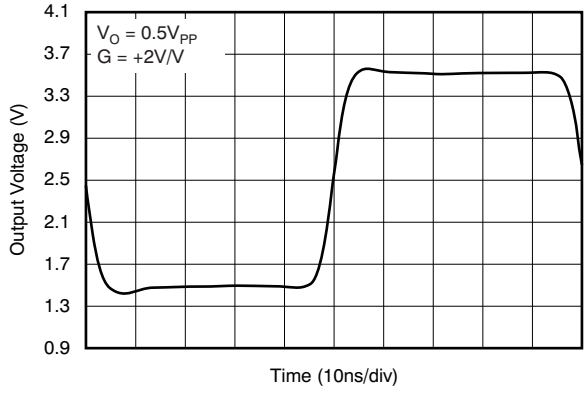


Figure 33.

RECOMMENDED R_S vs CAPACITIVE LOAD

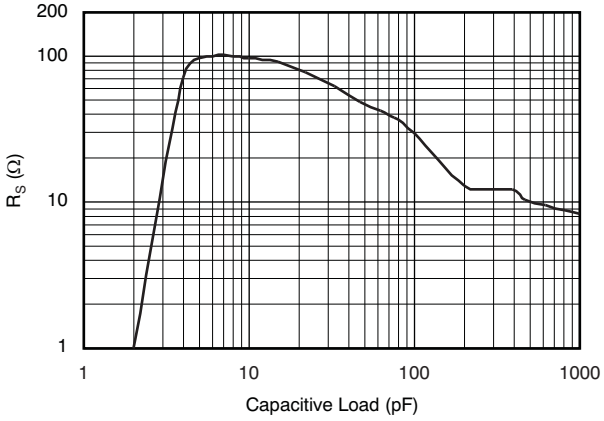


Figure 34.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

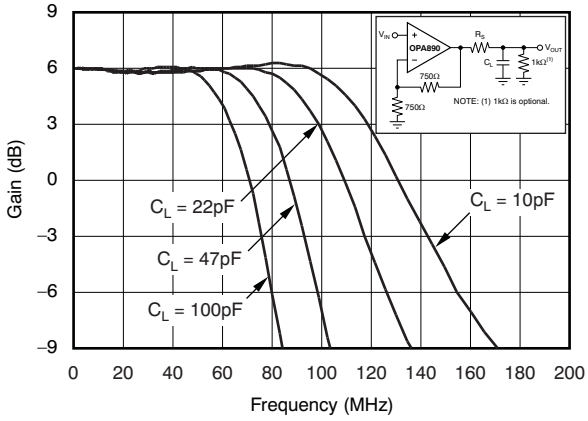


Figure 35.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted.

NONINVERTING OVERDRIVE RECOVERY

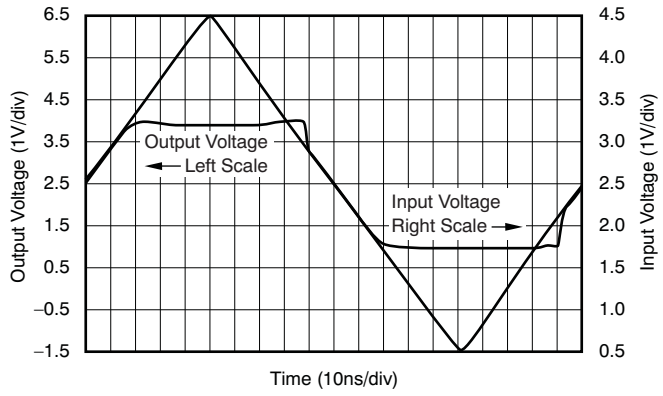


Figure 36.

HARMONIC DISTORTION vs LOAD RESISTANCE

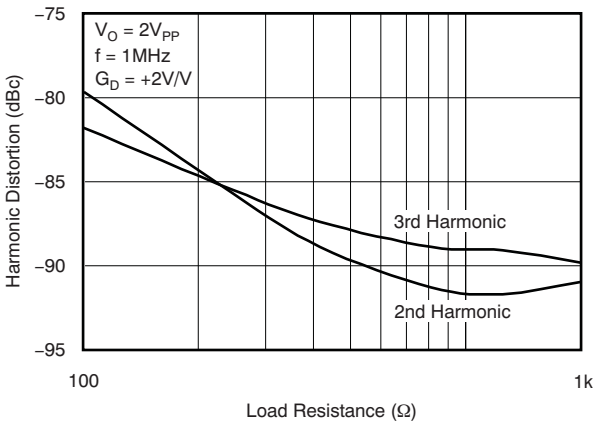


Figure 37.

HARMONIC DISTORTION vs FREQUENCY

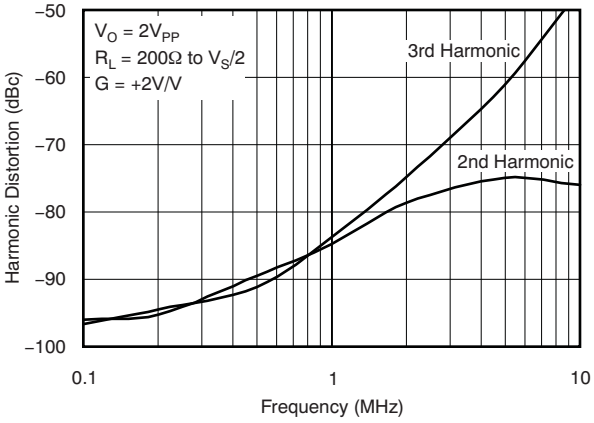


Figure 38.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

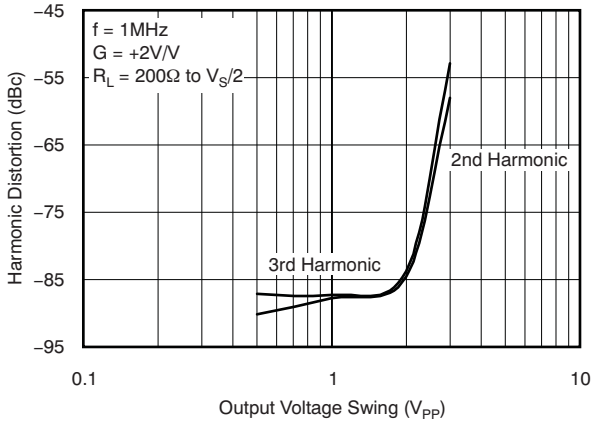


Figure 39.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

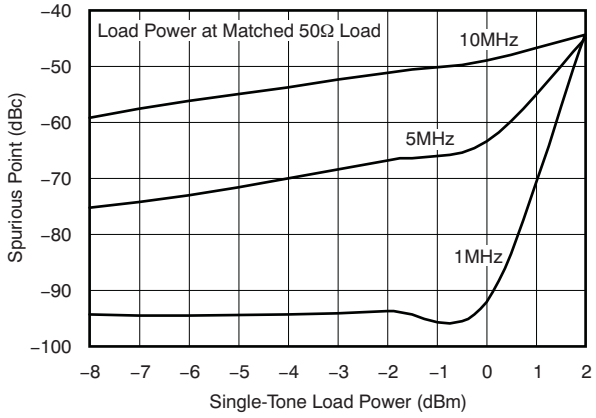


Figure 40.

TYPICAL CHARACTERISTICS: V_S = +5V, Differential

At T_A = +25°C, Differential Gain = +2V/V, R_F = 750Ω, and R_L = 400Ω, unless otherwise noted.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

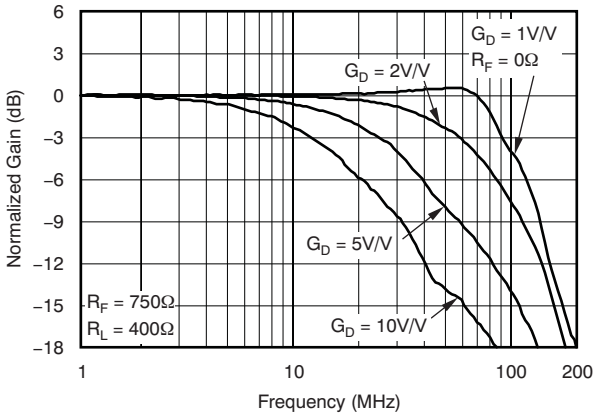


Figure 41.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

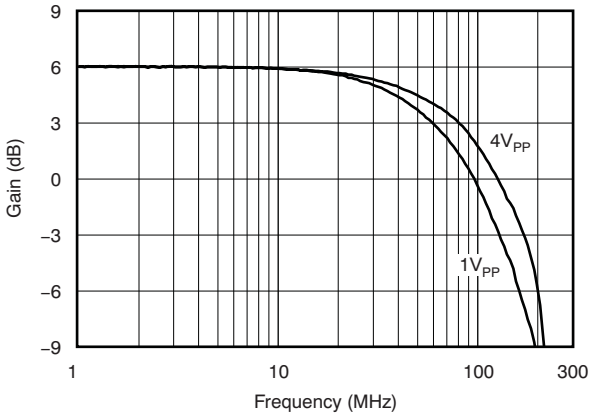


Figure 42.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

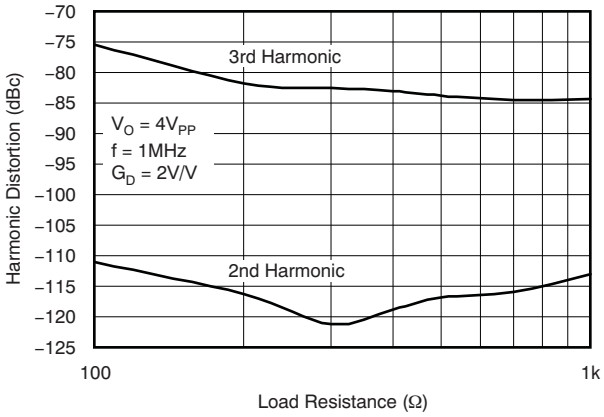


Figure 43.

DIFFERENTIAL DISTORTION vs FREQUENCY

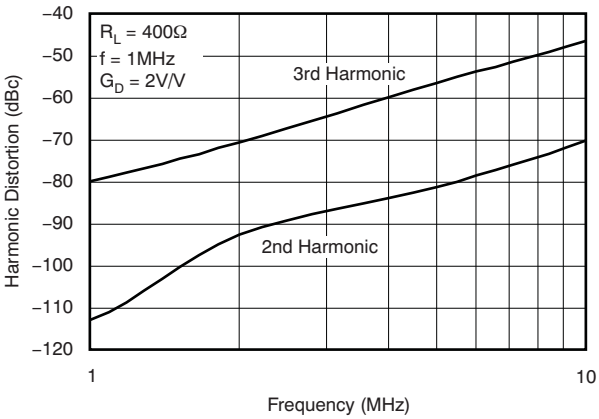


Figure 44.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

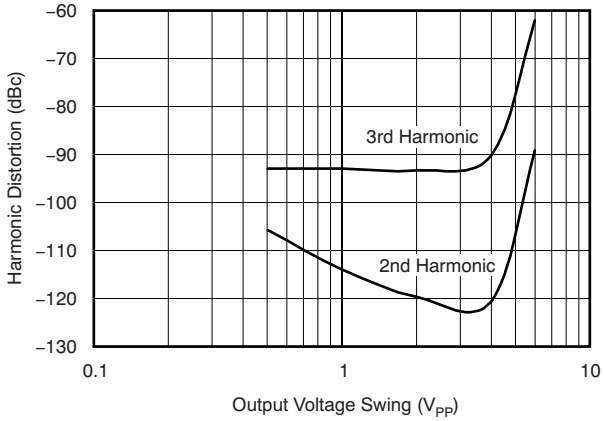


Figure 45.

APPLICATION INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA890 provides an exceptional combination of low quiescent current with a wideband, unity-gain stable, voltage-feedback op amp using a new high slew rate input stage. Typical differential input stages used for voltage-feedback op amps are designed to steer a fixed-bias current to the compensation capacitor, setting a limit to the achievable slew rate. The OPA890 uses an input stage that places the transconductance element between two input buffers, using the combined output currents as the forward signal. As the error voltage increases across the two inputs, an increasing current is delivered to the compensation capacitor. This increasing current provides very high slew rate (500V/µs) while consuming relatively low quiescent current (1.1mA). This exceptional full-power performance comes at the price of a slightly higher input noise voltage than alternative architectures. The 8nV/√Hz input voltage noise for the OPA890 is low for this combination of input stage and low quiescent current.

Figure 46 shows the dc-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Typical Characteristics are taken directly at the input and output pins, while output powers (dBm) are at the matched 50Ω load. For the circuit of Figure 46, the total effective load will be 100Ω 1.5kΩ. The disable control line is typically left open to ensure normal amplifier operation. Two optional components are included in Figure 46. An additional resistor (324Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance looking back towards the signal generator, this configuration gives an input bias current cancelling resistance that matches the 375Ω source resistance seen at the inverting input (see the *DC Accuracy and Offset Control* section). In addition to the usual power-supply decoupling capacitors to ground, a 0.1µF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional-added capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

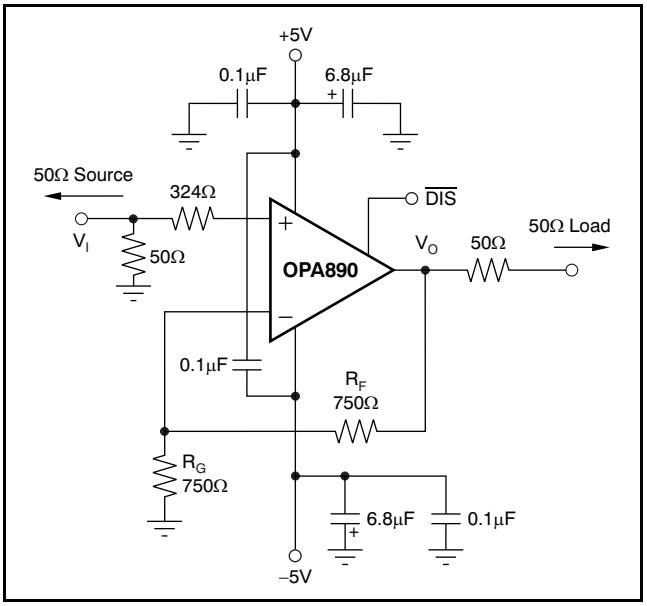


Figure 46. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit

Figure 47 shows the ac-coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V Electrical Characteristics and Typical Characteristics. Though not a *rail-to-rail* design, the OPA890 requires minimal input and output voltage headroom compared to other very wideband voltage-feedback op amps. It delivers a $2V_{PP}$ output swing on a single +5V supply with > 100MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 47 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 698Ω resistors). The input signal is then ac-coupled into the midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a $2V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (59Ω) used for testing is adjusted to give a 50Ω input load when the parallel combination of the biasing divider network is included.

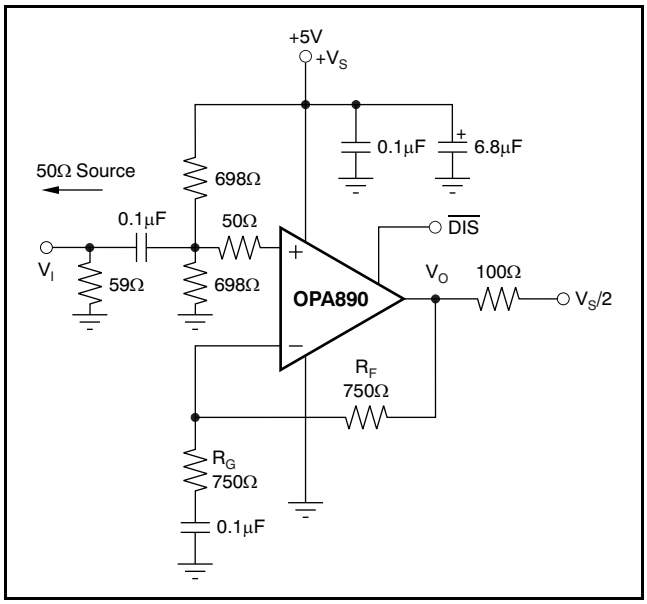


Figure 47. AC-Coupled, G = +2, Single-Supply, Specification and Test Circuit

Again, an additional resistor (50Ω, in this case) is included directly in series with the noninverting input. This minimum recommended value provides part of the dc source resistance matching for the noninverting input bias current. It is also used to form a simple parasitic pole to roll off the frequency response at very high frequencies (> 500MHz) using the input parasitic capacitance to form a bandlimiting pole. The gain resistor (R_G) is ac-coupled, giving the circuit a dc gain of +1, which puts the input dc bias voltage (2.5V) at the output as well. The voltage can swing to within 1.35V of either supply pin. Driving a demanding 100Ω load to a midpoint bias is used in this characterization circuit. Higher swings are possible using a lighter load.

MULTIPLYING DAC SINGLE-ENDED OUTPUT TRANSIMPEDANCE AMPLIFIER

Multiplying digital-to-analog converters (DACs), such as the DAC7822, can make good use of the low-power, high slew rate amplifier, OPA890.

The frequency response of the schematic shown in Figure 48 is shown in Figure 49.

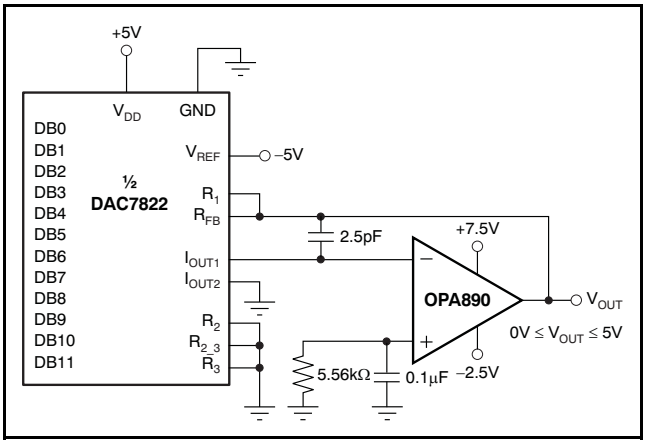


Figure 48. DAC Transimpedance Amplifier

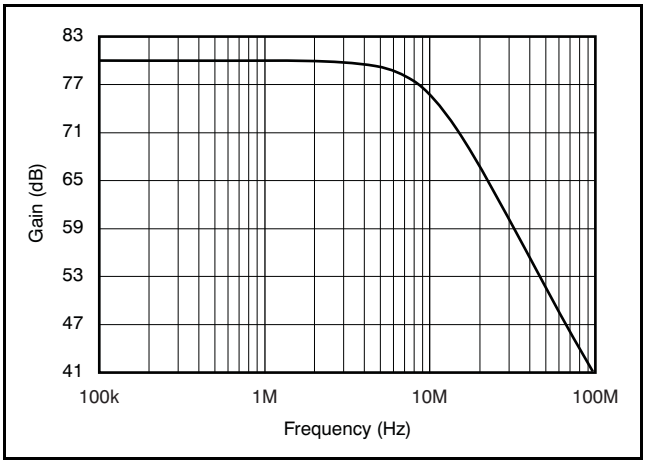


Figure 49. OPA890 (as DAC Transimpedance Amplifier) Frequency Response

Driving a light load, the OPA890 can output ±4V over ±5V supplies. Setting the reference voltage to –5V results in an output voltage swing from 0V to 5V. In order to optimize the OPA2890 operation for this application, the supply voltages have been adjusted so that the output voltage swing is balanced around mid-supply of the amplifier. Note that as a result of the internal architecture of the multiplying DAC, the I_{OUT1} output is not high impedance. The I_{OUT1} output resistance is between 4.5kΩ and 22.1kΩ (excluding code 000h) for a 10kΩ nominal V_{REF} input resistance. I_{OUT1} output resistance changes are directly related to the code change. This low impedance has multiple effects when a bipolar technology amplifier is used.

Some of these effects are:

- The noise gain of the amplifier changes for each code.
- The output offset voltage of the amplifier changes for each code, because of the input offset voltage.
- The input bias current cannot be cancelled. The effects of the input bias current can be reduced, but not eliminated, thereby affecting the total output offset voltage of the amplifier with each code.
- The noninverting pin of the amplifier must be tied to ground and cannot be used to create a dc offset on the output amplifier, as is the case for the transimpedance amplifier.

The following analysis excludes the input offset current.

The total output offset voltage variations because of code changing in the DAC can be expressed as:

$\Delta V_{OSO} = +\Delta NG \{[(R_F \quad R_{OUT1}) – R_S] + V_OS\}$

Where:

$4.5k\Omega \leq R_{OUT1} \leq 22.1k\Omega$

$R_F = 10k\Omega$

Using the previous values, the variation of the parallel combination of R_F and R_{OUT1} can be constrained to: $4.19k\Omega \leq (R_F \quad R_{OUT1}) \leq 6.88k\Omega$. In order to optimize the bias current cancellation, we select R_S to be the average of those limiting numbers, or $R_S = (6.88k\Omega + 4.19k\Omega)/2 = 5.56k\Omega$.

Looking at the variation for each code, the total error (when including all codes) is ~3.9LSB for the OPA890.

Notice that most of the error occurs mainly at the first codes (0, 1, 2); excluding these codes from the analysis yields the following results, shown in Table 1.

Table 1. DC Accuracy vs Code

CODES	TOTAL ERROR DUE TO V_{OS} and I_B
All codes	3.9LSB
Excluding code 0	2.5LSB
Excluding codes 0 and 1	2LSB
Excluding codes 0, 1, and 2	1.83LSB

Note that 1LSB = 1.221mV in the example shown in Figure 48

If more precision is required while maintaining the ac performance, a FET-input amplifier (such as the OPA656 or the THS4631) is a good alternative.

Figure 48 shows a single-ended output drive implementation. In this circuit, only one side of the complementary output drive signal is used. A dual amplifier, such as the OPA2890, provides both output drivers for the DAC7822. If even lower quiescent current is needed, the OPA2889 can be used instead, with minor modifications. The diagram shows the signal output current connected into the virtual ground summing junction of the OPA890, which is set up as a transimpedance stage or *I-V converter*. The unused current output of the DAC is connected to ground. The dc gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance produces a zero in the noise gain for the OPA890 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in the feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (2)$$

which gives a closed-loop transimpedance bandwidth, $f_{–3dB}$, of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \quad (3)$$

Using the DAC7822 internal output capacitance of 25pF gives a feedback capacitance (C_F) of 2.5pF and an 8.8MHz bandwidth.

SINGLE-SUPPLY ACTIVE FILTERS

The high bandwidth provided by the OPA890, while operating on a single +5V supply, lends itself well to high-frequency active filter designs. Again, the key additional requirement is to establish the dc operating point of the signal near the supply midpoint for highest dynamic range. See Figure 50 for an example design of a 5MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are ac-coupled using 0.1µF blocking capacitors (actually giving band pass response with the low-frequency pole set to 32kHz for the component values shown). As discussed for Figure 47, this configuration allows the midpoint bias formed by the two 1.87kΩ resistors to appear at both the input and output pins. The midband signal gain is set to +4 (12dB) in this case. The capacitor to ground on the noninverting input is intentionally set larger to dominate input parasitic terms. At a gain of +4, the OPA890 on a single supply shows ~30MHz small- and large-signal bandwidth. The resistor values have been slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit show a precise 5MHz, –3dB point with a maximally flat passband (above the 32kHz ac-coupling corner), and a maximum stop band attenuation of 24dB at the amplifier –3dB bandwidth of 30MHz.

Note that the dc impedance looking out of each input for this circuit has been set to 1.5kΩ to reduce the output offset voltage retaining maximum signal swing for a mid supply nominal operating voltage at the output.

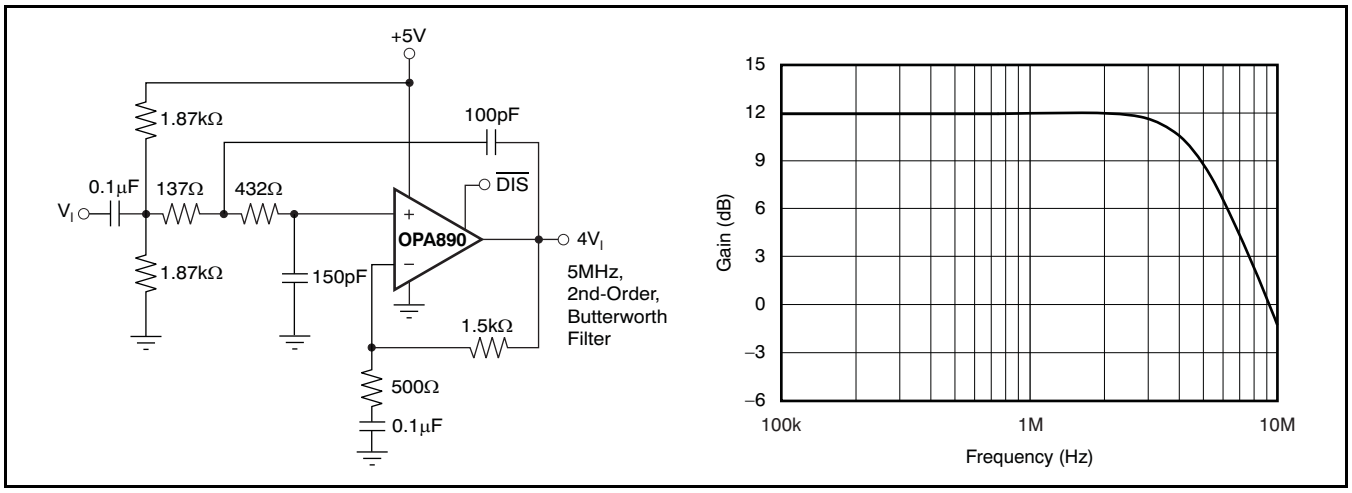


Figure 50. Single-Supply, High-Frequency Active Filter

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA890 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 2.

Table 2. Demonstration Board Summary

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA890ID	SO-8	DEM-OPA-SO-1A	SBOU009
OPA890IDBV	SOT23-6	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA890 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This practice is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA890 is available through the Texas Instruments web page (www.ti.com). These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between package types in the small-signal ac performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Because the OPA890 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values can be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. Usually, for G > 1 applications, the feedback resistor value should be between 200Ω and 1.5kΩ. Below 200Ω, the feedback network presents additional output loading that can degrade the harmonic distortion performance of the OPA890. Above 1.5kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band-limiting in the amplifier response.

The combined impedance of R_F || R_G interacts with the inverting input capacitance, placing an additional pole in the feedback network and thus, a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, having R_F || R_G < 400Ω keeps this pole above 250MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This increase is acceptable, as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

BANDWIDTH VERSUS GAIN

Noninverting Amplifier Operation

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the gain bandwidth product (GBP) shown in the *Electrical Characteristics*. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) predicts the closed-loop bandwidth. In practice, this relationship only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most amplifiers exhibit a more complex response with lower phase margin. The OPA890 is compensated to give a slightly peaked response in a noninverting gain of 2V/V (see Figure 46). This compensation results in a typical gain of +2V/V bandwidth of 115MHz, far exceeding that predicted by dividing the 130MHz GBP by 2. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10V/V, the 13MHz bandwidth shown in the *Electrical Characteristics* agrees with that predicted using the simple formula and the typical GBP of 130MHz.

The OPA890 exhibits minimal bandwidth reduction going to single-supply (+5V) operation as compared with ±5V. This difference in performance occurs because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins is changed.

Inverting Amplifier Operation

The OPA890 is a general-purpose, wideband voltage-feedback op amp; therefore, all of the familiar op amp application circuits are available to the designer. Inverting operation is one of the more common requirements and offers several performance benefits. Figure 51 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 46 are retained in an inverting circuit configuration.

In the inverting configuration, three key design considerations must be noted. First, the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted-pair, long PCB trace, or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This approach is the simplest, and results in optimum bandwidth and noise performance. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of –2V/V, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This option has the interesting advantage that the noise gain becomes equal to 2V/V for a 50Ω source impedance—the same as the noninverting circuits considered in the previous section. The amplifier output, however, now sees the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to a range of 200Ω to 1.5kΩ. In this case, it is preferable to increase both the R_F and R_G values, as shown in Figure 51, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

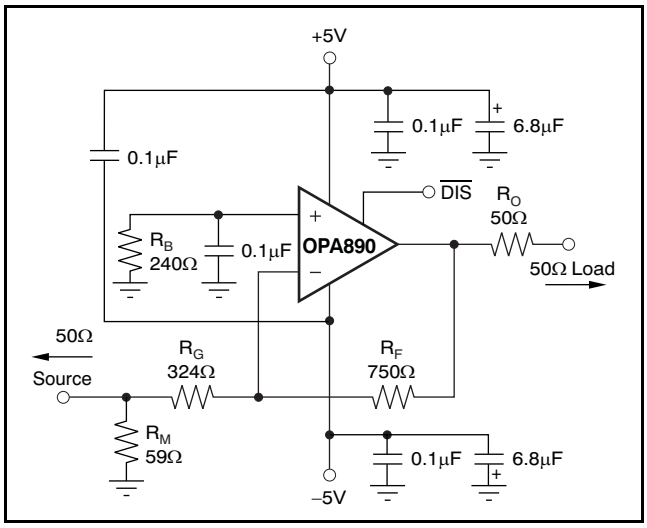


Figure 51. Gain of –2V/V Example Circuit

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and influences the bandwidth. For the example in Figure 51, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω 59Ω = 27Ω. This impedance is added in series with R_G for calculating the noise gain (NG). The resulting NG is 3.14V/V for Figure 51, as opposed to only 2 if R_M could be eliminated as discussed previously. The bandwidth is therefore slightly lower for the gain of –2V/V circuit of Figure 51 than for the gain of +2V/V circuit of Figure 46.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input (R_B). If this resistor is set equal to the total dc resistance looking out of the inverting node, the output dc error (because of the input bias currents) is reduced to (Input Offset Current) × R_F. If the 50Ω source impedance is dc-coupled in Figure 51, the total resistance to ground on the inverting input is 351Ω. Combining this resistance in parallel with the feedback resistor gives the value of R_B = 240Ω used in this example. To reduce the additional high-frequency noise introduced by this resistor, it is sometimes bypassed with a capacitor. As long as R_B < 350Ω, a capacitor is not required because the total noise contribution of all other terms is less than that of the op amp input noise voltage. As a minimum, the OPA890 requires an R_B value of 50Ω to damp out parasitic-induced peaking—a direct short to ground on the noninverting input runs the risk of a very high-frequency instability in the input stage.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier such as the OPA890 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series-isolation resistor between the amplifier output and the capacitive load. This solution does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to reduce the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The *Typical Characteristics* show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA890. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA890 output pin (see the *Board Layout Guidelines* section).

NOISE PERFORMANCE

The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 52 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

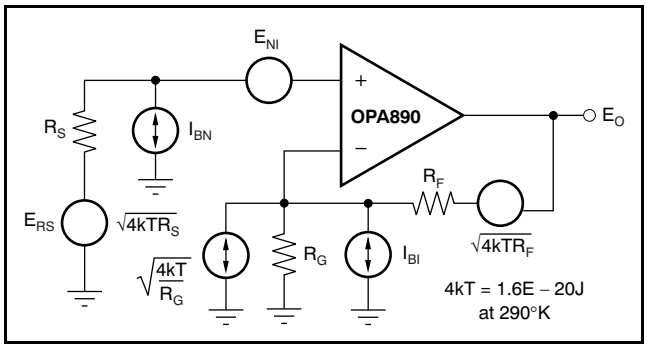


Figure 52. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms shown in Figure 52.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (4)$$

Dividing this expression by the noise gain [NG = (1 + R_F/R_G)] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 5.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (5)$$

Evaluating these two equations for the OPA890 circuit and component values (see Figure 46) gives a total output spot noise voltage of 17.4nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 8.7nV/$\sqrt{Hz}$. This total includes the noise added by the bias current cancellation resistor (175Ω) on the noninverting input. This total input-referred spot noise voltage is only slightly higher than the 8nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This result will be the case, as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 350Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 350Ω satisfies both noise and frequency response flatness considerations. Because the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_B) for the inverting op amp configuration of Figure 51 is not required.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output dc accuracy in a wide variety of applications. The power-supply current trim for the OPA890 gives even tighter control than comparable amplifiers. Although the high-speed input stage does require relatively high input bias current (+25°C worst case, 1.6μA at each input terminal), the close matching between them may be used to reduce the output dc error caused by this current. The total output offset voltage may be considerably reduced by matching the dc source resistances appearing at the two inputs. This matching reduces the output dc error resulting from the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 46, and using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

$\pm(NG \times V_{OS(MAX)}) \pm (R_F \times I_{OS(MAX)})$

$= \pm(2 \times 5mV) \pm (750\Omega \times 0.35\mu A)$

$= \pm 11.3mV$

with NG = noninverting signal gain

A fine-scale output offset null or dc operating point adjustment is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most of these techniques eventually reduce to adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the dc offset voltage on the summing junction will set up a dc current back into the source that must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a dc-coupled inverting amplifier, see Figure 53 for one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the dc offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This configuration ensures that the adjustment circuit has minimal effect on the loop gain and thus, the frequency response.

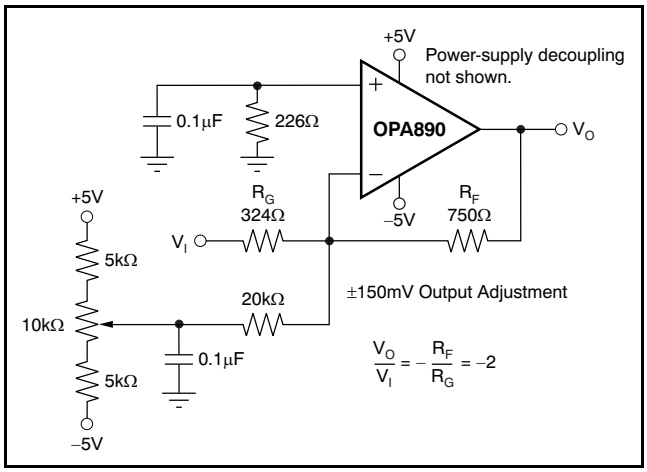


Figure 53. DC-Coupled, Inverting Gain of -2V/V, with Offset Adjustment

DISABLE OPERATION

The OPA890 provides an optional disable feature that may be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{DIS}$ control pin is left unconnected, the OPA890 operates normally. To disable the OPA890, the control pin must be asserted low. Figure 54 shows a simplified internal circuit for the disable control feature.

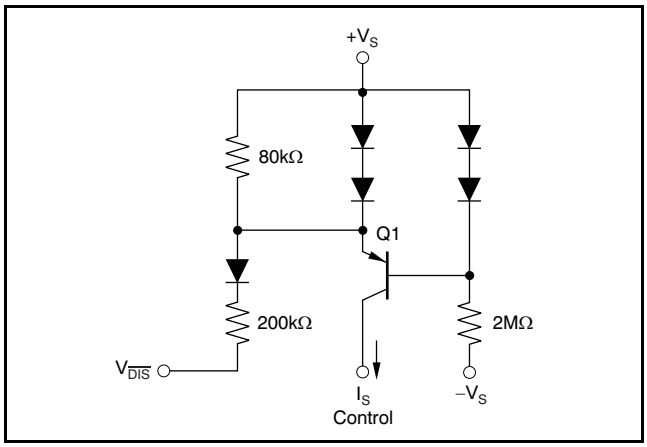


Figure 54. Simplified Disable Control Circuit

In normal operation, base current to Q1 is provided through the 2MΩ resistor, while the emitter current through the 80kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in the Q1 emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 80kΩ resistor, eventually turning on those two diodes (15µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes, holding the emitter-base voltage of Q1 at approximately 0V. This process shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode is only that required to operate the circuit of Figure 54. Additional circuitry ensures that turn-on time occurs faster than turn-off time (*make-before-break*).

When disabled, the output and input nodes go to a high-impedance state. If the OPA890 is operating at a gain of +1V/V, it shows a very high impedance at the output and exceptional signal isolation. If operating at a gain greater than +1V/V, the total feedback network resistance ($R_F + R_G$) appears as the impedance looking back into the output, but the circuit still shows very-high forward and reverse isolation. If configured as an inverting amplifier, the input and output are connected through the feedback network resistance ($R_F + R_G$) and the isolation is very poor, as a result.

THERMAL ANALYSIS

Maximum desired junction temperature sets the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, but for a grounded resistive load is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S{}^2/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA890IDBV (SOT23-6 package) in the circuit of Figure 46 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load.

$P_D = 10V \times 1.25mA + 5^2/(4 \times (100\Omega \parallel 1.5k\Omega)) = 79mW$

Maximum $T_J = +85°C + (79W \times 150°C/W) = +97°C$.

Although this result is still well below the specified maximum junction temperature, system reliability considerations may require lower operating junction temperatures. The highest possible internal dissipation occurs if the load requires current to be forced into the output for positive output voltages, or sourced from the output for negative output voltages. This configuration puts a high current through a large internal voltage drop in the output transistors.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA890 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include the following:

a. **Minimize parasitic capacitance** to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b. **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c. **Careful selection and placement of external components preserves the high-frequency performance of the OPA890**. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB traces as short as possible. Never use wirewound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 750Ω feedback used in the *Typical Characteristics* is a good starting point for design. Note that a direct short is suggested for the unity-gain follower application.

d. **Connections to other wideband devices** on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA890 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on the board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA890 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA890 allows multiple destination devices to be handled as separate transmission lines, each with its respective series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be

series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of *Recommended R_S vs Capacitive Load*. This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation because of the voltage divider formed by the series output into the terminating impedance.

e. **Socketing a high-speed part such as the OPA890 is not recommended**. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA890 directly onto the board.

INPUT AND ESD PROTECTION

The OPA890 is built using a very high-speed, complementary, bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 55.

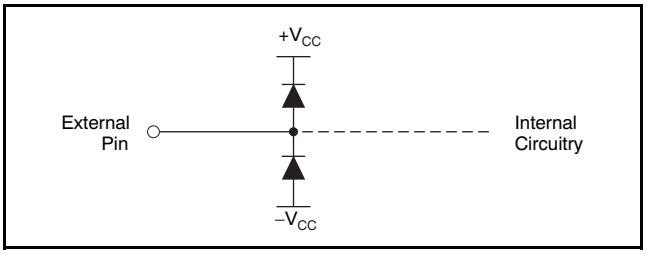


Figure 55. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA890), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, because high values degrade both noise performance and frequency response.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2008) to Revision B **Page**

- Changed min/max over temperature specifications for Input, *Common-Mode Input Range (CMIR)* parameter of ±5V electrical characteristics 3
- Changed min/max over temperature specifications for Input, *Most Positive Input Voltage* parameter of +5V electrical characteristics 5
- Changed min/max over temperature specifications for Input, *Least Positive Input Voltage* parameter of +5V electrical characteristics 5
- Corrected x-axis in Figure 18 9
- Corrected typo in Figure 49 title 16

Changes from Original (May 2007) to Revision A **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C 2
- Deleted *Channel-to-Channel Crosstalk* row from *AC Performance* section of ±5V Electrical Characteristics 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA890ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA890	Samples
OPA890IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRI	Samples
OPA890IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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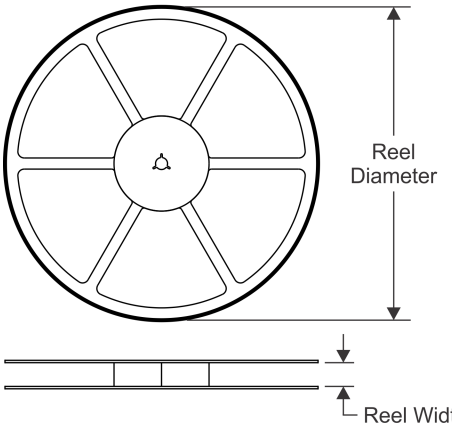
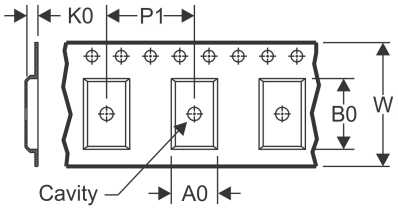
TAPE AND REEL INFORMATION

REEL DIMENSIONS

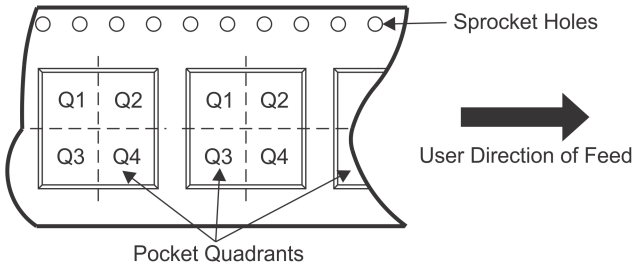


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

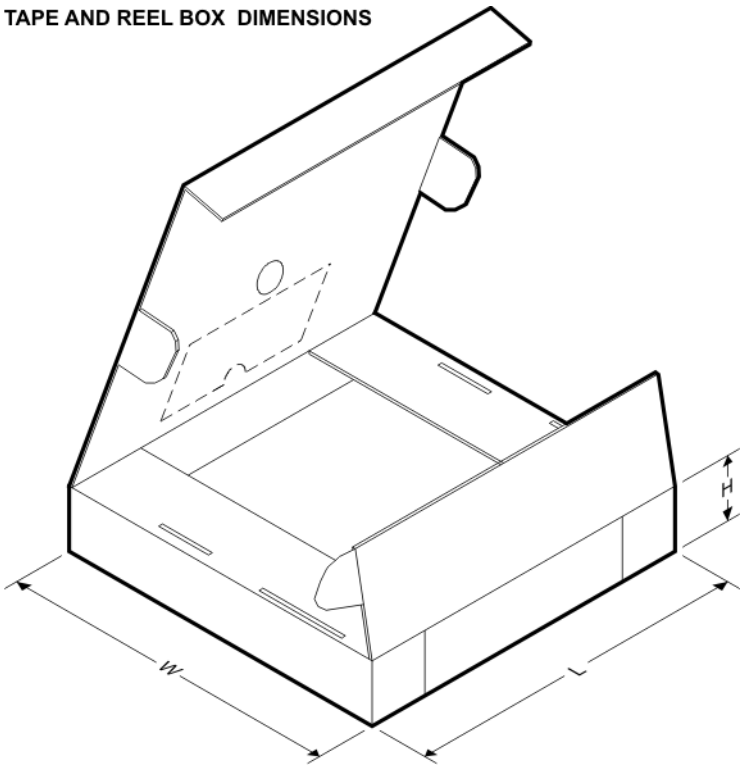
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA890IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA890IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3

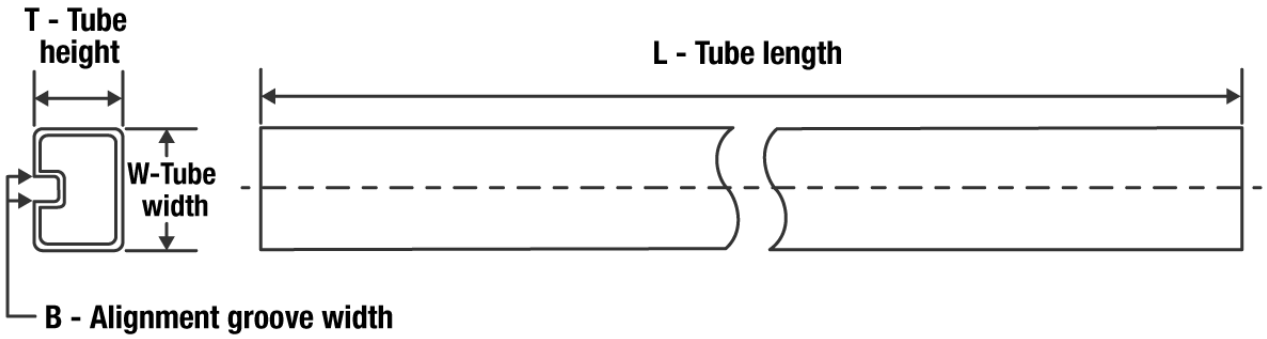
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA890IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA890IDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

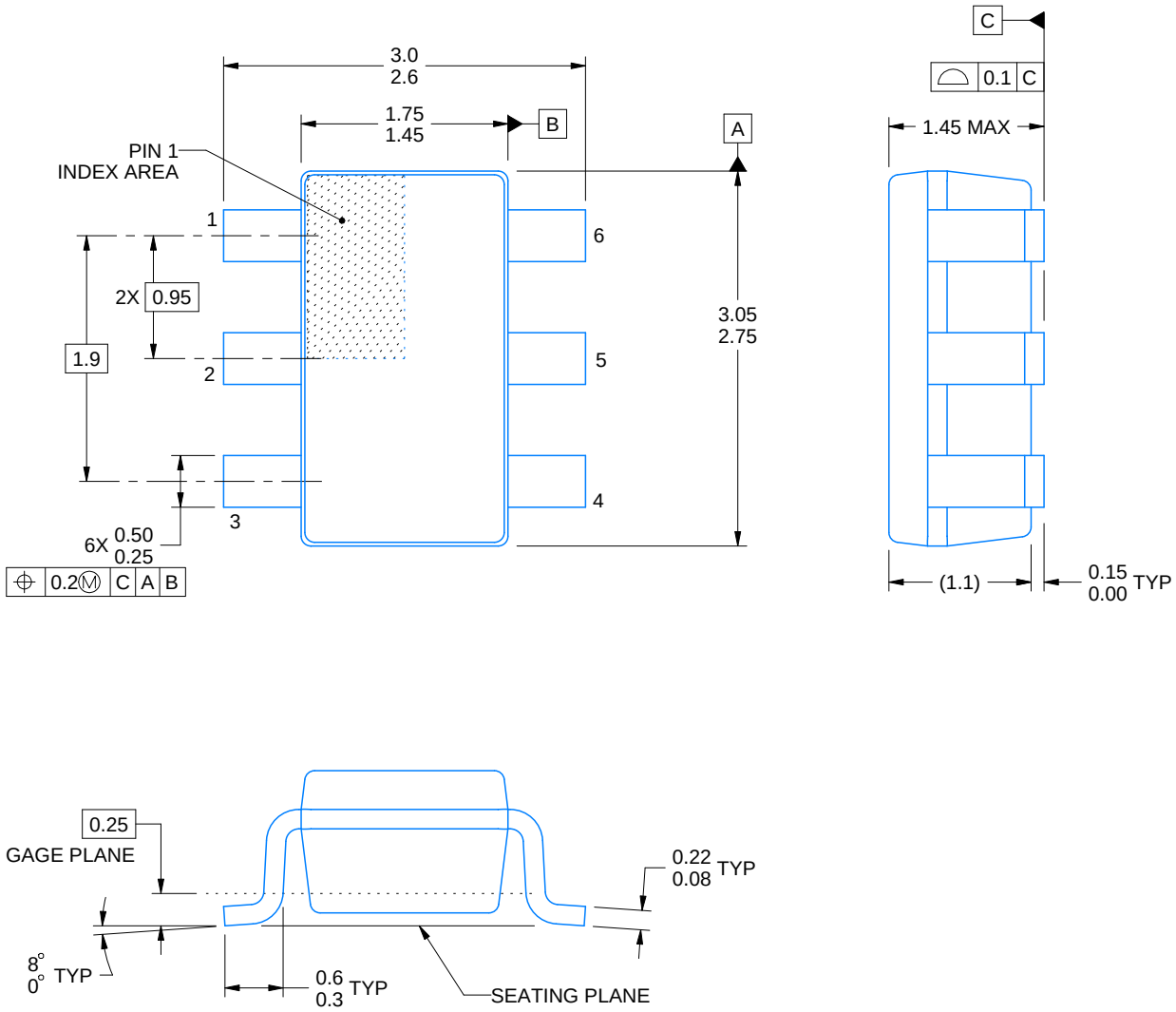
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA890ID	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

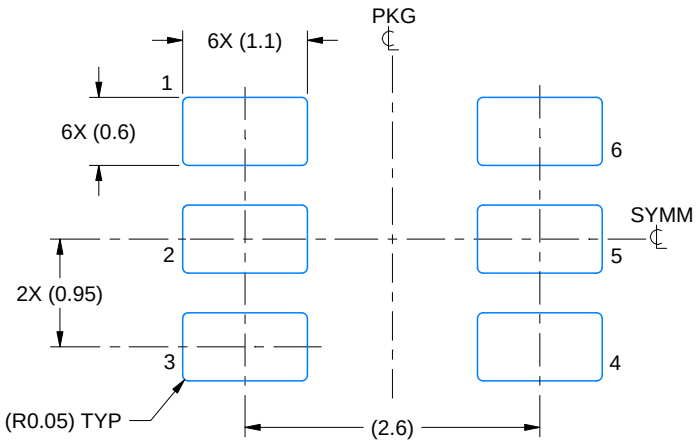
SMALL OUTLINE TRANSISTOR



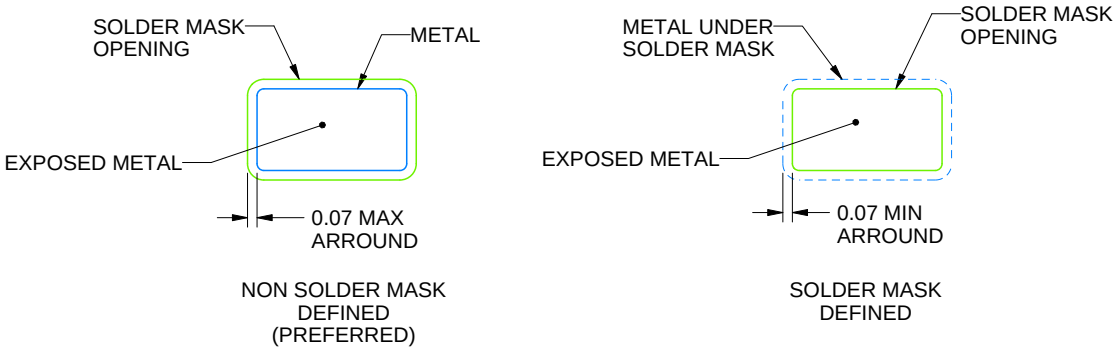
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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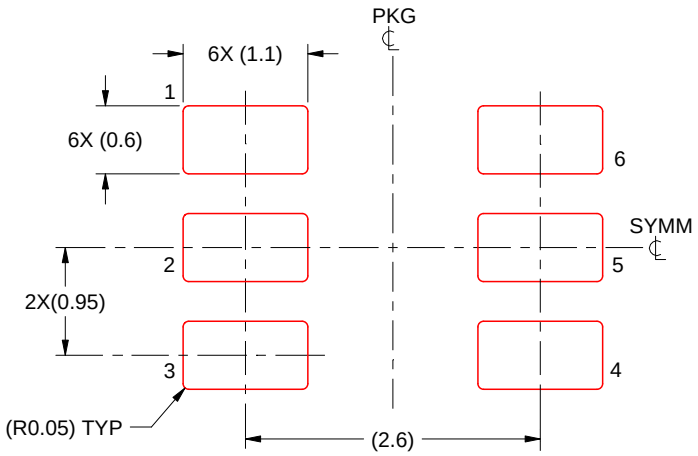
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

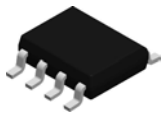


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

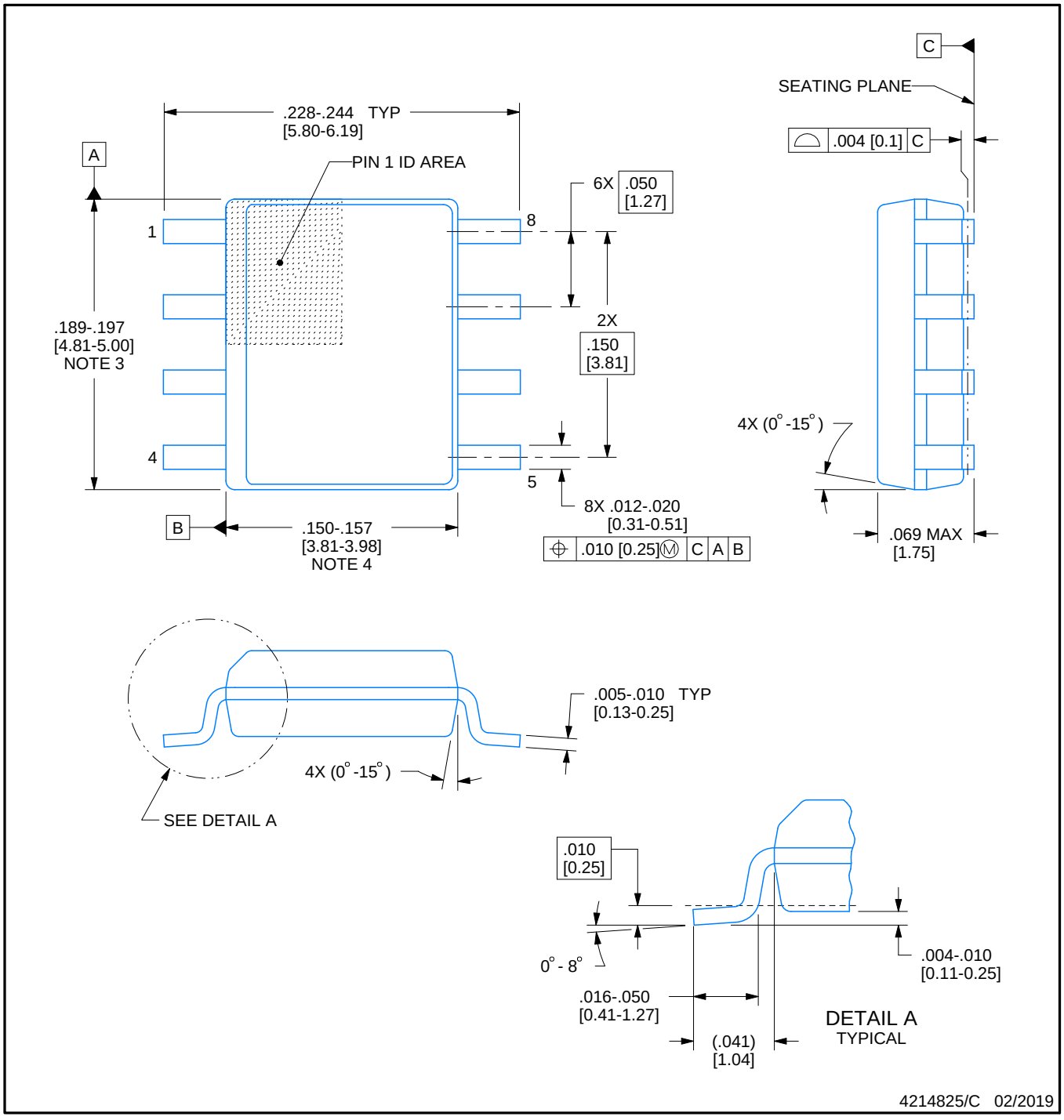


PACKAGE OUTLINE

D0008A

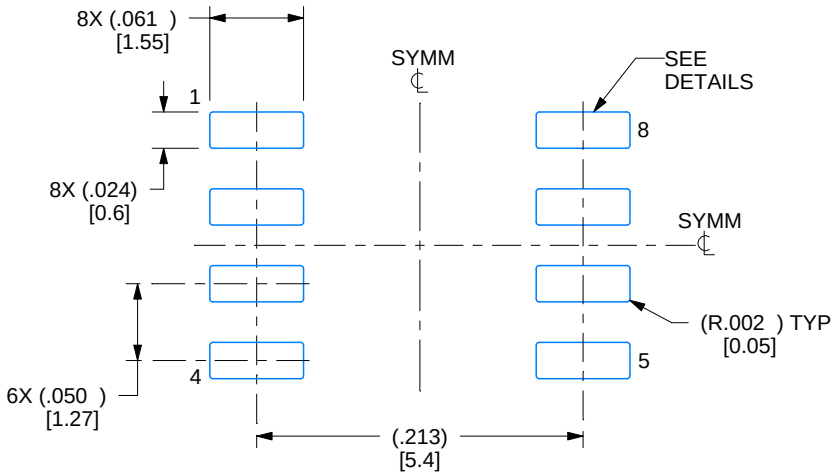
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

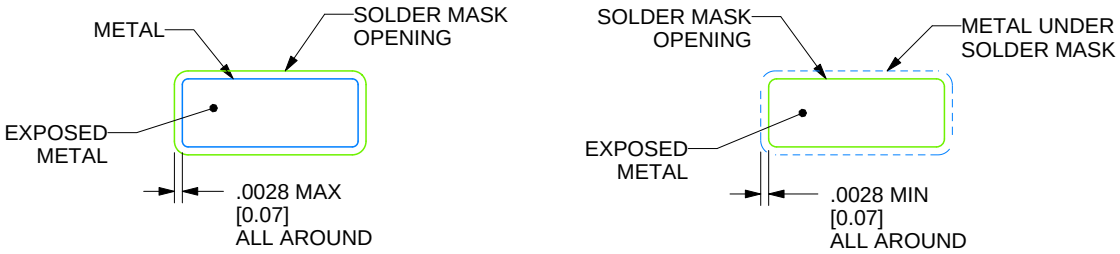


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

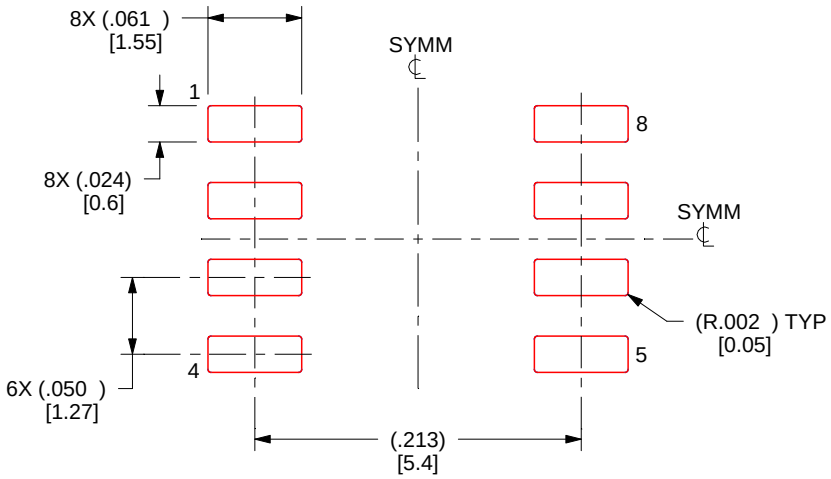
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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