Dual, 12-Bit, Parallel Input, Multiplying Digital-to-Analog Converter

FEATURES

- **±1LSB INL**
- **2.5V to 5.5V Supply Operation**
- **Fast Parallel Interface: 17ns Write Cycle**
- **Update Rate of 20.4MSPS**
- **10MHz Multiplying Bandwidth**
- **±15V Reference Input**
- **Extended Temperature Range: –40°C to +125°C**
- **40-Lead QFN**
- **12-Bit Monotonic**
- **4-Quadrant Multiplication**
- **Power-On Reset with Brownout Detection**
- **Readback Function**
- **Industry-Standard Pin Configuration**
- **Pin-Compatible with the AD5405**

APPLICATIONS

- **Portable Battery-Powered Instruments**
- **Waveform Generators**
- **Analog Processing**
- **Programmable Amplifiers and Attenuators**
- **Digitally-Controlled Calibration**
- **Programmable Filters and Oscillators**
- **Ultrasound**

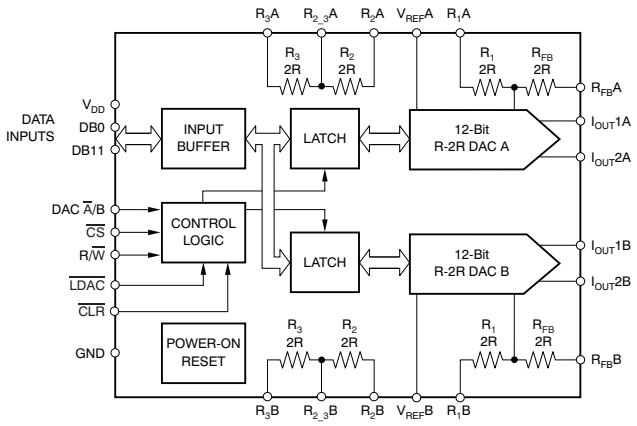
DESCRIPTION

The DAC7822 is a dual, CMOS, 12-bit, current output digital-to-analog converter (DAC). This device operates from a 2.5V to 5.5V power supply, making it suitable for battery-powered and many other applications.

The DAC7822 operates with a fast parallel interface. Data readback allows the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeroes and the DAC outputs are at zero scale.

The DAC7822 offers excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidth of 10MHz. The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier. The DAC7822 also includes the resistors necessary for 4-quadrant multiplication and other configuration modes.

The DAC7822 is available in a 40-lead QFN package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	DAC7822	UNIT
V_{DD} to GND	–0.3 to +7.0	V
Digital input voltage to GND	–0.3 to V_{DD} + 0.3	V
V_{OUT} to GND	–0.3 to V_{DD} + 0.3	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature (T_J max)	+150	°C
ESD Rating, HBM	2000	V
ESD Rating, CDM	1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

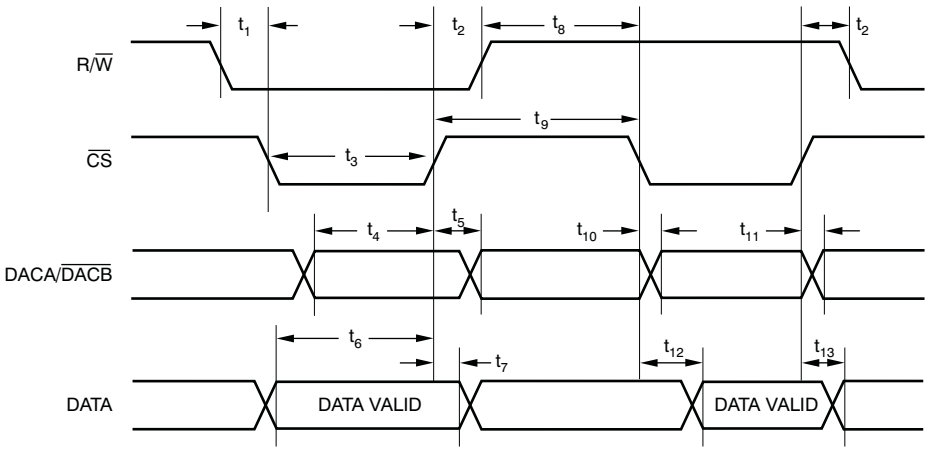
ELECTRICAL CHARACTERISTICS

V_{DD} = +2.5V to +5.5V; $I_{OUT}1$ = Virtual GND; $I_{OUT}2$ = 0V; V_{REF} = 10V; T_A = full operating temperature. All specifications –40°C to +125°C, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7822 MIN	DAC7822 TYP	DAC7822 MAX	UNITS
STATIC PERFORMANCE					
Resolution		12			Bits
Relative accuracy				±1	LSB
Differential nonlinearity				±1	LSB
Output leakage current	Data = 000h, T_A = +25°C			±1	nA
Output leakage current	Data = 000h, $T_A = T_{MAX}$			±15	nA
Full-scale gain error	All ones loaded to DAC register		±10	±25	mV
Full-scale tempco(1)			±5		ppm/°C
Bipolar zero-code error	Circuit configuration as shown in Figure 41			±25	mV
Output capacitance	DAC latches leaded with all 1s		25	30	pF
REFERENCE INPUT					
V_{REF} range		–15		15	V
$V_{REF}A$, $V_{REF}B$, Input resistance		8	10	12	kΩ
R_1, R_{FB} resistance		17	20	25	kΩ
R_2, R_3 resistance		17	20	25	kΩ
$V_{REF}A$ to $V_{REF}B$ Input Mismatch			1.6	2.5	%
R_2 to R_3 Mismatch			0.06	0.18	%
LOGIC INPUTS AND OUTPUT(1)					
Input low voltage V_{IL}	V_{DD} = +2.5V			0.6	V
	V_{DD} = +5V			0.8	V
Input high voltage V_{IH}	V_{DD} = +2.5V	2.1			V
	V_{DD} = +5V	2.4			V
Input leakage current I_{IL}				1	µA
Input capacitance C_{IL}				10	pF
POWER REQUIREMENTS					
V_{DD}		2.5		5.5	V
I_{DD} (normal operation)	Logic inputs = 0V			5	µA
V_{DD} = +4.5V to +5.5V	$V_{IH} = V_{DD}$ and V_{IL} = GND		0.8	5	µA
V_{DD} = +2.5V to +3.6V	$V_{IH} = V_{DD}$ and V_{IL} = GND		0.4	2.5	µA
AC CHARACTERISTICS(1)					
Output voltage settling time				0.2	µs
Reference multiplying BW	V_{REF} = 7V_{PP}, Data = FFFh		10		MHz
DAC glitch impulse	V_{REF} = 0V to 10V, Data = 7FFh to 800h to 7FFh		10		nV-s
Feedthrough error V_{OUT}/V_{REF}	Data = 000h, V_{REF} = 100kHz		–70		dB
Digital feedthrough			2		nV-s
Total harmonic distortion			–105		dB
Output spot noise voltage			25		nV/√Hz

(1) Specified by design and characterization; not production tested.

TIMING INFORMATION



TIMING REQUIREMENTS: 2.5V to 5.5V

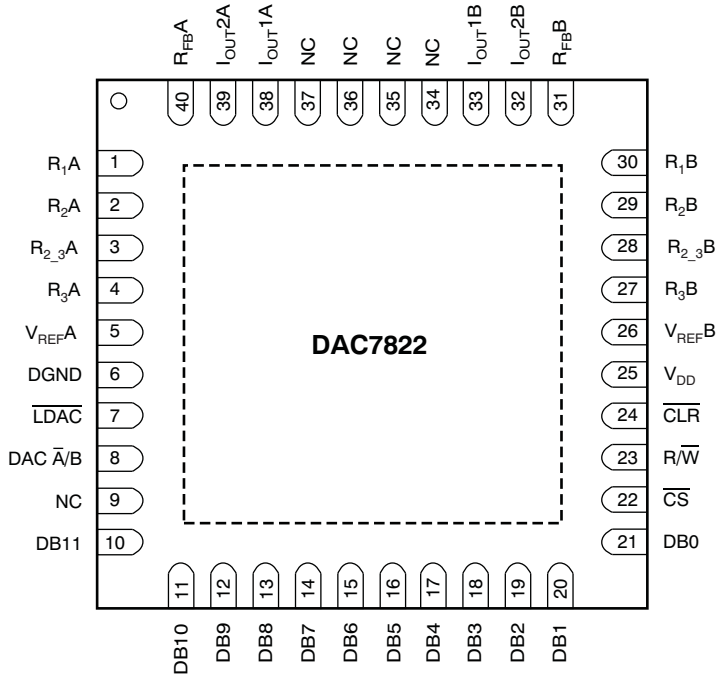
At $t_r = t_f$ = 1ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; V_{DD} = 2.5V to 5.5V, V_{REF} = 10V, $I_{OUT}2$ = 0V. All specifications –40°C to +125°C, unless otherwise noted.

PARAMETER[1]	TEST CONDITIONS	DAC7822			UNIT
		MIN	TYP	MAX	
t_1	R/$\overline{W}$ to $\overline{CS}$ setup time	0			ns
t_2	R/$\overline{W}$ to $\overline{CS}$ hold time	0			ns
t_3	$\overline{CS}$ low time (write cycle)	10			ns
t_4	Address setup time	10			ns
t_5	Address hold time	0			ns
t_6	Data setup time	6			ns
t_7	Data hold time	0			ns
t_8	R/$\overline{W}$ high to $\overline{CS}$ low	5			ns
t_9	$\overline{CS}$ minimum high time	7			ns
t_{10}	Address setup time (Read Cycle)	0			ns
t_{11}	Address hold time (Read Cycle)	0			ns
t_{12}	Data access time		5	35	ns
t_{13}	Bus relinquish time		5	10	ns

(1) Ensured by design; not production tested.

DEVICE INFORMATION

RTA PACKAGE
QFN-40
(TOP VIEW)



TERMINAL FUNCTIONS

PIN NO.	PIN NAME	DESCRIPTION
1-4	R_1A, R_2A, $R_{2\_3}A$, R_3A	DAC A 4-Quadrant Resistors. Allows a number of configuration modes, including bipolar operation with minimum of external components.
5, 26	$V_{REF}A$, $V_{REF}B$	DAC Reference Voltage Input Terminals.
6	DGND	Digital Ground Pin.
7	$\overline{LDAC}$	Load DAC Input. Allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected whereby the DAC is updated on the rising edge of $\overline{CS}$.
8	DAC $\overline{A}$/B	Selects DAC A or B. Low selects DAC A, and high selects DAC B.
9, 34-37	NC	Not internally connected.
10-21	DB11 to DB0	Parallel Data Bits 11 through 0.
22	$\overline{CS}$	Chip Select Input; active low. Used in conjuction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Edge sensitive; when pulled high, the DAC data is latched.
23	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, used in conjunction with $\overline{CS}$ to read back contents of DAC register.
24	$\overline{CLR}$	Active Low Control Input. Clears DAC output and input and DAC registers.
25	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5V to 5.5V.
27-30	R_3B, $R_{2\_3}B$, R_2B, R_1B	DAC B 4-Quadrant Resistors. Allow a number of configuration modes, including bipolar operation with a minimum of external components.
31, 40	$R_{FB}B$, $R_{FB}A$	External Amplifier Output.
32	$I_{OUT}2B$	DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation.
33	$I_{OUT}1B$	DAC B Current Output.
38	$I_{OUT}1A$	DAC A Current Output.
39	$I_{OUT}2A$	DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation.

TYPICAL CHARACTERISTICS: V_{DD} = +5V

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

Channel A

LINEARITY ERROR vs DIGITAL INPUT CODE

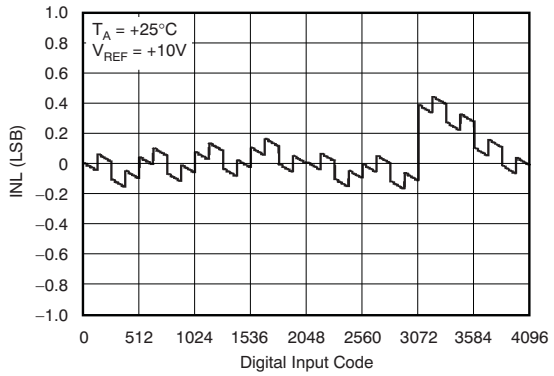


Figure 1.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

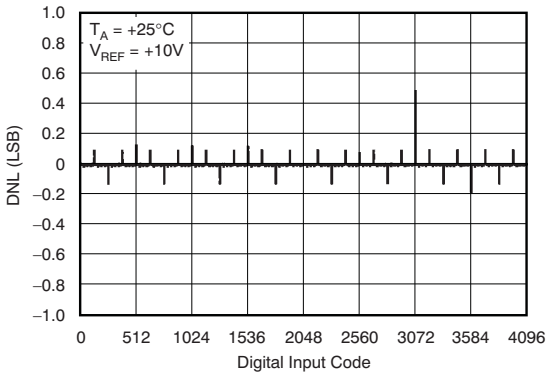


Figure 2.

LINEARITY ERROR vs DIGITAL INPUT CODE

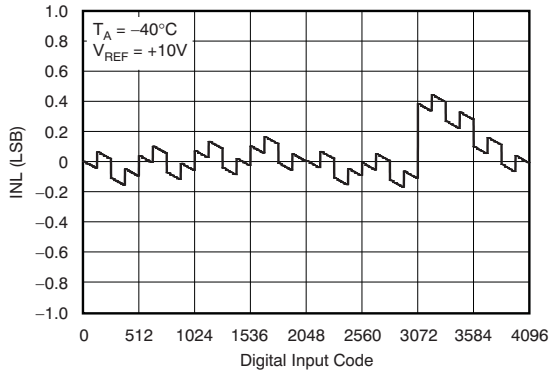


Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

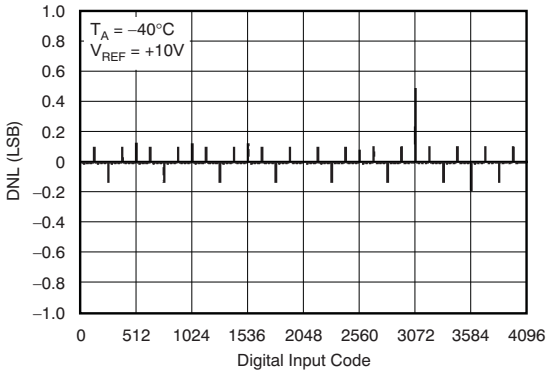


Figure 4.

LINEARITY ERROR vs DIGITAL INPUT CODE

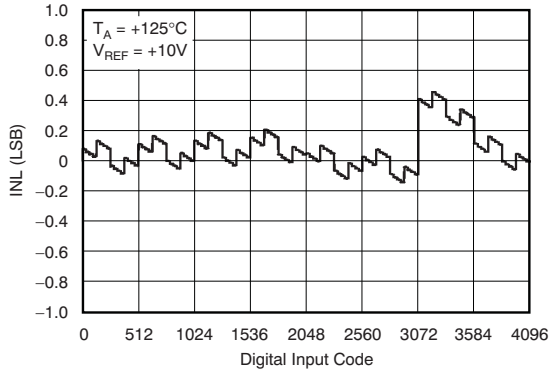


Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

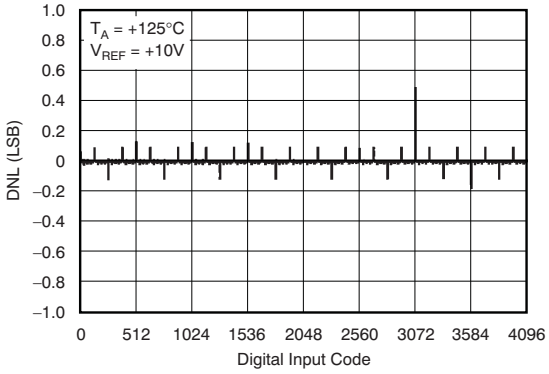


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

Channel B

LINEARITY ERROR vs DIGITAL INPUT CODE

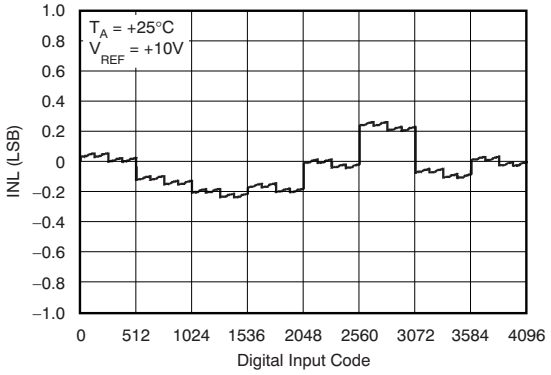


Figure 7.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

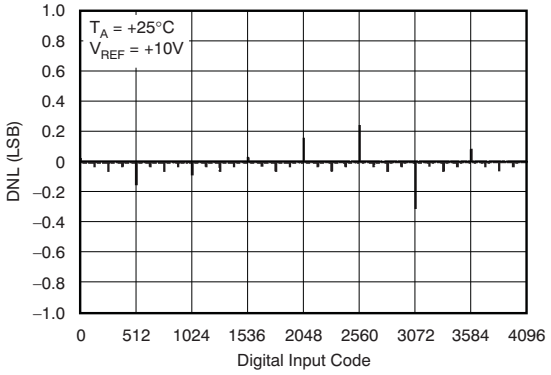


Figure 8.

LINEARITY ERROR vs DIGITAL INPUT CODE

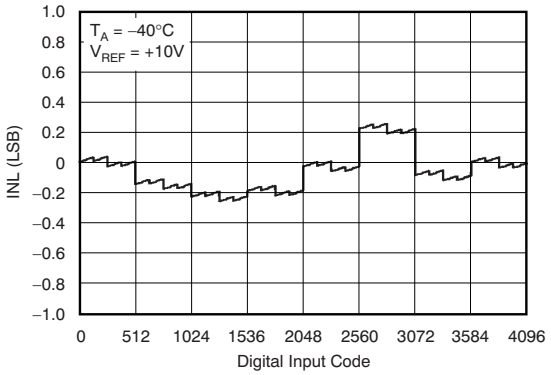


Figure 9.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

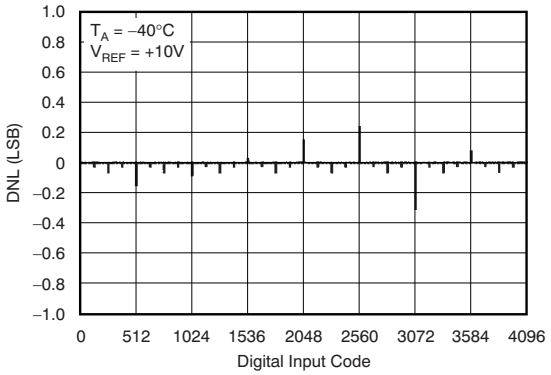


Figure 10.

LINEARITY ERROR vs DIGITAL INPUT CODE

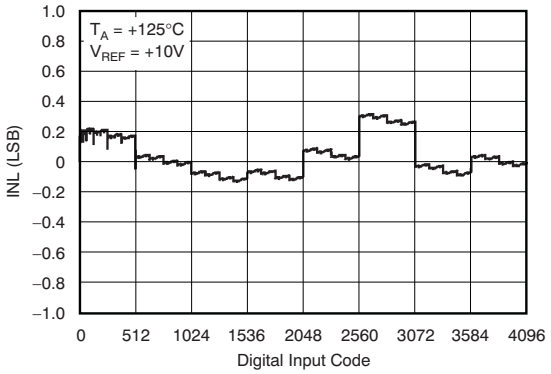


Figure 11.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

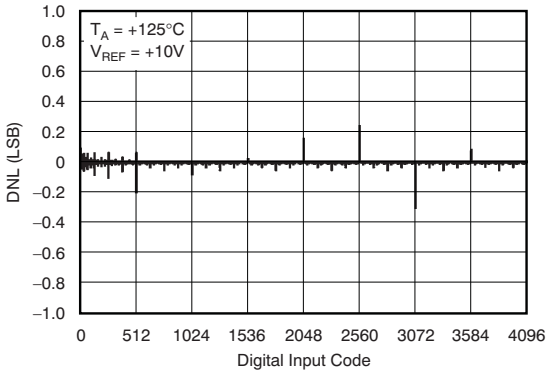


Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

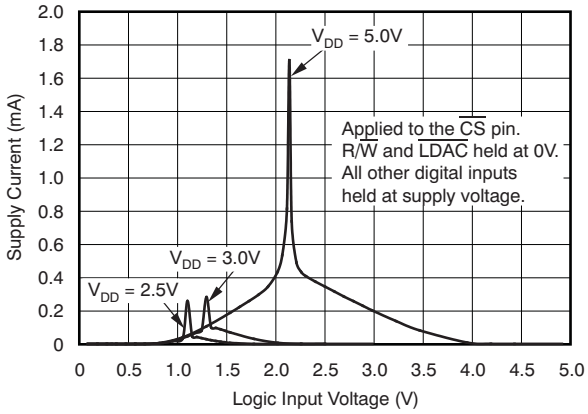


Figure 13.

REFERENCE MULTIPLYING BANDWIDTH

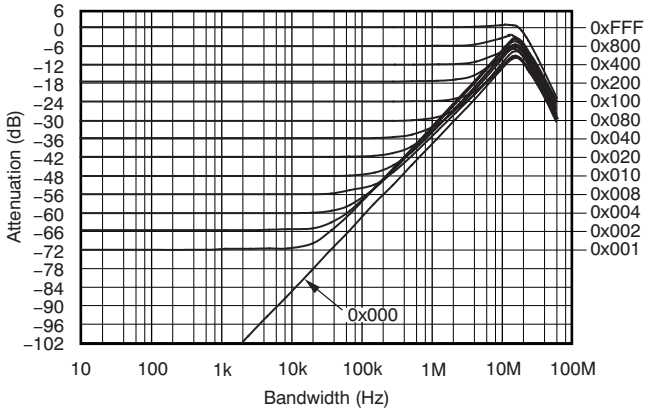


Figure 14.

MIDSCALE DAC GLITCH

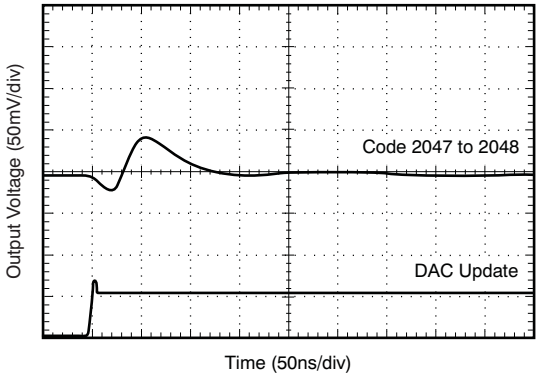


Figure 15.

MIDSCALE DAC GLITCH

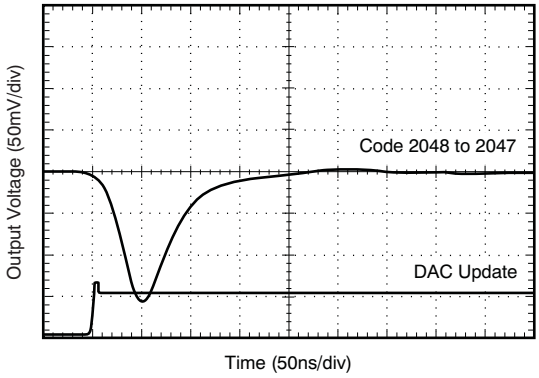


Figure 16.

DAC SETTLING TIME

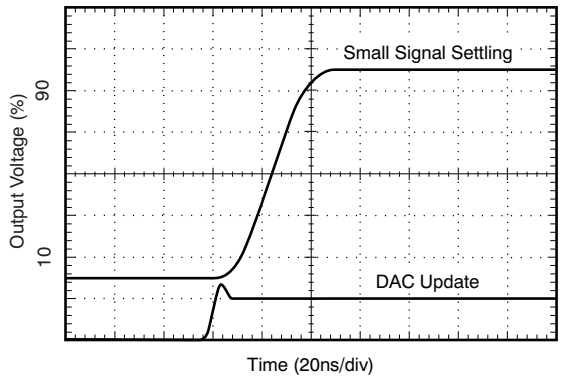


Figure 17.

GAIN ERROR vs TEMPERATURE

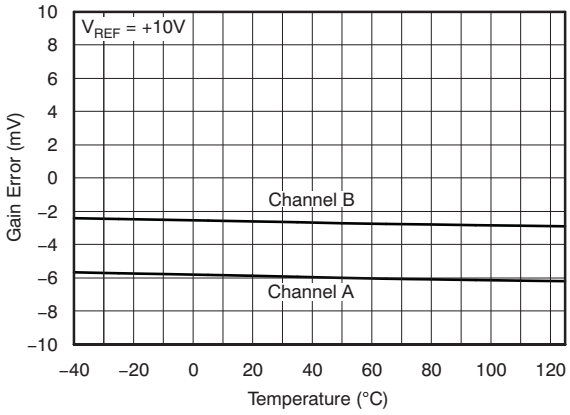


Figure 18.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

SUPPLY CURRENT vs TEMPERATURE

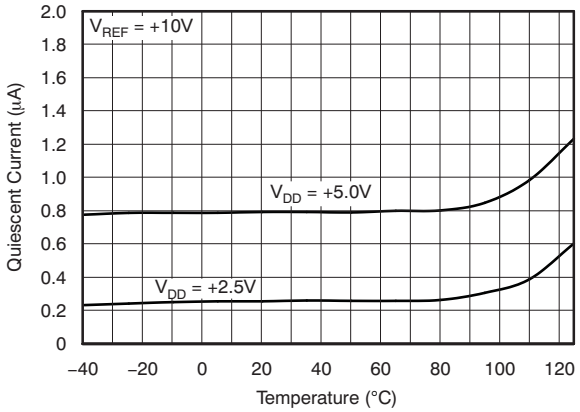


Figure 19.

OUTPUT LEAKAGE vs TEMPERATURE

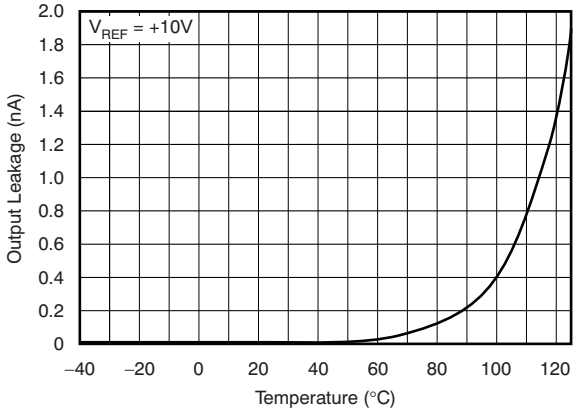


Figure 20.

TYPICAL CHARACTERISTICS: V_{DD} = +2.5V

At T_A = +25°C, $+V_{DD}$ = +2.5V, unless otherwise noted.

Channel A

LINEARITY ERROR vs DIGITAL INPUT CODE

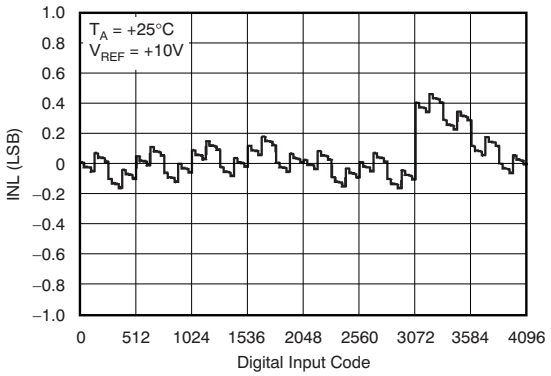


Figure 21.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

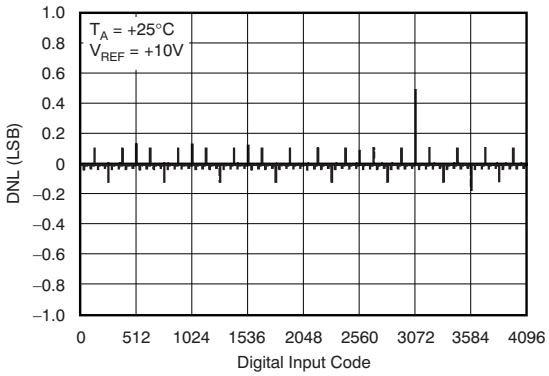


Figure 22.

LINEARITY ERROR vs DIGITAL INPUT CODE

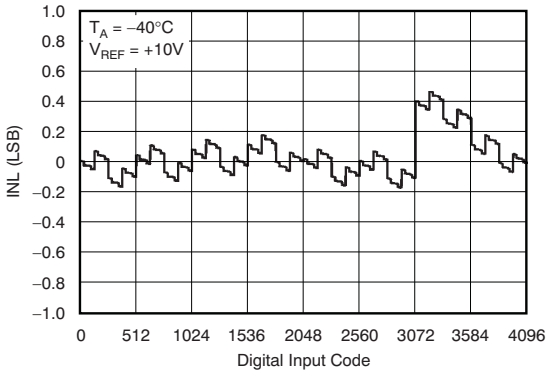


Figure 23.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

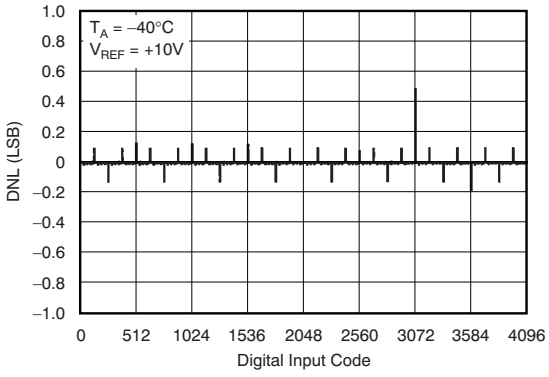


Figure 24.

LINEARITY ERROR vs DIGITAL INPUT CODE

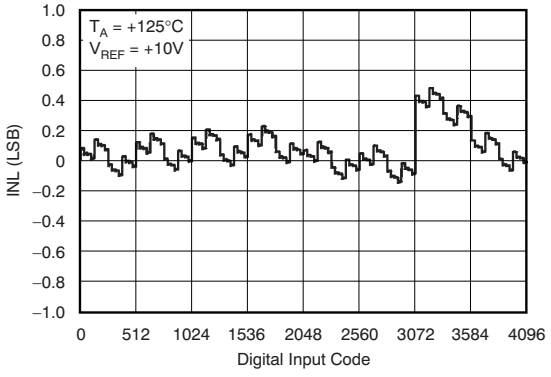


Figure 25.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

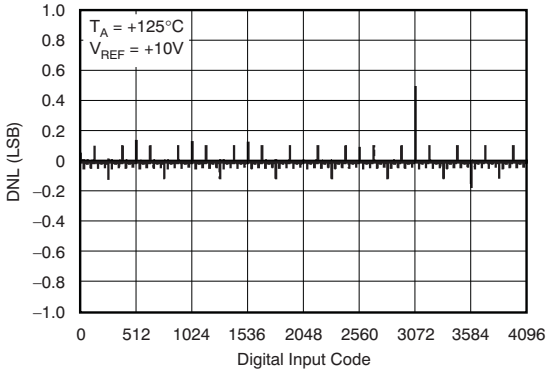


Figure 26.

TYPICAL CHARACTERISTICS: V_{DD} = +2.5V (continued)

At T_A = +25°C, +V_{DD} = +2.5V, unless otherwise noted.

Channel B

LINEARITY ERROR vs DIGITAL INPUT CODE

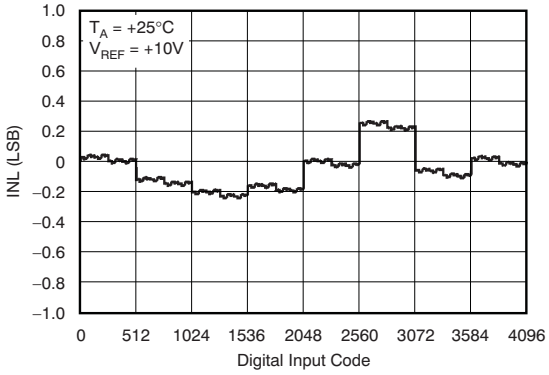


Figure 27.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

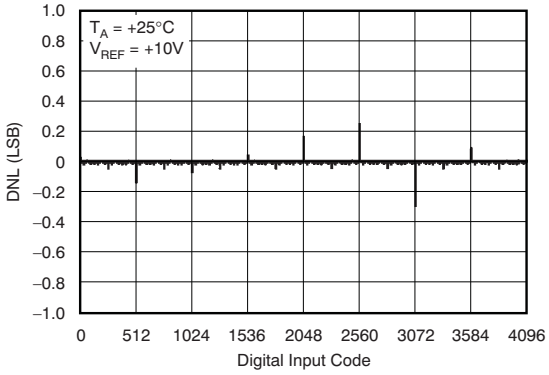


Figure 28.

LINEARITY ERROR vs DIGITAL INPUT CODE

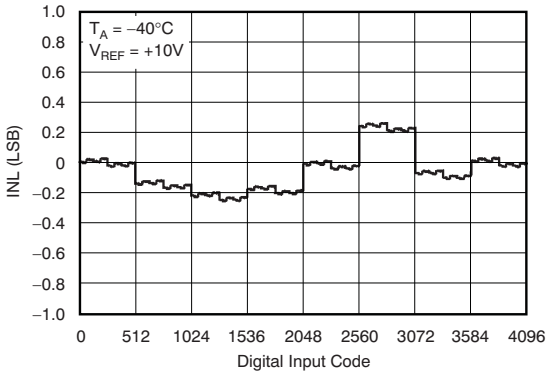


Figure 29.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

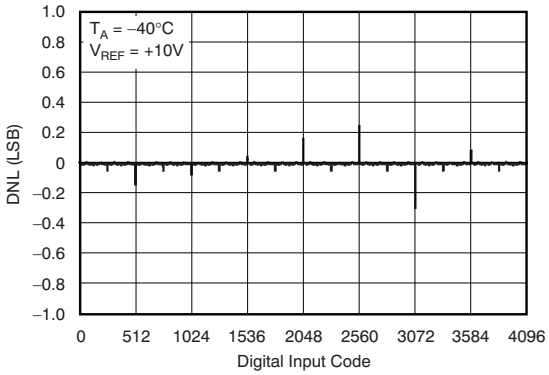


Figure 30.

LINEARITY ERROR vs DIGITAL INPUT CODE

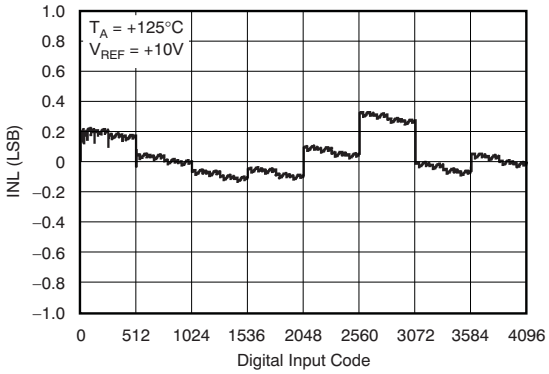


Figure 31.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

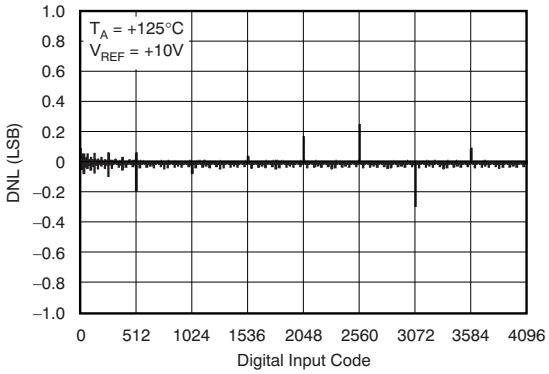


Figure 32.

TYPICAL CHARACTERISTICS: V_{DD} = +2.5V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.5V, unless otherwise noted.

MIDSCALE DAC GLITCH

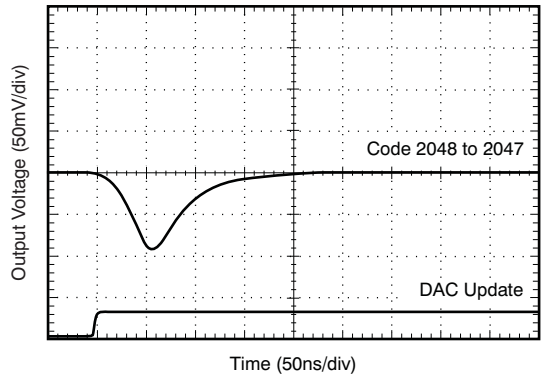


Figure 33.

MIDSCALE DAC GLITCH

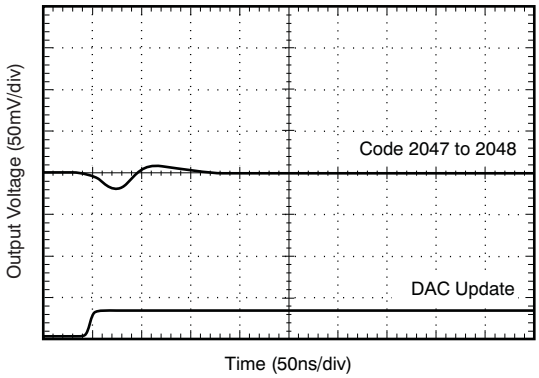


Figure 34.

GAIN ERROR vs TEMPERATURE

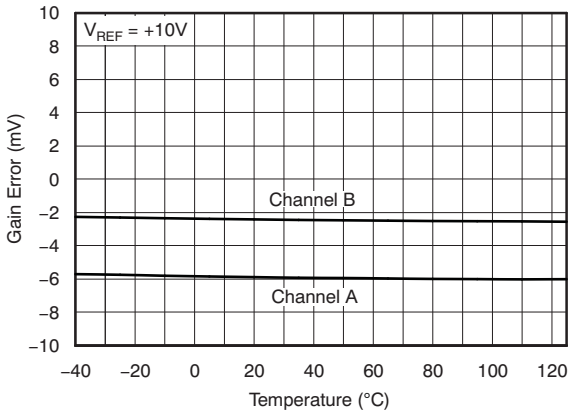


Figure 35.

OUTPUT LEAKAGE vs TEMPERATURE

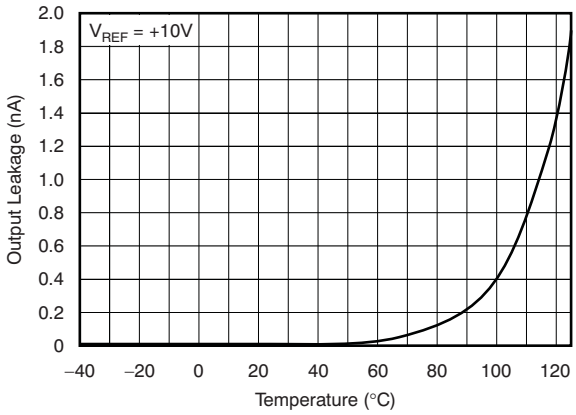


Figure 36.

THEORY OF OPERATION

The DAC7822 is a dual channel, current output, 12-bit, digital-to-analog converter (DAC). The architecture, illustrated in Figure 37, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to $I_{OUT}1$ or the $I_{OUT}2$ terminal. The $I_{OUT}1$ terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V_{REF} that determines the DAC full-scale current. The R-2R ladder presents a code-independent load impedance to the external reference of 10kΩ ±20%. The external reference voltage can vary over a range of –15V to +15V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter and the DAC7822 R_{FB} resistor, output voltage ranges of $–V_{REF}$ to V_{REF} can be generated.

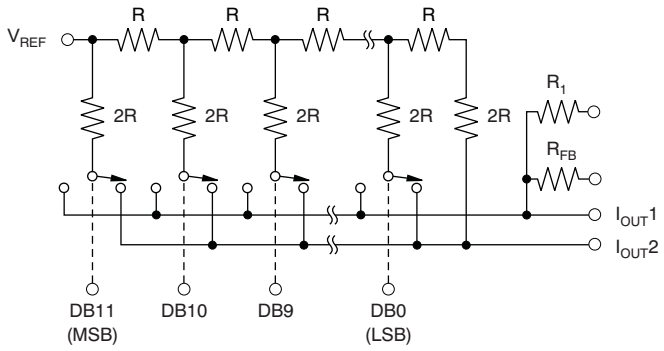


Figure 37. Equivalent R-2R DAC Circuit

When using an external I/V converter and the DAC7822 R_{FB} and R_1 resistors, the DAC output voltage is given by Equation 1:

$$V_{OUT} = - V_{REF} \times \frac{CODE}{4096} \quad (1)$$

Each DAC code determines the 2R leg switch position to either GND or I_{OUT}. Because the DAC output impedance as seen looking into the $I_{OUT}1$ terminal changes versus code, the external I/V converter noise gain also changes. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC $I_{OUT}1$ terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC7822 as a result of offset modulation versus DAC code.

For best linearity performance of the DAC7822, a low input offset voltage op amp (such as the OPA277) is recommended (see Figure 38). This circuit allows V_{REF} swinging from –10V to +10V.

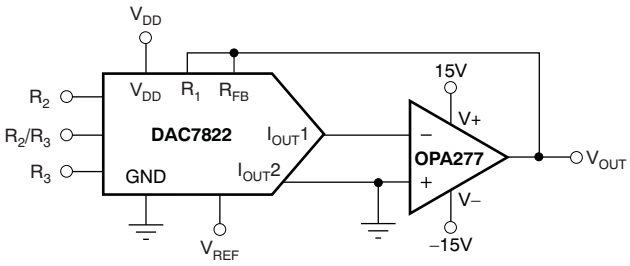


Figure 38. Voltage Output Configuration

APPLICATION INFORMATION

Stability Circuit

For a current-to-voltage design (see Figure 39), the DAC7822 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct printed circuit board (PCB) layout design practices. For each code change, there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C_1 (1pF to 5pF typ) can be added to the design, as shown in Figure 39.

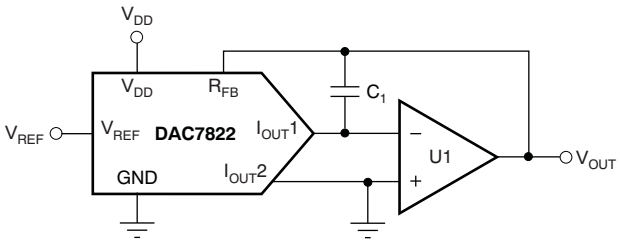


Figure 39. Gain Peaking Prevention Circuit with Compensation Capacitor

Amplifier Selection

There are many choices and many differences in selecting the proper operational amplifier for a multiplying DAC (MDAC). Making the analog signal out of the MDAC is one critical aspect. However, there are also other issues to take into account such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy. Table 1 and Table 2 suggest some suitable operational amplifiers for low power, fast settling, and high-speed applications. A greater selection of operational amplifiers can be found at www.ti.com/amplifer.

Table 1. Suitable Precision Operational Amplifiers from Texas Instruments

PRODUCT	TOTAL SUPPLY VOLTAGE (V) (min)	TOTAL SUPPLY VOLTAGE (V) (max)	I_Q PER CHANNEL (max) (mA)	GBW (typ) (MHz)	SLEW RATE (typ) (V/µs)	OFFSET DRIFT (typ) (µV/°C)	I_{IB} (max) (pA)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
Low Power										
OPA703	4	12	0.2	1	0.6	4	10	70	SOT5-23, PDIP-8, SOIC-8	12V, CMOS, Rail-to-Rail I/O, Operational Amplifier
OPA735	2.7	12	0.75	1.6	1.5	0.01	200	115	SOT5-23, SOIC-8	0.05µV/°C (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier
OPA344	2.7	5.5	0.25	1	1	2.5	10	80	SOT5-23, PDIP-8, SOIC-8	Low Power, Single-Supply, Rail-To-Rail Operational Amplifiers MicroAmplifier Series
OPA348	2.1	5.5	0.065	1	0.5	2	10	70	SC5-70, SOT5-23, SOIC-8	1MHz, 45µA, Rail-to-Rail I/O, Single Op Amp
OPA277	4	36	0.825	1	0.8	0.1	1000	130	PDIP-8, SOIC-8, SON-8	High Precision Operational Amplifiers
Fast Settling										
OPA350	2.7	5.5	7.5	38	22	4	10	76	MSOP-8, PDIP-8, SOIC-8	High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series
OPA727	4	12	6.5	20	30	0.6	500	86	MSOP-8, SON-8	e-trim 20MHz, High Precision CMOS Operational Amplifier
OPA227	5	36	3.8	8	2.3	0.1	10000	120	PDIP-8, SOIC-8	High Precision, Low Noise Operational Amplifiers

Table 2. Suitable High Speed Operational Amplifiers from Texas Instruments (Multiple Channel Options)

PRODUCT	SUPPLY VOLTAGE (V)	GBW PRODUCT (MHz)	VOLTAGE NOISE nV/√Hz	GBW (typ) (MHz)	SLEW RATE (V/µs)	V_{OS} (typ) (µV)	V_{OS} (max) (µV)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
Single Channel										
THS4281	±2.7 to ±15	38	12.5	35	500	3500	500	1000	SOT5-23, MSOP-8, SOIC-8	Very Low-Power High Speed Rail-To-Rail Input/Output Voltage Feedback Operational Amplifier
THS4031	±4.5 to ±16.5	200	1.6	100	500	3000	3000	8000	CDIP-8, MSOP-8, SOIC-8	100-MHz Low Noise Voltage-Feedback Amplifier
THS4631	±4.5 to ±16.5	210	7	900	260	2000	50pA	2	SOIC-8, MSOP-8	High Speed FET-Input Operational Amplifier
OPA656	±4 to ±6	230	7	290	250	2600	2pA	5pA	SOIC-8, SOT5-23	Wideband, Unity Gain Stable FET-Input Operational Amplifier
OPA820	±2.5 to ±6	280	2.5	240	200	1200	900	23,000	SOIC-8, SOT5-23	Unity Gain Stable, Low Noise, Voltage Feedback Operational Amplifier
Dual Channel										
THS4032	±4.5 to ±16.5	200	1.6	100	500	3000	3000	8000	SOIC-8, MSOP-8	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
OPA2822	±2 to ±6.3	220	2	170	200	1200	9600	12000	SOIC-8, MSOP-8	SpeedPlus Dual Wideband, Low-Noise Operational Amplifier

Positive Voltage Output Circuit

As Figure 40 illustrates, in order to generate a positive voltage output, a negative reference is input to the DAC7822. This design is suggested instead of using an inverting amp to invert the output as a result of resistor tolerance errors. For a negative reference, V_{OUT} and GND of the reference are level-shifted to a virtual ground and a –2.5V input to the DAC7822 with an op amp.

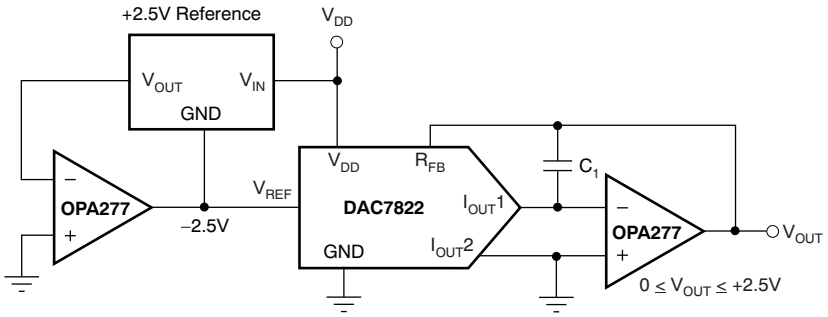


Figure 40. Positive Voltage Output Circuit

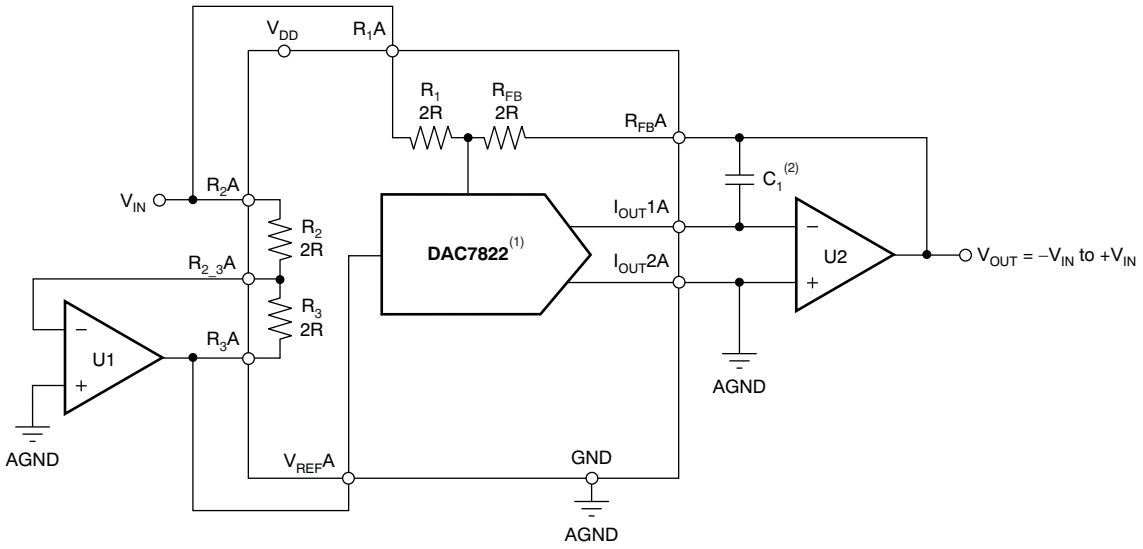
Bipolar Output Section

The DAC7822, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 41, external op amp U2 is added as a summing amp and has a gain of 2X that widens the output span to 5V. A 4-quadrant multiplying circuit is implemented by using a 2.5V offset of the reference voltage to bias U2. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full-scale produce output voltages of V_{OUT} = –2.5V to V_{OUT} = +2.5V.

$$V_{OUT} = \left(\frac{D}{0.5 \times 2^{N}} - 1 \right) \times V_{REF} \quad (2)$$

External resistance mismatching is the significant error in Figure 41.



NOTES: (1) Similar configuration for DAC B.
(2) C_1 phase compensation (1pF to 5pF) may be required if U2 is a high-speed amplifier.

Figure 41. Bipolar Output Circuit

Parallel Interface

Data are loaded to the DAC7822 as a 12-bit parallel word. The bi-directional bus is controlled with $\overline{CS}$ and R/$\overline{W}$, allowing data to be written to or read from the DAC register. To write to the device, $\overline{CS}$ and R/$\overline{W}$ are brought low, and data available on the data lines fills the input register. The rising edge of $\overline{CS}$ latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent; therefore, a write sequence must consist of a falling and rising edge on $\overline{CS}$ in order to ensure that data are loaded to the DAC register and its analog equivalent is reflected on the DAC output.

To read data stored in the device, R/$\overline{W}$ is held high and $\overline{CS}$ is brought low. Data are loaded from the DAC register back to the input register and out onto the data line, where it can be read back to the controller.

Cross-Reference

The DAC7822 has an industry-standard pinout. Table 3 provides the cross-reference information.

Table 3. Cross-Reference

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC7822	±1	±1	–40°C to +125°C	40-Lead QFN	QFN-40	AD5405

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7822IRTAR	ACTIVE	WQFN	RTA	40	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC7822	Samples
DAC7822IRTAT	ACTIVE	WQFN	RTA	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC7822	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

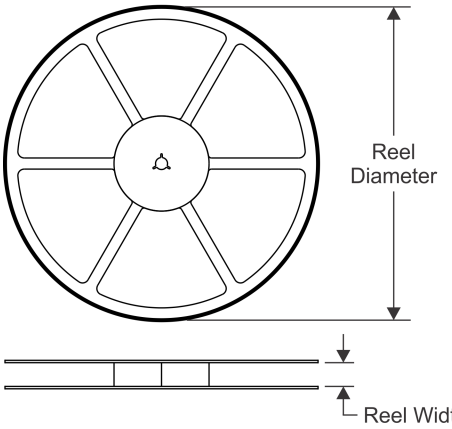
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

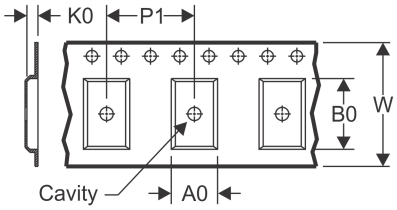
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

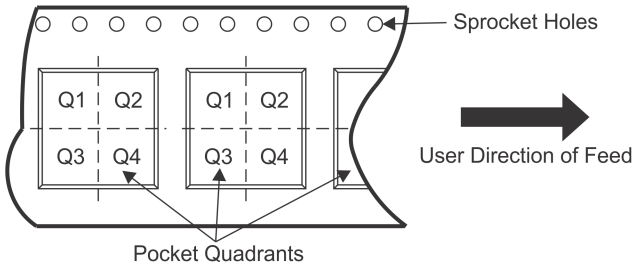


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

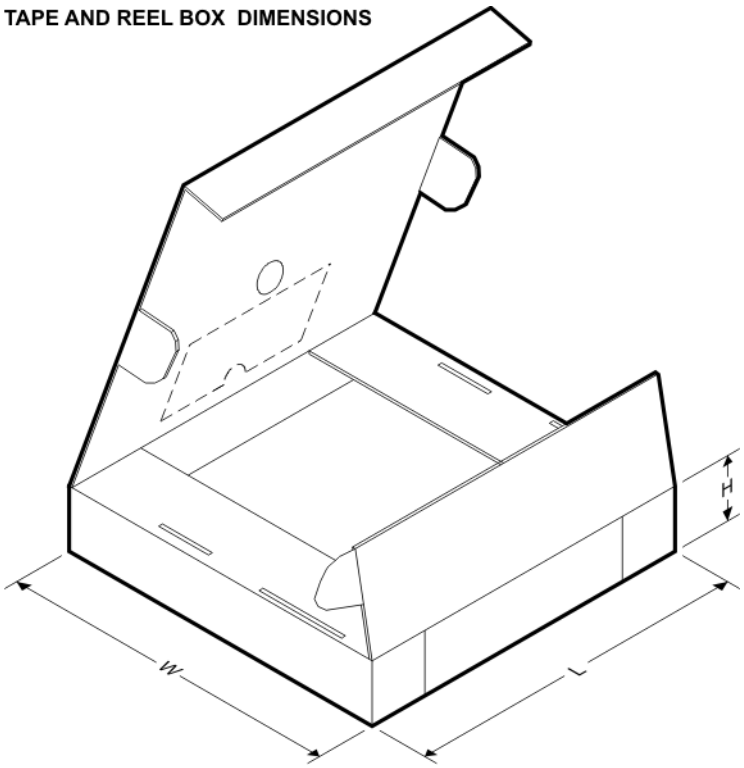
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7822IRTAR	WQFN	RTA	40	2000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

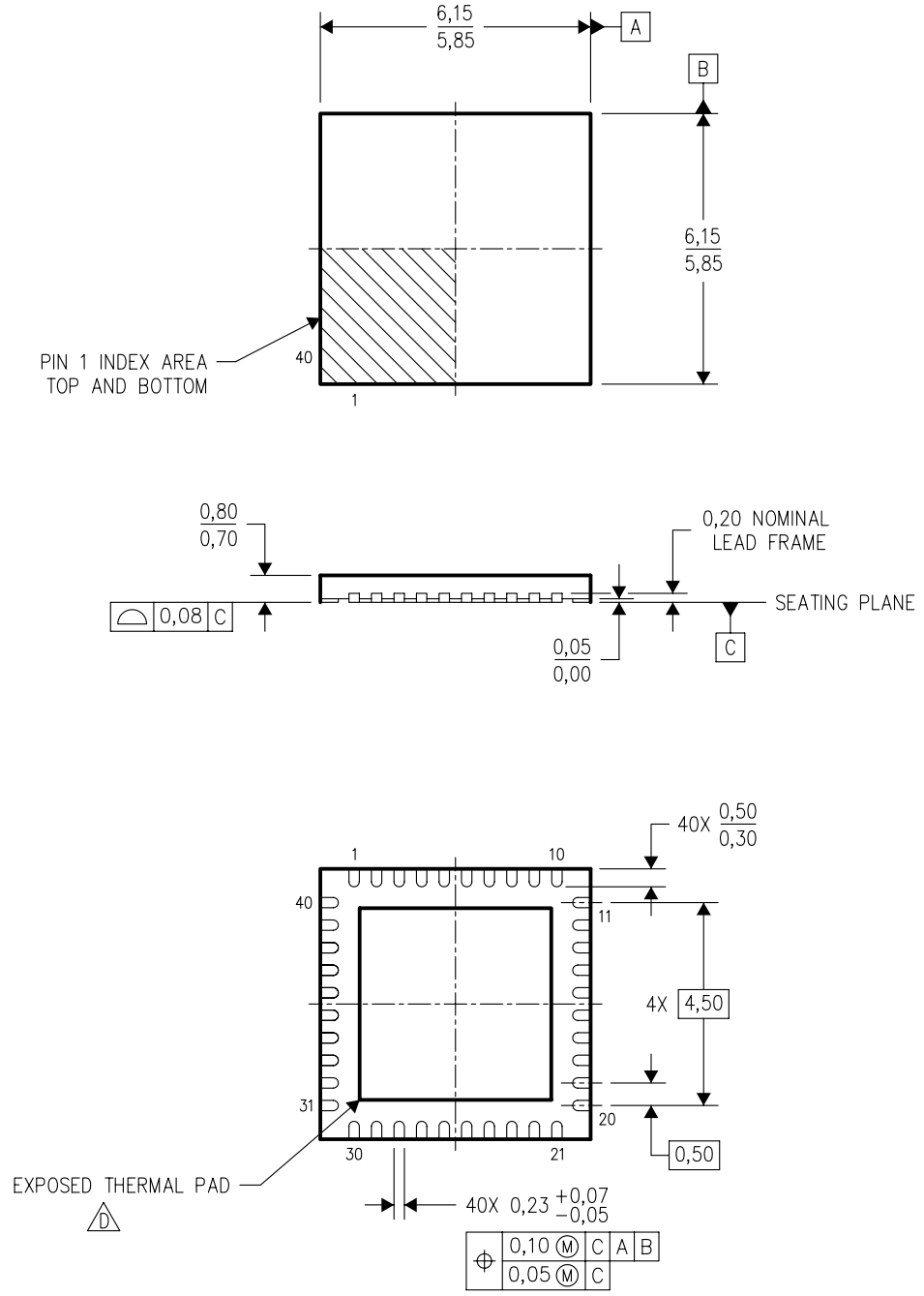
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7822IRTAR	WQFN	RTA	40	2000	350.0	350.0	43.0

RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



4204422/B 11/04

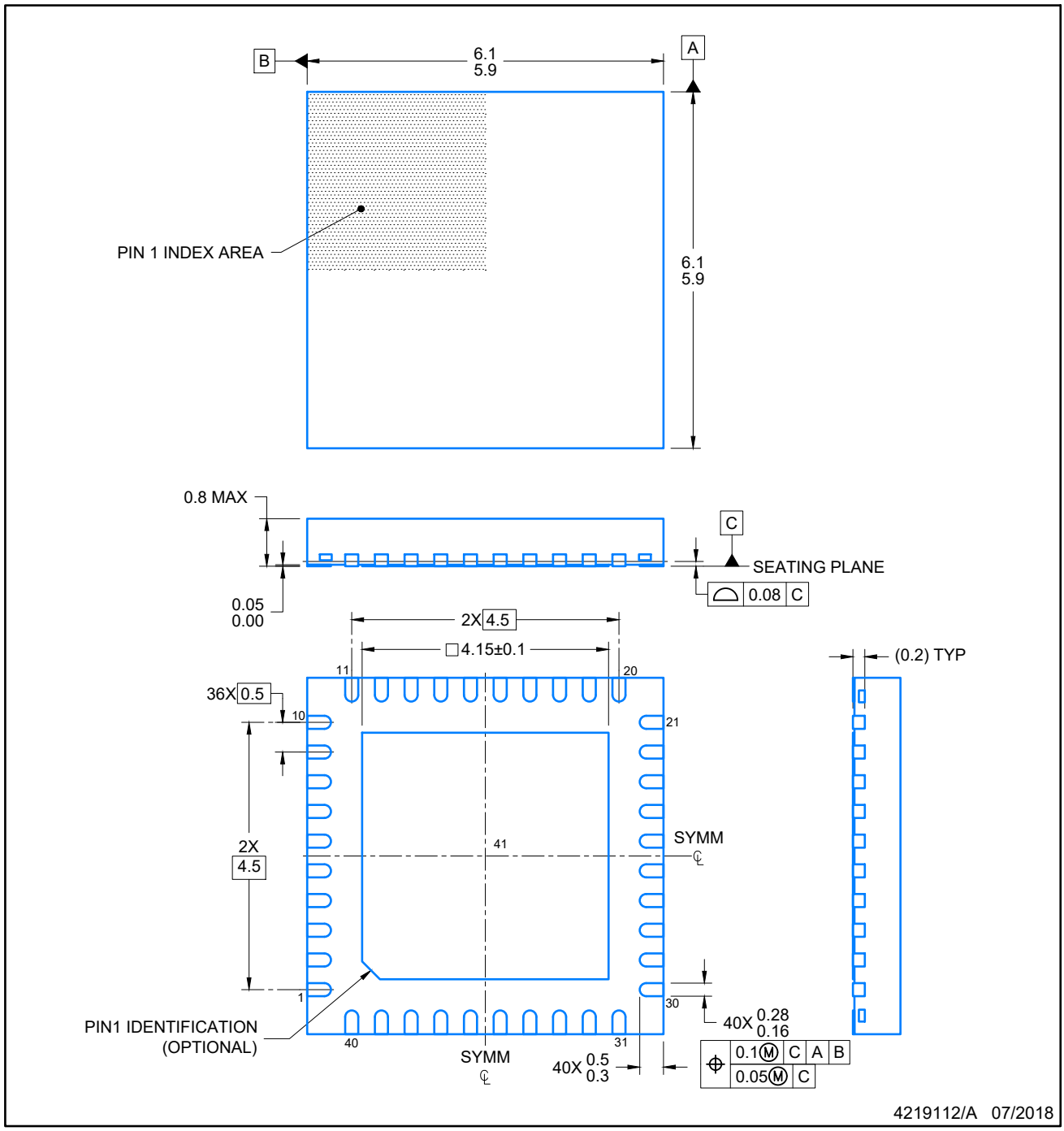
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

PACKAGE OUTLINE

RTA0040B

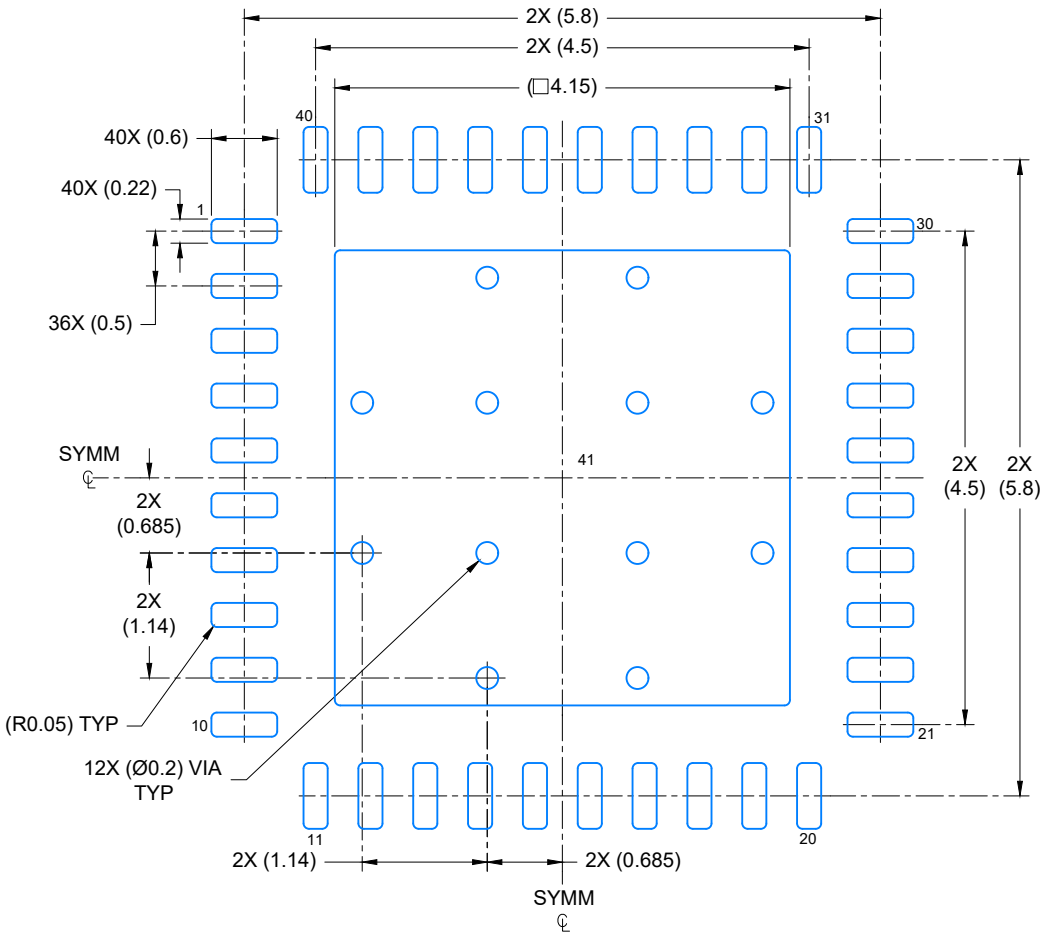
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



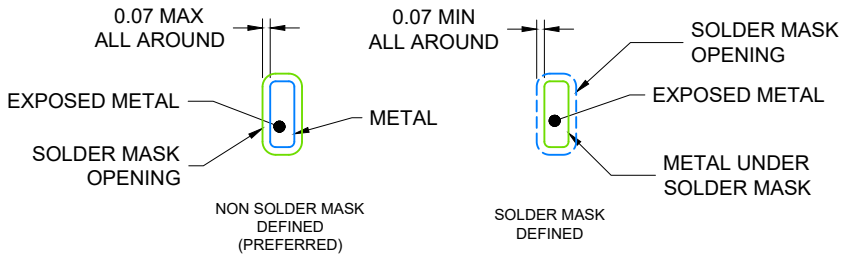
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X



SOLDER MASK DETAILS

4219112/A 07/2018

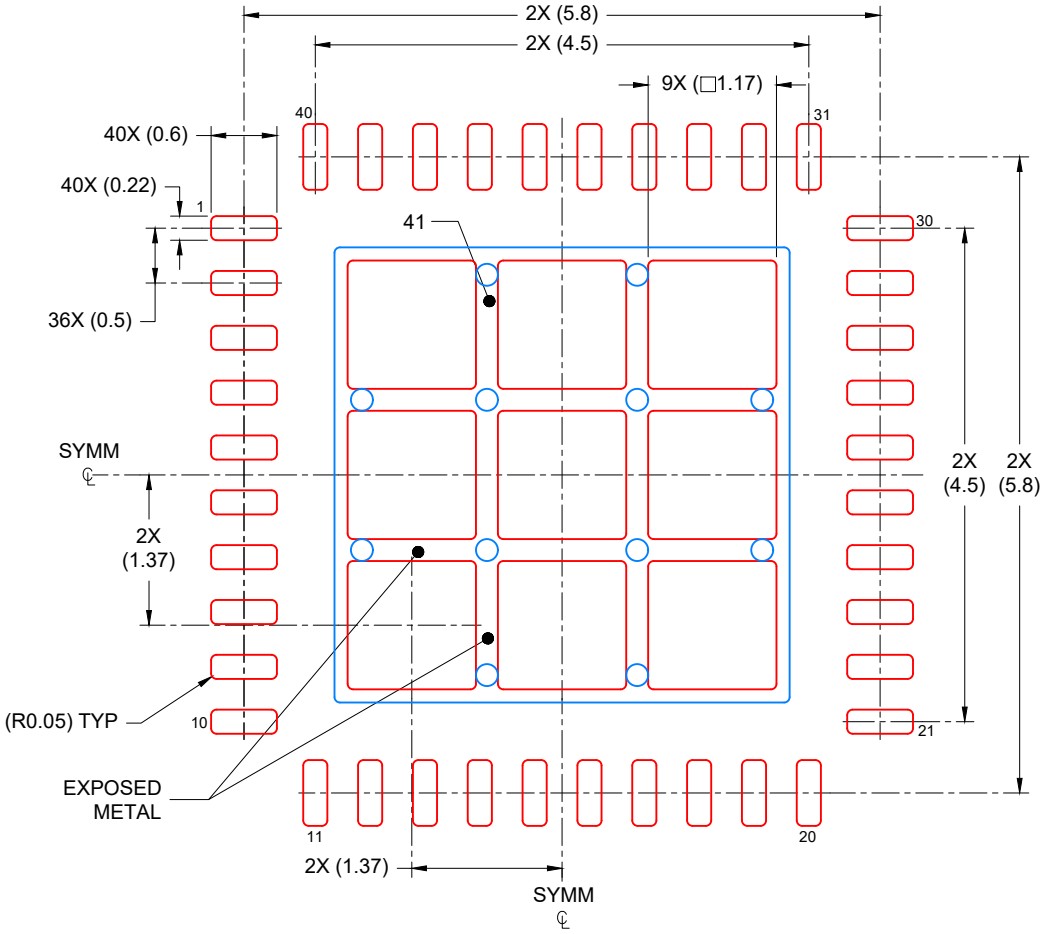
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
71% PRINTED COVERAGE BY AREA
SCALE: 15X

4219112/A 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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