具有超低可闻噪声和待机功率的 UCC25640x LLC 谐振控制器

ADVANCE INFORMATION

1 特性

- 优化的低功耗模式和突发模式算法
  - 具有软启动和软关断周期的突发模式
  - 在空载和待机状态下最大程度降低可闻噪声
  - 用于禁用突发模式的用户选项
  - 光耦合器低功耗运行
  - 效率性能超过 DoE 第 6 级和 EU CoC 第 2 级外部电源标准
- 混合迟滞控制 (HHC)
  - 出色的瞬态响应特性
  - 从突发模式快速退出
- 强大的自适应死区时间控制
- 具有 0.6A 拉电流和 1.2A 灌电流能力的集成高电压栅极驱动器
- 强大的电容区 (ZCS) 规避方案
- 具有过热、输出过压、输入欠压保护以及三级过流保护
- 集成高电压启动功能
- X 电容器主动放电功能

2 应用

- 电视 SMPS 电源
- 照明
- 交流/直流适配器
- 电动工具
- 医疗电源
- 多功能打印机
- 企业和影院投影仪
- PC 电源
- 游戏机电源

3 说明

UCC25640x 是一款具有集成高电压栅极驱动器的全功能 LLC 控制器。此器件设计用于与 PFC 控制器配对使用，以使用最少的外部组件提供完整的电源系统。根据设计，所产生的电源系统无需单独的待机功率转换器即可满足最严格的待机功率要求。

UCC25640x 可提供具有软启动和软关断周期的高效突发模式，以最大限度降低待机运行时的可闻噪声。突发功率电平和迟滞是可编程的，因此能够简化对效率和突发模式运行的优化过程。也可通过引脚配置来禁用突发模式。UCC25640x 使用混合迟滞控制来提供出色的线路和负载瞬态响应特性。

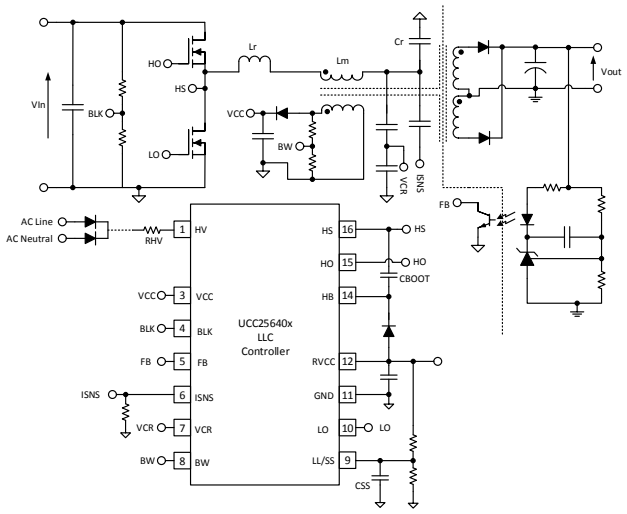
UCC25640x 包括一系列 特性， 旨在使 LLC 转换器的运行得到良好控制和保护。该器件可与 UCC28056 或 UCC28064A PFC 控制器搭配使用，并结合 UCC24624 同步整流器控制器以提供完整的电源解决方案。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC256403	SOIC (14)	9.9mm x 3.9mm
UCC256404	SOIC (14)	9.9mm x 3.9mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

ADVANCE INFORMATION

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

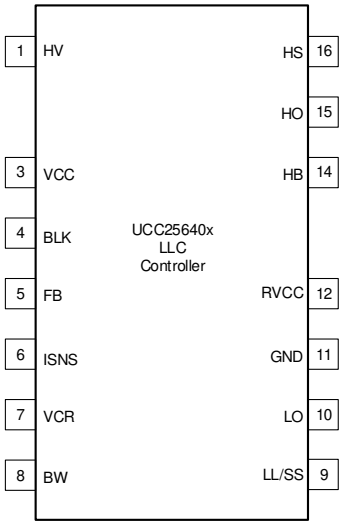
Changes from Original (June 2019) to Revision A	Page
• 已更改 图 17 , Burst Mode Switching Pattern	31

5 Device Comparison Table

Device	Integrated High Voltage Startup	Integrated X-Capacitor Discharge	Requires External Bias Supply
UCC256403	No	No	Yes
UCC256404	Yes	Yes	No

6 Pin Configuration and Functions

DDB Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BLK	4	I	This pin is used to sense the LLC stage input voltage level. A resistor divider should be used to attenuate the signal before it is applied to this pin. The voltage level on this pin will determine when the LLC converter starts/stops switching.
BW	8	I	This pin is used to sense the output voltage through the bias winding. The sensed voltage is used for output over voltage protection. During startup, the pin is also used to program the ratio between the two burst mode thresholds (BMT_L and BMT_H).
FB	5	I	LLC stage control feedback input. The amount of current sourced from this pin will determine the LLC input power level.
GND	11	G	Ground reference for all signals.
HB	14	I	High-side gate-drive floating supply voltage. The bootstrap capacitor is connected between this pin and HS pin. A high voltage, high speed diode should be connected from RVCC to this pin to supply power to the high-side gate-driver during the period when the low-side MOSFET is conducting.
HO	15	O	High-side floating gate-drive output.
HS	16	I	High-side gate-drive floating ground. Current return for the high-side gate-drive current.
HV	1	I	Connects to internal HV startup JFET. For UCC256404, this pin provides start up power for both PFC and LLC stage. This pin also monitors the AC line voltage for x-capacitor discharge function. For UCC256403, this pin needs to be connected to ground.
ISNS	6	I	Resonant current sense. The resonant capacitor voltage is differentiated with a first order filter to measure the resonant current.
LL/SS	9	I	The capacitance value connected from this pin to ground will impact the duration of the soft-start period. The resistor divider connected to the pin will define the initial voltage applied on the pin for startup. After system startup, this pin is used to program the burst mode threshold.
LO	10	O	Low-side gate-drive output.
Missing	2	N/A	Functional creepage and clearance
Missing	13	N/A	Functional creepage and clearance
RVCC	12	P	Regulated 13-V supply. This pin is used to supply the gate driver and PFC controller.
VCC	3	P	Supply input.
VCR	7	I	Resonant capacitor voltage sense.

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted), all voltages are with respect to GND, currents are positive into and negative out of the specified terminal.(1)

		MIN	MAX	UNIT
Input voltage	HV, HB	-0.3	640	V
	BLK, LL/SS	-0.55	7.2	V
	VCR	-0.55	7.2	V
	HB - HS	-0.3	17	V
	VCC	-0.55	30	V
	BW, ISNS	-5	7.2	V
RVCC output voltage	DC	-0.3	17	V
HO output voltage	DC	HS – 0.3	HB + 0.3	V
	Transient, less than 100ns	HS - 2	HB + 0.3	
LO output voltage	DC	-0.3	RVCC + 0.3	V
	Transient, less than 100ns	-2	RVCC + 0.3	
Floating ground slew rate	dV_{HS}/dt	-50	50	V/ns
HO, LO pulsed current	I_{OUT_PULSED}	-0.6	1.2	A
Junction temperature range	T_J	-40	150	°C
Storage temperature range, T_{stg}	T_{stg}	-65	150	
Lead temperature	Soldering, 10 second		300	
	Reflow		260	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, high voltage pins(1)	±1000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

		MIN	NOM	MAX	UNIT
HV, HS	Input voltage			600	V
V_{CC}	Supply voltage	13	15	26	V
HB - HS	Driver bootstrap voltage	10	12	16	V

ADVANCE INFORMATION

Recommended Operating Conditions (continued)

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

		MIN	NOM	MAX	UNIT
C_B	Ceramic bypass capacitor from HB to HS	0.1			µF
C_{SS}	Soft start pin capacitor	4.7		470	nF
C_{RVCC}	RVCC pin decoupling capacitor	4.7			µF
$I_{RVCCMAX}$	Maximum output current of RVCC (1)			100	mA
T_A	Operating ambient temperature	-40		125	°C

(1) Not tested in production. Insured by characterization

7.4 Thermal Information

THERMAL METRIC(1)		UCC256403/UCC256404 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15 V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{CCShort}$	Below this threshold, use reduced start up current	UCC256404		0.5		V
$V_{CCReStartJfet}$	Below this threshold, re-enable JFET.			10.5		V
$V_{CCStartSelf}$	In self bias mode, gate starts switching above this level			26		V
$V_{CCUVLOrising}$	VCC under voltage lockout voltage (rising)			8.25		V
$V_{CCUVLOHYS}$	VCC under voltage lockout voltage hysteresis			0.25		V
SUPPLY CURRENT						
$I_{CCSleep}$	Current drawn from VCC rail during burst off period	UCC256403		780		µA
		UCC256404		780		µA
I_{CCRun}	Current drawn from VCC Pin while gate is switching. Excluding Gate Current	Dead time = 1us maximum dead time		2.5		mA
REGULATED SUPPLY						
V_{RVCC}	Regulated supply voltage	VCC = 15 V, no load		13		V
V_{RVCC}	Regulated supply voltage	VCC = 15 V, 100 mA load		13		V
V_{RVCC}	Regulated supply voltage	VCC = 13 V, no load		12.8		V
V_{RVCC}	Regulated supply voltage	VCC = 13 V, 30 mA load		12.6		V
$V_{RVCCUVLO}$	RVCC under voltage lock out voltage (1)			7		V

(1) Not production tested.

ADVANCE INFORMATION

Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15 V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH VOLTAGE STARTUP						
I_{HVLow}	Reduced startup pin current	V_{HV} = 20 V		0.5		mA
I_{HVHigh}	Full startup pin current	V_{HV} = 20 V		10.20		mA
I_{HVLeak}	HV current source leakage current	V_{HV} = 600 V		3.37		µA
I_{HVZCD}	Highest AC zero crossing detection test current			1.7		mA
$I_{HVZCDStep}$	AC zero crossing detection test current steps			0.38		mA
$I_{XCAPDischarge}$	X-cap discharge current			11.5		mA
$V_{zero-crossing}$	HV pin voltage threshold that zero-crossing is detected			9		V
$t_{XCAPZCD}$	AC zero crossing detection window length for first three test current stage (1)			12		ms
$t_{XCAPZCDLast}$	AC zero crossing detection window length for final test current stage (1)			46		ms
$t_{XCAPIdle}$	AC zero crossing detection idle period length (1)			700		ms
$t_{XCAPDischarge}$	Time for X-cap discharge current active (1)			360		ms
$t_{XCAPJFETON}$	Time of first X-cap detection after JFETON			12		ms
BULK VOLTAGE SENSE						
$V_{BLKStart}$	BLK voltage that allows LLC to start switching	UCC256403		3		V
		UCC256404		1		V
$V_{BLKStop}$	BLK voltage that forces LLC operation to stop	UCC256403		2.2		V
		UCC256404		0.9		V
FEEDBACK PIN						
$R_{FBInternal}$	Internal pull down resistor value			101.5		kΩ
I_{FB}	FB internal current source	UCC256403		160		µA
		UCC256404		85.1		µA
V_{FB}	FB pin voltage when FB pin sink current is at (I_{FB} - 50 µA)			5.5		V
ΔV_{FB}	FB pin voltage variation when FB pin sink current ranges from (I_{FB} - 50 µA) to (I_{FB} - 5 µA)			0.28		V
ΔV_{clamp}	FB pin voltage variation when FB pin sink current ranges from (I_{FB} - 5 µA) to (I_{FB} + 5 µA)			0.5		V
$I_{FBclamp}$	Maximum FB internal current source when FB is clamped			82		µA
$\Delta V_{FBclamp}$	FB pin voltage variation when FB pin sink current ranges from (I_{FB} + 5 µA) to (I_{FB} + $I_{FBClamp}$ - 5 µA)			0.25		V
f_{-3dB}	Feedback chain -3dB cut off frequency (1)		1			MHz
RESONANT CURRENT SENSE						
V_{ISNS_OCP1}	OCP1 threshold			4		V
$V_{ISNS\_OCP1\_SS}$	OCP1 threshold during soft start (1)			5		V

ADVANCE INFORMATION

Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15 V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISNS_OCP2}	OCP2 threshold			0.6		V
V_{ISNS_OCP3}	OCP3 threshold			0.43		V
t_{ISNS_OCP2}	The time the average input current needs to stay above OCP2 threshold before OCP2 is triggered (1)			2		ms
t_{ISNS_OCP3}	The time the average input current needs to stay above OCP3 threshold before OCP3 is triggered (1)			50		ms
$V_{IpolarityHyst}$	Resonant current polarity detection hysteresis			30		mV
n_{OCP1}	Number of OCP1 cycles before OCP1 fault is tripped (1)			4		
RESONANT CAPACITOR VOLTAGE SENSE						
V_{CM}	Internal common mode voltage			3		V
I_{RAMP}	Frequency compensation ramp current source value			2		mA
$I_{Mismatch}$	Pull up and pull down ramp current source mismatch (2)		-1.25		1.25	%
GATE DRIVER						
V_{LOL}	LO output low voltage	I_{sink} = 20 mA		0.05		V
V_{RVCC} - V_{LOH}	LO output high voltage	I_{source} = 20 mA		0.18		V
V_{HOL} - V_{HS}	HO output low voltage	I_{sink} = 20 mA		0.05		V
V_{HB} - V_{HOH}	HO output high voltage	I_{source} = 20 mA		0.18		V
$V_{HB-HSUVLORise}$	High side gate driver UVLO rising threshold			7.94		V
$V_{HB-HSUVLOFall}$	High side gate driver UVLO falling threshold			7.25		V
$I_{source\_pk\_HO}$	HO peak source current (1)			-0.6		A
$I_{source\_pk\_LO}$	LO peak source current (1)			-0.6		A
$I_{sink\_pk\_HO}$	HO peak sink current (1)			1.2		A
$I_{sink\_pk\_LO}$	LO peak sink current (1)			1.2		A
BOOTSTRAP						
$I_{BOOT\_QUIESCENT}$	(HB - HS) quiescent current	HB - HS = 12 V		66		µA
I_{BOOT_LEAK}	HB to GND leakage current	V_{HB}= 600 V		0.40		µA
$t_{ChargeBoot}$	Length of charge boot state			267		µs
SOFT START AND BURST MODE						
I_{SSUp}	Current output from SS pin to charge up the soft start capacitor			37		µA
R_{SSDown}	SS pin pull down resistance	ZCS or OCP1		400		Ω
$V_{SSInitVolPrgm}$	SS pin voltage during the initial voltage programming			5		V
$t_{SSInitVolPrgm}$	SS initial voltage programming time			1.5		ms

(2) $I_{Mismatch}$ calculated as $[I_{PU}-(I_{PD}+I_{PU})/2]/[(I_{PD}+I_{PU})/2]$

ADVANCE INFORMATION

Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15 V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$K_{SSInitVolPrgm}$	Ratio between the current that flows through R_{LL} and current sourcing from SS pin during initial voltage programming	I_{SSLL} = 24 µA (current sourcing from SS pin)		1		
R_{LL}	LL/SS voltage scaling resistor value			100		kΩ
N_{burst}	Minimum number of pulses in each burst packet (including burst soft on/off pulses)			40		
Nsoftmax	Maximum number of pulses for burst soft on/off			7		
Ksoft	Minimal ratio of Vcomp/VFBreplica during burst soft on/off			0.5		
$V_{LLVolPrgm}$	LL pin voltage during the burst mode exit threshold (BMT_H) programming			3.5		V
$K_{LLVolPrgm}$	Ratio between the current flows through RLL and current sinking to LL pin during burst mode threshold programming	I_{SSLL} = 40 µA (current sinking to LL pin)		1		
BMT_{Hhys}	Burst mode exit threshold comparator hysteresis			120		mV
BMT_{Hmin}	Minimal burst mode exit threshold			0.2		V
BMT_{Lmin}	Minimal burst mode entry threshold			0.2		V
BIAS WINDING						
$V_{BWOVPos}$	Output voltage OVP, Positive Threshold			4		V
$V_{BWOVNeg}$	Output voltage OVP, Negative Threshold			-4		V
n_{BWOV}	Number of BW OVP cycles before BW OVP fault is tripped (1)			5		
I_{BWPrgm}	BW pin sourcing current for BMT_L/BMT_H programming			54		µA
t_{BWPrgm}	BMT_L/BMT_H programming time			2		ms
$K_{BMTL/BMTH1}$	Ratio of BMT_L/BMT_H Option 1			0.95		
$K_{BMTL/BMTH2}$	Ratio of BMT_L/BMT_H Option 2			1		
$K_{BMTL/BMTH3}$	Ratio of BMT_L/BMT_H Option 3			0.9		
$K_{BMTL/BMTH4}$	Ratio of BMT_L/BMT_H Option 4			0.8		
$K_{BMTL/BMTH5}$	Ratio of BMT_L/BMT_H Option 5			0.6		
$K_{BMTL/BMTH7}$	Ratio of BMT_L/BMT_H Option 7 (Burst mode disable)			1		
$R_{BWPrgm1}$	BW pin equivalent resistance to choose BMT_L/BMT_H ratio option 1		24730			Ω
$R_{BWPrgm2}$	BW pin equivalent resistance to choose BMT_L/BMT_H ratio option 2		17125		19976	Ω
$R_{BWPrgm3}$	BW pin equivalent resistance to choose BMT_L/BMT_H ratio option 3		12562		13624	Ω
$R_{BWPrgm4}$	BW pin equivalent resistance to choose BMT_L/BMT_H ratio option 4		9018		9813	Ω
$R_{BWPrgm5}$	BW pin equivalent resistance to choose BMT_L/BMT_H ratio option 5		6478		6849	Ω

ADVANCE INFORMATION

Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15 V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{BWPrgm6}$	BW pin equivalent resistance to choose BMT_L/BMT_H ratio option 6 (BMT_L=BMT_{Lmin})		4450		4732	Ω
$R_{BWPrgm7}$	BW pin equivalent resistance to choose BMT_L/BMT_H ratio option 7 (Burst mode disable)		2422		3038	Ω
ADAPTIVE DEADTIME						
dV_{HS}/dt	Detectable slew rate (1)		-0.1		-50	V/ns
FAULT RECOVERY						
$t_{PauseTimeOut}$	Paused timer (1)			1		s
THERMAL SHUTDOWN						
T_{J_r}	Thermal shutdown temperature (1)	Temperature rising	125	145		°C
T_{J_H}	Thermal shutdown hsyterisis (1)			10		°C

7.6 Switching Characteristics

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =12 V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(LO)}$	Rise time	10% to 90%, 1 nF load		30		ns
$t_{f(LO)}$	Fall time	10% to 90%, 1 nF load		20		ns
$t_{r(HO)}$	Rise time	10% to 90%, 1 nF load		30		ns
$t_{f(HO)}$	Fall time	10% to 90%, 1 nF load		20		ns
$t_{DT(min)}$	Minimum dead time (1)			100		ns
$t_{DT(max)}$	Maximum dead time (dead time fault) (1)	ZCS event is not detected		1		µs
$t_{DT(max\_ZCS)}$	Maximum dead time (dead time fault) (1)	ZCS event is detected		150		µs
$t_{ON(min)}$	Minimum gate on time (1)			250		ns
$t_{ON(max)}$	Maximum gate on time (1)			16		µs

(1) Not tested in production. Insured by design

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The UCC25640x is a fully featured LLC resonant controller for AC/DC power supplies. The high level of integration of UCC25640x enables significant reduction of component count and solution size without compromising functionality. UCC25640x achieves very low standby power and low audible noise standby operation using an optimized burst mode. The device's novel control scheme offers excellent transient performance.

Many consumer applications, including large screen televisions, AC-DC adapters, industrial power supplies, and LED drivers, employ PFC + LLC power supplies because they offer improved efficiency, and small size, compared with a PFC + flyback topology. A disadvantage of the PFC + LLC power supply system is that it has poor light load efficiency and high no-load power consumption because the LLC stage requires a minimum amount of circulating current to maintain regulation. To meet light load efficiency and standby power consumption requirements, traditionally an auxiliary flyback converter is used. It runs continuously to allow the main PFC + LLC power system to be shut down when the system enters low power or standby mode. UCC25640x contains a number of novel features that enable it to offer excellent light load efficiency and low no-load power. This will allow power supply designers to create systems that meet the stringent no-load power target without needing an auxiliary flyback converter.

UCC25640x uses a novel control algorithm, Hybrid Hysteretic Control (HHC), to achieve regulation. In this control algorithm, the switching frequency is defined by the resonant capacitor voltage, which carries accurate input current information. This allows the controller monitors and corrects the input current directly. Compared with traditional Direct Frequency Control (DFC), HHC makes the system close to a first order system if the frequency control portion is small. This enables excellent load and line transient response.

UCC25640x adopts an advanced burst mode to meet the stringent requirements on standby power consumption and audible noise level. At low output power levels UCC25640x automatically transitions into light-load burst mode. In burst mode, UCC25640x repetitively delivers a burst packet with a fixed number of switching pulses and a shut-off period. The shut-off time period between burst packets is terminated by the secondary regulator loop based on the FB pin current. The LLC equivalent load current level during the burst on period is a programmable value. For each burst packet, the switching frequency slowly ramps down at the first few switching periods and ramps up at the last few switching periods, to slowly ramp up and ramp down the resonant current during burst operation. This burst soft-on and soft-off can effectively help to minimize the audible noise during burst mode operation. In addition, UCC25640x operates in a low power mode during burst mode with a very low quiescent current and biased optocoupler operation with low current.

UCC25640x monitors the half-bridge switch node to determine the required dead-time for the gate signals. In this way the dead-time is automatically adjusted to provide optimum efficiency and robust operation. UCC25640x includes a slew rate detector with improved sensitivity of the switch node voltage for adaptive dead-time that makes its operation inherently robust compared with alternative parts.

UCC25640x includes high and low-side drivers that can directly drive N-channel MOSFETs in an LLC power stage. This allows complete and fully featured power systems to be realized with minimum component count.

UCC256404 includes a high-voltage startup JFET to initially charge the VCC capacitor to provide the energy needed to start the PFC and LLC power system. Once running, power for the PFC and LLC controllers is derived from a bias winding on the LLC transformer. UCC256404 also includes the active x-capacitor discharge feature to discharge the remaining voltage on the x-capacitor of the EMC filters after unplugging the AC input. UCC256403 does not include the high voltage startup and active x-capacitor discharge features. It requires an auxiliary supply to power the VCC.

UCC25640x includes robust algorithms for avoiding the zero-current switching (ZCS) operation region. When ZCS operation is detected, UCC25640x overrides the feedback signal and ramps up the switching frequency until non-capacitive operation is restored. After which the switching frequency is ramped back down at a rate determined by the soft-start capacitor until control has been handed back to the voltage control loop.

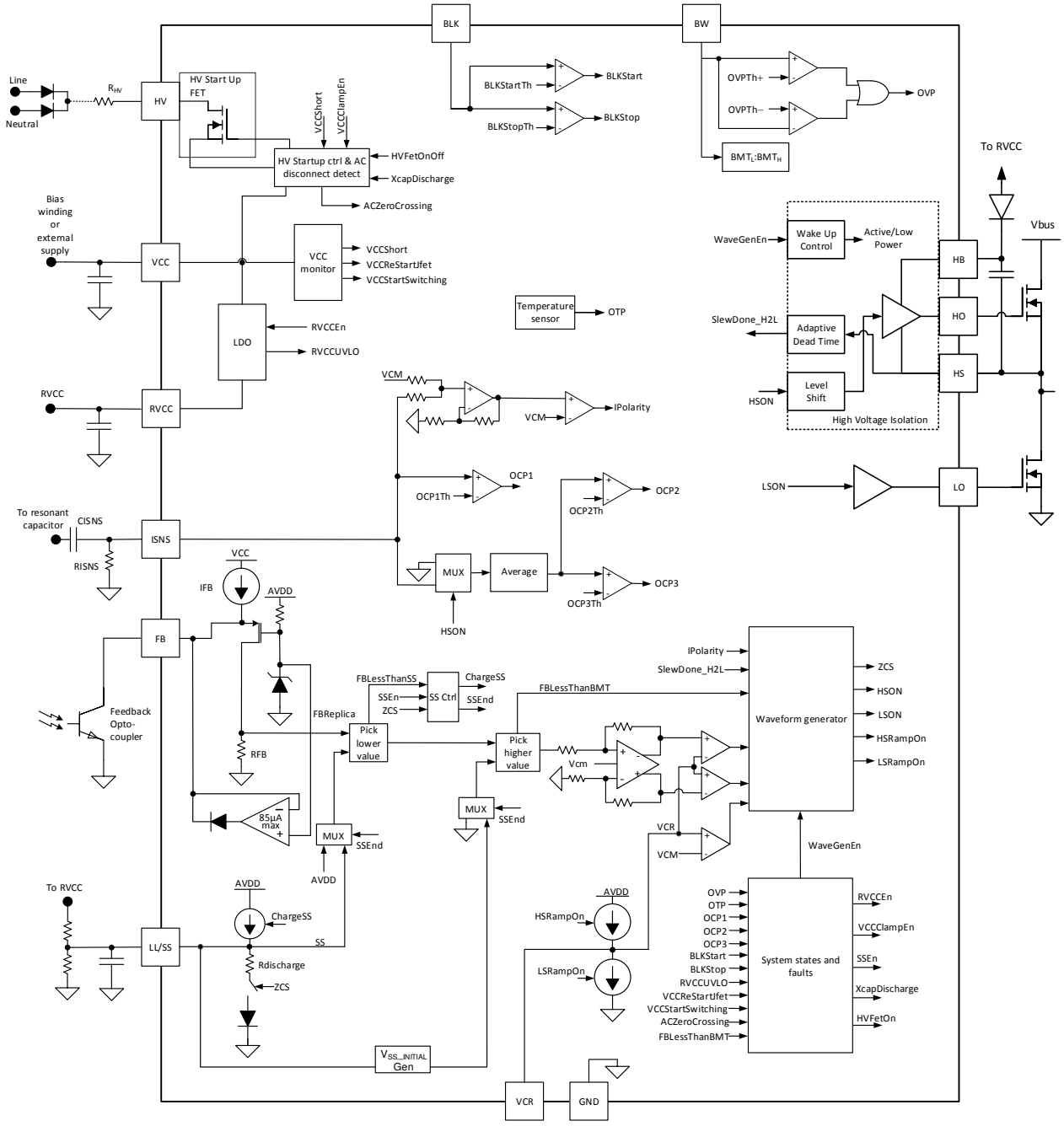
Overview (接下页)

Additional protection features of UCC25640x include three-level over current protection (OCP), output over voltage protection (OVP), input voltage under-voltage protection (UVP), gate driver under-voltage lock-out (UVLO) protection, and over temperature protection (OTP).

The key features of UCC25640x can be summarized as follows:

- Hybrid Hysteretic Control helps achieve best-in-class load and line transient response
- Optimized light load burst mode enables less than 150-mW standby power designs
- Burst soft-on and soft-off enables ultra-quiet standby operation
- Robust adaptive dead time control
- Integrated high-voltage gate driver
- Integrated high-voltage startup for UCC256404
- Active x-capacitor discharge for UCC256404
- Improved capacitive region operation prevention scheme
- Comprehensive protection feature set

8.2 Functional Block Diagram



ADVANCE INFORMATION

8.3 Feature Description

8.3.1 Hybrid Hysteretic Control

UCC25640x uses a novel control scheme, Hybrid Hysteretic Control (HHC), to achieve best-in-class line and load transient performance. The control method makes the compensator easier to design. The control method also makes light load management easier and more efficient. Improved line transient enables lower bulk capacitor and output capacitor value, reducing system cost.

HHC is a control method which combines traditional frequency control and charge control. It is a charge control with added frequency compensation ramp. Compared with traditional frequency control, it changes the power stage transfer function from a second order system to a first order system, so that it makes the compensation network design easier. The control effort is directly related to input current, so the line and load transients are best-in-class. Compared with charge control, Hybrid Hysteretic Control avoids instability by adding in a frequency compensation ramp. The frequency compensation ensures system stability, and makes the output impedance lower as well. Lower output impedance makes the transient performance better than charge control. The frequency compensation also makes the implementation of burst mode soft-on and soft-off much easier, as changing the control effort can directly impact the switching frequency. For burst mode soft-on and soft-off, the converter switching frequency needs to be adjusted to achieve a reduced resonant current.

In summary, HHC solves the following problems:

- Help LLC converters achieve best in class load transient and line transient
- Changes the small-signal transfer function to a first order system to easily achieve very high bandwidth
- Inherently stable via frequency compensation
- Makes burst mode control easier to optimize light load efficiency
- Makes the implementation of burst mode soft-on and soft-off much easier, to achieve lower audible noise

图 1 shows the HHC implementation in UCC25640x: a capacitor divider (C1 and C2) and two well matched controlled current sources. The resonant capacitor voltage is divided down by the capacitor divider formed by C1 and C2. The current sources are controlled by the gate drive signals. When the high-side switch is on, the upper current source injects a constant current into the capacitor divider; when the low-side switch is on, the lower current source pulls the same amount of constant current out of the capacitor divider. The two current sources add a triangular compensation ramp to the VCR node. The current sources are supplied by a reference voltage AVDD. AVDD needs to be equal to or larger than twice the common mode voltage V_{CM}. The divided resonant capacitor voltage and the compensation ramp voltage are then added together to get the VCR node voltage. If the frequency compensation ramp dominates, the VCR node voltage will look like a triangular waveform, and the control will be similar to direct frequency control. If the resonant capacitor voltage dominates, the shape of the VCR node voltage will look like the actual resonant capacitor voltage, and the control will be similar to charge control. This is why the control method is called “hybrid” and the compensation ramp is called frequency compensation.

This set up has an inherent negative feedback to keep the high-side and low-side on-time balanced, and also to keep the common mode voltage at VCR node at V_{CM}.

There are two input signals needed for the new control scheme: VCR and V_{COMP}. VCR is the sum of the scaled down version of the resonant capacitor voltage and the frequency compensation ramp. V_{COMP} is the voltage loop compensator output. The waveform below shows how the high-side and low-side switches are controlled based on VCR and V_{COMP}. The common mode voltage of VCR is V_{CM}.

Based on V_{COMP} and V_{CM} (3 V), two thresholds: V_{TH} and V_{TL} are created.

$$V_{TH} = V_{CM} + \frac{V_{comp}}{2} \quad (1)$$

$$V_{TL} = V_{CM} - \frac{V_{comp}}{2} \quad (2)$$

The VCR voltage is compared with the two thresholds. When VCR > V_{TH}, the high-side switch is turned off; when VCR < V_{TL}, low-side switch is turned off. HO and LO turn on edges are controlled by the adaptive dead time circuit.

ADVANCE INFORMATION

Feature Description (接下页)

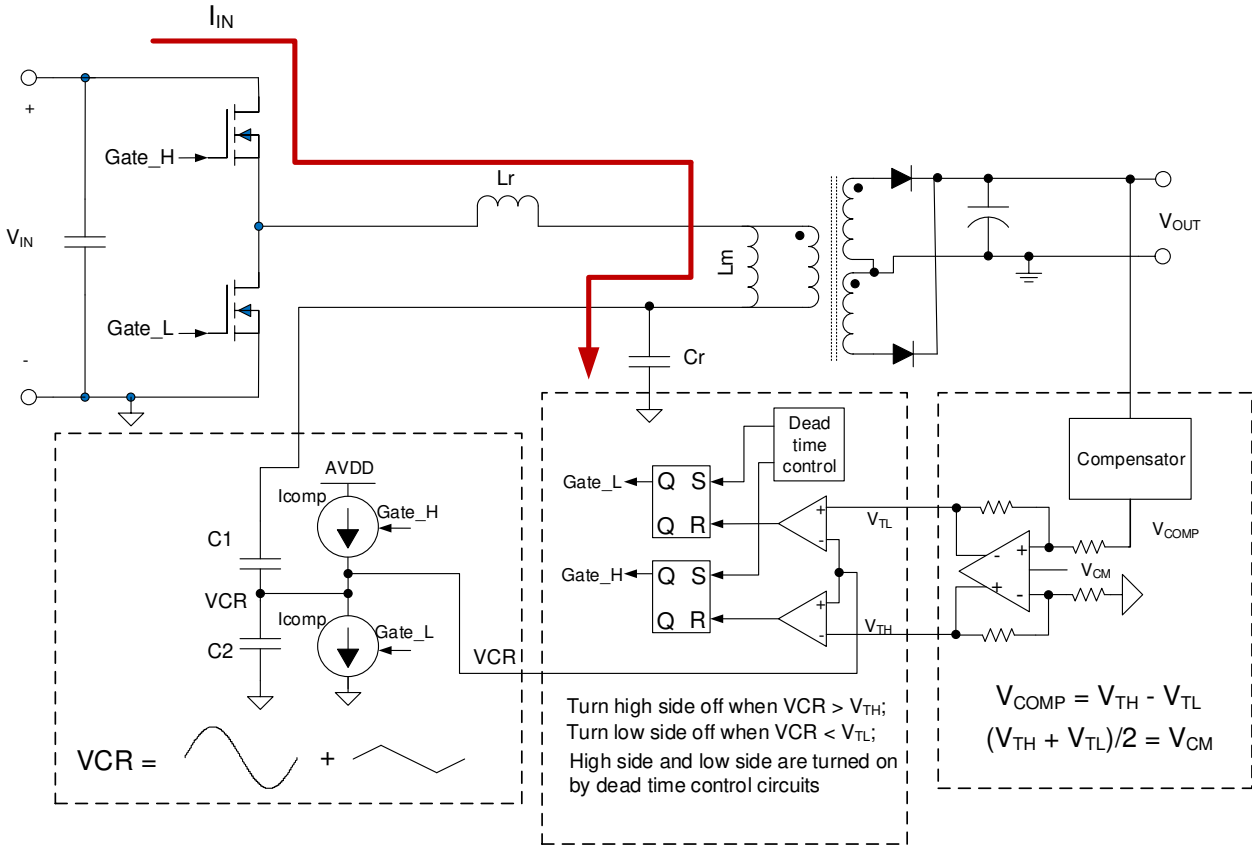


图 1. UCC25640x HHC Implementation

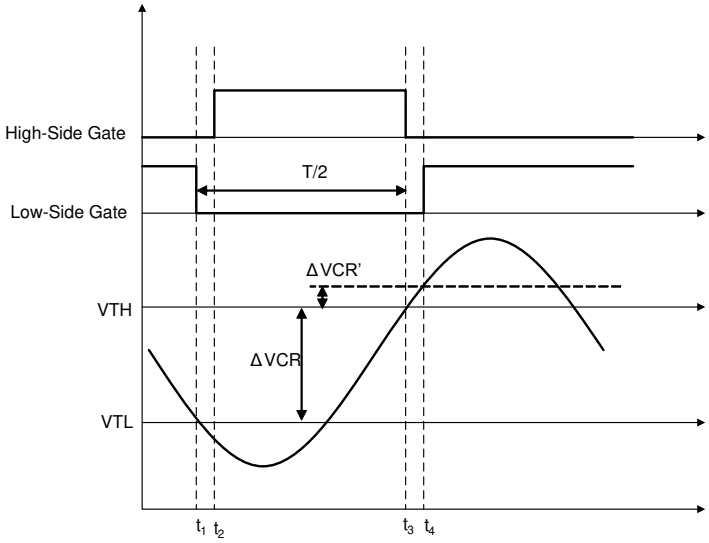


图 2. HHC Gate On/Off Control Principle

ADVANCE INFORMATION

Feature Description (接下页)

8.3.2 Regulated 13-V Supply

RVCC pin is the regulated 13-V supply. This regulated rail is used to supply the PFC and LLC as a bias. RVCC has under voltage lock out (UVLO) function. During normal operation, if the RVCC voltage is less than $RVCC_{UVLO}$ threshold, the system will enter FAULT state. Details about the FAULT handling will be discussed in the Protections section.

8.3.3 Feedback Chain

Control of the output voltage is provided by a voltage regulator circuit located on the secondary side of the isolation barrier. The demand signal from the secondary regulator circuit is transferred across the isolation barrier using an optocoupler and is fed into the FB pin on UCC25640x. This section discusses about the whole feedback chain. 图 3 shows the block diagram of the FB chain, and 图 4 shows the typical timing diagram with a normal soft start followed by a ZCS event, and load step into burst mode, and then exiting burst mode.

The feedback chain has the following functions:

- Optocoupler feedback signal input and bias
- FB voltage clamp
- Soft start function selection by a "pick lower value" block
- Burst mode selection by a "pick higher value" block
- Convert single ended feedback demand into two thresholds V_{TH} and V_{TL}; and VCR comparison with the thresholds and the common mode voltage V_{CM}

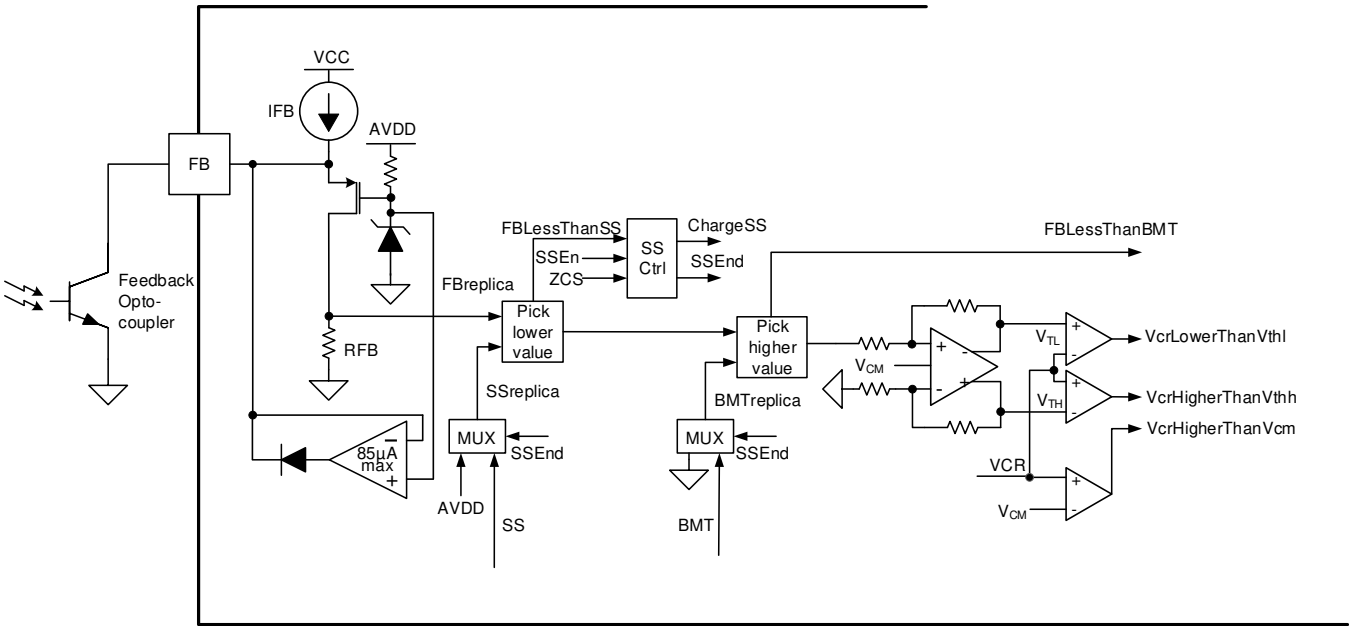


图 3. Feedback Chain Block Diagram

ADVANCE INFORMATION

Feature Description (接下页)

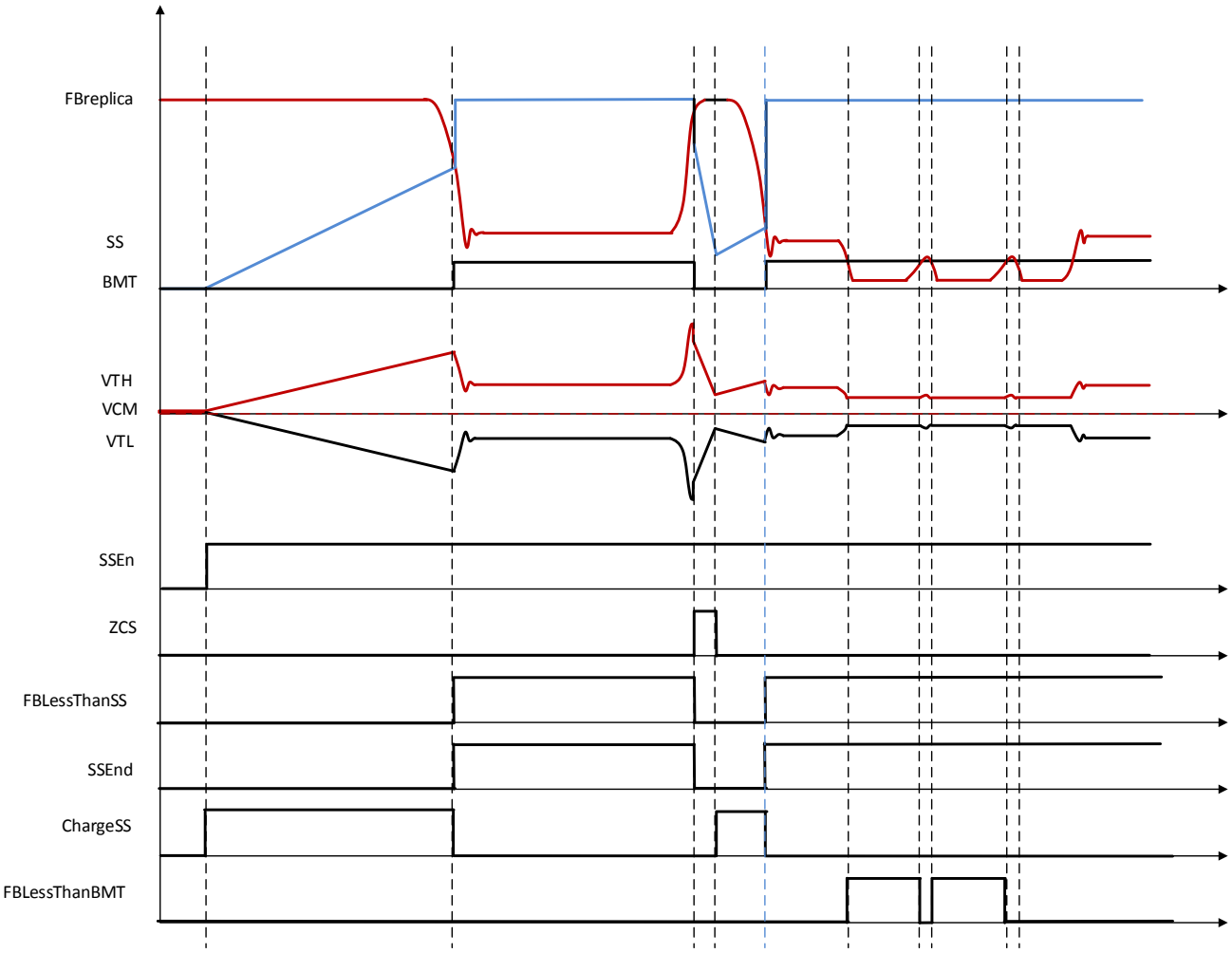


图 4. Feedback Chain Timing Diagram

8.3.3.1 Optocoupler Feedback Signal Input and Bias

The secondary regulator circuit and optocoupler feedback circuit all add directly to the standby power consumed by the system. To achieve very low standby power it is necessary to drive the optocoupler in a low current mode.

As shown in 图 3, a constant current source IFB is generated out of VCC voltage and connected to FB pin. A resistor RFB is also connected to this current source with a PMOS in series. During normal operation, the PMOS is always on, so that the FB pin voltage will be equal to the zener diode reference voltage plus the voltage drop on the PMOS source to gate.

$$I_{FB} = I_{opto} + I_{RFB} \quad (3)$$

From this equation, when I_{opto} increases, I_{RFB} will decrease, making FBreplica decrease. In this way, the control effort is inverted. A conventional way to bias the optocoupler is using a pull up resistor on the collector of the optocoupler output. To reduce the power consumption, the pull up resistor needs to be big, which will limit the loop bandwidth. For the bias current method used in UCC25640x, the FB pin voltage is maintained constant so that the parasitic capacitor of the optocoupler will not introduce an extra pole to the system, and subsequently limit the loop bandwidth.

ADVANCE INFORMATION

Feature Description (接下页)

8.3.3.2 FB Pin Voltage Clamp

As shown in the Optocoupler Feedback Signal Input and Bias section, the FBreplica decreases while I_{opto} increases. When I_{opto} reaches the value of I_{FB}, the FB pin voltage starts to drop because there is no current flow through the PMOS. FB pin pulled low will impact the system transient response, due to the extra delay introduced by charging the parasitic capacitor of the optocoupler to pull up the FB pin voltage. A FB pin voltage clamp circuit is used to prevent this scenario. When FB pin voltage drops below the FB pin clamp voltage threshold, an extra current source is turned on to clamp the FB voltage. The clamp strength is $I_{FBclamp}$. The FB pin clamp circuit improves the system transient performance from light load to heavy load.

8.3.3.3 "Pick Lower Value" Block and Soft Start Multiplexer

This part of the circuit consists of 3 elements:

- A pick lower block
- A MUX which selects AVDD or SS signal as the second input to the pick lower block
- A SS control block which handles the charge and discharge of the SS capacitor in the case of a ZCS fault

The pick lower block has two inputs. The first input is FBreplica. The second input is selected between AVDD and SS pin voltage. The output of the block is the lower of the two inputs.

The MUX selects between SS and AVDD. The selection is based on SSEnd (soft start end) signal, which is an output of the SS Ctrl block. SSEnd is high when SS is higher than FBreplica, and the soft start process has been initiated by the state machine, and there is no ZCS condition. Switching to AVDD after soft start has ended helps make sure that during non-soft start or non-ZCS fault condition, FBreplica signal is always sent through the pick lower block. It also releases the SS pin to perform the light load threshold programming.

The SS control block handles the charge and discharge of the SS capacitor in the case of a ZCS fault. It resets the SSEnd signal when ZCS happens, so the effect of pulling down on SS pin to increase the switching frequency can pass through the pick lower block.

8.3.3.4 Pick Higher Block and Burst Mode Multiplexer

The output of the pick lower block goes into a pick higher block, which selects the higher of the pick lower block output and the burst mode threshold setting.

The burst mode multiplexer selects between burst mode threshold (BMT) and ground. During soft start, the multiplexer selects ground. The startup process is open loop and controlled by the soft start ramp. Burst mode is not enabled during soft start phase.

After soft start, the higher of the two inputs are sent to the differential amplifier. The output of the block is FBLessThanBMT. It is sent to the waveform generator state machine to control burst mode and system external shut down.

8.3.3.5 VCR Comparators

The output of the pick higher block is sent to a differential amplifier to convert the signal tino two thresholds symmetrical to V_{CM}. The difference between the two thresholds V_{TH} and V_{TL} equals the input amplitude. The VCR pin voltage is then compared with V_{TH}, V_{TL}, and V_{CM}. The results are sent to the waveform generator.

Feature Description (接下页)

8.3.4 Resonant Capacitor Voltage Sensing

The resonant capacitor voltage sense pin senses the resonant capacitor voltage through a capacitor divider. Inside the device, two well matched, controlled current sources are connected to the VCR pin to generate the frequency compensation ramp. The on/off control signals of the two current sources come from the waveform generator block.

During waveform generator IDLE state or before startup, the VCR node is clamped to V_{CM}. This action will help reduce the startup peak current, and help the VCR voltage to settle down quickly during burst mode.

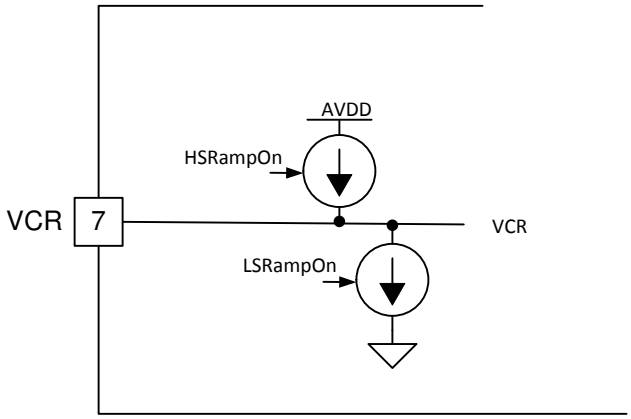


图 5. VCR Block Diagram

The ramp current on/off sequence is shown in 图 6. The ramp current is on all the time. It changes direction at the falling edge of the high-side on or low-side on signal.

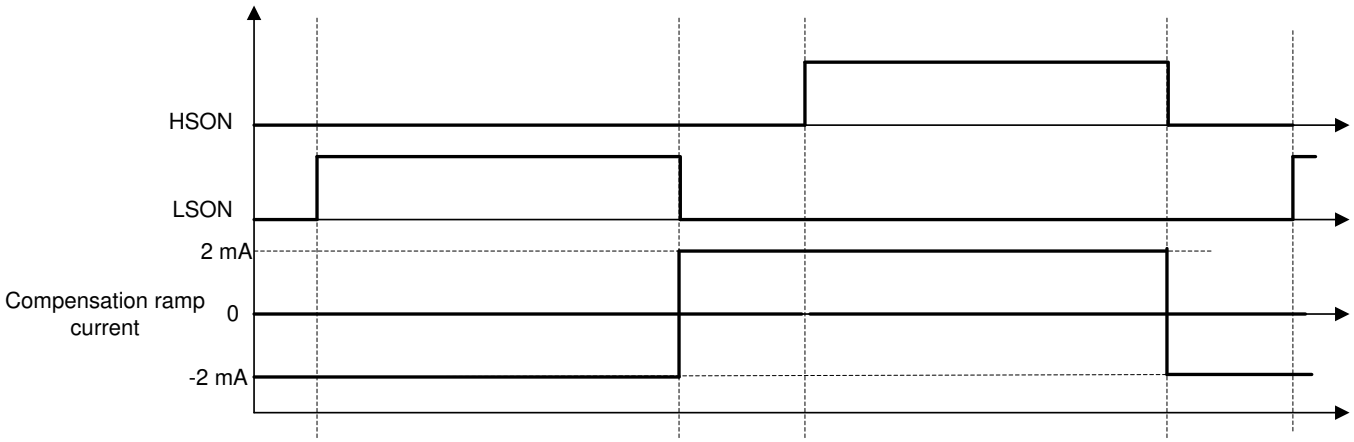


图 6. VCR Compensation Ramp Current On/Off

On the VCR pin, a capacitor divider is used to combine the resonant capacitor waveform and the compensation ramp waveform. Adjusting the size of the external capacitors can change the contribution of charge control and direct frequency control. Assuming the divided down version of the resonant capacitor voltage by the capacitor divider is V_{div}, the compensation ramp current resultant voltage on the VCR pin is V_{ramp}. If V_{div} is much larger than V_{ramp}, the control method is similar to charge control, in which the control effort is proportional to the input charge of one switching cycle. If V_{ramp} is much larger than V_{div}, the control method is similar to direct frequency control, in which the control effort is proportional to the switching frequency. The most optimal transient response can be achieved by adjusting the ratio between V_{div} and V_{ramp}.

ADVANCE INFORMATION

Feature Description (接下页)

8.3.5 Resonant Current Sensing

The ISNS pin is connected to the resonant capacitor using a high voltage capacitor. The capacitor CISNS and the resistor RISNS form a differentiator. The resonant capacitor voltage is differentiated to get the resonant current. The differentiated signal is AC and goes both positive and negative. In order to sense the zero crossing, the signal is level shifted using an op amp adder. The IPolarity comparator detects the direction of the resonant current. IPolarity is checked at LSON and HSON falling edges for ZCS protection, with more details described in ZCS Region Prevention section. The digital state machine implements a blanking time on IPolarity. The IPolarity edges during the first 400 ns of dead time are ignored considering the noise on ISNS pin introduced by the switching node transition.

OCP2 and OCP3 thresholds are based on average input current. To get the average input current, the differentiator output is multiplexed with the high-side switch on signal HSON. When HSON is on, the MUX output is the differentiator output; when HSON is off, the MUX output is 0. The MUX output is then averaged using a low pass filter. The output of the filter is the sensed average input current. Note that the MUX needs to pass through both positive and negative voltages. OCP2 and OCP3 faults have a 2 ms and 50 ms timer respectively. Only when the OCP2/OCP3 comparators output high for continuous 2 ms or 50 ms, will the faults be activated.

OCP1 threshold is set on the peak resonant current. The voltage on the ISNS pin gets compared to OCP1 threshold OCP1Th directly. The peak resonant current is checked once per cycle on the positive half cycle. OCP1 fault is only activated when there are 4 consecutive cycles of OCP1 event detected. During start up, the OCP1 comparator output of the first 15 cycles are ignored.

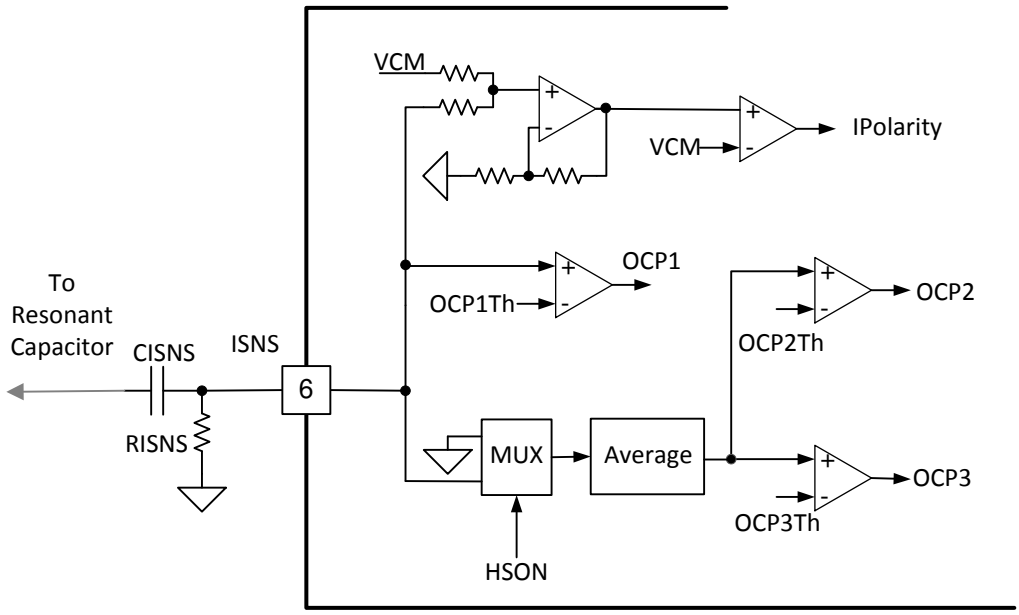


图 7. ISNS Block Diagram

8.3.6 Bulk Voltage Sensing

The BLK pin is used to sense the LLC DC input voltage (bulk voltage) level. The comparators on BLK pin have the following two thresholds:

- Bulk voltage level when LLC starts switching – BLKStartTh
- Bulk voltage level when LLC stops switching – BLKStopTh

UCC256403 and UCC256404 have different sets of BLKStartTh and BLKStopTh, to accommodate the need for different applications. A resistor divider is connected to the pin, to achieve the desired system input range. A fault is triggered if BLK pin voltage drops lower than BLKStopTh during operation. The detailed action of Input Under Voltage Protection is described in Input Under Voltage Protection (VINUVP) section.

图 8 shows the block diagram of the BLK pin.

Feature Description (接下页)

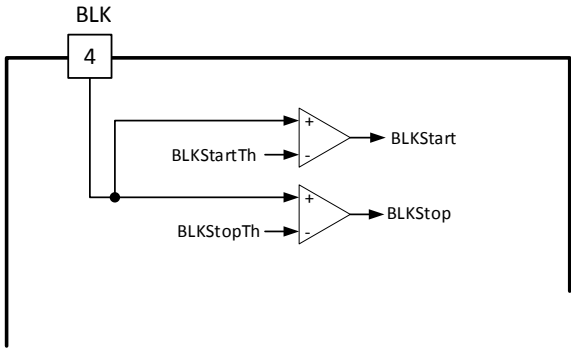


图 8. BLK Pin Block Diagram

8.3.7 Output Voltage Sensing

The output voltage is sensed through the bias winding (BW) voltage sense pin. With one terminal of the bias winding connected to primary side ground. The bias winding voltage at the other terminal represents the output voltage when the secondary side rectifier diode conducts. A resistor divider is typically used to connect from the bias winding terminal to the BW pin. The BW voltage is compared with a positive and a negtive threshold to generate an output OVP fault. During startup, BW pin is multiplexed for burst mode threshold programming. The details are introduced in the Soft-Start and Burst-Mode Threshold section. The block diagram of the bias winding voltage sense block is shown below.

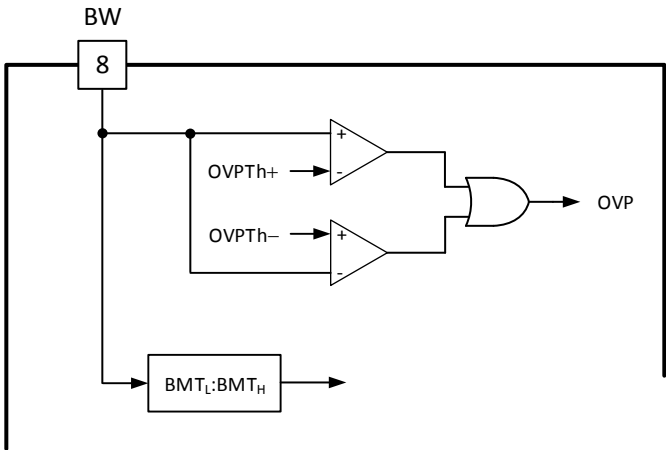


图 9. Bias Winding Sensing Block Diagram

If the OVP event is high for 5 consecutive switching cycles, the system will enter FAULT state. The actions during an OVP fault are described in the Bias Winding Over Voltage Protection (BWOVP) section.

ADVANCE INFORMATION

Feature Description (接下页)

8.3.8 High Voltage Gate Driver

LO is the low-side gate driver output. The gate driver is supplied by the 13-V RVCC rail.

The high-side driver module consists of three physical device pins. HB and HS form the positive and negative bias rail, respectively, of the high-side driver, and HO connects to the gate of the upper half-bridge MOSFET.

During periods when the lower half-bridge MOSFET is conducting, HS is shorted to GND via the conducting lower MOSFET. At this time power for the high-side driver is obtained from RVCC via the high voltage diode DBOOT, and capacitor CBOOT is charged to RVCC minus the forward drop on the diode.

During periods when the upper half-bridge MOSFET is conducting, HS is connected to the LLC input voltage rail. At this time the HV diode is reverse biased and the high-side driver is powered by the charge stored in CBOOT.

Both the high-side and low-side gate drivers have under voltage lock out (UVLO) protection. The low-side gate driver UVLO is implemented on RVCC; the high-side gate driver UVLO is implemented on (HB - HS) voltage.

When operating at light load, UCC25640x enters burst mode. During the burst off period, the gate driver enters low power mode to reduce power consumption.

The block diagram of the gate driver is shown in 图 10.

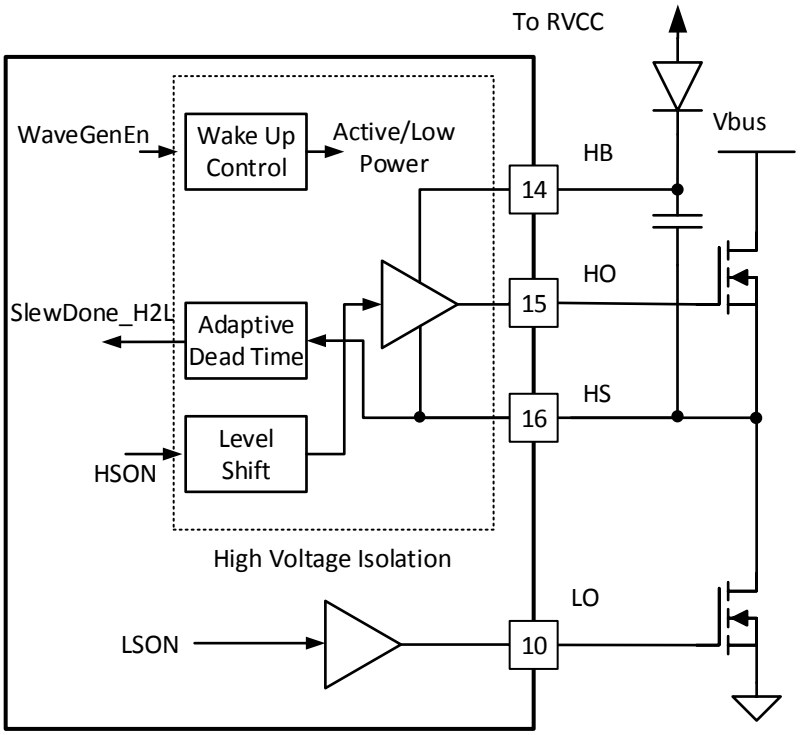


图 10. Gate Driver Block Diagram

8.3.8.1 Adaptive Dead Time Control

The Dead Time describes the time interval between an outgoing LLC MOSFET turning off and the incoming LLC MOSFET turning on. Dead time control is critical for LLC operation. A certain amount of dead time is required to prevent shoot through. During the dead time, the HS node slews from one input rail to the other due to the inductive resonant current. In order to achieve zero voltage switching (ZVS) turn on, the dead time needs to be long enough for the resonant current to fully charge or discharge the HS node. But after the bode diode starts conducting, the MOSFET should be turned on quickly. Too long of a turn on delay can result in reverse resonant current, and lead to the loss of ZVS. Also, the voltage drop on the body diode is higher than that on the MOSFET channel. Optimized dead time can help to minimize the power loss.

Feature Description (接下页)

The resonant current flowing through the HS node during the dead time depends on the LLC resonant tank design and varies by operating frequency and output/input voltage ratio. Therefore, the optimized dead time varies widely with LLC operating conditions. UCC25640x includes an adaptive dead time control to automatically find the optimized dead time across the entire operating range. It detects the change of slew rate of the HS node voltage. During a switching transition, the slew rate rises up first and then drops back to zero. A slew rate detector is used to detect the moment when the slew rate drops below a pre-defined threshold. A slew done event is only detected when the slew rate during dead time crosses the threshold and then drops back below the threshold. If the slew rate is lower than the threshold (i.e. minimal detectable slew rate) during the whole dead time period, no slew done will be detected. This is to prevent the mis-detection due to noise on the HS node voltage. If slew done is not detected, 1 us maximum dead time is used.

Because of the natural symmetric operation of LLC, only the dead time between high-side MOSFET turn off and low-side MOSFET turn on is determined by the slew rate detector. This dead time is copied and then applied to the dead time between low-side MOSFET turn off and high-side MOSFET turn on.

Feature Description (接下页)

8.3.9 Protections

8.3.9.1 ZCS Region Prevention

The capacitive region is an LLC operating region in which the voltage gain increases when the switching frequency increases. It is also called the ZCS region. Capacitive mode operation should be avoided for two reasons:

- The feedback loop becomes positive feedback in the capacitive region
- The MOSFET may be damaged because of body diode reverse recovery

The capacitive region detection is done by checking the resonant current polarity at HSON or LSON falling edge. If the resonant current is positive at LSON falling edge, or negative at HSON falling edge, the ZCS signal in the waveform generator is turned high. The ZCS signal stays high until ZCS is cleared at the next HSON or LSON falling edge.

If ZCS is detected, the next gate will be turned on at the next IPolarity flip event when the resonant current becomes inductive again. The IPolarity flip indicates that the capacitive operation cycle has already passed. The resonant current reverses direction and begins to discharge the switch node. In this stage, the body diode is no longer conducting and it is allowed to turn on the next gate. If there is a slew done event detected, it suggests that the opposite body diode must not be conducting and the next gate will be turned on as well. If neither the IPolarity flip event or slew done event is detected, the next gate will be turned on by the maximum dead time timer expiration. During a ZCS event, the maximum dead time is changed to 150 us.

ZCS happens due to the switching frequency being too low. Therefore, the SS pin is pulled low through a diode to ground and the system enters a "ZCS soft start" process. The switching frequency is forced to ramp up in order for the system to recover from ZCS. The details of the "ZCS soft start" are described in the Soft-Start and Burst-Mode Threshold section. If ZCS is detected in burst mode, since the switching frequency is already high, SS pin will not be pulled low and there will be no "ZCS soft start" process.

Below is the flow chart of the capacitive region prevention algorithm and the timing diagram of a ZCS event:

Feature Description (接下页)

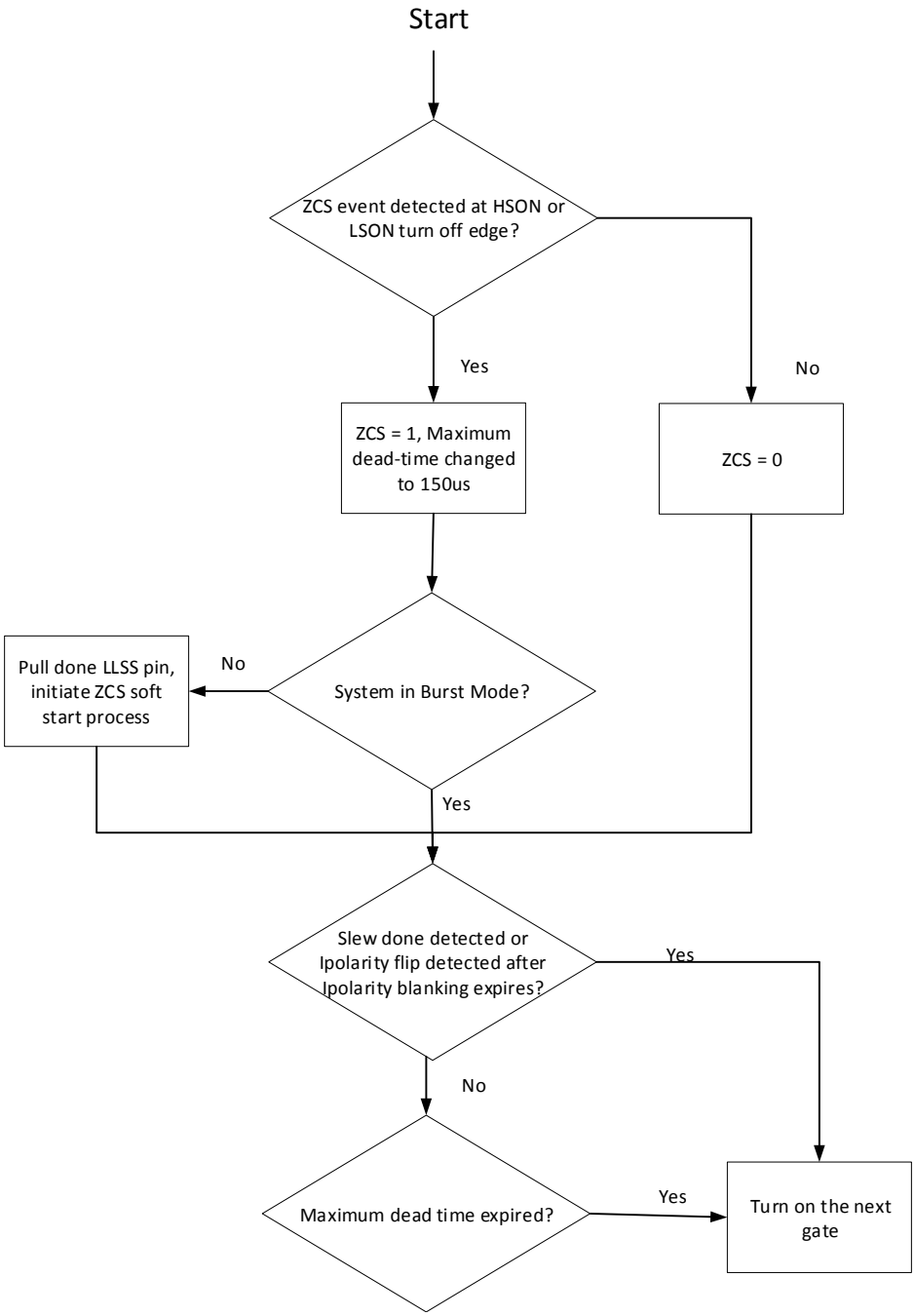


图 11. ZCS Prevention Algorithm Flow Chart

Feature Description (接下页)

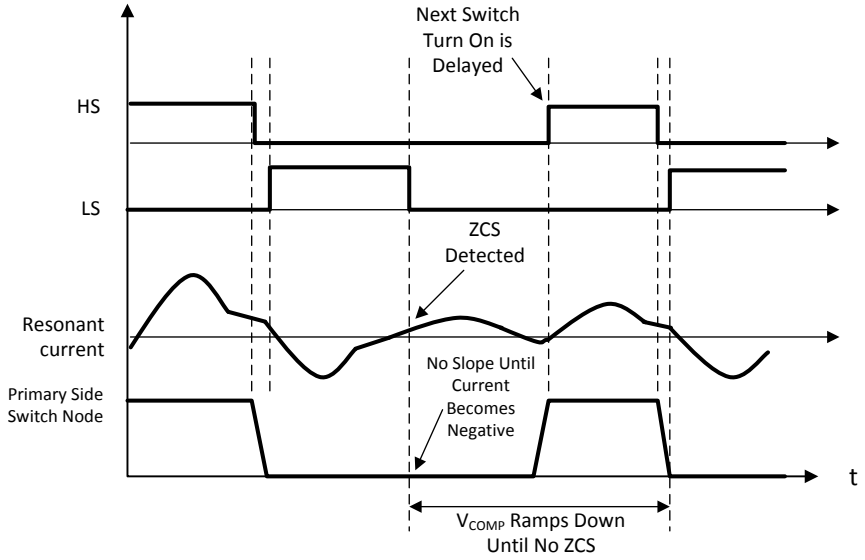


图 12. Timing Diagram of a ZCS Event

8.3.9.2 Over Current Protection (OCP)

There are three levels of OCP:

1. OCP1: peak current protection (highest threshold)
    1. Fault action: If ISNS is higher than OCP1 threshold for 4 consecutive switching cycles, the switching will stop. The system enters FAULT state, and waits for 1 s and then re-enters the startup state.
2. OCP2: average input current protection (high threshold)
    1. Fault action: If sensed ISNS average value is above the threshold for 2 ms, the switching will stop. The system enters FAULT state, and waits for 1 s and then re-enters the startup state.
3. OCP3: average input current protection (low threshold)
    1. Fault action: If sensed ISNS average value is above the threshold for 50 ms, the switching will stop. The system enters FAULT state, and waits for 1 s and then re-enters the startup state.

The circuit block diagram has been discussed in the *Resonant Current Sensing* section.

8.3.9.3 Bias Winding Over Voltage Protection (BWOVP)

This is typically used for output over voltage protection when the transformer has a bias winding. The output over voltage trip point can be set by configuring the voltage divider on the BW pin. When the BW OVP comparator is high for 5 consecutive switching cycles, the switching will stop. The system enters fault state, and waits for 1 s and then re-enters the startup state.

8.3.9.4 Input Under Voltage Protection (VINUVP)

This is the input under voltage protection. The trip point can be set by configuring the voltage divider on the BLK pin. If the BLK voltage drops below BLKStop, switching will stop immediately. The system enters FAULT state, and waits for 1 s and then re-enters the startup state.

8.3.9.5 Boot UVLO

This is the high-side gate driver UVLO. When (HB – HS) voltage is less than the threshold, the high-side gate output will be shut down. The system does not enter FAULT state.

Feature Description (接下页)

8.3.9.6 RVCC UVLO

This is the regulated 13-V UVLO. When RVCC voltage is less than the threshold, both the high-side gate output and the low-side gate output will be turned off immediately. The system enters FAULT state, and waits for 1 s and then re-enters the startup state.

8.3.9.7 Over Temperature Protection (OTP)

This is the device over temperature protection. When OTP threshold is exceeded, the switching will stop. The system enters FAULT state, and waits for 1 s and then re-enters the startup state if the temperature is back below the OTP threshold.

8.4 Device Functional Modes

8.4.1 High Voltage Start-Up

UCC256404 uses a self bias start up scheme, thus eliminating the need for a separate auxiliary supply. When AC power is first plugged in, the PFC and LLC are both off. The internal JFET on the HV pin will be enabled and will start to deliver current from a source connected from the HV pin to the VCC capacitor. The charge current is small when VCC pin voltage is below $V_{CCShort}$, and then becomes larger when VCC pin voltage is above $V_{CCShort}$.Once the VCC pin voltage exceeds its VCCStartSwitching threshold, the current source will be turned off and RVCC will be enabled to turn on the PFC. When the PFC output voltage reaches a certain level, the LLC is turned on. When the LLC is operating and the output voltage is established, the bias winding will supply current for both the PFC and the LLC controller devices.

UCC256403 does not include a high voltage start-up feature. It requires an external auxiliary supply to power on the IC. The HV pin needs to be grounded when using the UCC256403.

8.4.2 X-Capacitor Discharge

X-capacitors used in EMC filters on the AC side of the diode bridge rectifier must have a mean to allow them to discharge down to a reasonable voltage within a specific amount of time. This is to ensure that voltage does not remain present on the pins of the AC plug indefinitely after it is physically removed from the AC power.

Typically, discharge resistors are provided in parallel with the x-capacitors to provide this discharge path, but these resistors then lead to fixed standing power loss as long as the power supply is connected to AC power, and can be significant in the context of achieving very low standby power.

For every 100 nF of capacitance, a maximum bleed resistor of 10 MΩ must be added in parallel. For a typical 60-W to 100-W power supply with a typical capacitance of 330 nF, this requires 3 MΩ of discharge resistance. At nominal high line 230 V, these resistors dissipate 17.63 mW of standing power loss. Thus it is necessary to find alternative ways to discharge the x-capacitors using switched discharge paths in order to avoid the static standing loss.

There are several standards for x-capacitor discharge. IEC60950 and IEC60065 requires that the discharge time constant is less than 1s. IEC62368 requires that after 2 seconds of AC unplug, the remaining voltage on the x-capacitor is less than 60 V (for 300 nF or more capacitance). UCC256404 uses an active discharge scheme to support the fast discharge of up to 5-μF x-capacitance.

To meet the requirements of the standards, AC disconnect events must be detected. UCC256404 detects AC disconnect by monitoring the AC zero crossings through the HV pin. When AC is present, there will be two AC zero crossings in one line cycle. When AC is disconnected, there will be no zero crossings for an extended period of time. 图 13 shows the rectified AC waveform. In the figure, the AC is disconnected at the peak of the last half AC cycle. In reality, it can be disconnected anywhere within a switching cycle.

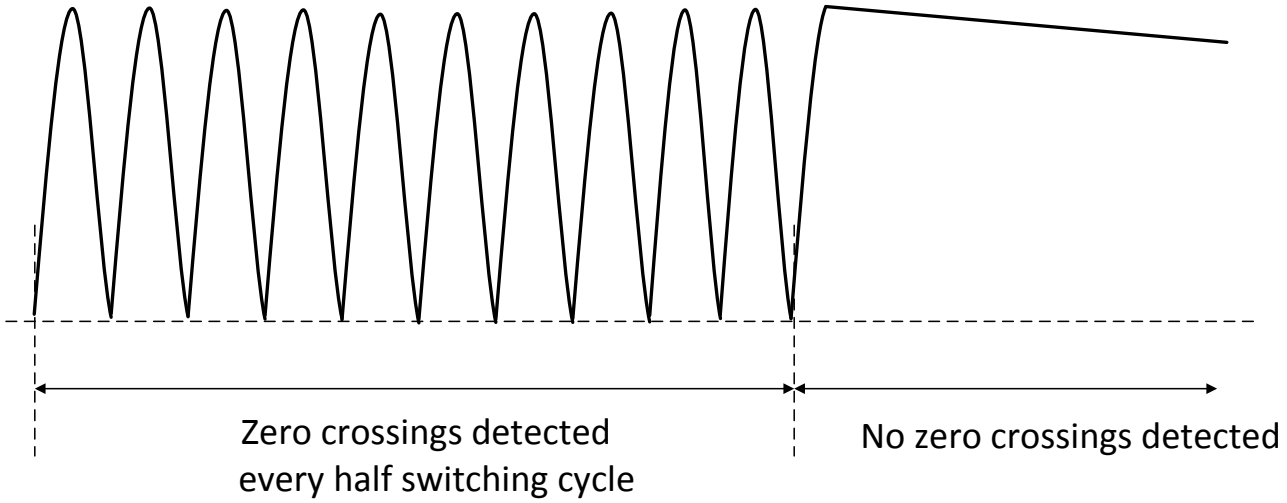


图 13. AC Disconnect Waveform

Device Functional Modes (接下页)

To detect the zero crossings reliably as well as save power consumption, a staircase test current is generated every 700 ms. When there are 4 zero crossings missing in a row at the highest test current setting, AC disconnect is confirmed and the IXCapDischarge current source is enabled. The waveform below shows the staircase current waveform:

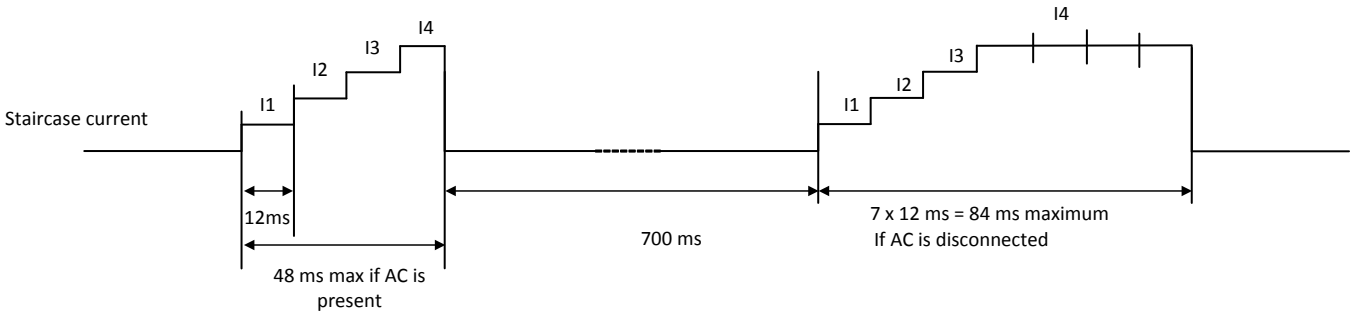


图 14. Staircase Test Current for X-Capacitor Discharge

The test current is required for reliable AC zero crossing sensing. In short, this is because the leakage current in the AC bridge rectifier diodes will affect the zero crossing detection at very light load. The added test current on the HV pin will overcome the leakage current and make sure that AC zero crossing is detected on the HV pin. If one zero crossing is detected during any test current stage, it means that AC is not disconnected. The test current will shut off immediately and the system goes to the 700-ms no test current stage.

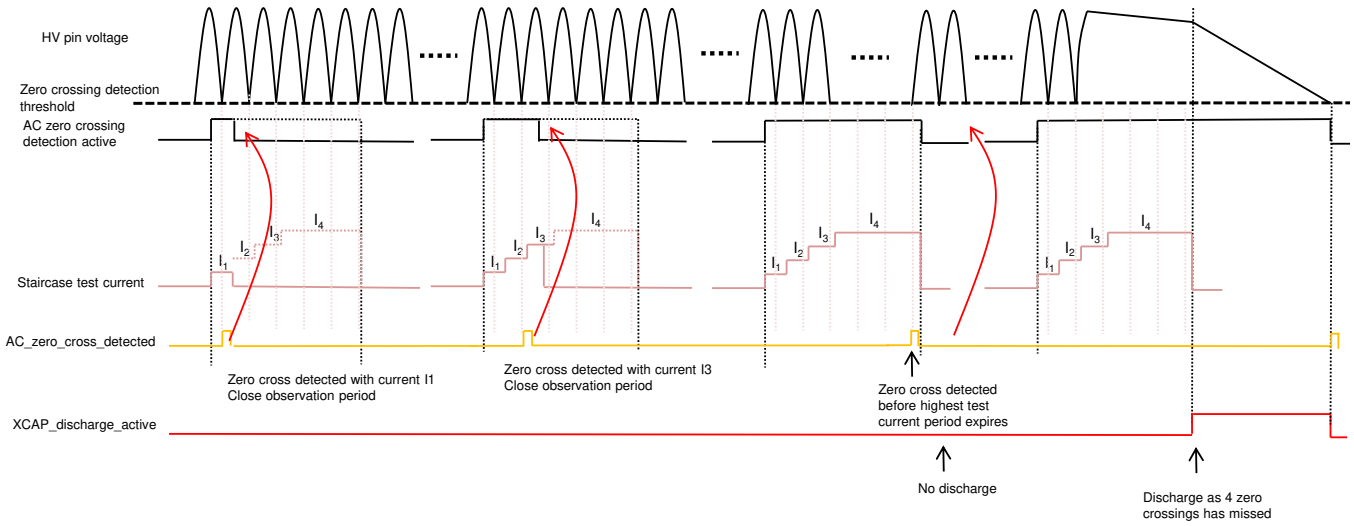


图 15. Different Staircase Current Waveforms

图 15 shows different staircase current waveforms. The last waveform shows the AC disconnect is detected and x-capacitor discharge current is enabled. The x-capacitor discharge current is enabled for 350 ms. AC zero crossing function is available in all operation modes and available all the time. 图 16 shows the flow chart of AC zero crossing detection and x-capacitor discharge. The zero crossing test starts 12 ms after HV startup is completed. The discharge current IXCapDischarge is created by turning on the JFET and enabling a current source from JFET source to GND. During a fault restart process, HV startup is higher priority, so that the JFET is connected to VCC. A zero crossing test current will be sent out 12 ms after HV startup is completed, regardless of whether the detection idle timer has expired.

UCC256403 does not have a x-capacitor discharge feature. The HV pin needs to be grounded for normal operation when using the UCC256403 IC variant.

ADVANCE INFORMATION

Device Functional Modes (接下页)

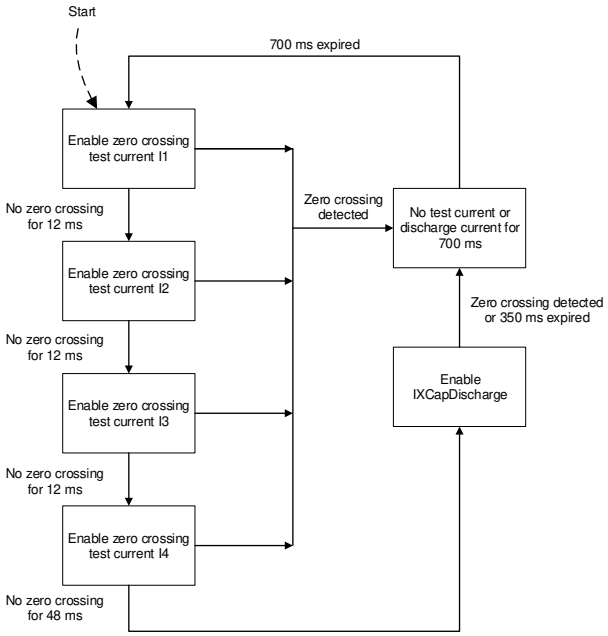


图 16. AC ZCD and X-Capacitor Discharge Flow Chart

8.4.3 Burst Mode Control

The efficiency of an LLC converter power stage drops rapidly with falling output power. To maintain reasonable light load efficiency it is necessary to operate the LLC converter in burst mode. In this mode the LLC converter operates at relatively high power for a short burst period and then switching is stopped for a time period. During the burst period excess charge is transferred to and stored in the output capacitor. During the burst off period this stored charge is used to supply the load current. The burst mode operation is critical to meet strict standby power consumption requirements. But a challenge with burst mode operation is the audible noise performance. Due to the need to stop switching for certain time, there will be a pattern of switching pulses with the frequency that fall within the audible frequency range from 20 Hz to 20 kHz. UCC25640x includes a burst mode with soft on and soft off periods at the first few and last few switching pulses, minimizing the audible noise during standby operation.

图 17 describes the timing diagram of the burst mode operation. Two burst mode thresholds are used (BMT_H for burst mode exit and BMT_L for burst mode entry). The details of how to program these two thresholds are described in Soft-Start and Burst-Mode Threshold section. The FBreplica from the FB chain is compared with the two thresholds, and determines the burst mode operation.

- At t_1, FBreplica is below BMT_L. The system enters burst mode and stops switching immediately. During the burst off period, UCC25640x disables some internal blocks to save power consumption.
- At t_2, FBreplica is above BMT_H. The system starts to switch again, and this period is referred to burst on period. During burst on period, the control effort V_{comp} sent to the VCR comparator is the higher value of FBreplica and BMT_L. For the first switching pattern after the system enters burst mode, there is no burst soft on.
- At t_3, FBreplica falls below BMT_L again. Switching will not stop until it reaches the predefined number (40) of a burst packet. The V_{comp} still selects the higher value of FBreplica and BMT_L. For the last 7 switching cycles, soft off will be applied (only 3 soft on/off steps are shown in 图 17 for conceptual introduction). The V_{comp} is a fraction of the higher value between FBreplica and BMT_L. The number of fractions for different switching cycles are described in 表 1. For burst soft off, it starts from step 7 and ramps down. After it reaches step 1, soft off steps are completed and the system enters burst off period. This helps to achieve slow ramping down of the LLC transformer current. For burst soft on, it reverses the direction by starting from step 1 and ends at step 7. If FBreplica becomes greater than BMT_L before the soft off steps are completed, the burst soft off will end immediately and the system transitions to burst soft on. In this condition, the soft on step starts from the

ADVANCE INFORMATION

Device Functional Modes (接下页)

step where soft off ends at, to ensure a smooth transition between soft off and soft on.

- At t_4, FBreplica is greater than BMT_L. The system enters burst on period, and since this is not the first burst on period, there is soft on period at the first 7 switching cycles. The fraction of Vcomp to the higher value of FBreplica and BMT_L is also described in 表 1. After burst soft on steps are completed, Vcomp uses the higher value of FBreplia and BMT_L until it reaches burst soft off periods.
- At t_5, FBreplica is greater than BMT_L again after another burst off period. This time the difference is that FBreplica is greater than BMT_H at t_6, when the burst soft on steps are not completed yet. The burst soft on will get terminated immediately, so that V_{comp} can follow the FBreplica. This is to ensure a quick system response during a load transient from burst mode operation to out-of-burst mode operation.

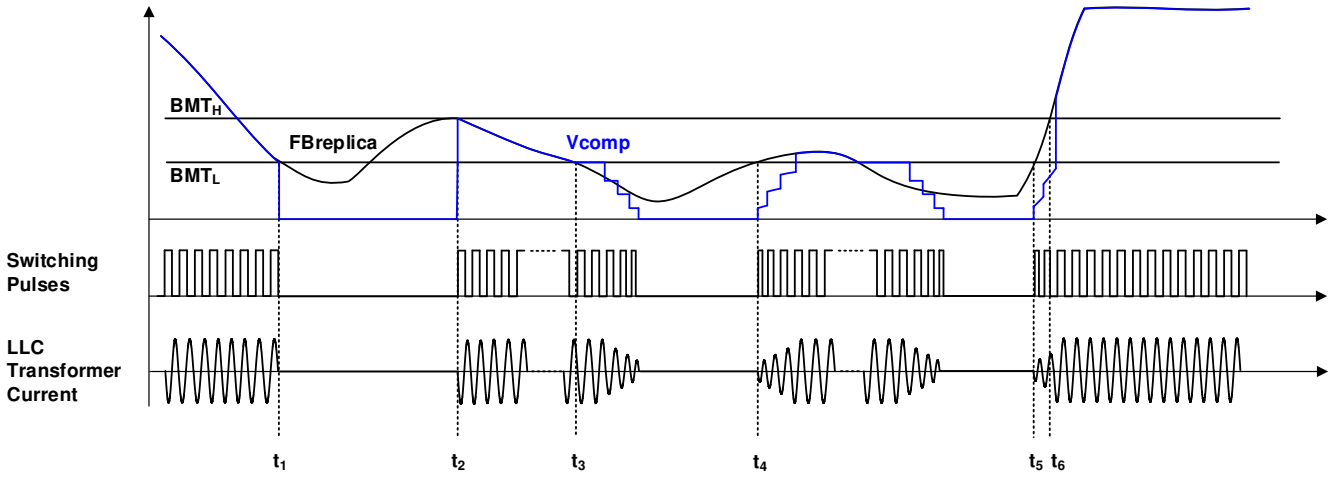


图 17. Burst Mode Switching Pattern

表 1. Burst Mode Soft On and Soft Off V_{comp} Control

Burst Soft On and Soft Off Step	Fraction used for Reduced V_{comp} During Soft On
1	1/3
2	9/21
3	11/21
4	13/21
5	15/21
6	17/21
7	19/21

The HHC control makes the implementation of the burst soft on and soft off very straight forward. Due to the frequency control portion in HHC, changing the V_{comp} can directly impact the LLC switching frequency to control the resonant current magnitude within switching cycles. Also the last pulse of each burst on period is turned off when the VCR node voltage equals the common mode voltage VCM. In HHC control, this is approximately equivalent to resonant capacitor voltage equal to $V_{IN}/2$. This operation keeps the resonant capacitor voltage to about $V_{IN}/2$ for each burst off period, thus enabling the burst pattern to settle as soon as possible during the burst on period.

ADVANCE INFORMATION

8.4.3.1 Soft-Start and Burst-Mode Threshold

The soft-start programming and burst mode threshold programming are multiplexed on the pin LL/SS. In addition, when ZCS region operation happens, this pin is pulled down to ground through a diode to increase the switching frequency. The pin block diagram is shown in 图 18.

图 19 shows the timing diagram of the LL/SS pin programming. It includes 5 phases:

- SS pin initial voltage programming/settling phase - during this phase, the SS pin is buffered at 5V. The current sourcing from the pin is internally mirrored to flow through R_{FB} with a 4 µA bias current. The voltage on R_{FB} is stored and then used for SS pin initial voltage. This time period is also used to program the ratio of BMT_L/BMT_H.
- SS pre-charge phase - the stored R_{FB} voltage is buffered to the SS pin as the initial voltage for soft start.
- Soft start phase - An internal constant current source charges the soft start capacitor right after the charge boot stage, and ends when FBreplica becomes lower than the SS pin voltage.
- BMT_L settling phase - BMT_L is determined by the ratio of BMT_L/BMT_H set during the SS pin initial voltage program/settling phase. During this phase, BMT_H is maintained at 0.6 V.
- BMT_L and BMT_H programming/setting phase - during this phase, BMT_H first ramps to the target value programmed by the resistor divider on the LL/SS pin. The pin is buffered at 3.5 V. The current sink to the pin is internally mirrored to flow through R_{FB}, and the voltage on R_{FB} is used for BMT_H. BMT_L follows BMT_H with the programmed ratio.

The programmability of the SS initial voltage provides a freedom to limit the maximum switching frequency during startup. This can help to prevent hard switching due to excessively high switching frequency. The flexibility on burst mode threshold programming makes it much easier to optimize efficiency of the LLC.

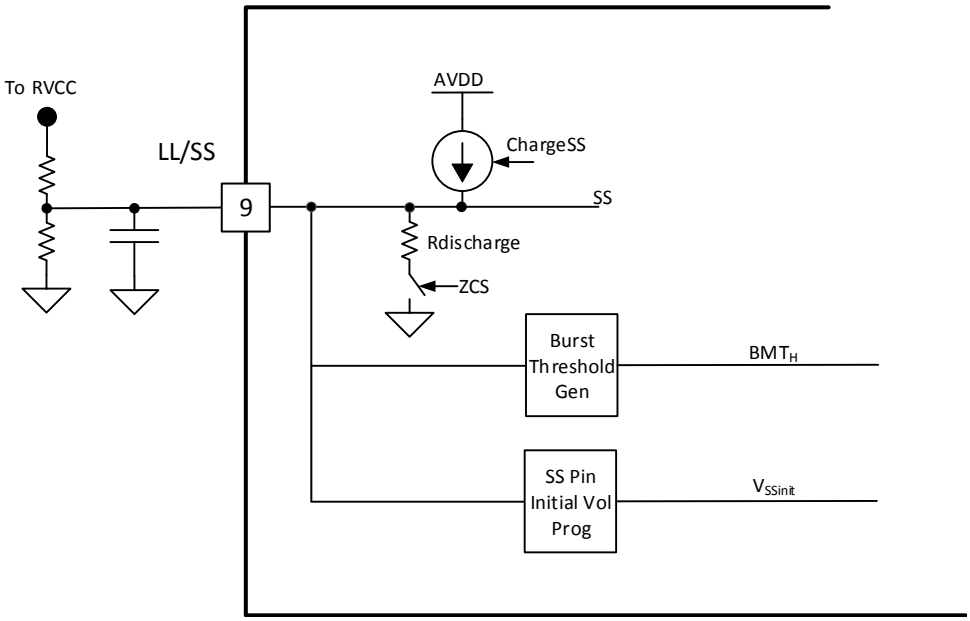


图 18. LL/SS Block Diagram

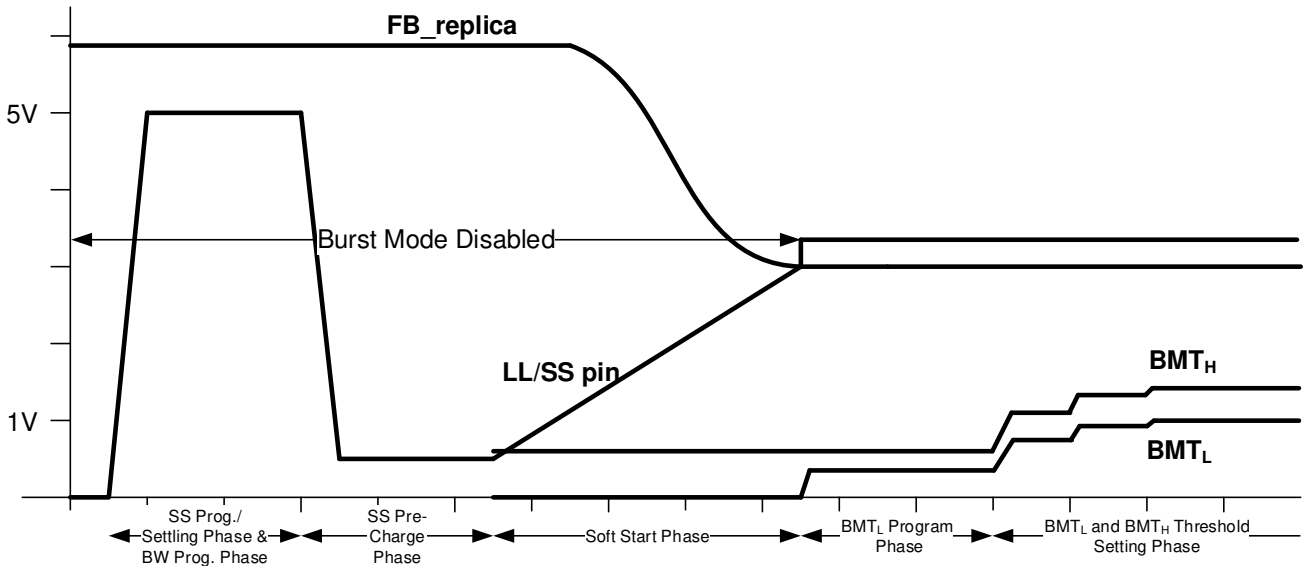


图 19. Timing Diagram of LL/SS Pin Programming

8.4.3.2 BMT_L/BMT_H Ratio Programming

During the SS programming/settling phase mentioned in Soft-Start and Burst-Mode Threshold section, the BW pin is used to program the ratio of BMT_L/BMT_H. It sources a constant 54 µA and measures the voltage on the pin. 表 2 lists the different ratio of BMT_L/BMT_H provided by the BW pin programming. The required BW equivalent resistance is listed in electrical characteristics section.

For Option 7, burst mode is disabled. In this case, even the burst entry criteria - FBreplica less than BMT_L is met and the system will continue switching without entering the burst mode. BMT_L/BMT_H ratio will be set at 1. V_{comp} still selects the higher value between BMT_L and FBreplica. Therefore, the burst mode threshold in this case is used to limit the maximum switching frequency of the LLC.

表 2. BMT_L/BMT_H Ratio Programming

Option	BMT_L/BMT_H
1	0.95
2	1
3	0.9
4	0.8
5	0.6
6	Minimal
7	1 (Burst Mode Disabled)

ADVANCE INFORMATION

8.4.4 System State Machine

Below is an overview of the system states sequence:

The state transition diagram starts from the un-powered condition of UCC25640x. For UCC256404, as soon as the AC input is plugged in, the internal JFET of the HV pin will be enabled and will start to deliver current from a source connected from the HV pin to the VCC capacitor. Once the VCC pin voltage exceeds its VCCStartSwitching threshold, the system state will change to JFETOFF. For UCC256403 which does not have HV startup feature, there is no JFETon state. Once VCC exceeds its VCCStartSwitching threshold, the system state will change to JFETOFF. When the PFC output voltage reaches a certain level, the LLC is turned on. Before the LLC starts running, the LO pin is kept high to pull the HS node of the LLC bridge low, thus allowing the capacitor between the HB and HS pins to be charged from VCC via the bootstrap diode. UCC25640x will remain in the CHARGE_BOOT state for a certain time to ensure the boot capacitor is fully charged. When the LLC output voltage reaches a certain level, both PFC and LLC controllers get power from the LLC transformer bias winding. When the load drops below a certain level, the LLC operates in burst mode.

Fault conditions encountered by UCC25640x will cause normal operation to stop, or pause for a certain period of time followed by an automatic re-start. This is to ensure that while a persistent fault condition is present, it is not possible for UCC25640x or the power converter temperature to continue to rise as a result of the repeated re-start attempts.

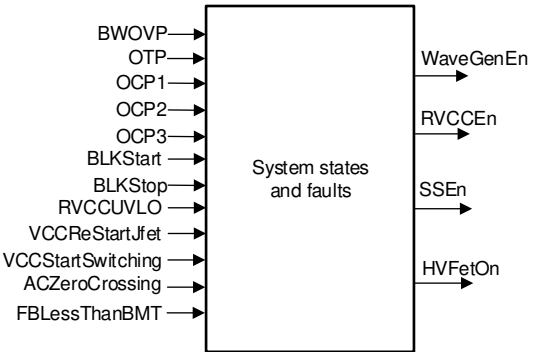


图 20. Block Diagram of System State Machine

ADVANCE INFORMATION

表 3 summarizes the inputs and outputs of 图 20.

表 3. System State Machine Block Inputs and Outputs

SIGNAL NAME	I/O	DESCRIPTION
BWOVP	I	Output over voltage fault
OTP	I	Over temperature fault
OCP1	I	Peak current fault
OCP2	I	Average current fault with 2ms timer
OCP3	I	Average current fault with 50ms timer
BLKStart	I	Bulk voltage is above start threshold
BLKStop	I	Bulk voltage is below stop threshold
RVCCUVLO	I	RVCC UVLO fault
VCCReStartJfet	I	VCC is below restart threshold
VCCStartSwitching	I	VCC is above start switching threshold (the threshold is different in UCC256403 and UCC256404)
ACZeroCrossing	I	AC zero crossing is detected
WaveGenEn	O	Waveform generator enable
RVCCEn	O	RVCC enable
SSEn	O	Soft start enable
HVFetOn	O	Turn on or off JFET

The state machine is shown in 图 21 and the description of the states and state transition conditions are in the tables below.

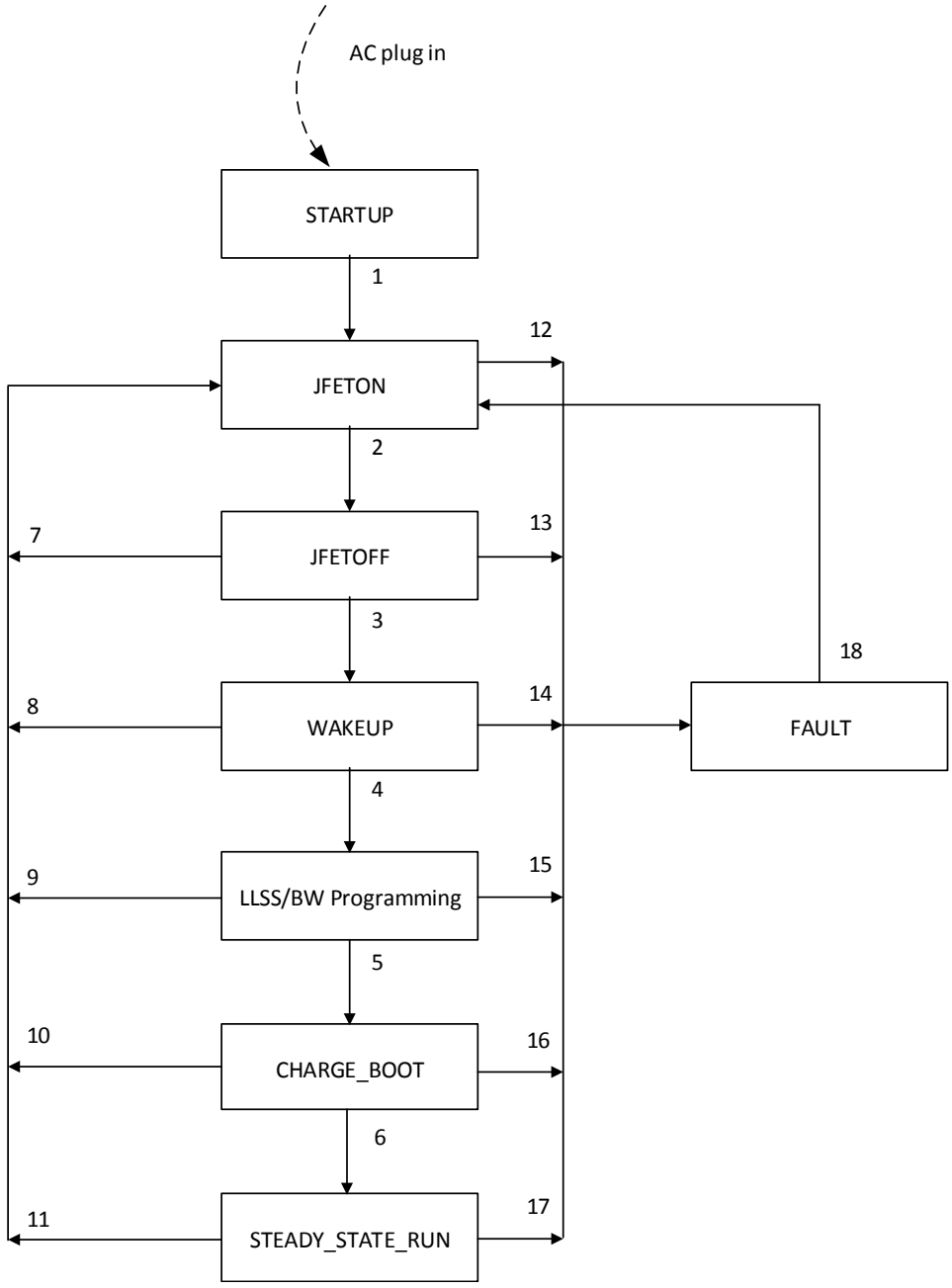


图 21. System State Machine Transition

表 4. States in System State Machine

STATE	OUTPUT STATUS	DESCRIPTION
STARTUP	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 0	This is the first state after AC input is plugged-in for the system to load trim.
JFETON	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 1	In this state, the JFET is on. VCC is charged with a current source connected from HV pin. For UCC256403, this state does not exist as there is no HV startup feature.
JFETOFF	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	When VCC is higher than VCCStartSwitching threshold, the JFET is turned off and the system enters JFETOFF state. The regulated RVCC is turned on. If RVCC is supplied to PFC voltage supply pin, PFC soft start begins.
WAKEUP	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	When BLK voltage reaches BLKStart level, the system enters WAKEUP state and stays in WAKEUP state for a short time for the analog circuits to wake up.
LLSS/BW Programming	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	In this state, the system goes through the LL/SS pin and BW pin programming phase.
CHARGE_BOOT	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	In this state, the BOOT capacitor is charged by turning on the low-side switch for a certain period of time. The programmed initial voltage is buffered to SS pin.
STEADY_STATE_RUN	WaveGenEn = 1 RVCCEn = 1 SSEn = 1 HVFetOn = 0	In this state, the waveform generator is enabled. Soft start module is enabled. The LLC starts to soft start. When soft start is done, the system enters normal operation.
FAULT	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 0	In fault state, the waveform generator is disabled to stop switching. The system will stay in FAULT state for 1s before re-start. The 1s timer allows the system to cool down and prevents frequent repetitive start ups in case of a persistent fault.

ADVANCE INFORMATION

表 5. System State Machine Transition Conditions

STATE TRANSITION CONDITION	DESCRIPTION
1	System ready (trim load done)
2	VCCStartSwitching = 1 VCCReStartJfet = 0
3	BLKStart = 1 BLKStop = 0 RVCCUVLO = 0
4	BLKStart = 1 BLKStop = 0 RVCCUVLO = 0 FBLessThanBMT = 0
5	LLSS/BW programming done
6	Charge boot done
7	VCCReStartJfet = 1
8	VCCReStartJfet = 1
9	VCCReStartJfet = 1
10	VCCReStartJfet = 1
11	VCCReStartJfet = 1
12	OTP = 1
13	OTP = 1
14	OTP = 1
15	OTP = 1
16	OTP = 1
17	OTP = 1 or BLKStop = 1 or BWOVP = 1 or OCP1 = 1 or OCP 2 = 1 or OCP3 = 1 or RVCCUVLO = 1
18	1s pause time out

图 22 and 图 23 show the most commonly used state transition (assuming no faults during start up states so all the states are captured in the timing diagram) for UCC256403 and UCC256404, respectively. Many different ways of state transitions may happen according to the state machine, but are not captured in this section.

In 图 23, a normal start up procedure is shown. The system enters normal operation and then a fault (OCP, OVP, or OTP) happens.

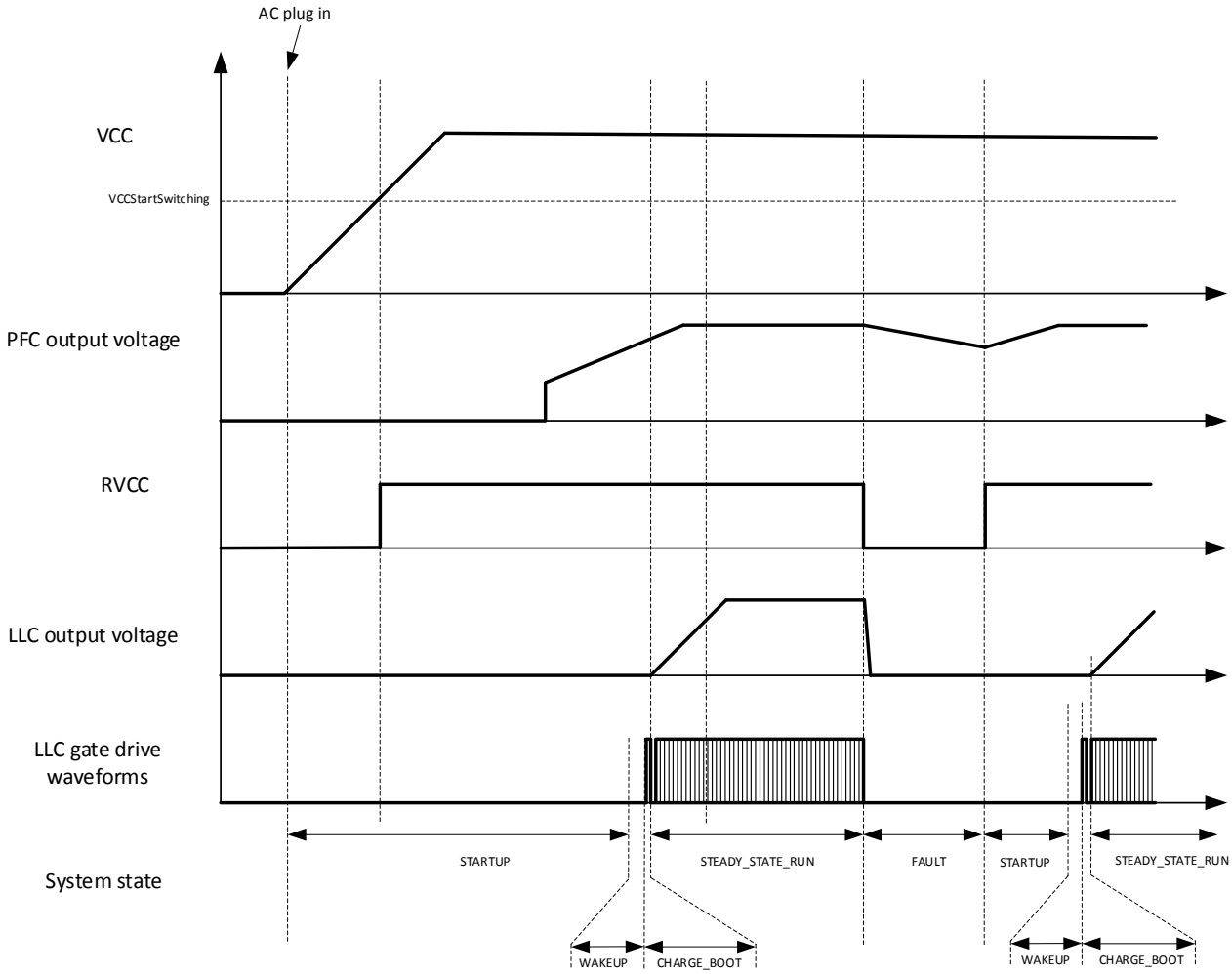


图 22. Timing Diagram of System State Machine for UCC256403

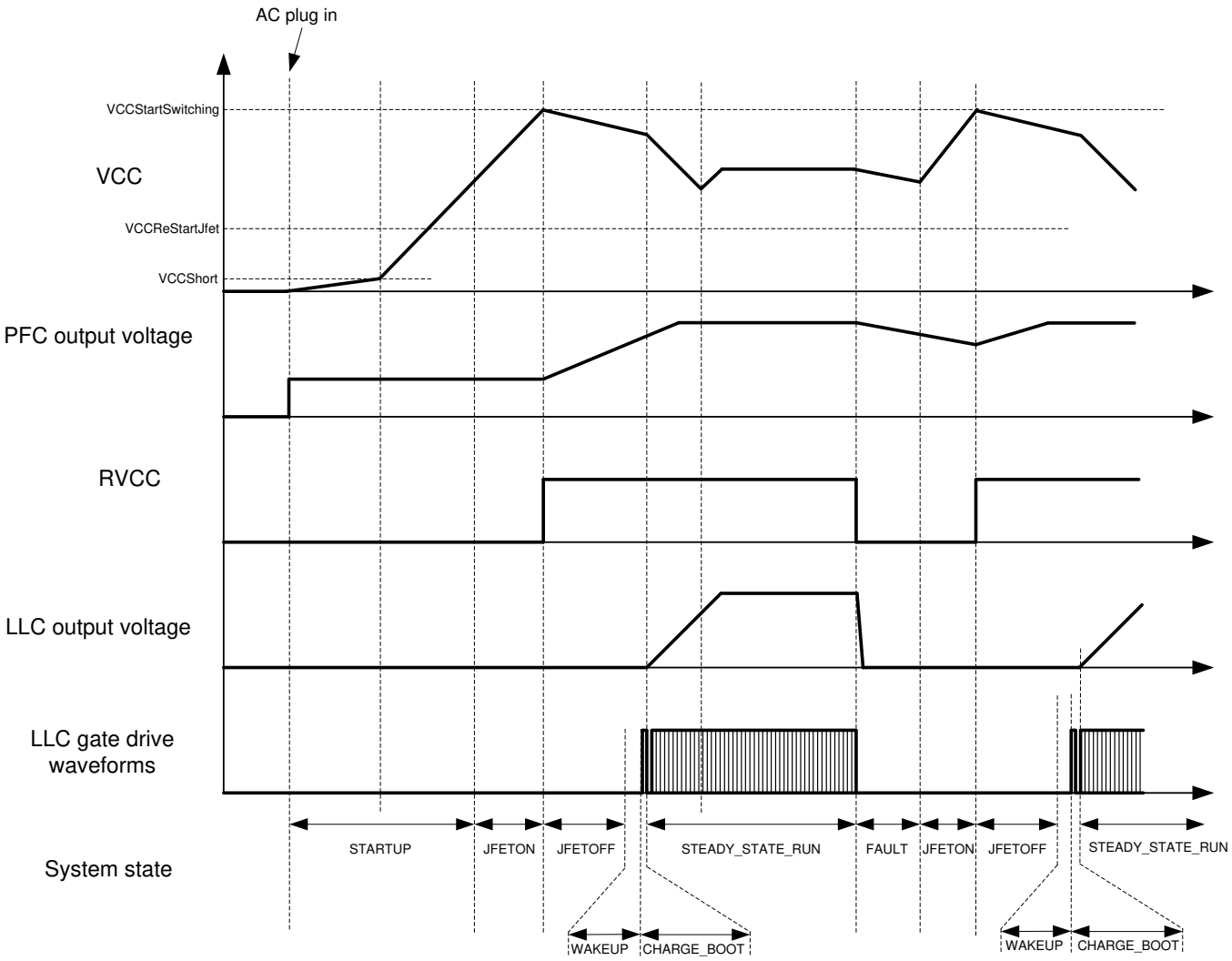


图 23. Timing Diagram of System State Machine for UCC256404

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

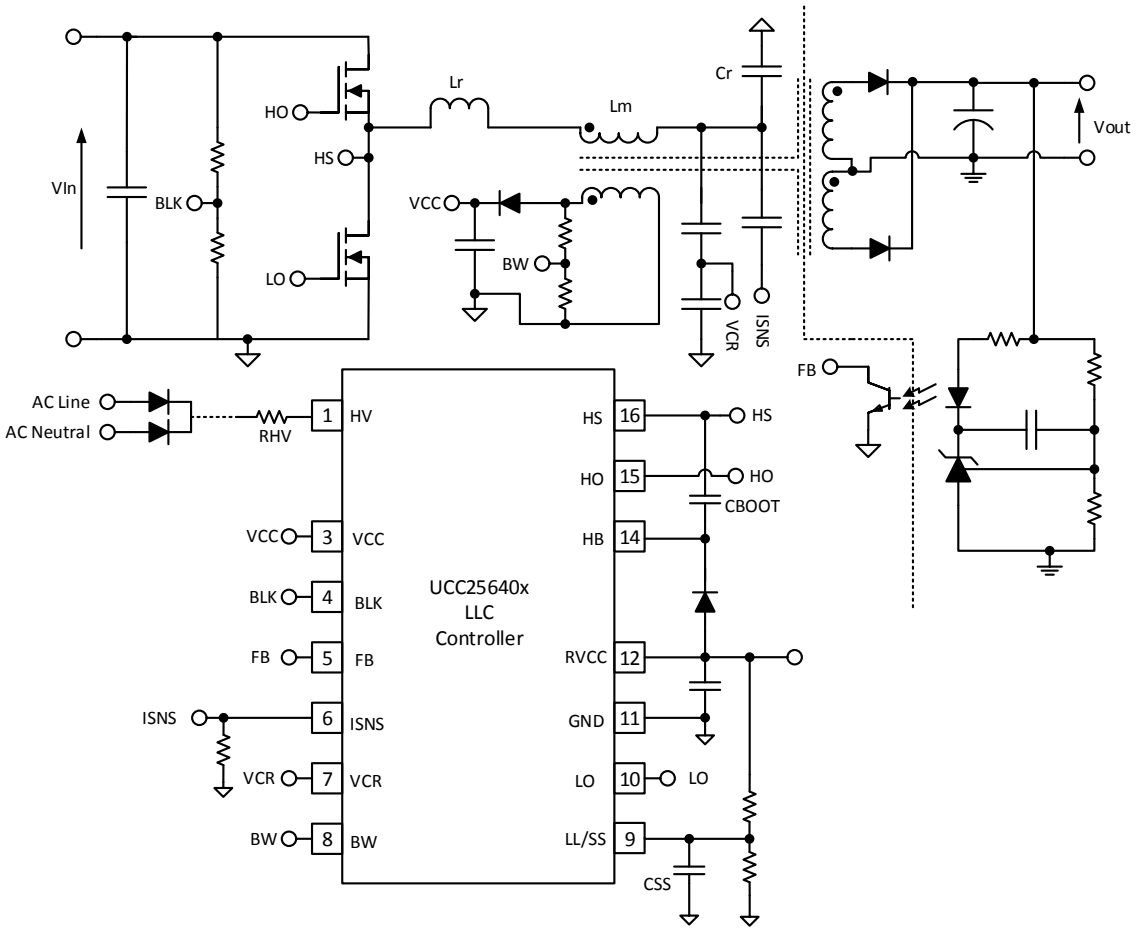
UCC25640x can be used in a wide range of applications in which LLC topology is implemented. In order to make the part easier to use, TI has prepared a list of materials to demonstrate the features of the device:

- Full featured EVM hardware
- A excel design calculator
- Simulation models
- Application notes on Hybrid Hysteretic Control theory

In the following sections, a typical design example is presented.

9.2 Typical Application

Shown below is a typical half bridge LLC application using UCC25640x as the controller.



ADVANCE INFORMATION

Typical Application (接下页)

9.2.1 Design Requirements

The design specifications are summarized in 表 6.

表 6. System Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
DC Voltage range		360	390	410	VDC
AC Voltage range		85		264	VAC
AC Voltage frequency		47		63	Hz
Input DC UVLO On			360		VDC
Input DC UVLO Off			310		VDC
OUTPUT CHARACTERISTICS					
Output voltage, VOUT	No load to full load		12		VDC
Output load current, IOUT	360 VDC to 410 VDC			15	A
Output voltage ripple	390 VDC and full load = 10 A		120		mVpp
SYSTEMS CHARACTERISTICS					
Resonant Frequency			100		kHz
Peak efficiency	390 VDC		92		
Operating temperature	Natural convection		25		ºC

ADVANCE INFORMATION

9.2.2 Detailed Design Procedure

9.2.2.1 LLC Power Stage Requirements

Start the design by deciding the LLC power stage component values. The LLC power stage design procedure outlined here follows the one given in the TI application note “Designing an LLC Resonant Half-Bridge Power Converters”. The application note contains a full explanation of the origin of each of the equations used. The equations given below are based on the First Harmonic Approximation (FHA) method commonly used to analyze the LLC topology. This method gives a good starting point for any design, but a final design requires an iterative approach combining the FHA results, circuit simulation, and hardware testing. An alternative design approach is given in TI application note SLUA733, LLC Design for UCC29950.

9.2.2.2 LLC Gain Range

First, determine the transformer turns ratio by the nominal input and output voltages.

$$n = \frac{V_{IN(nom)} / 2}{V_{OUT(nom)}} = \frac{390 / 2}{12} = 16.25 \Rightarrow 16.5 \tag{4}$$

Then determine the LLC gain range $M_{g(min)}$ and $M_{g(max)}$. Assume there is a 0.5-V drop in the rectifier diodes (V_f) and a further 0.5-V drop due to other losses (V_{loss}).

$$M_{g(\min)} = n\frac{V_{OUT(min)} + V_f}{V_{IN(max)} / 2} = 16.5\frac{12 + 0.5}{410 / 2} = 1.006 \tag{5}$$

$$M_{g(\max)} = n\frac{V_{OUT(max)} + V_f + V_{\text{loss}}}{V_{IN(min)} / 2} = 16.5\frac{12 + 0.5 + 0.5}{360 / 2} = 1.192 \tag{6}$$

9.2.2.3 Select L_n and Q_e

L_n is the ratio between the magnetizing inductance and the resonant inductance.

$$L_n = \frac{L_m}{L_r} \tag{7}$$

Q_e is the quality factor of the resonant tank.

$$Q_e = \frac{\sqrt{L_r / C_r}}{R_e} \tag{8}$$

In this equation, R_e is the equivalent load resistance.

Selecting L_n and Q_e values should result in an LLC gain curve, that intersects with $M_{g(min)}$ and $M_{g(max)}$ traces. The peak gain of the resulting curve should be larger than $M_{g(max)}$. Details of how to select L_n and Q_e are not discussed here. They are available in the UCC25640x Design Calculator.

In this case, the selected L_n and Q_e values are:

$$L_n = 6 \tag{9}$$

$$Q_e = 0.3 \tag{10}$$

ADVANCE INFORMATION

9.2.2.4 Determine Equivalent Load Resistance

Determine the equivalent load resistance by 公式 11.

$$R_e = \frac{8 \times n^2}{\pi^2} \times \frac{V_{OUT(nom)}}{I_{OUT(nom)}} = \frac{8 \times 16.5^2}{\pi^2} \times \frac{12}{15} = 177\Omega \tag{11}$$

9.2.2.5 Determine Component Parameters for LLC Resonant Circuit

Before determining the resonant tank component parameters, a nominal switching frequency (resonant frequency) should be selected. In this design, 100 kHz is selected as the resonant frequency.

$$f_0 = 100\,kHz \tag{12}$$

The resonant tank parameters can be calculated as the following:

$$C_r = \frac{1}{2\pi \times Q_e \times f_0 \times R_e} = \frac{1}{2\pi \times 0.3 \times 100\,kHz \times 177\,\Omega} = 30.0nF \tag{13}$$

$$L_r = \frac{1}{(2\pi \times f_0)^2 C_r} = \frac{1}{(2\pi \times 100\,kHz)^2 \times 30.0\,nF} = 84.4\,\mu H \tag{14}$$

$$L_m = L_n \times L_r = 6 \times 84.4\,\mu H = 506.4\,\mu H \tag{15}$$

After the preliminary parameters are selected, find the closest actual component value that is available, re-check the gain curve with the selected parameters, and then run time domain simulation to verify the circuit operation.

The following resonant tank parameters are:

$$C_r = 30\,nF \tag{16}$$

$$L_r = 85\ \mu H \tag{17}$$

$$L_m = 510\,\mu H \tag{18}$$

Based on the final resonant tank parameters, the resonant frequency can be calculated:

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi\sqrt{30\,nF \times 85\,\mu H}} = 97.7\,kHz \tag{19}$$

Based on the new LLC gain curve, the normalized switching frequency at maximum and minimum gain are given by:

$$f_{n(Mgmax)} = 0.65 \tag{20}$$

$$f_{n(Mgmin)} = 1.05 \tag{21}$$

The maximum and minimum switching frequencies are:

$$f_{SW(Mgmin)} = 64.8kHz \tag{22}$$

$$f_{SW(Mgmax)} = 104.7\,kHz \tag{23}$$

ADVANCE INFORMATION

9.2.2.6 LLC Primary-Side Currents

The primary-side currents are calculated for component selection purpose. The currents are calculated based on a 110% overload condition.

The primary side RMS load current is given by:

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \times \frac{I_o}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 15\,A}{16.5} = 1.11\,A \tag{24}$$

The RMS magnetizing current at minimum switching frequency is given by:

$$I_m = \frac{2\sqrt{2}}{\pi} \times \frac{nV_{OUT}}{\omega L_m} = \frac{2\sqrt{2}}{\pi} \times \frac{16.5 \times 12}{2\pi \times 64.8\,kHz \times 510\,\mu H} = 0.859\,A \tag{25}$$

The total current in resonant tank is given by:

$$I_r = \sqrt{I_m^2 + I_{oe}^2} = \sqrt{(1.111\,A)^2 + (0.859\,A)^2} = 1.404\,A \tag{26}$$

9.2.2.7 LLC Secondary-Side Currents

The total secondary side RMS load current is the current referred from the primary side current (I_{oe}) to the secondary side.

$$I_{oes} = n \times I_{oe} = 16.5 \times 1.111\,A = 18.332\,A \tag{27}$$

In this design, the transformer's secondary side has a center-tapped configuration. The current of each secondary transformer winding is calculated by:

$$I_{ws} = \frac{\sqrt{2} \times I_{oes}}{2} = \frac{\sqrt{2} \times 18.332\,A}{2} = 12.963\,A \tag{28}$$

The corresponding half-wave average current is:

$$I_{sav} = \frac{\sqrt{2} \times I_{oes}}{\pi} = \frac{\sqrt{2} \times 18.332\,A}{\pi} = 8.252\,A \tag{29}$$

9.2.2.8 LLC Transformer

A bias winding is needed in order to utilize the HV self start up function. It is recommended to design the bias winding so that the VCC voltage is greater than 13 V.

The transformer can be built or purchased according to these specifications:

- Turns ratio: Primary : Secondary : Bias = 33 : 2 : 3
- Primary terminal voltage: 450Vac
- Primary magnetizing inductance: L_M = 510 µH
- Primary side winding rated current: I_r = 1.404 A
- Secondary terminal voltage: 36V_{ac}
- Secondary winding rated current: I_{ws} = 12.963 A
- Minimum switching frequency: 64.8 kHz
- Maximum switching frequency: 107.6 kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

The minimum operating frequency during normal operation is calculated above but during shutdown the LLC can operate at right above ZCS boundary condition, which is a lower frequency. The magnetic components in the resonant circuit, the transformer and resonant inductor, should be rated to operate at this lower frequency.

ADVANCE INFORMATION

9.2.2.9 LLC Resonant Inductor

The AC voltage across the resonant inductor is given by its impedance times the current:

$$V_{L_R} = \omega L_R I_R = 2\pi \times 64.8\text{kHz} \times 85\mu\text{H} \times 1.404\text{A} = 48.589V \quad (30)$$

The inductor can be built or purchased according to the following specifications:

- Inductance: L_r = 85 µH
- Rated current: I_r = 1.404 A
- Terminal AC voltage:
- Frequency range: 64.8 kHz to 107.6 kHz

The minimum operating frequency during normal operation is that calculated above but during shutdown the LLC can operate at right above ZCS boundary condition, which is a lower frequency. The magnetic components in the resonant circuit, the transformer and resonant inductor, should be rated to operate at this lower frequency.

9.2.2.10 LLC Resonant Capacitor

This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

The AC voltage across the resonant capacitor is given by its impedance times the current.

$$V_{CR} = \frac{I_r}{\omega C_r} = \frac{1.404\text{A}}{2\pi \times 64.8\text{kHz} \times 30\text{nF}} = 114.95V \quad (31)$$

$$V_{CR(rms)} = \sqrt{\left(\frac{V_{IN(max)}}{2}\right)^2 + V_{CR}^2} = \sqrt{\left(\frac{410}{2}\right)^2 + 114.95^2} = 235V \quad (32)$$

Peak voltage:

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2}V_{CR} = \frac{410}{2} + \sqrt{2} \times 114.95 = 367.6V \quad (33)$$

Valley voltage:

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2}V_{CR} = \frac{410}{2} - \sqrt{2} \times 114.95 = 42.4V \quad (34)$$

Rated current:

$$I_r = 1.404\,A \quad (35)$$

9.2.2.11 LLC Primary-Side MOSFETs

Each MOSFET sees the input voltage as its maximum applied voltage. Choose the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage:

$$V_{QLLC(peak)} = 1.5 \times V_{IN(max)} = 615V \quad (36)$$

Choose the MOSFET current rating to be 1.1 times of the maximum primary side RMS current:

$$I_{QLLC} = 1.1 \times I_r = 1.544\,A \quad (37)$$

9.2.2.12 LLC Rectifier Diodes

The voltage rating of the output diodes is given by:

$$V_{DB} = 1.2 \times \frac{V_{IN(max)}}{n} = 1.2 \times \frac{410}{16.5} = 29.82V \quad (38)$$

The current rating of the output diodes is given by:

$$I_{SAV} = \frac{\sqrt{2} \times I_{oes}}{\pi} = \frac{\sqrt{2} \times 18.332}{\pi} = 8.252\,A \quad (39)$$

ADVANCE INFORMATION

9.2.2.13 LLC Output Capacitors

The LLC converter topology does not require an output filter although a small second stage filter inductor may be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the rectifier's full wave output current then the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} I_{OUT} = \frac{\pi}{2\sqrt{2}} \times 15 = 16.66\,A \tag{40}$$

Use 20 V rating for 12-V output voltage:

$$V_{LLCcap} = 20\,V \tag{41}$$

The capacitor's RMS current rating is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{OUT}\right)^2 - I_{OUT}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 15\right)^2 - 15^2} = 7.25\,A \tag{42}$$

Solid Aluminum capacitors with conductive polymer technology have high ripple-current ratings and are a good choice here. The ripple-current rating for a single capacitor may not be sufficient so multiple capacitors are often connected in parallel.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate this voltage, assume that all the current, including the DC current in the load, flows in the filter capacitors.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{0.12\,V}{2\frac{\pi}{4} \times 15\,A} = 5.1\,m\Omega \tag{43}$$

The capacitor specifications are:

- Voltage Rating: 20 V
- Ripple Current Rating: 7.25 A
- ESR: < 5.1 mΩ

9.2.2.14 HV Pin Series Resistors

Multiple resistors are connected in series with HV pin to limit the power dissipation of the UCC25640x device. The recommended series resistor with HV pin is 5 kΩ.

ADVANCE INFORMATION

9.2.2.15 BLK Pin Voltage Divider

BLK pin senses the LLC input voltage and determines when to turn on and off the LLC converter. Different versions of UCC25640x have different BLK thresholds.

Choose bulk startup voltage at 360 V, then the BLK resistor divider ratio can be calculated as below:

$$k_{BLK} = \frac{360\,V}{1V} = 360 \tag{44}$$

The desired power consumption of the BLK pin resistor divider is P_{BLKsns} = 10 mW. The BLK sense resistor total value is given by:

$$R_{BLKsns} = \frac{V_{IN(nom)}^2}{P_{BLKsns}} = \frac{390^2}{0.01} = 15.21M\Omega \tag{45}$$

The lower BLK divider resistor value is given by:

$$R_{BLKlower} = \frac{R_{BLKsns}}{k_{BLK}} = \frac{15.21M\Omega}{360} = 42.2\,k\Omega \tag{46}$$

The higher BLK divider resistor value is given by:

$$R_{BLKupper} = R_{BLKsns} - R_{BLKlower} = 15.16\,M\Omega \tag{47}$$

The actual bulk voltage thresholds can be calculated:

$$V_{BulkStart} = 360\,V \tag{48}$$

$$V_{BulkStop} = 360V \times \frac{0.9}{1} = 324V \tag{49}$$

9.2.2.16 ISNS Pin Differentiator

ISNS pin sets the over current protection level. OCP1 is peak current protection level; OCP2 and OCP3 are average current protection levels. The threshold voltages are 4.0 V, 0.6 V, and 0.425 V, respectively.

Set OCP3 level at 150% of full load. Thus, the sensed average input current level at full load is given by:

$$V_{ISNSfullload} = \frac{0.425\,V}{140\%} = 0.304\,V \tag{50}$$

The current sense ratio can then be calculated:

$$k_{ISNS} = \frac{V_{ISNSfullload}}{\left(\frac{P_{OUT}}{\eta} \times \frac{1}{V_{bulknom}}\right)} = \frac{0.304\,V}{\left(\frac{180\,W}{0.92} \times \frac{1}{390\,V}\right)} = 0.606\Omega \tag{51}$$

Select a current sense capacitor first, since there are less high voltage capacitor choices than resistors:

$$C_{ISNS} = 150\,pF \tag{52}$$

Then calculate the required ISNS resistor value:

$$R_{ISNS} = \frac{k_{ISNS}C_r}{C_{ISNS}} = \frac{0.606\Omega \times 30\,nF}{150\,pF} = 121.2\,\Omega \tag{53}$$

After the current sense ratio is determined, the peak ISNS pin voltage at full load can be calculated:

$$V_{ISNSpeak} = \sqrt{2}I_r \times k_{ISNS} = \sqrt{2} \times 1.404\,A \times 0.606\,\Omega = 1.20\,V \tag{54}$$

The peak resonant current at OCP1 level is given by:

$$I_{respeakOCP1} = \frac{4\,V}{0.606\,\Omega} = 6.6\,A \tag{55}$$

The peak secondary-side current at OCP1 level is given by:

$$I_{secpeakOCP1} = I_{respeakOCP1}\frac{N_{pri}}{N_{sec}} = 6.6A \times 16.5 = 108.9\,A \tag{56}$$

ADVANCE INFORMATION

9.2.2.17 VCR Pin Capacitor Divider

The capacitor divider on the VCR pin sets two parameters: (1) the divider ratio of the resonant capacitor voltage; (2) the amount of frequency compensation to be added. The first criteria the capacitor divider needs to meet is that under over load condition, the peak-to-peak voltage on the VCR pin is with in 6V.It is recommended to size the VCR capacitance to give a total peak to peak voltage between 3V and 4.5V at full load with the frequency compensation ramp contributing between 1V and 2V to the total VCR peak to peak voltage. For this design, the VCR pin capacitance was selected to give a maximum peak to peak voltage of approximately 4.5V at full load with the internal ramp contributing 2V to the total VCR waveform.

The required VCR capacitance can be calculated directly from the resonant capacitor peak to peak voltage and the minimum expected switching frequency.

$$V_{CR(pk-pk)} = V_{CR(peak)} - V_{CR(valley)} = 367.6V - 42.4V = 325.2V \tag{57}$$

Based on the expected peak to peak resonant capacitor voltage, the required capacitor divider ratio can be derived

$$k_{CapDiv} = \frac{V_{CR(pk-pk)}}{V_{VCR\_total} - V_{Ramp}} = \frac{325.2V}{4.5V - 2V} = 130.08 \tag{58}$$

From the expected minimum switching frequency, the lower VCR capacitance can be derived

$$C_{VCR\_Lower} = \frac{1}{V_{Ramp}} \times \frac{I_{Ramp}}{2 \times F_{SW\_min}} = \frac{1}{2V} \times \frac{2mA}{2 \times 64.8kHz} = 7.7nF \tag{59}$$

A standard value of 8.2nF is chosen for the lower VCR capacitor. From the selected lower VCR capacitor and calculated capacitor divider ratio, the upper VCR capacitance is given by:

$$C_{VCR\_Upper} = \frac{C_{VCR\_Lower}}{k_{CapDiv} - 1} = \frac{8.2nF}{130.07 - 1} = 63.5pF \tag{60}$$

A standard value of 68pF is selected for the upper VCR capacitor. From the selected upper and lower VCR capacitors, the actual peak to peak voltage on the VCR pin can be calculated

$$k_{CapDiv} = \frac{C_{VCR\_Lower}}{C_{VCR\_Upper}} + 1 = \frac{8.2nF}{68pF} + 1 = 121.59 \tag{61}$$

$$C_{VCR(pk-pk)} = \frac{1}{C_{VCR\_Lower}} \times \frac{I_{Ramp}}{2 \times F_{SW(Mgmin)}} + \frac{V_{CR(pk-pk)}}{k_{CapDiv}} = \frac{1}{8.2nF} \times \frac{2mA}{2 \times 64.8kHz} + \frac{325.2V}{121.59} = 4.56V \tag{62}$$

ADVANCE INFORMATION

9.2.2.18 Soft Start and Burst Mode Programming

The LL/SS and BW pins allow the designer to select a burst mode threshold as well as program hysteresis for entering and exiting burst mode. The resistor divider of connected to the LL/SS pin sets the BMT_H threshold while the BW pin sets the ratio between BMT_L and BMT_H. In addition to programming the burst mode threshold, the LL/SS pin provides the capability to program an initial voltage onto the LL/SS pin in order to limit the maximum switching frequency during startup. For initial selection of LL/SS components, it is recommended to select an initial LL/SS pin voltage between 0V and 1V and to select burst mode threshold between 1V and 2V. The LL/SS pin parameters can be fine tuned later based on bench measurement.

In this design, an initial LL/SS pin voltage of 0V and a BMT_H threshold of 1.8V were selected. The LL/SS resistor values can then be calculated

$$R_{LL/SS\_Upper} = R_{BMT} \times \frac{V_{RVCC} \times V_{LL/SS\_Init} - V_{RVCC} \times V_{BMT\_Set}}{V_{LL/SS\_Init} \times V_{BMT\_Exit} + V_{BMT\_Set} \times \left(V_{LL/SS\_precharge} + 4\mu A \times R_{BMT}\right)} \quad (63)$$

$$R_{LL/SS\_Upper} = 100k\Omega \times \frac{13V \times 5V - 13V \times 3.5V}{5V \times V_{BMT\_Exit} + 3.5V \times \left(V_{LL/SS\_precharge} + 400mV\right)} = 187k\Omega \quad (64)$$

$$R_{LL/SS\_Lower} = R_{BMT} \times \frac{V_{RVCC} \times V_{LL/SS\_Init} - V_{RVCC} \times V_{BMT\_Set}}{(V_{RVCC-} V_{LL/SS\_Init}) \times V_{BMT\_Exit} + (V_{RVCC-} V_{BMT\_Set}) \times \left(V_{LL/SS\_precharge} + 4\mu A \times R_{BMT}\right)} \quad (65)$$

$$R_{LL/SS\_Lower} = 100k\Omega \times \frac{13V \times 5V - 13V \times 3.5V}{(13V - 5V) \times V_{BMT\_Exit} + (13V - 3.5V) \times \left(V_{LL/SS\_precharge} + 400mV\right)} = 107k\Omega \quad (66)$$

The soft start capacitor sets the speed of the soft start ramp. The soft start time varies with load condition. At full load or over load condition, the soft start time is the longest. It is not easy to calculate the exact soft start time value. However, it can be estimated that under full load condition, the longest possible soft start time si determined by how quickly the soft start pin voltage rises to the maximum VCR peak to peak voltage. For a start up time of 10ms, the soft start capacitor is sized to be the following:

$$C_{LL/SS} = I_{SS} \times \frac{T_{SS\_Max}}{V_{VCR(pk-pk)} - V_{LL/SS\_precharge}} = 37.5\mu A \times \frac{10ms}{4.56V - 0V} = 82nF \quad (67)$$

9.2.2.19 BW Pin Voltage Divider

The BW pin programs the ratio between burst mode entry and exit thresholds as well as senses the output voltage through the bias winding and protects the power stage from over voltage. The nominal output voltage is 12 V. The bias winding has 3 turns, and the secondary side winding has 2 turns. Therefore the nominal voltage of the bias winding is given by:

$$V_{BiasWindingNom} = 12V \times \frac{3}{2} = 18V \quad (68)$$

The desired OVP threshold in this design is 140% of the nominal value. The OVP threshold level in UCC25640x device is 4 V, so the nominal BW pin voltage is given by:

$$V_{BWnom} = \frac{4V}{140\%} = 2.85V \quad (69)$$

The required BW divider ratio is then given by:

$$k_{BW} = \frac{V_{BiasWindingNom}}{V_{BWNom}} = \frac{18V}{2.85V} = 6.32 \quad (70)$$

In this design, the burst mode threshold ratio is chosen to be 0.6 (Option 5).The target programming resistance is then:

$$R_{BMT\_Program} = 6.664k\Omega \quad (71)$$

$$k_{BMT} = 0.6 \quad (72)$$

The lower BW resistor can be calculated by:

$$R_{Lower} = R_{BMT\_Program} \times \left(1 + \frac{1}{K_{BW}}\right) = 6.664k\Omega \times \left(1 + \frac{1}{6.32}\right) = 7.72k\Omega \quad (73)$$

A standard value of 8.06kΩ is chosen for the lower BW resistor

$$R_{Lower} = 8.06k\Omega \quad (74)$$

The upper resistor can be calculated by:

$$R_{BWupper} = R_{BWlower} \times \left(\frac{V_{BiasWindingNom} - V_{BWnom}}{V_{BWnom}}\right) = 8.06\,k\Omega \times \left(\frac{18 - 2.85}{2.85}\right) = 42.85\,k\Omega \quad (75)$$

ADVANCE INFORMATION

9.2.3 Application Curves

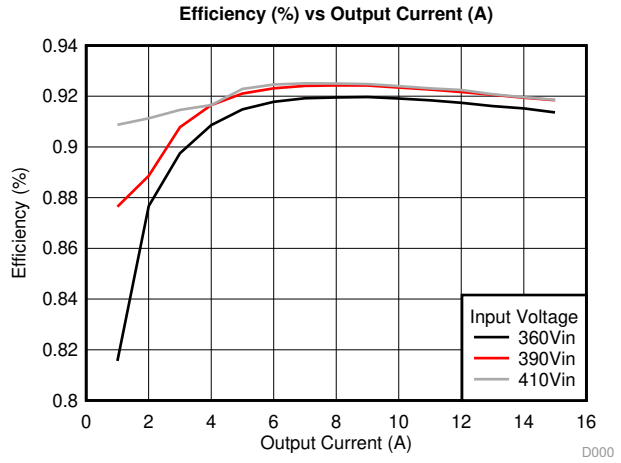


图 24. Efficiency

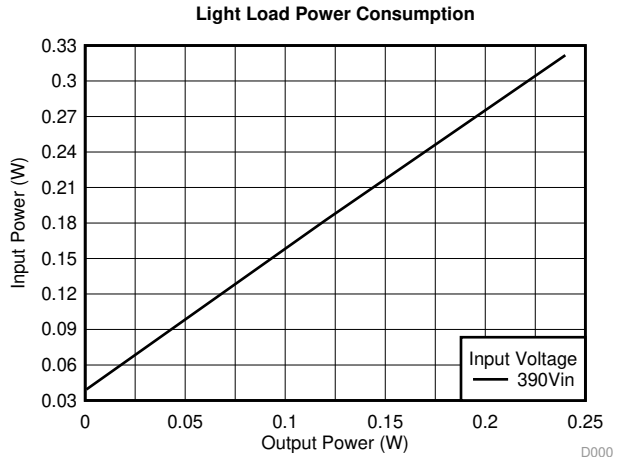


图 25. Light Load Power Consumption

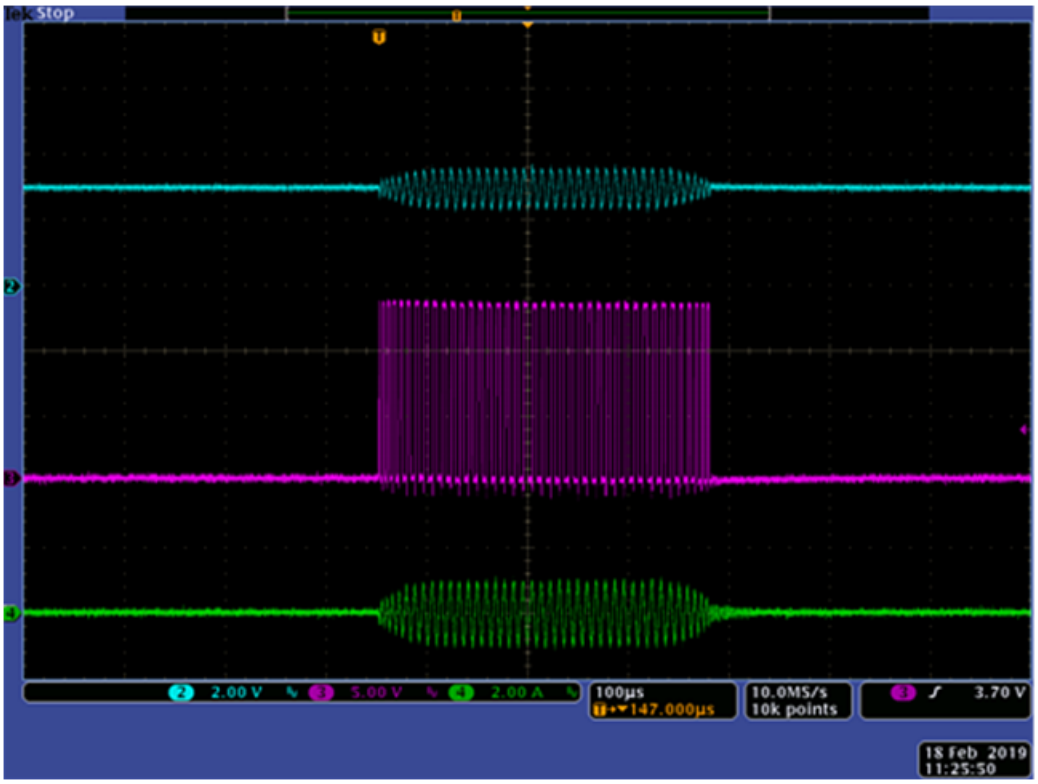


图 26. Burst Mode with Soft On/Off

ADVANCE INFORMATION

10 Power Supply Recommendations

10.1 VCC Pin Capacitor

The VCC capacitor should be sized based on the total start-up charge required by the system. The start-up charge will mostly be consumed by the gate driver circuit. Thus the total start-up charge can be estimated by the start-up switching frequency, MOSFET gate charge, and the soft-start time.

Assume the total start-up charge required by the system is shown in 公式 76

$$Q_{tot} = 1.6\,mC \tag{76}$$

During PFC and LLC startup phase, the maximum VCC voltage drop allowed is

$$V_{ccdropmax} = 26V - 10.5V = 15.5V \tag{77}$$

The minimum VCC capacitor needed:

$$C_{VCC} = \frac{Q_{tot}}{V_{ccdropmax}} = 103\,\mu F \tag{78}$$

Choose 110-µF capacitor.

10.2 Boot Capacitor

During burst off period, power consumed by the high-side gate driver from the HB pin must be drawn from C_{BOOT} and will cause its voltage to decay. At the start of the next burst period there must be sufficient voltage remaining on C_{BOOT} to power the high-side gate driver until the conduction period of LO allows it to be replenished from C_{RVCC}. The power consumed by the high-side driver during this burst off period will therefore have a direct impact on the size and cost of capacitors that must be connected to C_{BOOT} and RVCC.

Assume the system has a maximum burst off period of 10 ms.

$$t_{maxoff} = 10\,ms \tag{79}$$

Assume the bootstrap diode has a forward voltage drop of 1 V:

$$V_{bootforwarddrop} = 1V \tag{80}$$

Assume the boot voltage to be always above 8 V to avoid UVLO fault. Then the maximum allowed voltage drop on boot capacitor is:

$$V_{boot\,max\,drop} = V_{RVCC} - V_{bootforwarddrop} - 8V = 13V - 1V - 8V = 4V \tag{81}$$

Boot capacitor can then be sized:

$$C_{boot} = \frac{I_{bootleak} \times t_{max\,off}}{V_{bootforwarddrop}} = \frac{85\mu A \times 10ms}{4V} = 212.5nF \tag{82}$$

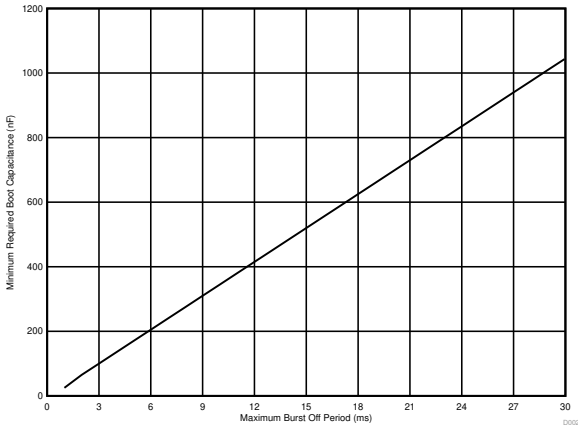


图 27. Minimum Required Boot Capacitance vs. Maximum Burst Off Period

ADVANCE INFORMATION

10.3 RVCC Pin Capacitor

The RVCC capacitor needs to be at least 5 times greater than boot capacitor. In addition, sizing of the RVCC capacitor depends on the stability of the RVCC LDO. If the load is light on RVCC, smaller capacitors can be used. The larger the load, the larger the capacitor is needed. In a typical system, the RVCC LDO powers the PFC and LLC gate drivers.

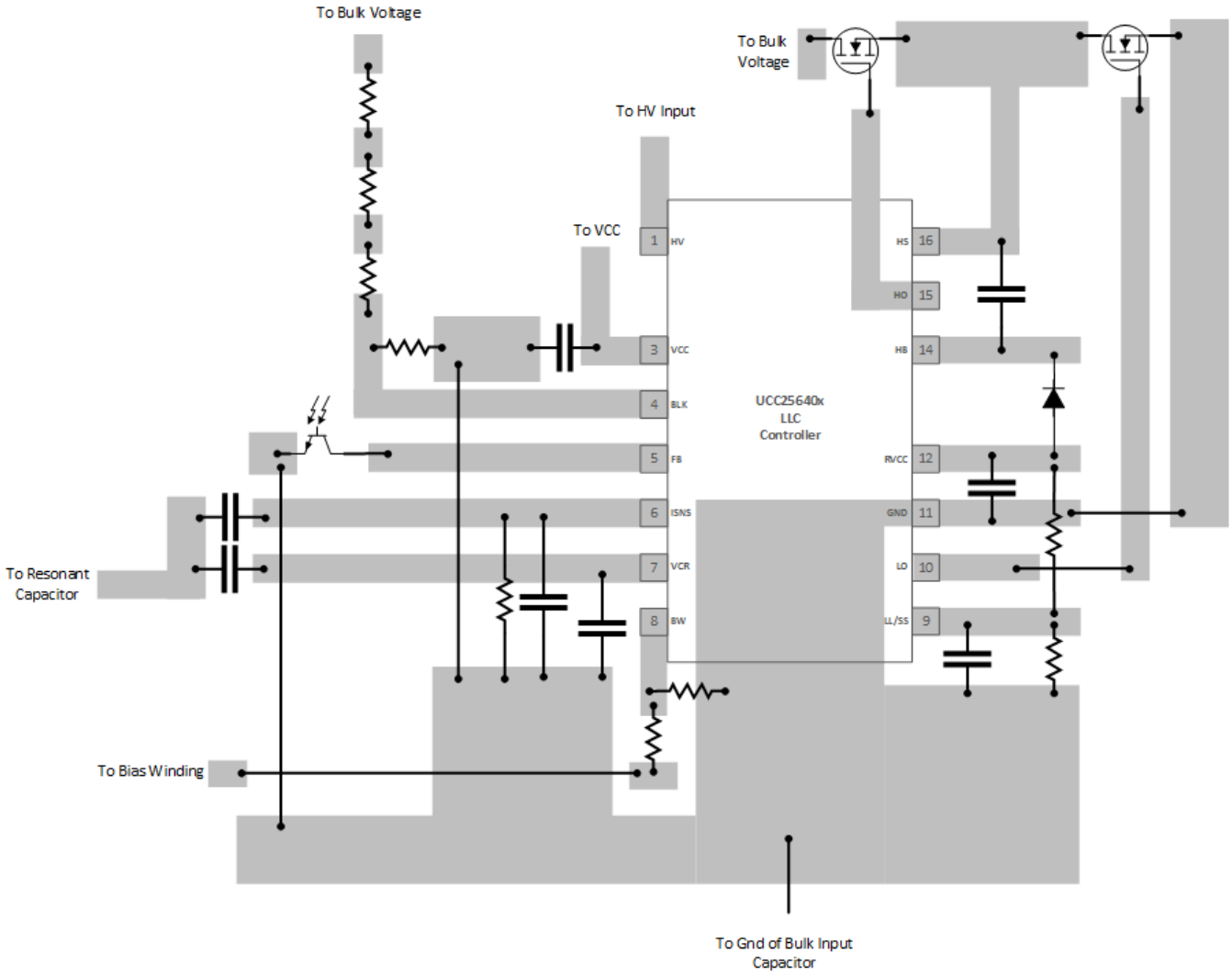
11 Layout

11.1 Layout Guidelines

- Put a 2.2-µF ceramic capacitor on VCC pin in addition to the energy storage electrolytic capacitor. The 2.2-µF ceramic capacitor should be put as close as possible to the VCC pin.
- RVCC pin should have a bypass capacitor of 4.7 µF or more. It is recommended to add a 0.1-µF ceramic capacitor in addition to the 4.7 µF. The capacitors should be put as close as possible to the RVCC pin. RVCC cap is recommended to be size at least 5 times of boot capacitor.
- Minimum recommended boot capacitor, C_{BOOT}, is 0.1 µF. The minimum value of the boot capacitor needs to be determined by the minimum burst frequency. The boot capacitor should be large enough to hold the bootstrap voltage during the lowest burst frequency. Please refer to the boot leakage current in the electrical table.
- Signal ground and power ground should be single-point connected. Power ground is recommended to connect to the negative terminal of the LLC input bulk capacitor.
- The filtering capacitors for ISNS and BLK should be put as close as possible to the pins.
- The bottom capacitor on VCR should be put as close as possible to the VCR pin.
- FB trace should be as short as possible
- Soft-start capacitor should be put as close as possible to LL/SS pin
- Use film capacitors or C0G, NP0 ceramic capacitors for the VCR divider and ISNS capacitor for low distortion
- Add necessary filtering capacitors on the BW pin to filter out the high spikes on the bias winding waveform. It is critical to filter out the high spikes because internally the signal is peak detected and then sampled at the low-side turn off edge.
- Do not put any capacitor from the HV pin to ground. The layout of this pin should result in low parasitic capacitance (< 60 pF) from HV pin to ground. For UCC256403, the HV pin should be connected to ground.
- Keep necessary high voltage clearance and creepage.

ADVANCE INFORMATION

11.2 Layout Example



12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 设计电子表格：*UCC25630 设计计算器*，UCC634
- 用户指南：*《使用 UCC25630-1EVM-291》*，

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 7. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
UCC256403	单击此处	单击此处	单击此处	单击此处	单击此处
UCC256404	单击此处	单击此处	单击此处	单击此处	单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 商标

E2E is a trademark of Texas Instruments.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC256403ADDBR	ACTIVE	SOIC	DDB	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403A	Samples
UCC256403DDBR	ACTIVE	SOIC	DDB	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403	Samples
UCC256403DDBT	ACTIVE	SOIC	DDB	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403	Samples
UCC256404ADDBR	ACTIVE	SOIC	DDB	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404A	Samples
UCC256404ADDBT	ACTIVE	SOIC	DDB	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404A	Samples
UCC256404BDDBR	ACTIVE	SOIC	DDB	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404B	Samples
UCC256404DDBR	ACTIVE	SOIC	DDB	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404	Samples
UCC256404DDBT	ACTIVE	SOIC	DDB	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

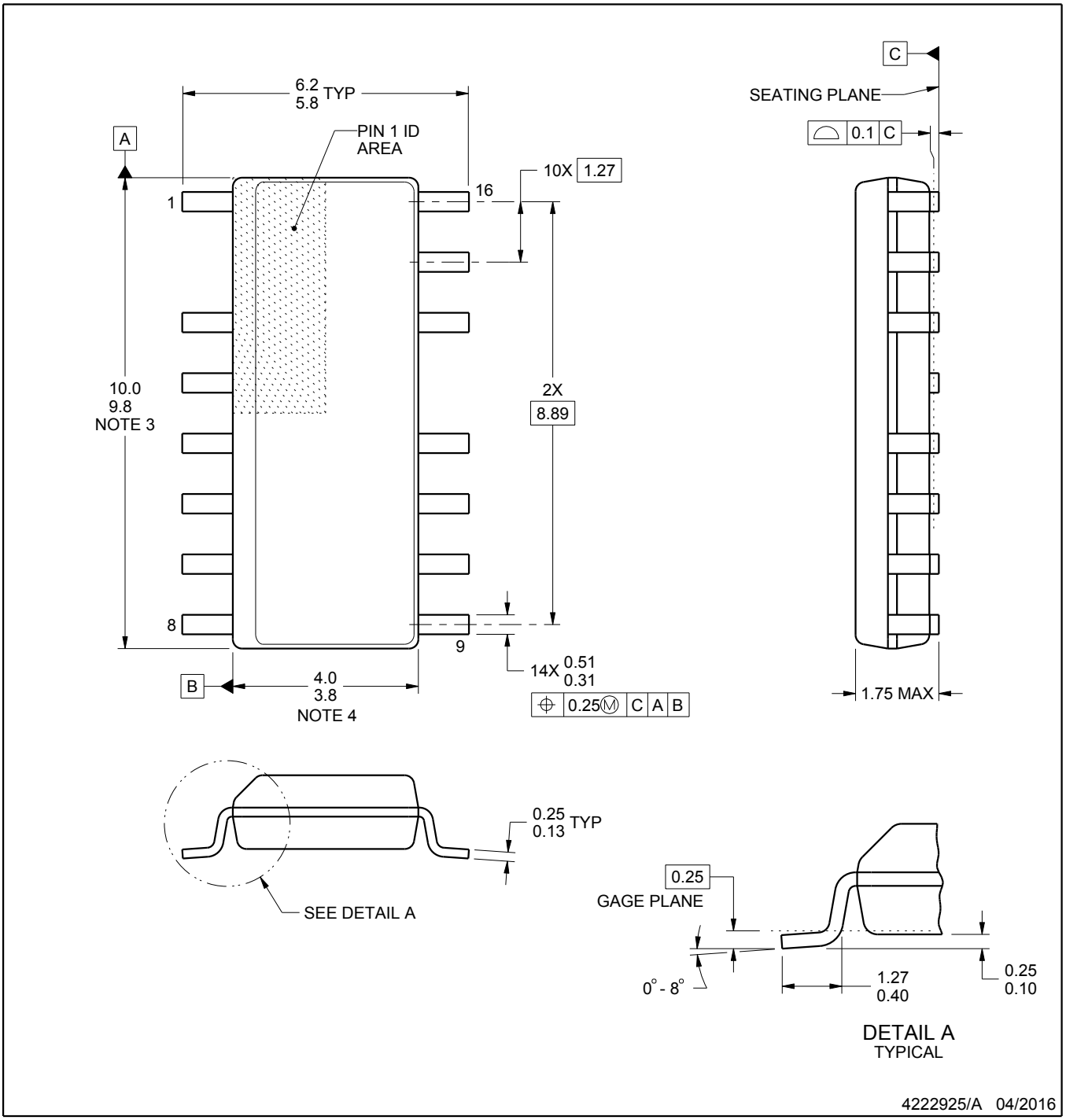
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DDB0014A

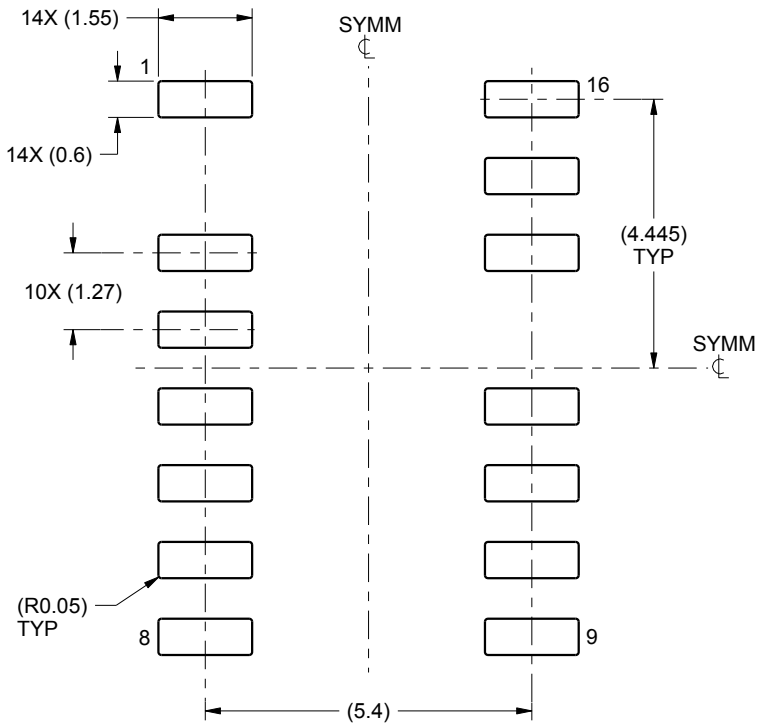
SOIC - 1.75 mm max height

SOIC

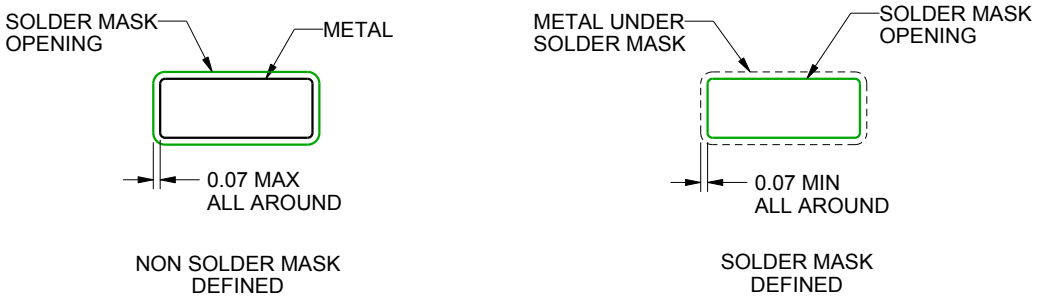


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-012, variation AC.



LAND PATTERN EXAMPLE
SCALE:8X

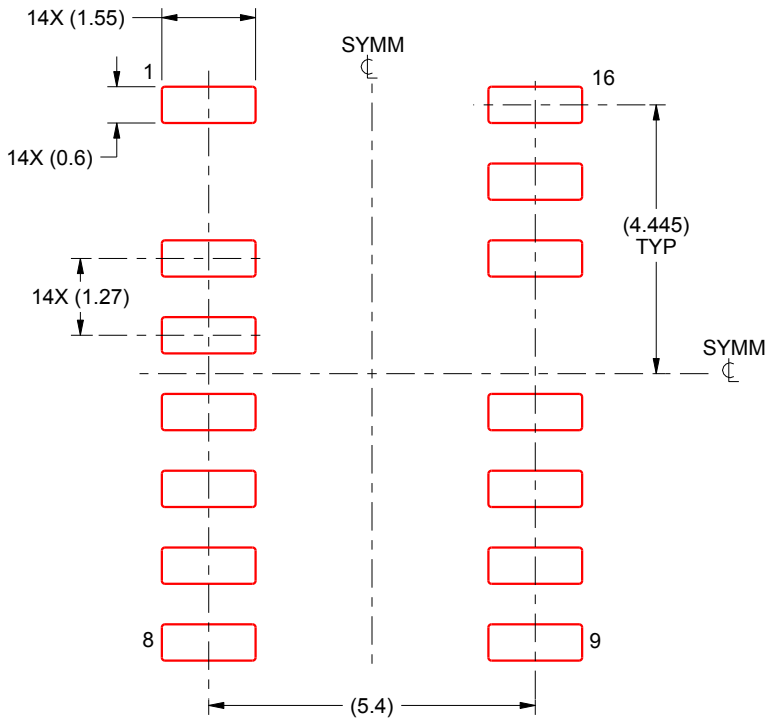


SOLDER MASK DETAILS

4222925/A 04/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4222925/A 04/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122