HD3SS3412A 4 通道高性能差动开关

1 特性

- 兼容运行速率高达 12Gbps 的多种接口标准，包括 PCI Express GEN III 和 USB 3.0
- 超过 8 GHz 的 –3dB 宽差动带宽
- 出色动态特性（4GHz 时）
  - 串扰 = -35dB
  - 断开隔离 = –19dB
  - 插入损耗 = –1.5dB
  - 回波损耗 = –11dB
- 双向“多路复用器/多路信号分离器”类型差动开关
- VDD 运行电压范围 3.3V ± 10%
- 小型 3.5mm × 9.0mm 42 引脚 WQFN 封装
- 通用行业标准引脚
- 支持 XAUI 和 SGMII

2 应用

- 台式机和笔记本电脑
- 服务器和存储局域网络
- PCI EXPress 背板
- 共享 I/O 端口

3 说明

HD3SS3412A 器件是一款高速无源开关，能够切换四条差分通道， 包括 在电脑或服务器应用中从一个源分别到两个目标位置的两条完整 PCI Express x1 通道等应用。具有双向功能的 HD3SS3412A 还 支持 一个目标设备与两个源设备相连，例如两个平台共享一个外设。HD3SS3412A 具有单个控制线（SEL 引脚），可用于控制端口 A 与端口 B 或端口 C 间的信号路径。

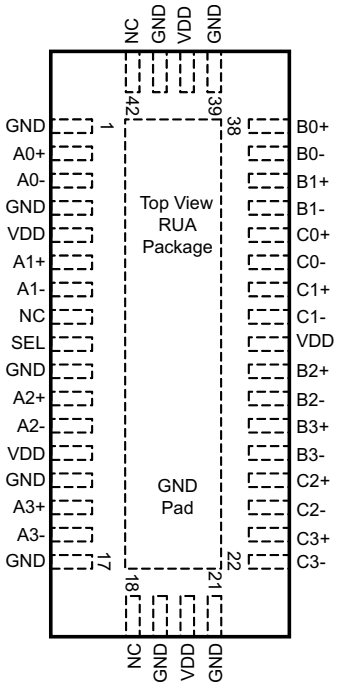
HD3SS3412A 采用行业标准的 42 引脚 WQFN 封装，采用多家供应商通用的尺寸。该器件需要在 0°C 至 70ºC 的完整温度范围内由电压为 3.3V 的单电源供电运行。

器件信息(1)

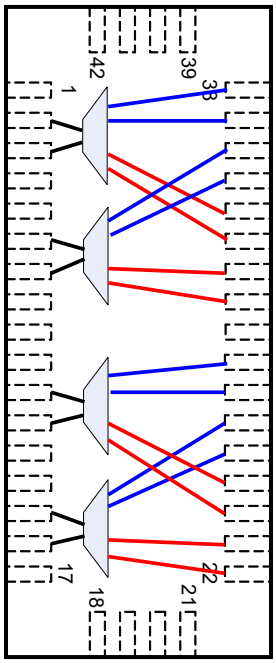
器件型号	封装	封装尺寸（标称值）
HD3SS3412A	WQFN (42)	9.00mm x 3.50mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

HD3SS3412A 引脚



HD3SS3412A 开关直通布线



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

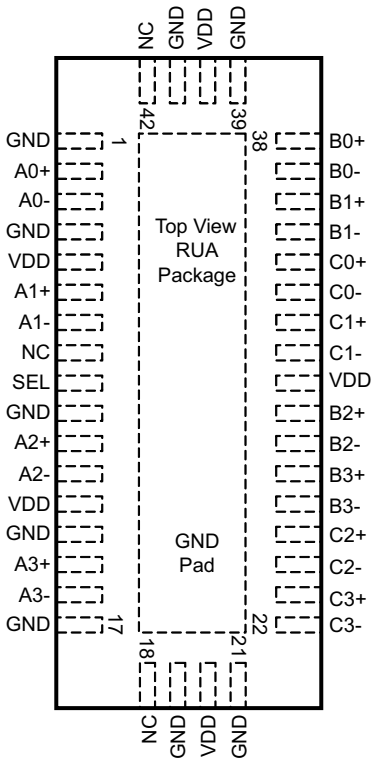
日期	修订版本	说明
2017 年 12 月	*	初始发行版

5 说明 （续）

HD3SS3412A 是通用的 4 通道高速多路复用器/多路信号分离器开关类型，可用于电路板上两个不同位置间的高速信号路由。虽然 HD3SS3412A 专为 PCI Express Gen III 应用而设计，但也支持其它多种差模电压＜1800mVpp、共模电压＜2.0V 的高速数据协议，与 USB 3.0 和 DisplayPort 1.2 相同。该器件的一个选择输入 (SEL) 引脚可通过系统内或微控制器提供的一个 GPIO 引脚轻松控制。

6 Pin Configuration and Functions

RUA Package
42-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCH PORT A			
A0+	2	I/O	Port A, Channel 0, High-Speed Positive Signal
A0–	3	I/O	Port A, Channel 0, High-Speed Negative Signal
A1+	6	I/O	Port A, Channel 1, High-Speed Positive Signal
A1–	7	I/O	Port A, Channel 1, High-Speed Negative Signal
A2+	11	I/O	Port A, Channel 2, High-Speed Positive Signal
A2–	12	I/O	Port A, Channel 2, High-Speed Negative Signal
A3+	15	I/O	Port A, Channel 3, High-Speed Positive Signal
A3–	16	I/O	Port A, Channel 3, High-Speed Negative Signal
SWITCH PORT B			
B0+	38	I/O	Port B, Channel 0, High-Speed Positive Signal
B0–	37	I/O	lPort B, Channel 0, High-Speed Negative Signal
B1+	36	I/O	Port B, Channel 1, High-Speed Positive Signal

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
B1–	35	I/O	Port B, Channel 1, High-Speed Negative Signal
B2+	29	I/O	Port B, Channel 2, High-Speed Positive Signal
B2–	28	I/O	Port B, Channel 2, High-Speed Negative Signal
B3+	27	I/O	Port B, Channel 3, High-Speed Positive Signal
B3–	26	I/O	Port B, Channel 3, High-Speed Negative Signal

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCH PORT C			
C0+	34	I/O	Port C, Channel 0, High-Speed Positive Signal
C0–	33	I/O	Port C, Channel 0, High-Speed Negative Signal
C1+	32	I/O	Port C, Channel 1, High-Speed Positive Signal
C1–	31	I/O	Port C, Channel 1, High-Speed Negative Signal
C2+	25	I/O	Port C, Channel 2, High-Speed Positive Signal
C2–	24	I/O	Port C, Channel 2, High-Speed Negative Signal
C3+	23	I/O	Port C, Channel 3, High-Speed Positive Signal
C3–	22	I/O	Port C, Channel 3, High-Speed Negative Signal
CONTROL, SUPPLY, AND NO CONNECT			
NC	8	—	Electrically not connected. May connect to VDD or GND, or leave unconnected.
	18		
	42		
GND	1	Supply	Negative power supply voltage
	4		
	10		
	14		
	17		
	19		
	21		
	39		
	41		
	Center Pad		
SEL	9	I	Select between port B or port C. Internally tied to GND through a 100-kΩ resistor
VDD	5	Supply	Positive power supply voltage
	13		
	20		
	30		
	40		

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage (V_{DD})	Absolute minimum/maximum supply voltage	–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	Control pin (SEL)	–0.5	VDD + 0.5	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values for all parameters are at V_{DD} = 3.3 V and T_A = 25°C. (Temperature limits are specified by design)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage (SEL pin)		2.0		VDD	V
V_{IL}	Input low voltage (SEL pin)		–0.1		0.8	V
V_{I/O_Diff}	Differential voltage (differential pins)	Switch I/O diff voltage	0		1.8	VPP
V_{I/O_CM}	Common voltage (differential pins)	Switch I/O common-mode voltage	0		2.0	V
T_A	Operating free-air temperature	Ambient temperature	0		70	°C

7.4 Thermal Information

THERMAL METRIC(1)		HD3SS3412A RUA (WQFN) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	27.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
I_{IH}	Input High Voltage (SEL)	V_{DD} = 3.6 V; V_{IN} = VDD			95	µA
I_{IL}	Input Low Voltage (SEL)	V_{DD} = 3.6 V; V_{IN} = GND			1	µA
I_{LK}	Leakage Current (Differential I/O pins)	V_{DD} = 3.6 V; V_{IN} = 0 V; V_{OUT} = 2 V (I_{LK} On OPEN outputs) [Ports B and C]			130	µA
		V_{DD} = 3.6 V, V_{IN} = 2 V; V_{OUT} = 0 V (I_{LK} On OPEN outputs) [Port A]			4	
I_{DD}	Supply Current	V_{DD} = 3.6 V; SEL = V_{DD}/GND; Outputs Floating		4.7	6	mA
C_{ON}	Outputs ON Capacitance	V_{IN} = 0 V; Outputs Open; Switch ON		1.5		pF
C_{OFF}	Outputs OFF Capacitance	V_{IN} = 0 V; Outputs Open, Switch OFF		1		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3 V; V_{CM} = 0.5 V to 1.5 V ; I_O = –8 mA		5	8	Ω
ΔR_{ON}	ON-resistance match between channels	V_{DD} = 3.3 V ; –0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = –8 mA			2	Ω
	ON-resistance match between pairs of the same channel	V_{DD} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = –8 mA			0.7	Ω
R_{FLAT_ON}	ON-resistance flatness ($R_{ON(MAX)}$ – $R_{ON(MAIN)}$)	V_{DD} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 1.2 V			1.15	Ω
t_{PD}	Switch propagation delay	Rsc and R_{LOAD} = 50 Ω			85	ps
	SEL-to-switch T_{ON}	Rsc and R_{LOAD} = 50 Ω		70	250	ns
	SEL-to-switch T_{OFF}			70	250	
T_{SKEW_Inter}	Inter-pair output skew (CH-CH)	Rsc and R_{LOAD} = 50 Ω			20	ps
T_{SKEW_Intra}	Intra-pair output skew (bit-bit)	Rsc and R_{LOAD} = 50 Ω			8	ps
R_L	Differential return loss (VCM = 0 V) Also see *Typical Characteristics*	f = 0.3 MHz		–28		dB
		f = 2500 MHz		–12		
		f = 4000 MHz		–11		
X_{TALK}	Differential Crosstalk(VCM = 0 V) Also see *Typical Characteristics*	f = 0.3 MHz		–90		dB
		f = 2500 MHz		–39		
		f = 4000 MHz		–35		
O_{IRR}	Differential Off-Isolation(VCM = 0 V) Also see *Typical Characteristics*	f = 0.3 MHz		–75		dB
		f = 2500 MHz		–22		
		f = 4000 MHz		–19		
I_L	Differential Insertion Loss (VCM = 0 V) Also see *Typical Characteristics*	f = 0.3 MHz		–0.5		dB
		f = 2500 MHz		–1.1		
		f = 4000 MHz		–1.5		
BW	Bandwidth	At –3 dB		8		GHz

7.6 Dissipation Ratings

		MIN	MAX	UNIT
P_D	Power Dissipation	15.5	21.6	mW

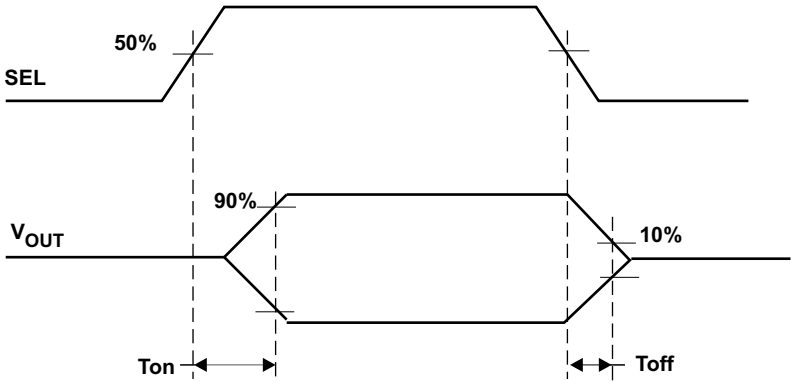
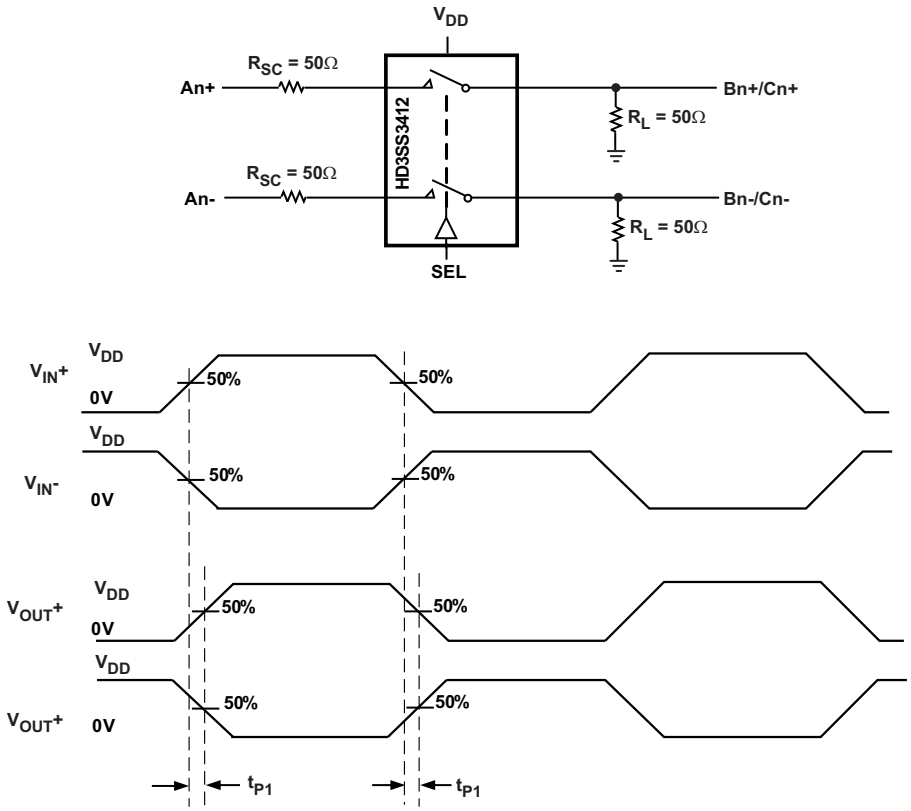


Figure 1. Switch ON and OFF Timing Diagram



$T_{SKEWInter}$ = Difference between t_{PD} for any two pairs of outputs

$T_{SKEWIntra}$ = Difference between t_{P1} and t_{P2} of same pair

Figure 2. Propagation Delay Timing Diagram and Test Setup

7.7 Typical Characteristics

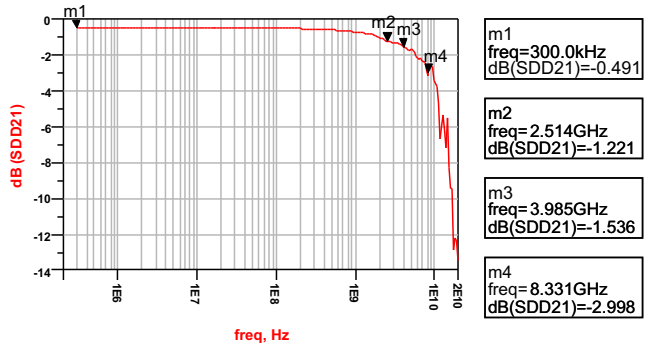


Figure 3. Differential Insertion Loss

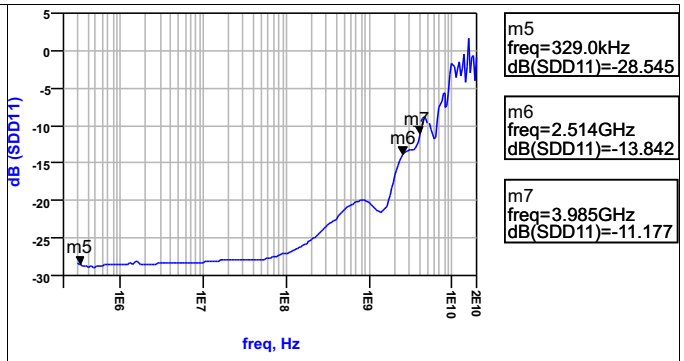


Figure 4. Differential Return Loss

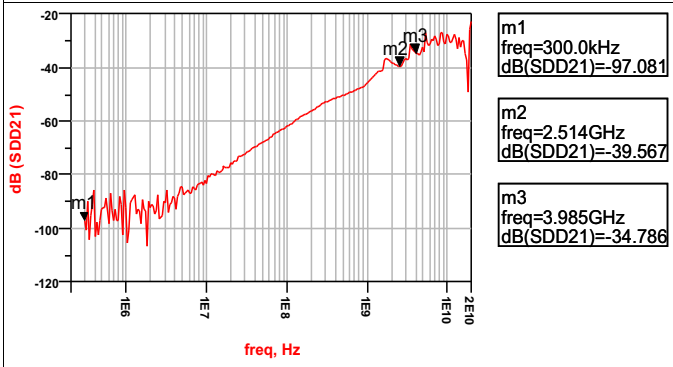


Figure 5. Differential Crosstalk

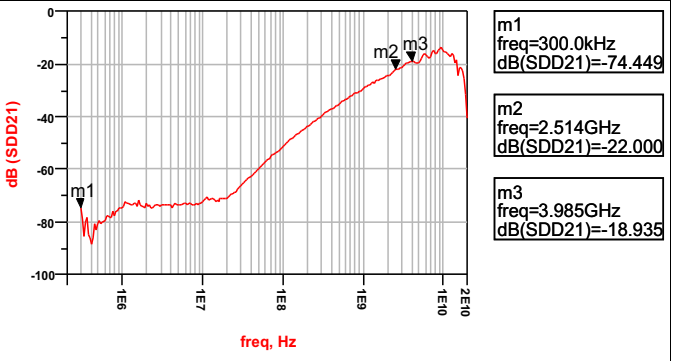


Figure 6. Differential Off Isolation

8 Parameter Measurement Information

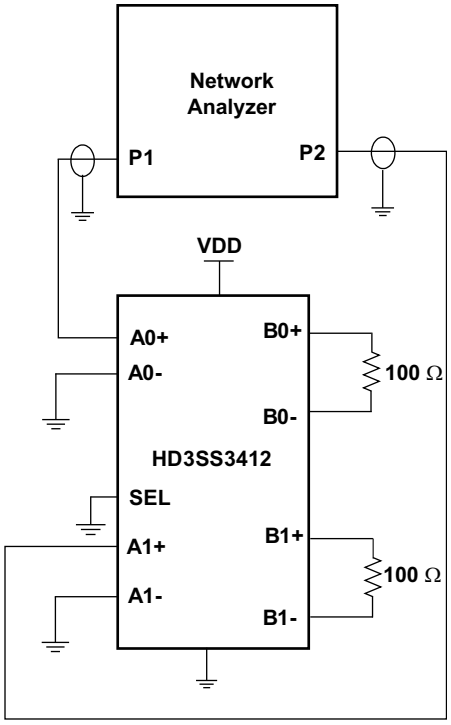


Figure 7. Cross Talk Measurement Setup

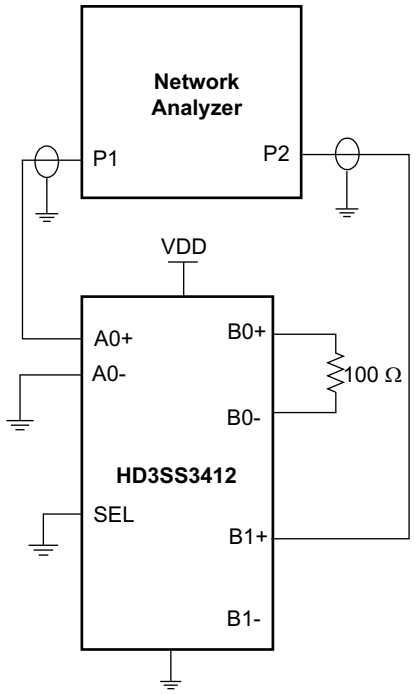


Figure 8. Off Isolation Measurement Setup

Parameter Measurement Information (continued)

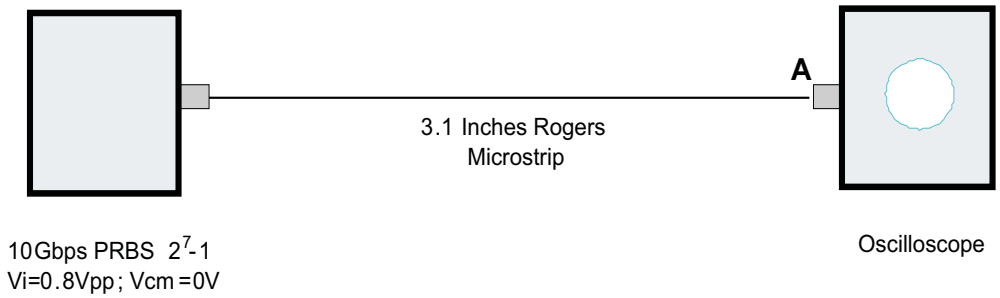


Figure 9. Source Eye Diagram Test Setup

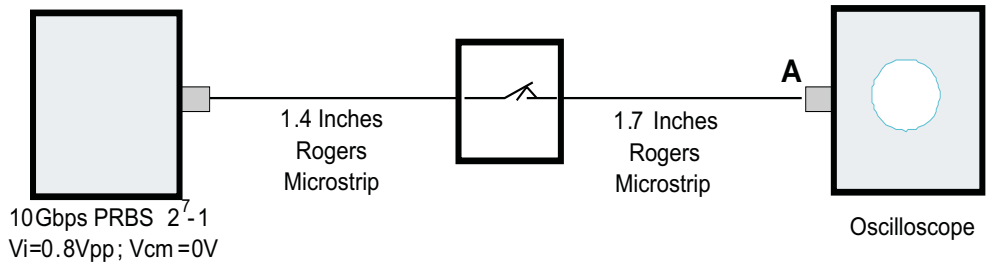


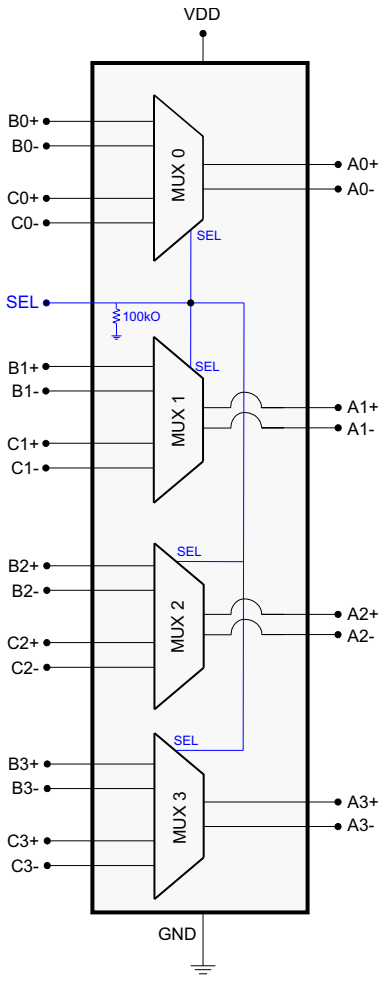
Figure 10. Output Eye Diagram Test Setup

9 Detailed Description

9.1 Overview

The HD3SS3412A is a high-speed passive switch offered in an industry standard 42-pin WQFN package available in a common footprint shared by several other vendors. The device is specified to operate from a single supply voltage of 3.3 V over the commercial temperature range of 0°C to 70°C. The HD3SS3412A is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. Although it was designed specifically to address PCI Express Gen III applications, the HD3SS3412A will also support several other high-speed data protocols with a differential amplitude of < 1800 mVpp and a common-mode voltage of < 2.0 V, as with USB 3.0 and DisplayPort 1.2. The device's one select input (SEL) pin can easily be controlled by an available GPIO pin within a system or from a microcontroller.

9.2 Functional Block Diagram



9.3 Feature Description

The HD3SS3412A has a single control line (SEL Pin) which can be used to control the signal path between Port A and either Port B or Port C. The one select input (SEL) pin of the device can easily be controlled by an available GPIO pin within a system or from a microcontroller. The input signal is selected using the SEL pin.

Table 1. Mux Pin Connections(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0+	B0+	C0+
A0–	B0–	C0–
A1+	B1+	C1+
A1–	B1–	C1–
A2+	B2+	C2+
A2–	B2–	C2–
A3+	B3+	C3+
A3–	B3–	C3–

(1) The HD3SS3412A can tolerate polarity inversions for all differential signals on Ports A, B, and C. Take care to ensure the same polarity is maintained on Port A versus Port B/C.

9.4 Device Functional Modes

Table 2 lists the functional modes for the HD3SS3412A.

Table 2. HD3SS3412A Control Logic

CONTROL PIN (SEL)	PORT A TO PORT B CONNECTION STATUS	PORT A TO PORT C CONNECTION STATUS
L (Default State)	Connected	Disconnected
H	Disconnected	Connected

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 AC Coupling Caps

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs should be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 µF is best and the value should be match for the ± signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board.

There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. A few placement options are shown below. In Figure 11, the coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

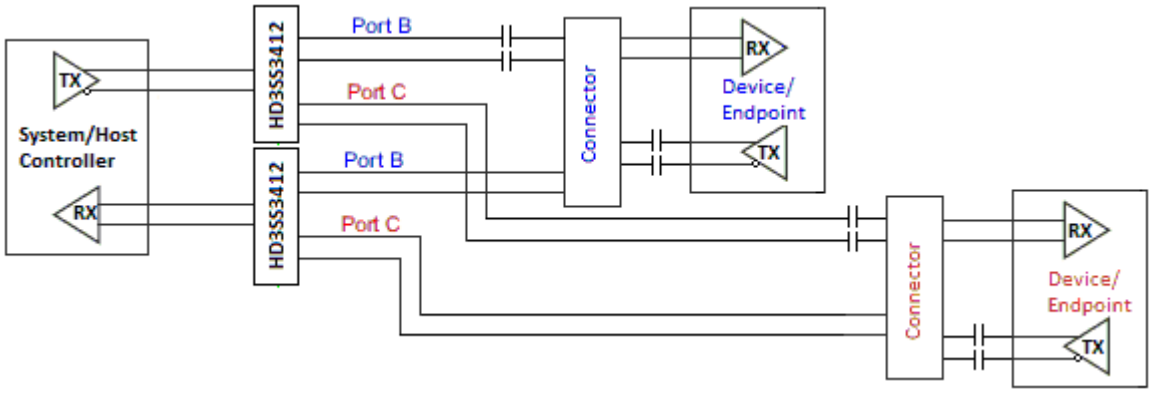


Figure 11. AC Coupling Capacitors Between Switch Tx and Endpoint Tx

In Figure 12, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on the top is biased by the endpoint and the lower switch is biased by the host controller.

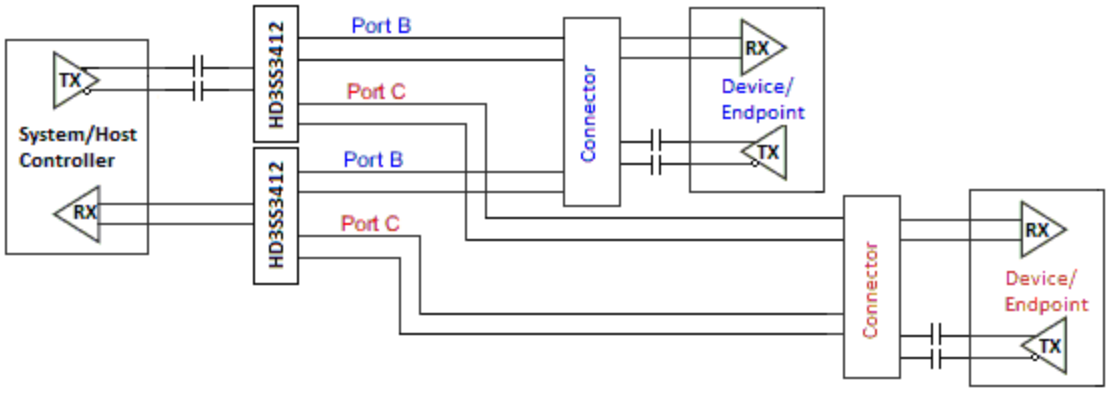


Figure 12. AC Coupling Capacitors on Host Tx and Endpoint Tx

Application Information (continued)

If the common-mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in Figure 13). A biasing voltage of less than 2 V is required in this case.

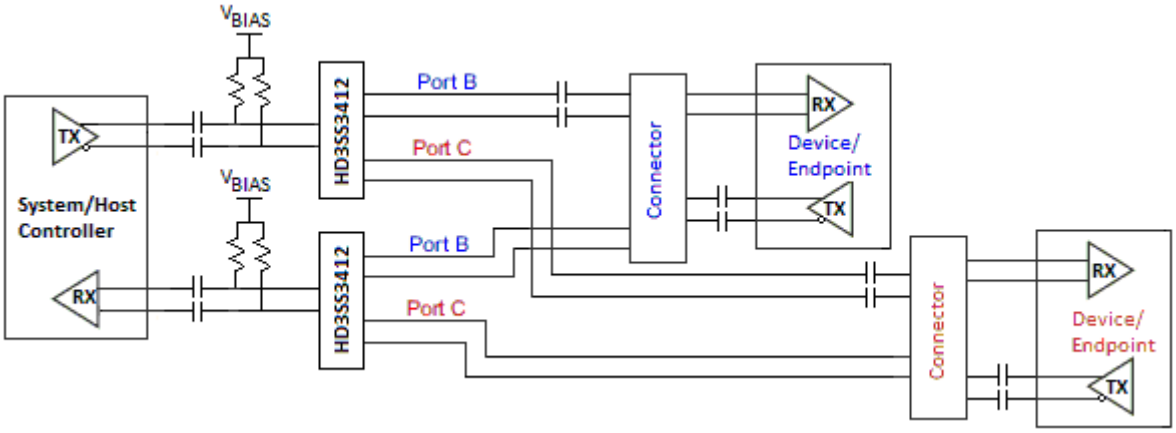


Figure 13. AC Coupling Capacitors on Both Sides of Switch

10.2 Typical Application

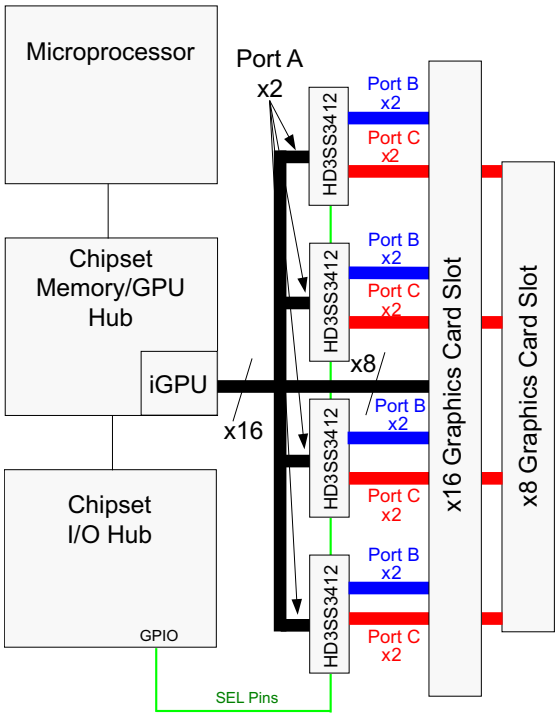


Figure 14. Typical Application Block Diagram

Typical Application (continued)

10.2.1 Design Requirements

Table 3 lists the design parameters of this example.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	3.3 V
Decoupling capacitors	0.1 µF
AC capacitors	75 nF – 200 nF (100 nF shown) USBAA TX p and n lines require AC capacitors. Alternate mode signals may or may not require AC capacitors

10.2.2 Detailed Design Procedure

- Connect VDD and GND pins to the power and ground planes of the printed circuit board, with 0.1-uF bypass capacitor
- Use +3.3-V TTL/CMOS logic level at SEL
- Use controlled-impedance transmission media for all the differential signals
- Ensure the received complimentary signals are with a differential amplitude of <1800 mVpp and a common-mode voltage of <2 V

10.2.3 Application Curves

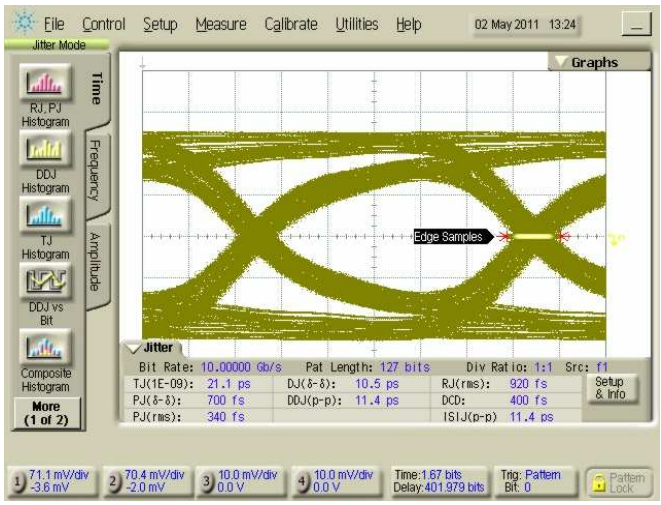


Figure 15. 10-gbps Source Eye Diagram at a: V_{ID} = 800 Mvpp; 2^7–1 Prbs; V_{CM}= 0 V

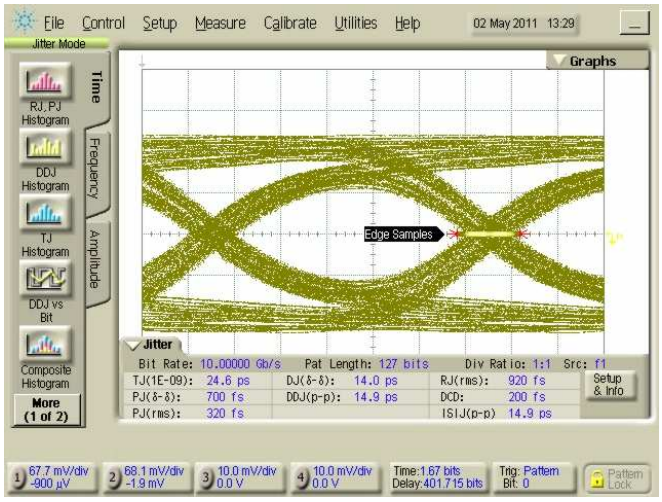


Figure 16. 10-gbps Output Eye Diagram at a: V_{ID} = 800 Mvpp; 2^7–1 Prbs; V_{CM}= 0v; V_{DD}= 3.3 V; Sel= 0 V

11 Power Supply Recommendations

The HD3SS3412A requires +3.3-V digital power sources. VDD 3.3 supply must have 0.1-μF bypass capacitors to VSS (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01-μF are also recommended on the digital supply terminals.

12 Layout

12.1 Layout Guidelines

- Decoupling caps should be placed next to each power terminal on the HD3SS3412A. Take care to minimize the stub length of the race connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling caps
- Place vias as close as possible to the decoupling cop solder pad
- Widen VDD/GND planes to reduce effect if static and dynamic IR drop
- The VBUS traces/planes must be wide enough to carry maximum of 2-A current

12.2 Layout Example

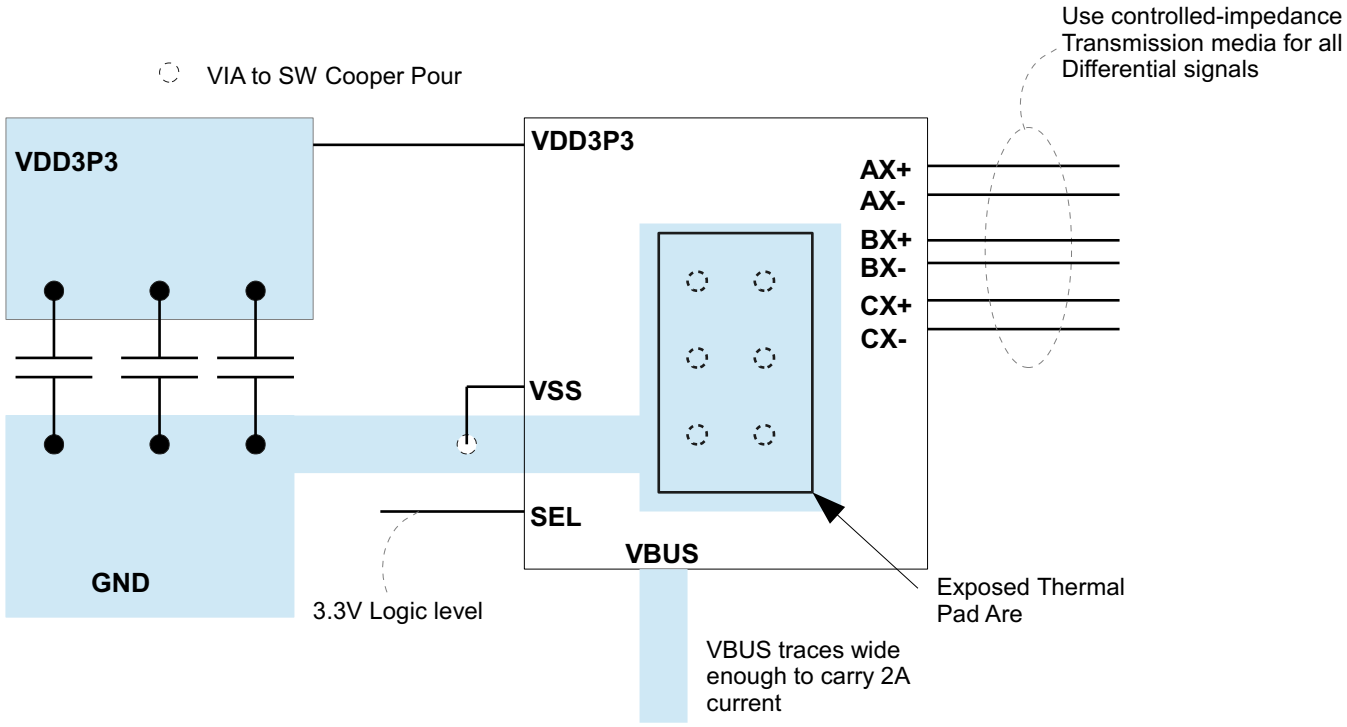


Figure 17. Layout Example

13 器件和文档支持

13.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

13.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS3412ARUAR	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HD3SS3412	Samples
HD3SS3412ARUAT	ACTIVE	WQFN	RUA	42	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HD3SS3412	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

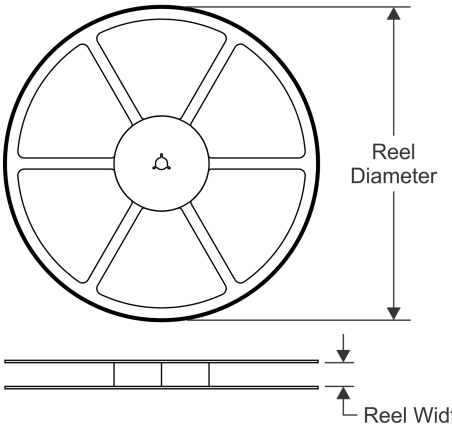
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

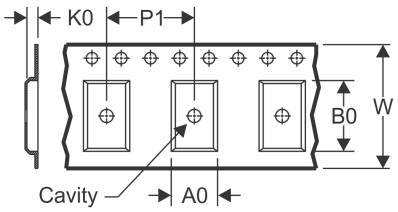
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

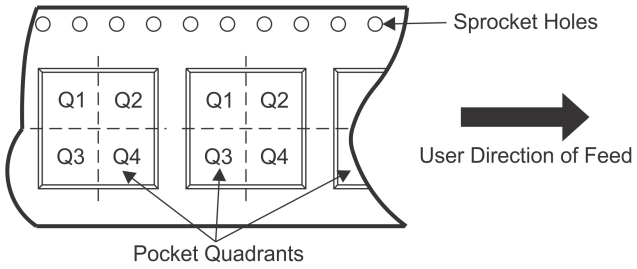


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

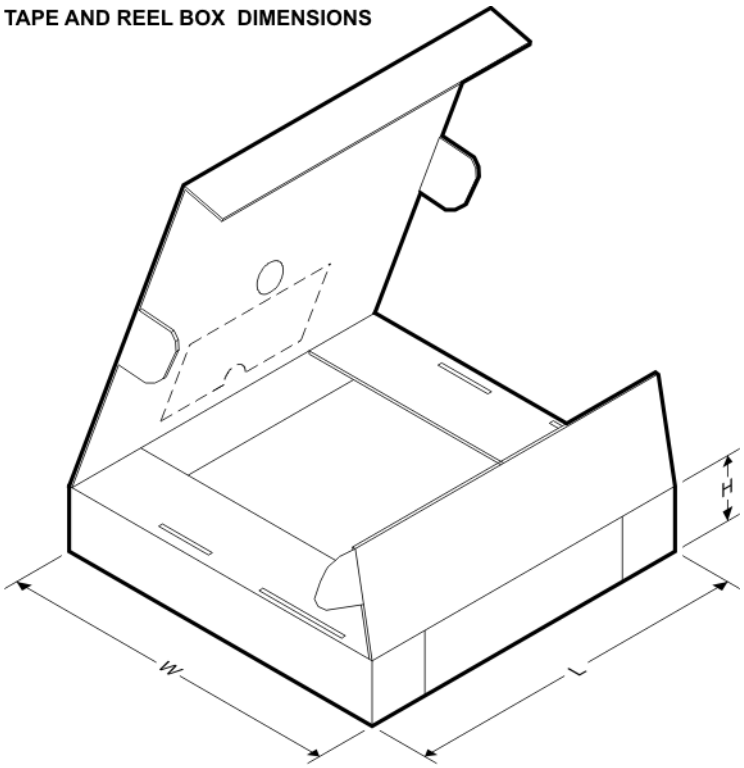
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3412ARUAR	WQFN	RUA	42	3000	330.0	24.4	3.9	9.4	1.0	8.0	24.0	Q1
HD3SS3412ARUAT	WQFN	RUA	42	250	180.0	24.4	3.9	9.4	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3412ARUAR	WQFN	RUA	42	3000	367.0	367.0	45.0
HD3SS3412ARUAT	WQFN	RUA	42	250	211.0	193.0	46.0

GENERIC PACKAGE VIEW

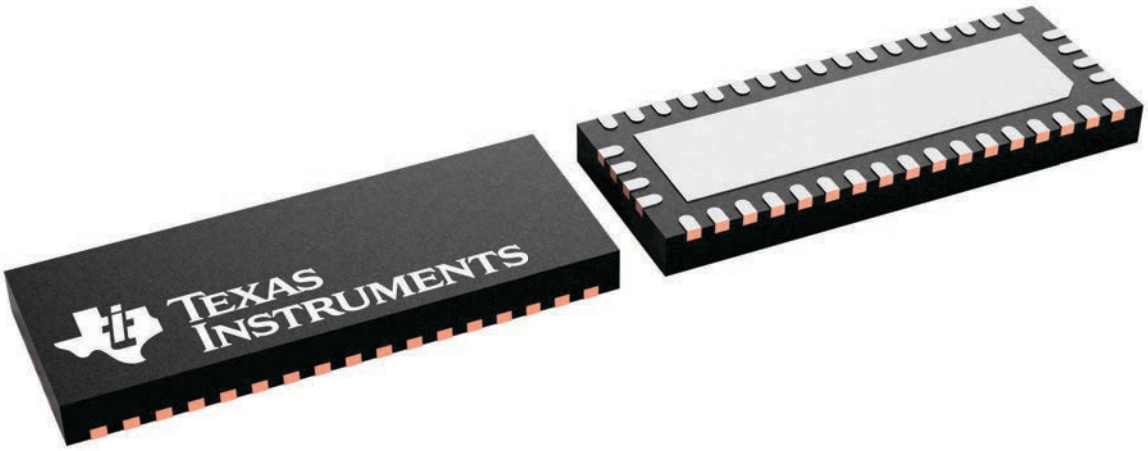
RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

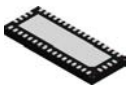
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226504/A

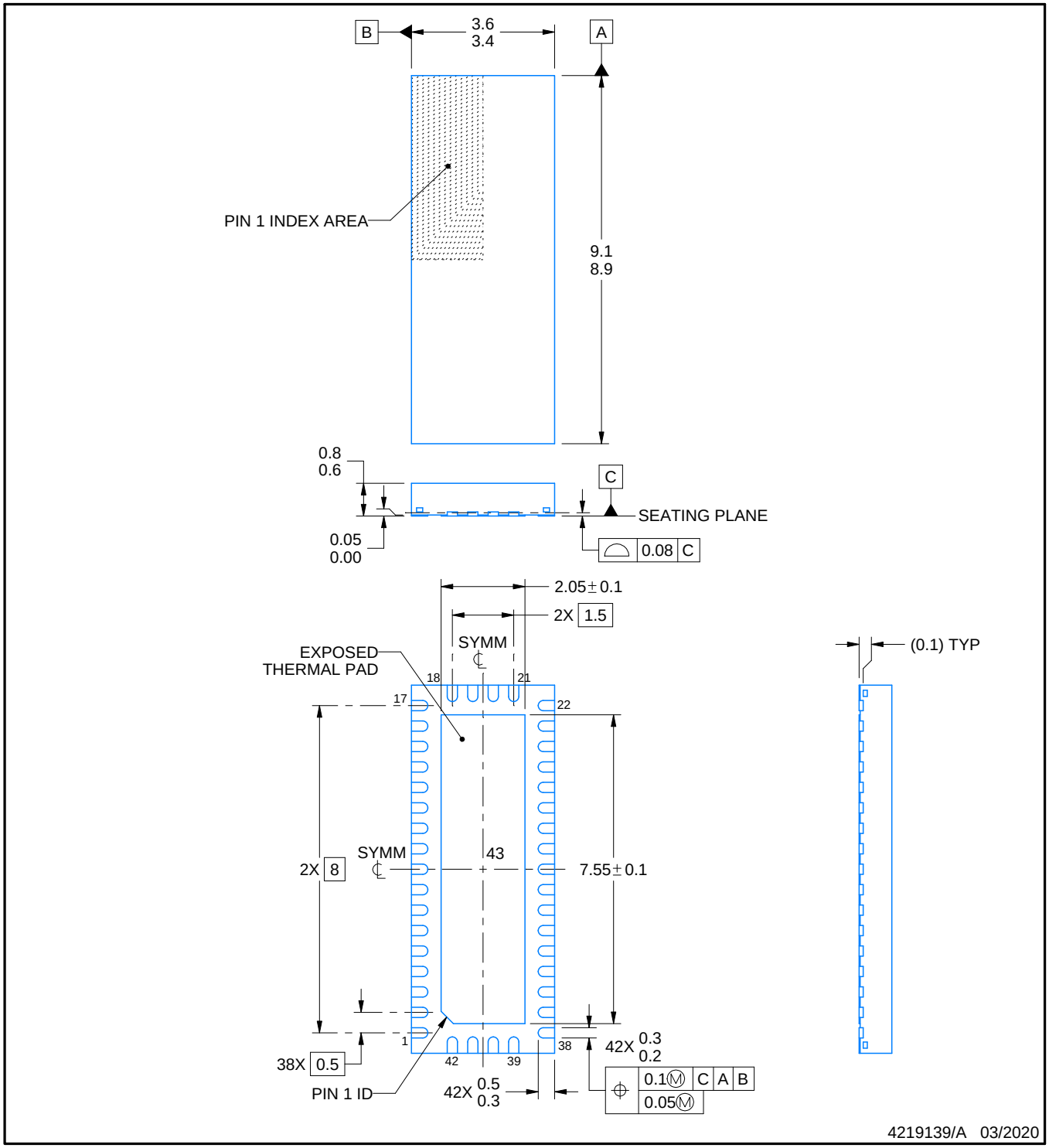
PACKAGE OUTLINE

RUA0042A



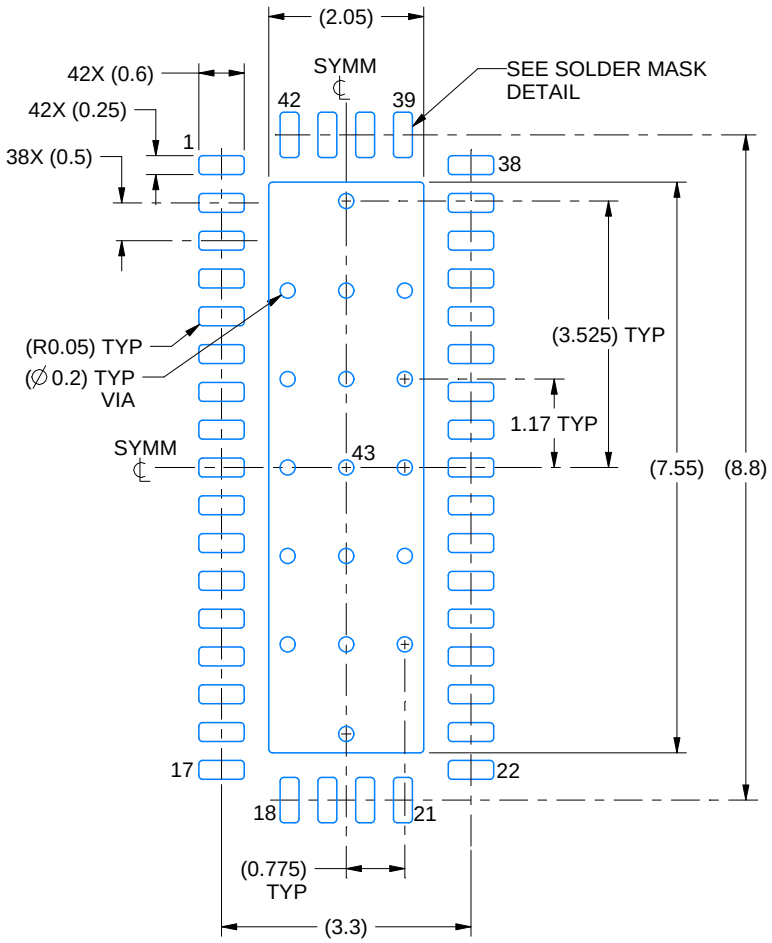
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

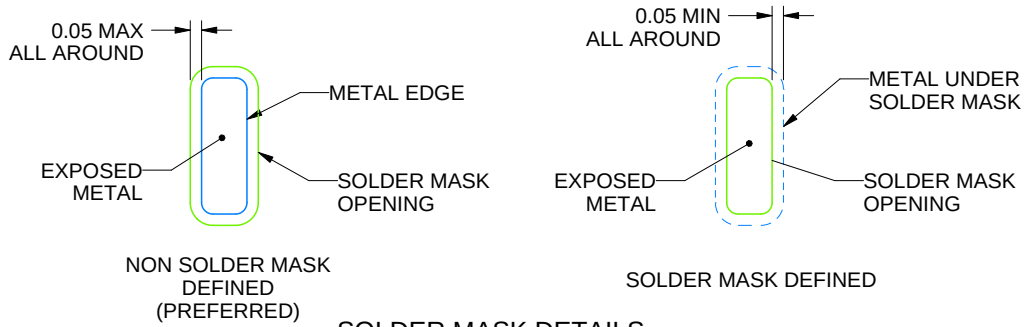


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

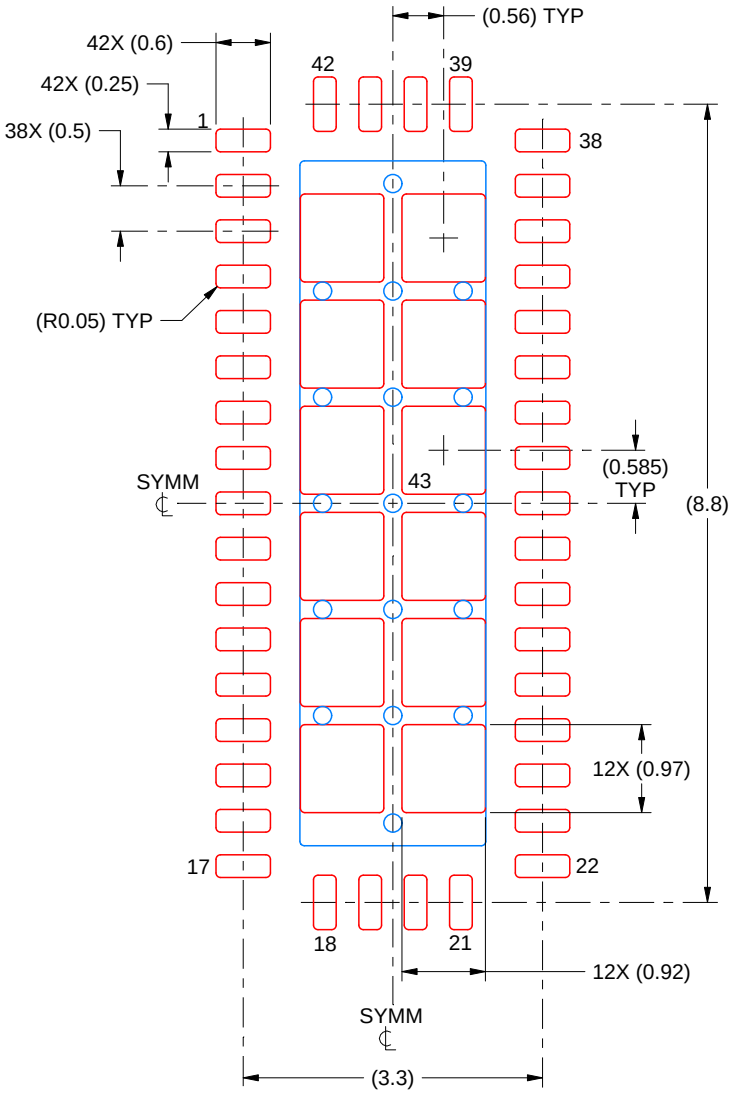
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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