LP5996 Dual Linear Regulator with 300mA and 150mA Outputs

Check for Samples: LP5996

FEATURES

- **2 LDO Outputs with Independent Enable**
- **1.5% Accuracy at Room Temperature, 3% over Temperature**
- **Thermal Shutdown Protection**
- **Stable with Ceramic Capacitors**

APPLICATIONS

- **Cellular Handsets**
- **PDA's**
- **Wireless Network Adaptors**

KEY SPECIFICATIONS

- **Input Voltage Range, 2.0V to 6.0V**
- **Low Dropout Voltage at 300mA, 210mV**
- **Ultra-Low I_Q (Enabled), 35µA**
- **Virtually Zero I_Q (Disabled), <10nA**

PACKAGE

- **All available in Lead Free option.**
- **10 pin SON 3mm x 3mm**

  For other package options contact your Texas Instruments sales office.

DESCRIPTION

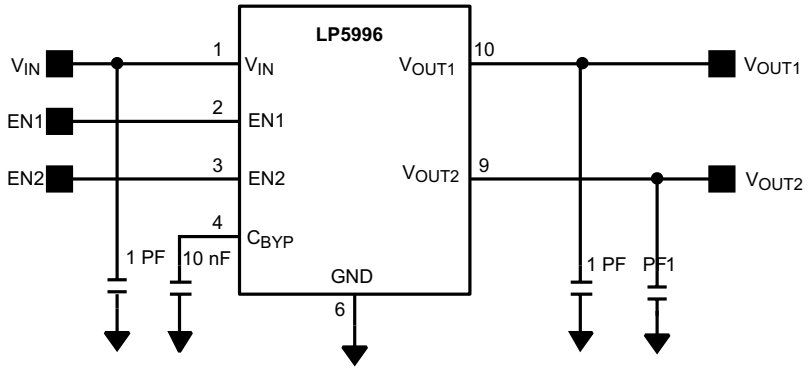
The LP5996 is a dual low dropout regulator. The first regulator can source 150mA, while the second is capable of sourcing 300mA.

The LP5996 provides 1.5% accuracy requiring an ultra low quiescent current of 35µA. Separate enable pins allow each output of the LP5996 to be shut down, drawing virtually zero current.

The LP5996 is designed to be stable with small footprint ceramic capacitors down to 1µF.

The LP5996 is available in fixed output voltages and comes in a 10 pin, 3mm x 3mm package.

Typical Application Circuit



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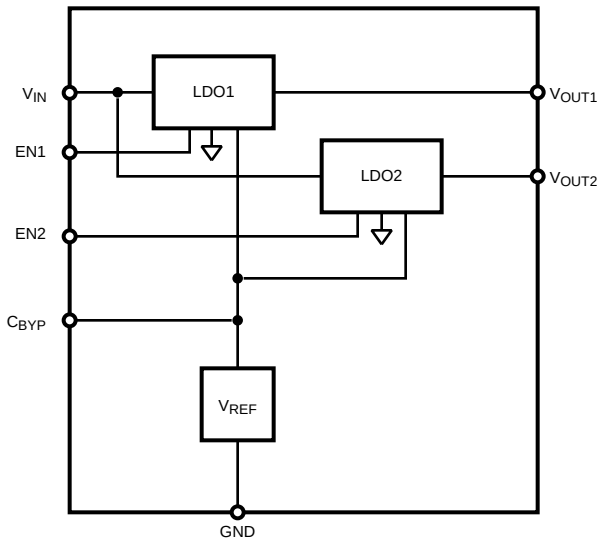
Functional Block Diagram



Pin Descriptions

Name	Pin No	Function
V_{IN}	1	Voltage Supply Input. Connect a 1µF capacitor between this pin and GND.
EN1	2	Enable Input to Regulator 1. Active high input. High = On. Low = OFF.
EN2	3	Enable Input to Regulator 2. Active high input. High = On. Low = OFF.
C_{BYP}	4	Internal Voltage Reference Bypass. Connect a 10nF capacitor from this pin to GND to reduce noise and improve line transient and PSRR. This pin may be left open.
N/C	5	No Connection. Do not connect to any other pin.
GND	6	Common Ground pin. Connect externally to exposed pad.
N/C	7	No Connection. Do not connect to any other pin.
N/C	8	No Connection. Do not connect to any other pin.
V_{OUT2}	9	Output of Regulator 2. 300mA maximum current output. Connect a 1µF capacitor between this pin to GND.
V_{OUT1}	10	Output of Regulator 1. 150mA maximum current output. Connect a 1µF capacitor between this pin to GND.
GND	Pad	Common Ground. Connect to Pin 6.

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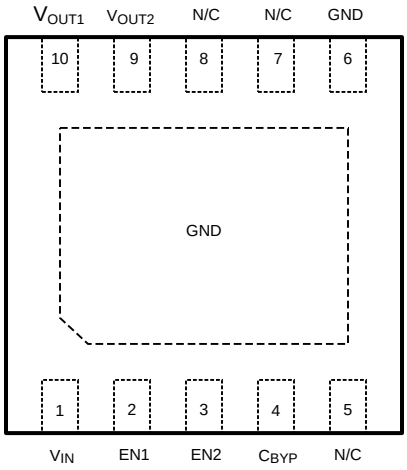
Connection Diagram

10-Pin SON Package



Top View

Figure 1. See Package Number DSC0010A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2) (3)

Input Voltage	-0.3V to 6.5V
V_{OUT1}, V_{OUT2}, EN1, and EN2 Voltage to GND	-0.3V to (V_{IN} + 0.3V) with 6.5V (max)
Junction Temperature (T_{J-MAX})	150°C
Lead/Pad Temp. (4)	235°C
Storage Temperature	-65°C to 150°C
Continuous Power Dissipation Internally Limited (5)	
ESD Rating (6)	
Human Body Model	2.0kV
Machine Model	200V

(1) All Voltages are with respect to the potential at the GND pin.
(2) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(4) For detailed soldering specifications and information, please refer to Application Note AN-1187, Leadless Leadframe Package SNOA401.
(5) Internal thermal shutdown circuitry protects the device from permanent damage.
(6) The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Operating Ratings (1) (2)

Input Voltage	2.0V to 6.0V
EN1, EN2 Voltage	0 to (V_{IN} + 0.3V) to 6.0V (max)

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All Voltages are with respect to the potential at the GND pin.

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Operating Ratings (1) (2) (continued)

Junction Temperature	-40°C to 125°C
Ambient Temperature Range, T_A (3)	-40°C to 85°C

(3) The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Thermal Properties (1)

Junction To Ambient Thermal Resistance (2)	
θ_{JA} SON-10 Package	55°C/W

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics (1) (2)

Unless otherwise noted, V_{EN} = 950mV, $V_{IN} = V_{OUT}$ + 1.0V, or 2.0V, whichever is higher, where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}. C_{IN} = 1 µF, I_{OUT} = 1 mA, $C_{OUT1} = C_{OUT2}$ = 1.0µF.
Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125°C.

Parameter		Test Conditions		Typ	Limit		Units
					Min	Max	
V_{IN}	Input Voltage	(3)			2	6	V
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA	1.5V < V_{OUT} ≤ 3.3V		-2.5 **-3.75**	+2.5 **+3.75**	%
			V_{OUT} ≤ 1.5V		-2.75 **-4**	+2.75 **+4**	
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 6.0V		0.03		**0.3**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 150mA (LDO 1)		85		**155**	µV/mA
		I_{OUT} = 1mA to 300mA (LDO 2)		26		**85**	
V_{DO}	Dropout Voltage (4)	I_{OUT} = 1mA to 150mA (LDO 1)		110		**220**	mV
		I_{OUT} = 1mA to 300mA (LDO 2)		210		**550**	
I_Q	Quiescent Current	LDO 1 ON, LDO 2 ON I_{OUT1}= I_{OUT2} = 0mA		35		**100**	µA
		LDO 1 ON, LDO 2 OFF I_{OUT1} = 150mA		45		**110**	
		LDO 1 OFF, LDO 2 ON I_{OUT2} = 300mA		45		**110**	
		LDO 1 ON, LDO 2 ON I_{OUT1} = 150mA, I_{OUT2} = 300m		70		**170**	
		$V_{EN1} = V_{EN2}$ = 0.4V		0.5		**10**	nA
I_{SC}	Short Circuit Current Limit	LDO 1		420		**750**	mA
		LDO 2		550		**840**	
I_{OUT}	Maximum Output Current	LDO 1			**150**		mA
		LDO 2			**300**		

(1) All Voltages are with respect to the potential at the GND pin.
(2) Min Max limits are ensured by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) $V_{IN(MIN)} = V_{OUT(NOM)}$ + 0.5V, or 2.0V, whichever is higher.
(4) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter only for output voltages above 2.0V

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Electrical Characteristics[1] [2] (continued)

Unless otherwise noted, V_{EN} = 950mV, V_{IN} = V_{OUT} + 1.0V, or 2.0V, whichever is higher, where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT1} = C_{OUT2} = 1.0µF.
Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125°C.

Parameter		Test Conditions		Typ	Limit		Units
					Min	Max	
PSRR	Power Supply Rejection Ratio[5]	f = 1kHz, I_{OUT} = 1mA to 150mA C_{BYP} = 10nF	LDO1	58			dB
			LDO2	70			
		f = 20kHz, I_{OUT} = 1mA to 150mA C_{BYP} = 10nF	LDO1	45			
			LDO2	60			
e_n	Output noise Voltage[5]	BW = 10Hz to 100kHz C_{BYP} = 10nF	V_{OUT} = 0.8V	36			μV_{RMS}
			V_{OUT} = 3.3V	75			
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature		160			°C
		Hysteresis		20			
Enable Control Characteristics							
I_{EN}	Input Current at V_{EN1} or V_{EN2}	V_{EN} = 0.0V		0.005		**0.1**	µA
		V_{EN} = 6V		2		**5**	
V_{IL}	Low Input Threshold					**0.4**	V
V_{IH}	High Input Threshold				**0.95**		V
Timing Characteristics							
T_{ON}	Turn On Time [5]	To 95% Level C_{BYP} = 10nF		300			µs
Transient Response	Line Transient Response $\lvert\delta V_{OUT}\rvert$ [5]	T_{rise} = T_{fall} = 10µs δV_{IN} = 1VC_{BYP} = 10nF		20			mV (pk - pk)
	Load Transient Response $\lvert\delta V_{OUT}\rvert$ [5]	T_{rise} = T_{fall} = 1µs	LDO 1 I_{OUT} = 1mA to 150mA	175			
			LDO 2 I_{OUT} = 1mA to 300mA	150			

(5) This electrical specification is ensured by design.

Output Capacitor, Recommended Specifications

Parameter		Test Conditions	Nom	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitance	Capacitance [1]	1.0	**0.7**		µF
		ESR		5	500	mΩ

(1) The Capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor is X7R. However, depending on the application, X5R, Y5V and Z5U can also be used. (See capacitor section in Applications Hints).

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Typical Performance Characteristics.

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT1} = C_{OUT2} = 1.0µF Ceramic, C_{BYP} = 10nF, V_{IN} = $V_{OUT2(NOM)}$ + 1.0V, T_A = 25°C, $V_{OUT1(NOM)}$ = 3.3V, $V_{OUT2(NOM)}$ = 3.3V, Enable pins are tied to V_{IN}.

Output Voltage Change vs Temperature

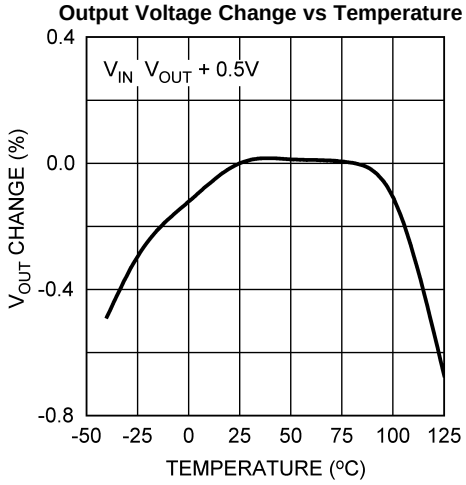

Figure 2.

Ground Current vs Load Current,LDO1

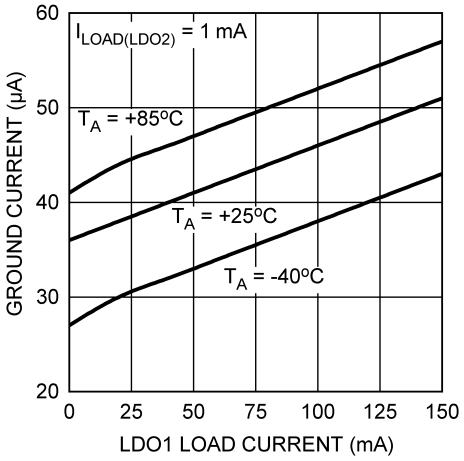

Figure 3.

Ground Current vs Load Current, LDO2

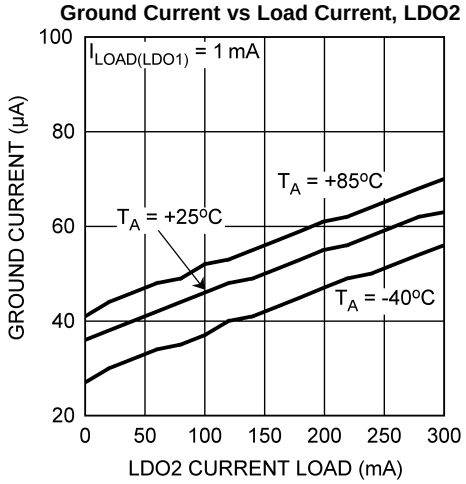

Figure 4.

Ground Current vs V_{IN}, I_{LOAD} = 1mA

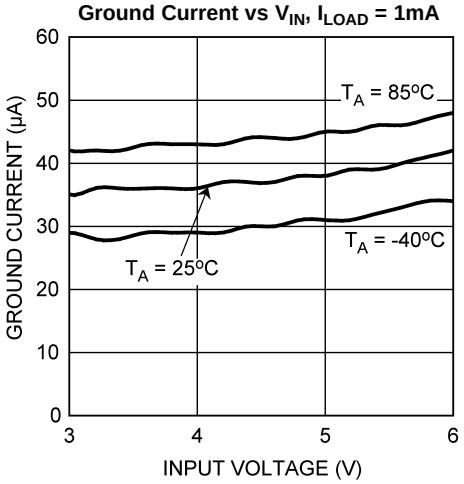

Figure 5.

Dropout Voltage vs I_{LOAD}, LDO1

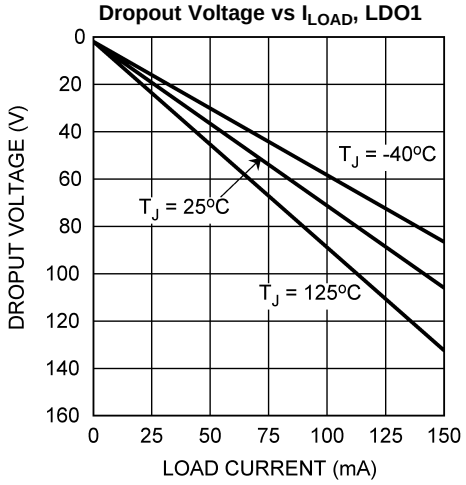

Figure 6.

Dropout Voltage vs I_{LOAD}, LDO2

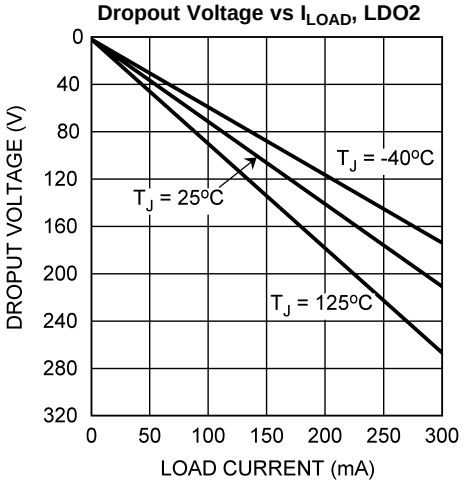

Figure 7.

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Typical Performance Characteristics. (continued)

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT1} = C_{OUT2} = 1.0µF Ceramic, C_{BYP} = 10nF, V_{IN} = $V_{OUT2(NOM)}$ + 1.0V, T_A = 25°C, $V_{OUT1(NOM)}$ = 3.3V, $V_{OUT2(NOM)}$ = 3.3V, Enable pins are tied to V_{IN}.

Line Transient, C_{BYP} = 10nF

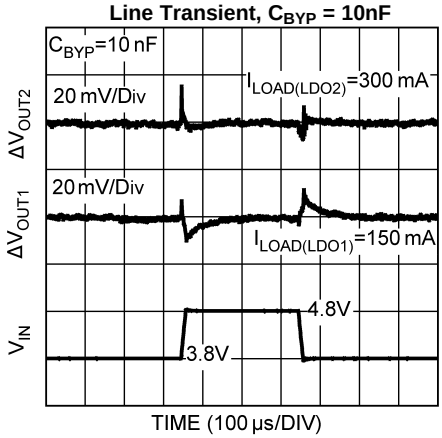

Figure 8.

Line Transient, C_{BYP} = 0

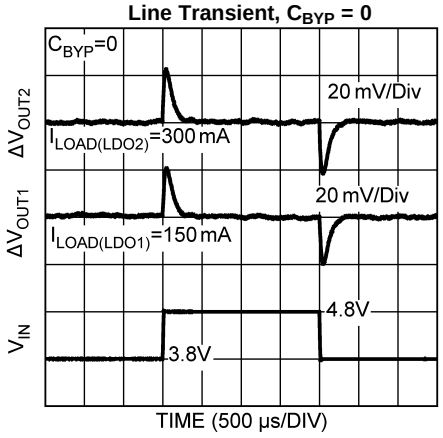

Figure 9.

Load Transient, LDO1

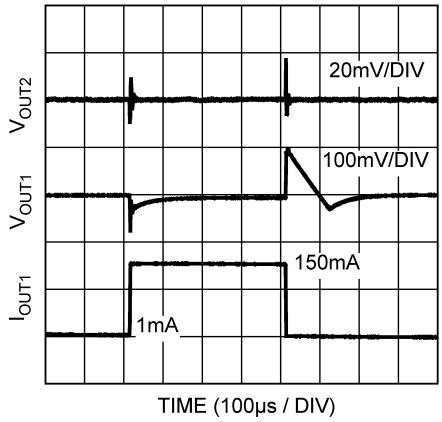

Figure 10.

Load Transient, LDO2

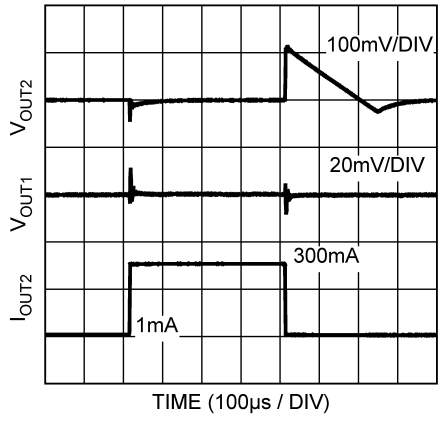

Figure 11.

Noise Density, LDO1

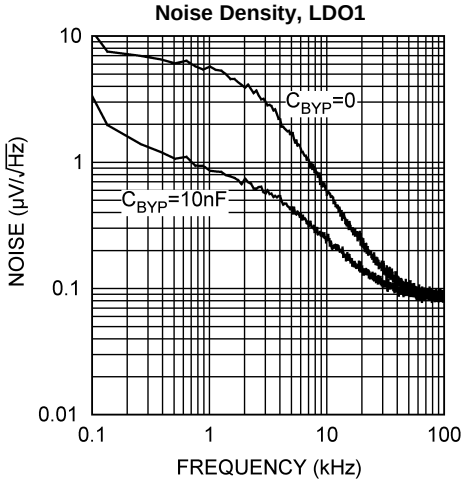

Figure 12.

Noise Density, LDO2

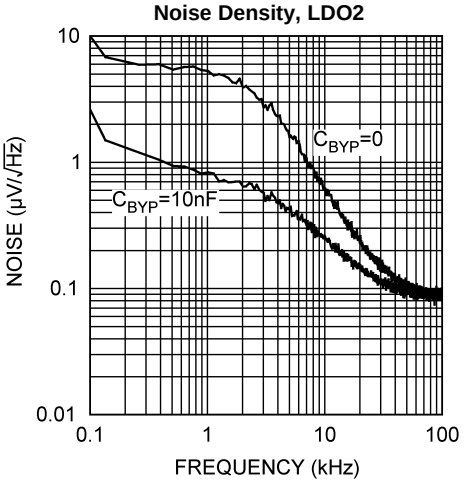

Figure 13.

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Typical Performance Characteristics. (continued)

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT1} = C_{OUT2} = 1.0µF Ceramic, C_{BYP} = 10nF, V_{IN} = $V_{OUT2(NOM)}$ + 1.0V, T_A = 25°C, $V_{OUT1(NOM)}$ = 3.3V, $V_{OUT2(NOM)}$ = 3.3V, Enable pins are tied to V_{IN}.

Short Circuit Current, LDO1

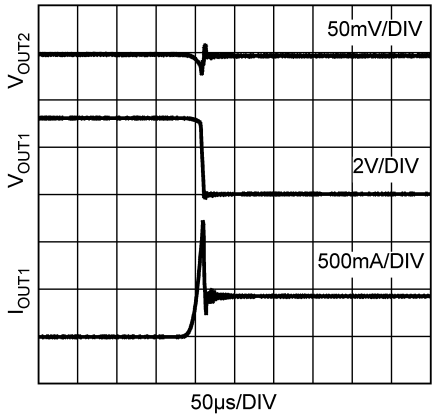

Figure 14.

Short Circuit Current, LDO2

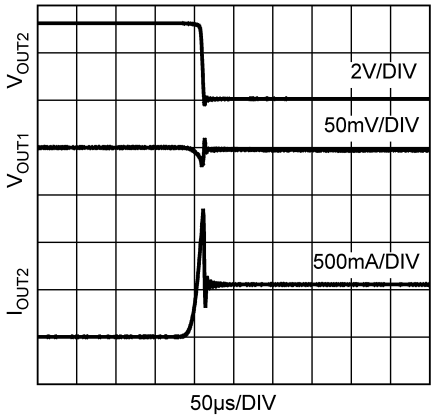

Figure 15.

Power Supply Rejection Ratio, LDO1

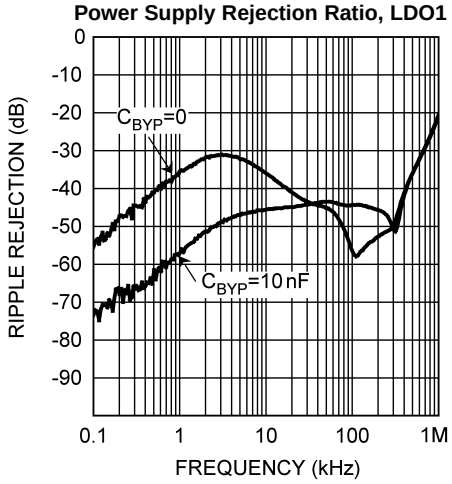

Figure 16.

Power Supply Rejection Ratio, LDO2

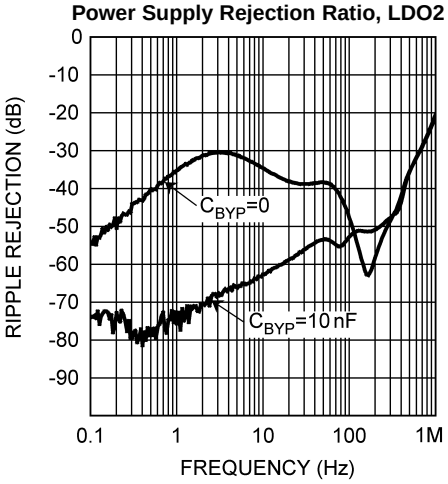

Figure 17.

Enable Start-up Time, C_{BYP} = 0

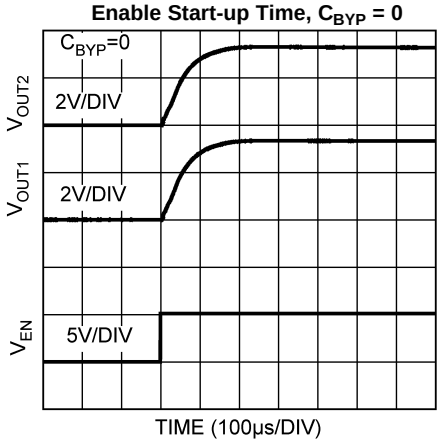

Figure 18.

Enable Start-up Time, C_{BYP} = 10nF

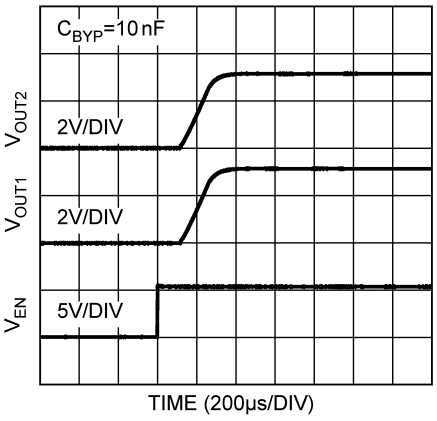

Figure 19.

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APPLICATION HINTS

OPERATION DESCRIPTION

The LP5996 is a low quiescent current, power management IC, designed specifically for portable applications requiring minimum board space and smallest components. The LP5996 contains two independently selectable LDOs. The first is capable of sourcing 150mA at outputs between 0.8V and 3.3V. The second can source 300mA at an output voltage of 0.8V to 3.3V.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP5996 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5996 is designed specifically to work with very small ceramic output capacitors. A 1.0µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5mΩ to 500mΩ, is suitable in the LP5996 application circuit.

For this device the output capacitor should be connected between the V_{OUT} pin and ground.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5mΩ to 500mΩ for stability.

NO-LOAD STABILITY

The LP5996 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP5996 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP5996.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 20 shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result

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in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

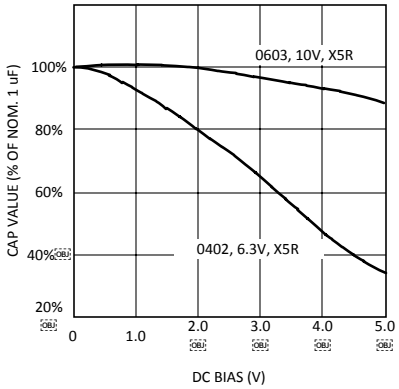

Figure 20. Graph Showing a Typical Variation in Capacitance vs DC Bias

The capacitance value of ceramic capacitors varies with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

ENABLE CONTROL

The LP5996 features active high enable pins for each regulator, EN1 and EN2, which turns the corresponding LDO off when pulled low. The device outputs are enabled when the enable pins are set to high. When not enabled the regulator output is off and the device typically consumes 2nA.

If the application does not require the Enable switching feature, one or both enable pins should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the enable inputs must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

BYPASS CAPACITOR

The internal voltage reference circuit of the LP5996 is connected to the C_{BYP} pin via a high value internal resistor. An external capacitor, connected to this pin, forms a low-pass filter which reduces the noise level on both outputs of the device. There is also some improvement in PSSR and line transient performance. Internal circuitry ensures rapid charging of the C_{BYP} capacitor during start-up. A 10nF, high quality ceramic capacitor with either NPO or COG dielectric is recommended due to their low leakage characteristics and low noise performance.

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SAFE AREA OF OPERATION

Due consideration should be given to operating conditions to avoid excessive thermal dissipation of the LP5996 or triggering its thermal shutdown circuit. When both outputs are enabled, the total power dissipation will be $P_{D(LDO1)} + P_{D(LDO2)}$ where PD = (V_{IN} - V_{OUT}) x I_{OUT} for each LDO

In general, device options which have a large difference in output voltage will dissipate more power with both outputs enabled, due to the input voltage required for the higher output voltage LDO. In such cases, especially at elevated ambient temperature, it may not be possible to operate both outputs at maximum current at the same time.

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5996SD-1018/NOPB	ACTIVE	WSON	DSC	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM		L224B	Samples
LP5996SD-1833/NOPB	ACTIVE	WSON	DSC	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM		L225B	Samples
LP5996SD-2533/NOPB	ACTIVE	WSON	DSC	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM		L226B	Samples
LP5996SD-2828/NOPB	ACTIVE	WSON	DSC	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L180B	Samples
LP5996SD-3033/NOPB	ACTIVE	WSON	DSC	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L179B	Samples
LP5996SD-3333/NOPB	ACTIVE	WSON	DSC	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L182B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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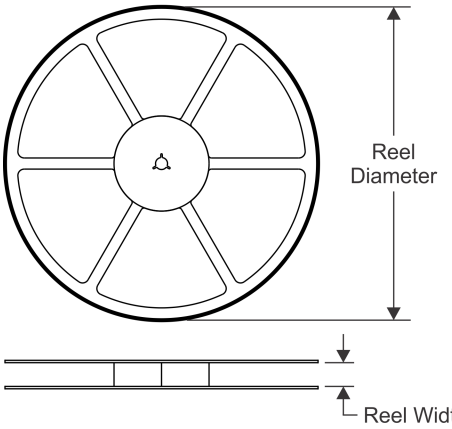
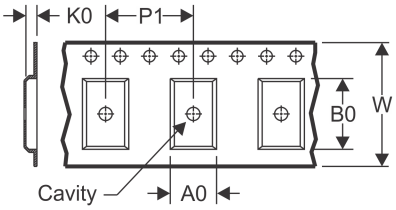
TAPE AND REEL INFORMATION

REEL DIMENSIONS

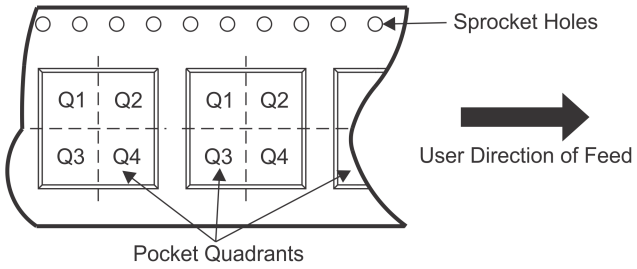


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

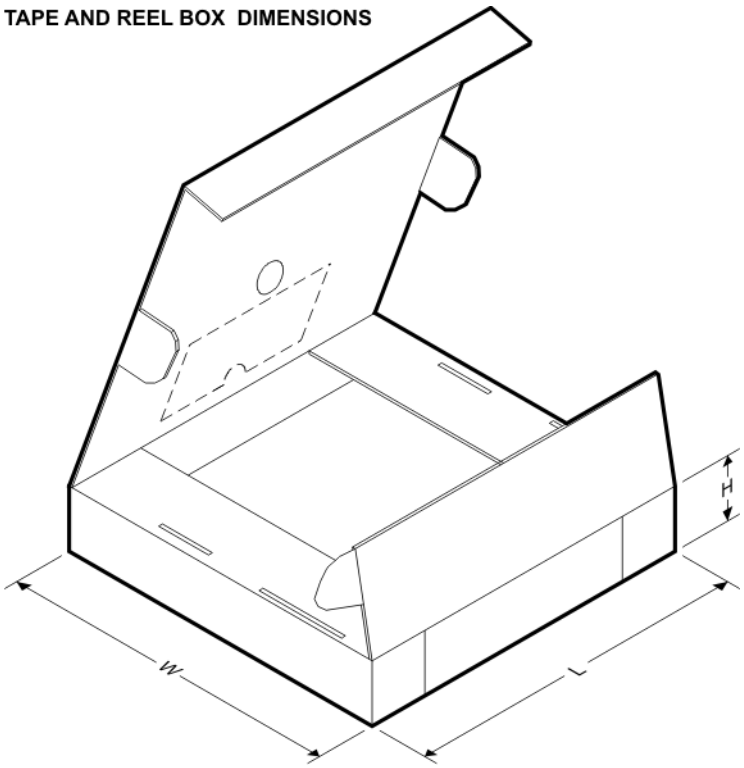
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5996SD-1018/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-1833/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-2533/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-2828/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3033/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3333/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

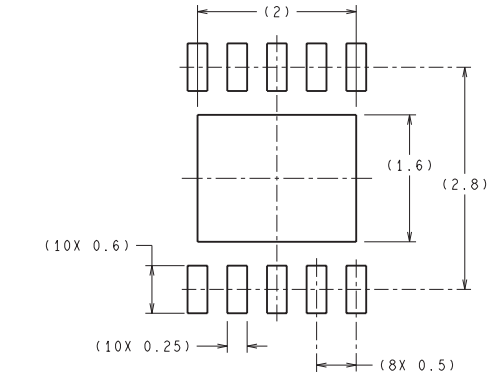
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

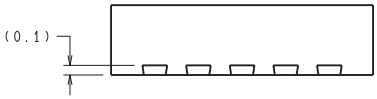
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5996SD-1018/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0
LP5996SD-1833/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0
LP5996SD-2533/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0
LP5996SD-2828/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0
LP5996SD-3033/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0
LP5996SD-3333/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0

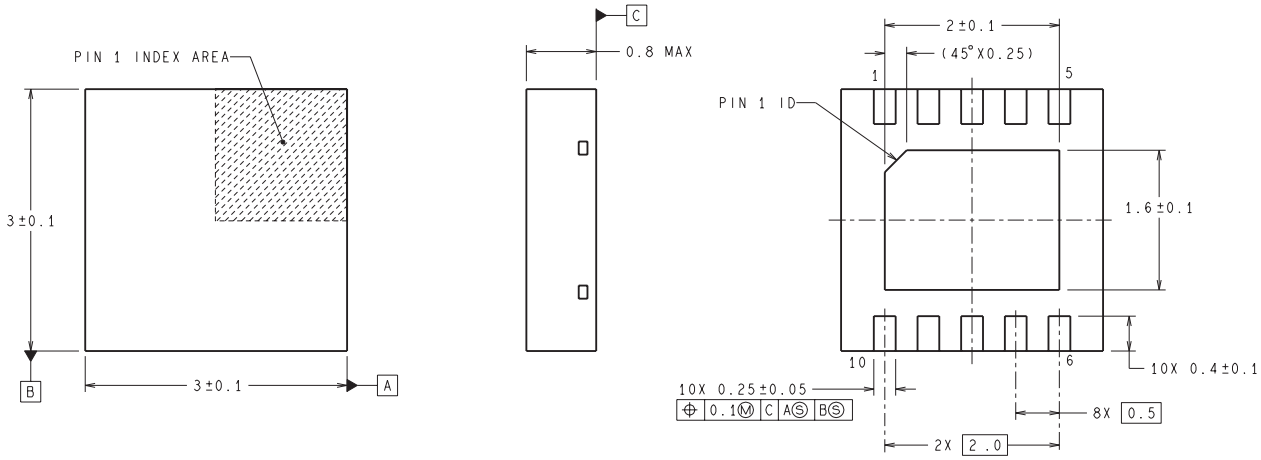
DSC0010A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





SDA10A (Rev A)

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