UCC27201A-Q1 120V 3A 峰值电流的高频高侧/低侧驱动器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度等级 1：-40°C 至 140°C 的环境运行温度范围
  - 器件人体模型 (HBM) 分类等级 1C
  - 器件充电器件模型 (CDM) 分类等级 C3
- HS 引脚具备 -18V 的负电压处理能力
- 可驱动两个采用高侧/低侧配置的 N 沟道金属氧化物半导体场效应晶体管 (MOSFET)
- 最大启动电压：120V
- 最大 VDD 电压：20V
- 片载0.65V VF， 0.6Ω RD 自举二极管
- 工作频率高于 1MHz
- 20ns 传播延迟时间
- 3A 吸收，3A 供电输出电流
- 8ns 上升时间和 7ns 下降时间（采用 1000pF 负载时）
- 1ns 延迟匹配
- 用于高端和低端驱动器的欠压闭锁功能
- 采用 8 引脚 PowerPad™ 小尺寸集成电路 (SOIC)-8 (DDA) 封装

2 应用

- 辅助反相器
- 功率传输电路的 DC-DC 转换器
- 开关模式电源
- 电机控制
- 半桥式应用和全桥式转换器
- 两开关正激式转换器
- 有源箝位正激式转换器
- 高电压同步降压型转换器
- D 类音频放大器

3 说明

UCC27201A-Q1 高频 N 沟道 MOSFET 驱动器由 120V 自举二极管和高侧/低侧驱动器组成，其中高侧/低侧驱动器配有独立输入，可最大限度提高控制灵活性。 这可在半桥式、全桥式、两开关正激式和有源箝位正激式转换器中提供N沟道 MOSFET 控制。 低端和高端栅极驱动器是独立控制的，并在彼此的接通和关断之间实现了至 1ns 的匹配。 UCC27201A-Q1 基于常见的 UCC27200 和 UCC27201 驱动器，但提供了一些增强功能。 UCC27201A-Q1 的 HS 引脚最高能够承受 -18V 电压，这使得其在电源噪声环境下的性能得到了改善。

由于在芯片上集成了一个自举二极管，因此无需采用外部分立式二极管。 为高端和低端驱动器提供了欠压闭锁功能，如果驱动电压低于规定的门限，则强制输出为低电平。

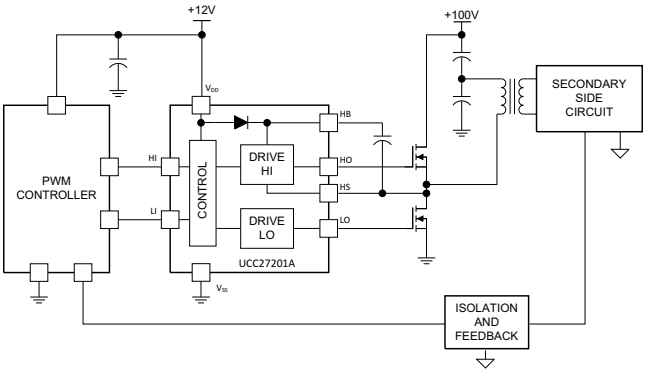
UCC27201A-Q1 具有 TTL 兼容阈值，并且采用带有散热焊盘的 8 引脚 SOIC 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC27201A-Q1	DDA (8)	4.89mm × 3.90mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化的应用示意图



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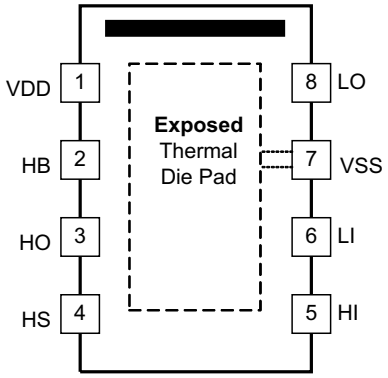
4 修订历史记录

日期	修订版本	注释
2015 年 3 月	*	首次发布。

5 Pin Configuration and Functions

8-Pin SOIC-8 Power Pad
Package DDA
(Top View)



Pin VSS and the exposed thermal die pad are internally connected.

Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	DDA		
HB	2	P	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF, the value is dependant on the gate charge of the high-side MOSFET however.
HI	5	I	High-side input.
HO	3	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	P	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
LI	6	I	Low-side input.
LO	8	O	Low-side output. Connect to the gate of the low-side power MOSFET.
N/C	-	-	No connection. Pins labeled N/C have no connection.
PowerPAD™	Pad(2)	G	Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.
VDD	1	P	Positive supply to the lower gate driver. De-couple this pin to VSS (GND). Typical decoupling capacitor range is 0.22 µF to 1.0 µF.
VSS	7	G	Negative supply terminal for the device which is generally grounded.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output
(2) Pin VSS and the exposed thermal die pad are internally connected on the DDA package. Electrically referenced to VSS (GND).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted). All voltages are with respect to V_{SS} (1)

PARAMETER			MIN	MAX	UNIT
V_{DD}	Supply voltage range(2)		-0.3	20	V
V_{HI}, V_{LI}	Input voltages on LI and HI		-0.3	20	
V_{LO}	Output voltage on LO	DC	-0.3	V_{DD} + 0.3	
		Repetitive pulse <100 ns(3)	-2	V_{DD} + 0.3	
V_{HO}	Output voltage on HO	DC	V_{HS} – 0.3	V_{HB} + 0.3	
		Repetitive pulse <100 ns(3)	V_{HS} - 2	V_{HB} + 0.3, (V_{HB} - V_{HS} <20)	
V_{HS}	Voltage on HS	DC	-1	120	
		Repetitive pulse <100 ns(3)	-18	120	
V_{HB}	Voltage on HB		-0.3	120	
	Voltage on HB-HS		-0.3	20	
T_J	Operating virtual junction temperature		-40	+150	°C
T_{stg}	Storage temperature		-65	+150	
	Lead temperature (soldering, 10 sec.)			+300	
	Power dissipation at T_A = 25°C (DDA package) (4)			2.7	W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to V_{ss}. Currents are positive into, negative out of the specified terminal.
(3) Values are verified by characterization and are not production tested.
(4) This data was taken using the JEDEC proposed high-K test PCB. See Thermal Information for details.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	8	12	17	V
V_{HS}	Voltage on HS	-1		105	
	Voltage on HS, (repetitive pulse <100 ns)	-15		110	
V_{HB}	Voltage on HB	V_{HS} + 8, V_{DD} –1		V_{HS} + 17, 115	
V_{sr}	Voltage slew rate on HS			50	V / ns
T_J	Operating junction temperature range	-40		+140	°C

6.4 Thermal Information

THERMAL METRIC		DDA (SOIC-8)	UNITS
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	40.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	49.0	
θ_{JB}	Junction-to-board thermal resistance	10.2	
ψ_{JT}	Junction-to-top characterization parameter	3.1	
ψ_{JB}	Junction-to-board characterization parameter	9.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.5	

6.5 Electrical Characteristics

over operating free-air temperature range, $V_{DD} = V_{HB} = 12$ V, $V_{HS} = V_{SS} = 0$ V, No load on LO or HO, $T_A = T_J = -40°C$ to +140°C, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I_{DD}	VDD quiescent current		$V_{LI} = V_{HI} = 0$		0.4	0.8	mA
I_{DDO}	VDD operating current		f = 500 kHz, $C_{LOAD} = 0$		3.8	5.5	
I_{HB}	Boot voltage quiescent current		$V_{LI} = V_{HI} = 0$ V		0.4	0.8	
I_{HBO}	Boot voltage operating current		f = 500 kHz, $C_{LOAD} = 0$		2.5	4	
I_{HBS}	HB to V_{SS} quiescent current		$V_{HS} = V_{HB} = 110$ V		0.0005	1	uA
I_{HBSO}	HB to V_{SS} operating current		f = 500 kHz, $C_{LOAD} = 0$		0.1		mA
INPUT							
V_{HIT}	Input voltage threshold				1.7	2.5	
V_{LIT}	Input voltage threshold			0.8	1.6		
V_{IHYS}	Input voltage Hysteresis				100		mV
R_{IN}	Input pulldown resistance			100	200	350	kΩ
UNDERVOLTAGE PROTECTION (UVLO)							
	VDD rising threshold			6.2	7.1	7.8	V
	VDD threshold hysteresis				0.5		
	VHB rising threshold			5.8	6.7	7.2	
	VHB threshold hysteresis				0.4		
BOOTSTRAP DIODE							
V_F	Low-current forward voltage		I_{VDD} - HB = 100 µA		0.65	0.85	V
V_{FI}	High-current forward voltage		I_{VDD} - HB = 100 mA		0.85	1.1	
R_D	Dynamic resistance, ΔVF/ΔI		I_{VDD} - HB = 100 mA and 80 mA		0.6	1.0	Ω
LO GATE DRIVER							
V_{LOL}	Low level output voltage		I_{LO} = 100 mA		0.18	0.4	V
V_{LOH}	High level output voltage	T_J = -40 to 125°C	I_{LO} = -100 mA, $V_{LOH} = V_{DD} - V_{LO}$		0.25	0.4	
		T_J = -40 to 140°C	I_{LO} = -100 mA, $V_{LOH} = V_{DD} - V_{LO}$		0.25	0.42	
	Peak pull-up current		V_{LO} = 0 V		3		A
	Peak pull-down current		V_{LO} = 12 V		3		

Electrical Characteristics (continued)

over operating free-air temperature range, V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_A = T_J = -40°C to +140°C, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
HO GATE DRIVER							
V_{HOL}	Low level output voltage		I_{HO} = 100 mA		0.18	0.4	V
V_{HOH}	High level output voltage	T_J = -40 to 125°C	I_{HO} = -100 mA, V_{HOH} = V_{HB}-V_{HO}		0.25	0.4	V
		T_J = -40 to 140°C	I_{HO} = -100 mA, V_{HOH} = V_{HB}-V_{HO}		0.25	0.42	V
	Peak pull-up current		V_{HO} = 0 V		3		A
	Peak pull-down current		V_{HO} = 12 V		3		A

6.6 Switching Characteristics

PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
PROPAGATION DELAYS							
t_{DLFF}	V_{LI} falling to V_{LO} falling	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	ns
t_{DHFF}	V_{HI} falling to V_{HO} falling	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	ns
t_{DLRR}	V_{LI} rising to V_{LO} rising	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	ns
t_{DHRR}	V_{HI} rising to V_{HO} rising	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	ns
DELAY MATCHING							
t_{MON}	LI ON, HI OFF				1	7	ns
t_{MOFF}	LI OFF, HI ON				1	7	ns
OUTPUT RISE AND FALL TIME							
t_R	LO, HO		C_{LOAD} = 1000 pF		8		ns
t_F	LO, HO		C_{LOAD} = 1000 pF		7		ns
t_R	LO, HO (3 V to 9 V)		C_{LOAD} = 0.1 µF		0.35	0.6	us
t_F	LO, HO (3 V to 9 V)		C_{LOAD} = 0.1 µF		0.3	0.6	us
MISCELLANEOUS							
	Minimum input pulse width that changes the output				50		ns
	Bootstrap diode turn-off time		I_F = 20 mA, I_{REV} = 0.5 A(1) (2)		20		ns

(1) Typical values for T_A = 25°C
(2) I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.

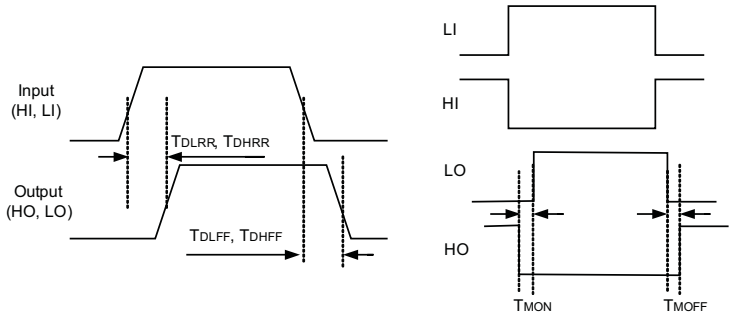
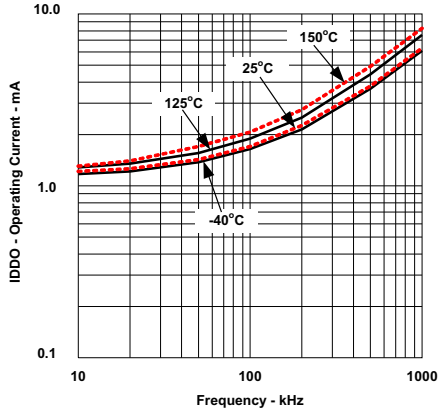


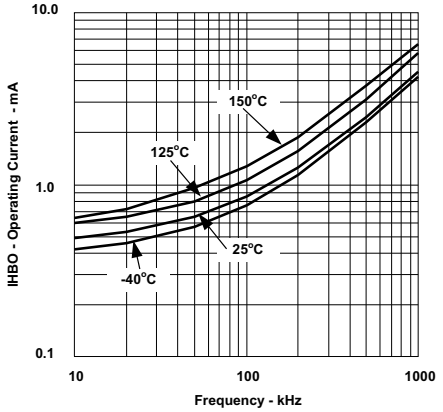
Figure 1. Timing Requirements

6.7 Typical Characteristics



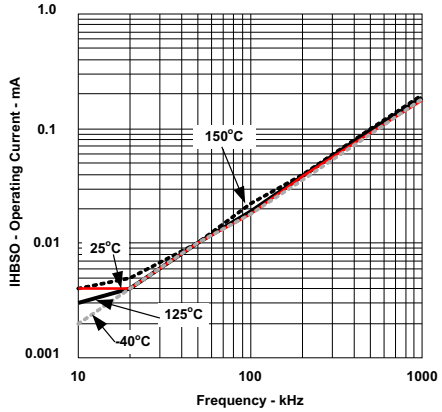
VDD = 12 V
No Load on Outputs

Figure 2. IDD Operating Current vs Frequency



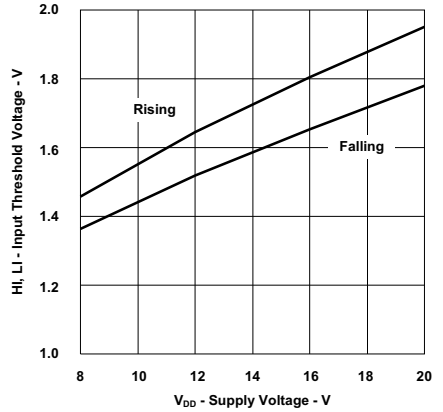
HB = 12 V
No Load on Outputs

Figure 3. Boot Voltage Operating Current vs Frequency



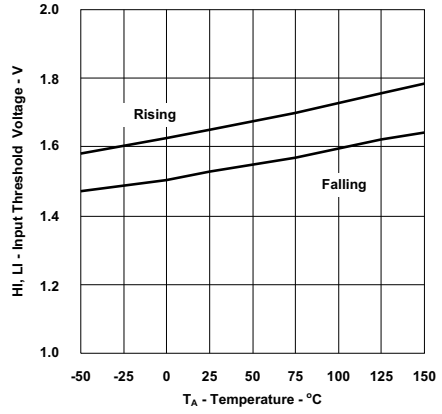
HB = 12 V
No Load on Outputs

Figure 4. HB TO VSS Operating Current vs Frequency



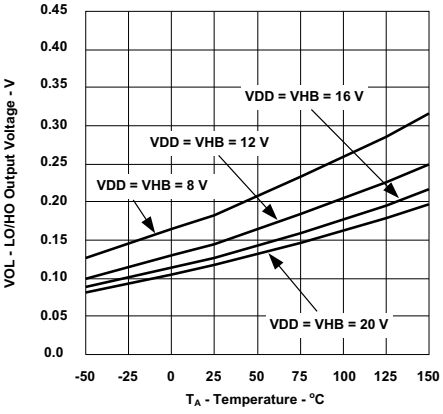
T = 25°C

Figure 5. Input Threshold vs Supply Voltage



VDD = 12 V

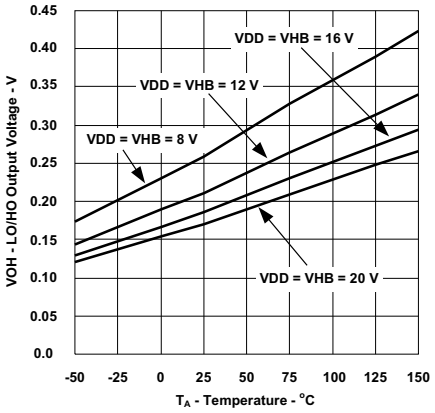
Figure 6. Input Threshold vs Temperature



I_{LO} = I_{HO} = -100 mA
V_{DD} = V_{HB} = 16 V

Figure 7. LO and HO High Level Output Voltage vs Temperature

Typical Characteristics (continued)



I_{LO} = I_{HO} = 100 mA

Figure 8. LO and HO Low Level Output Voltage vs Temperature

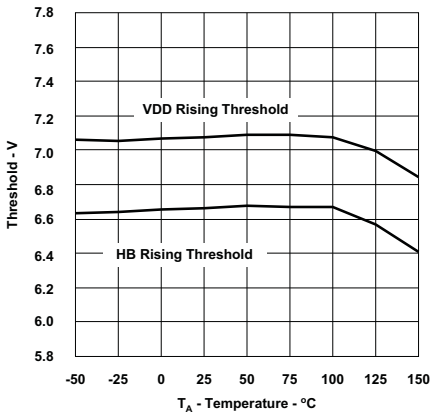


Figure 9. Undervoltage Lockout Threshold vs Temperature

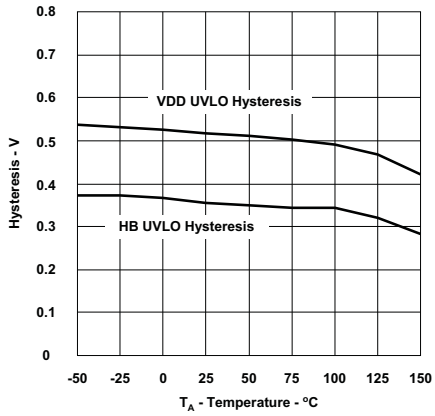
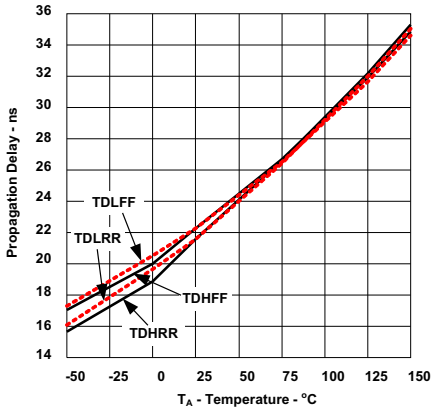
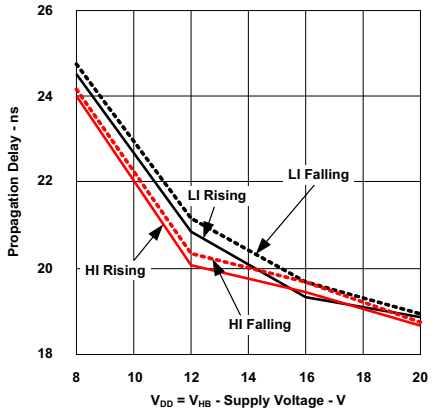


Figure 10. Undervoltage Lockout Threshold Hysteresis vs Temperature



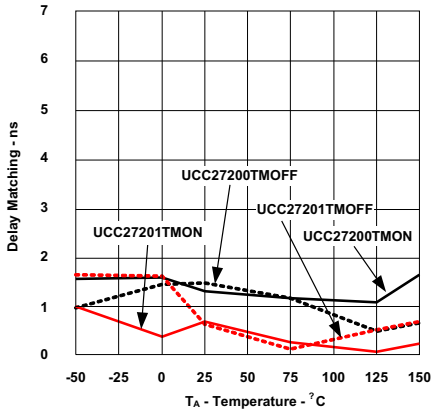
V_{DD} = V_{HB} = 12 V

Figure 11. Propagation Delays vs Temperature



T = 25°C

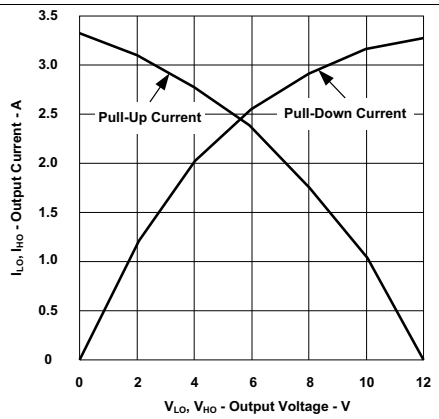
Figure 12. Propagation Delay vs Supply Voltage



V_{DD} = V_{HB} = 12 V

Figure 13. Delay Matching vs Temperature

Typical Characteristics (continued)



$V_{DD} = V_{HB} = 12$ V

Figure 14. Output Current vs Output Voltage

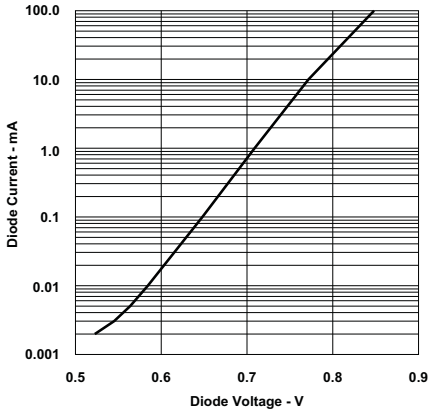
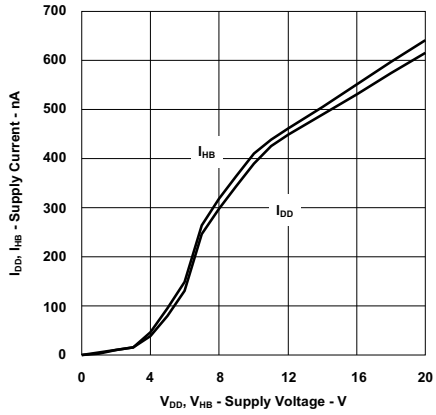


Figure 15. Diode Current vs Diode Voltage



Inputs Low
T = 25°C

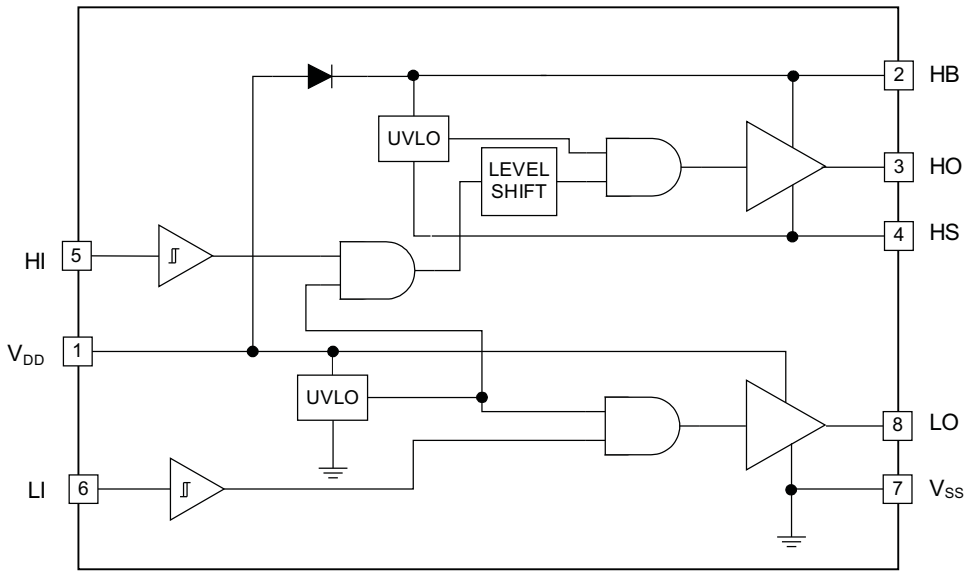
Figure 16. Quiescent Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The UCC27201A-Q1 is a high-side/low-side driver. The high-side and low-side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27201A-Q1. The UCC27201-Q1 inputs are TTL-compatible. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to VSS which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stages

The input stages provide the interface to the PWM output signals. The input stages of the UCC27201A-Q1 incorporate an open drain configuration to provide the lower input thresholds. The input impedance is 200 kΩ nominal and input capacitance is approximately 4 pF. The 200 kΩ is a pull-down resistance to VSS (ground). The logic level compatible input provides a rising threshold of 1.7 V and a falling threshold of 1.6 V.

7.3.1.1 UVLO (Under Voltage Lockout)

The bias supplies for the high-side and low-side drivers have UVLO protection. VDD as well as VHB to VHS differential voltages are monitored. The VDD UVLO disables both drivers when VDD is below the specified threshold. The rising VDD threshold is 7.1 V with 0.5-V hysteresis. The VHB UVLO disables only the high-side driver when the VHB to VHS differential voltage is below the specified threshold. The VHB UVLO rising threshold is 6.7 V with 0.4-V hysteresis.

7.3.1.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

Feature Description (continued)

7.3.1.3 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27201A-Q1 driver. The diode anode is connected to VDD and cathode connected to VHB. With the VHB capacitor connected to HB and the HS pins, the VHB capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

7.3.1.4 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from VDD to VSS and the high-side is referenced from VHB to VHS.

7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See *UVLO (Under Voltage Lockout)* for more information on UVLO operation mode. In normal mode, the output stage is dependent on the states of the HI and LI pins.

Table 1. Device Logic Table

HI PIN	LI PIN	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.
(2) LO is measured with respect to VSS.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

8.2 Typical Application

An open loop half-bridge converter was used to calculate performance in an actual application.

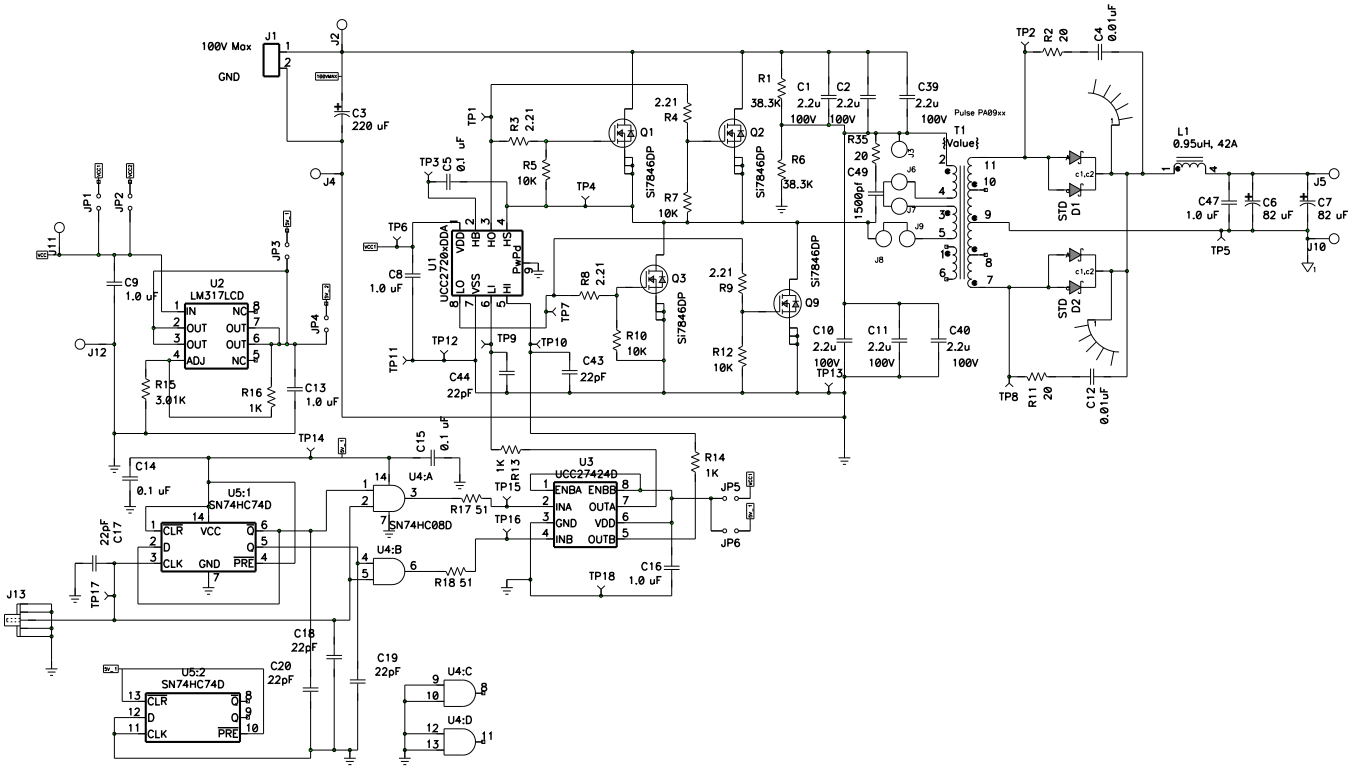


Figure 17. Open Loop Half-Bridge Converter

8.2.1 Design Requirements

Table 2. UCC27201A-Q1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Supply Voltage, VDD	12 V
Voltage on HS, VHS	0 V to 100 V
Voltage on HB, VHB	12 V to 112 V
Output	4 V, 20 A
Frequency	200 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Switching the MOSFETs

Achieving optimum drive performance at high frequency efficiently requires special attention to layout and minimizing parasitic inductances. Care must be taken at the driver die and package level as well as the PCB layout to reduce parasitic inductances as much as possible. Figure 18 shows the main parasitic inductance elements and current flow paths during the turn ON and OFF of the MOSFET by charging and discharging its CGS capacitance.

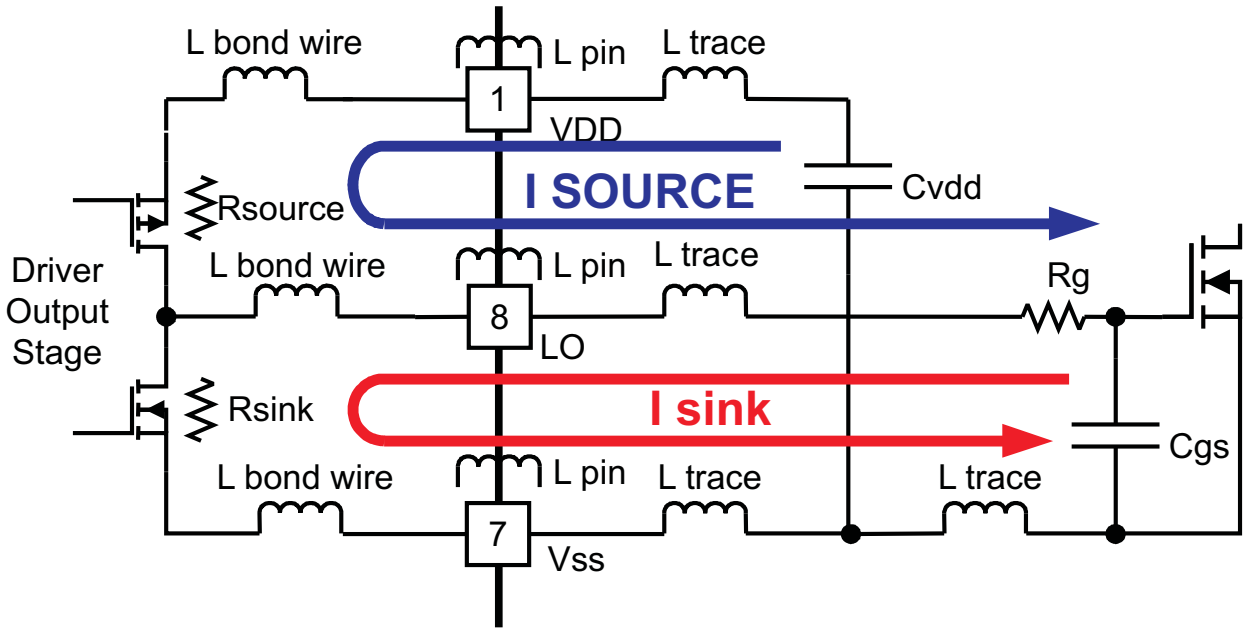


Figure 18. MOSFET Drive Paths and Circuit Parasitics

The I_{SOURCE} current charges the C_{GS} gate capacitor and the I_{SINK} current discharges it. The rise and fall time of the voltage across the gate to source defines how quickly the MOSFET can be switched. Based on actual measurements, the analytical curves in Figure 19 and Figure 20 indicate the output voltage and current of the drivers during the discharge of the load capacitor. Figure 19 shows voltage and current as a function of time. Figure 20 indicates the relationship of voltage and current during fast switching. These figures demonstrate the actual switching process and limitations due to parasitic inductances.

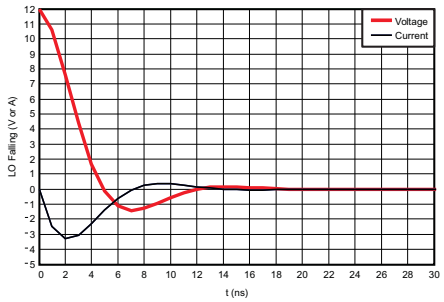


Figure 19. Turn-Off Voltage and Current vs Time

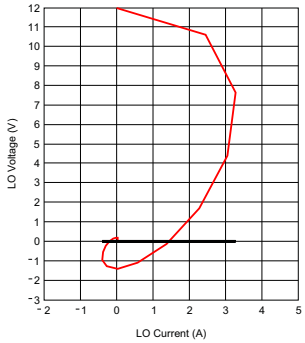


Figure 20. Turn-Off Voltage and Current Switching Diagram

Turning off the MOSFET needs to be achieved as fast as possible to minimize switching losses. For this reason, the UCC27201A-Q1 driver is designed for high peak currents and low output resistance. The sink capability is specified as 0.18 V at 100-mA dc current implying 1.8-Ω $R_{DS(on)}$. With 12-V drive voltage, no parasitic inductance and a linear resistance, one would expect initial sink current amplitude of 6.7 A for both high-side and low-side drivers. Assuming a pure R-C discharge circuit of the gate capacitor, one would expect the voltage and current waveforms to be exponential. Due to the parasitic inductances and non-linear resistance of the driver MOSFET'S, the actual waveforms have some ringing and the peak-sink current of the drivers is approximately 3.3 A as shown in Figure 14. The overall parasitic inductance of the drive circuit is estimated at 4 nH. The internal parasitic inductance of the SOIC-8 package is estimated to be 2 nH including bond wires and leads.

Actual measured waveforms are shown in Figure 21 and Figure 22. As shown, the typical rise time of 8 ns and fall time of 7 ns is conservatively rated.

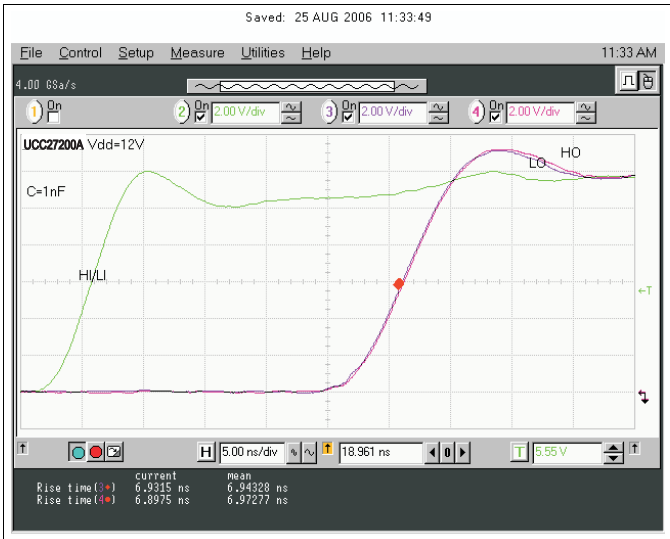


Figure 21. V_{LO} and V_{HO} Rise Time, 1-nF Load, 5 ns/Div

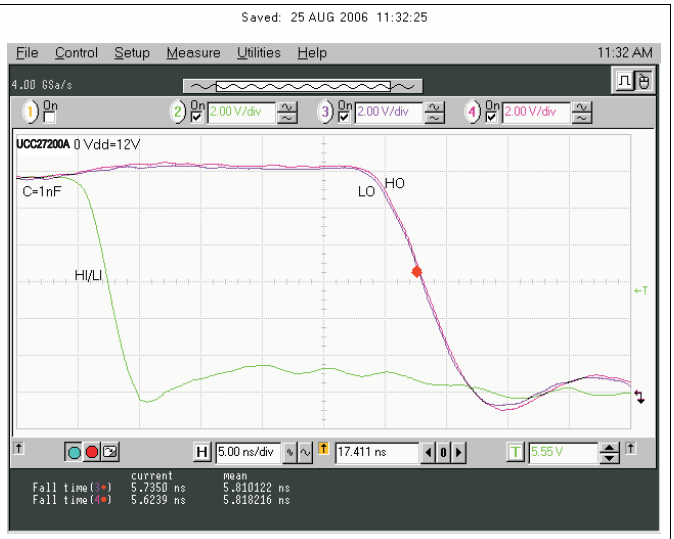


Figure 22. V_{LO} and V_{HO} Fall Time, 1-nF Load, 5-ns/Div

8.2.2.2 Dynamic Switching of the MOSFETs

The true behavior of MOSFETS presents a dynamic capacitive load primarily at the gate to source threshold voltage. Using the turn off case as the example, when the gate to source threshold voltage is reached the drain voltage starts rising, the drain to gate parasitic capacitance couples charge into the gate resulting in the turn off plateau. The relatively low threshold voltages of many MOSFETS and the increased charge that has to be removed (Miller charge) makes good driver performance necessary for efficient switching. An open loop half bridge power converter was utilized to evaluate performance in actual applications. The schematic of the half-bridge converter is shown in Figure 17. The turn off waveforms of the UCC27201A-Q1 driving two MOSFETs in parallel is shown in Figure 23 and Figure 24.

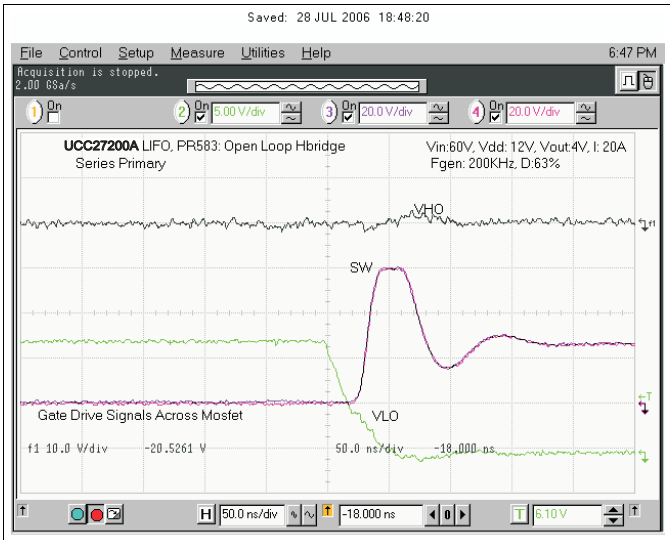


Figure 23. V_{LO} Fall Time in Half-Bridge Converter

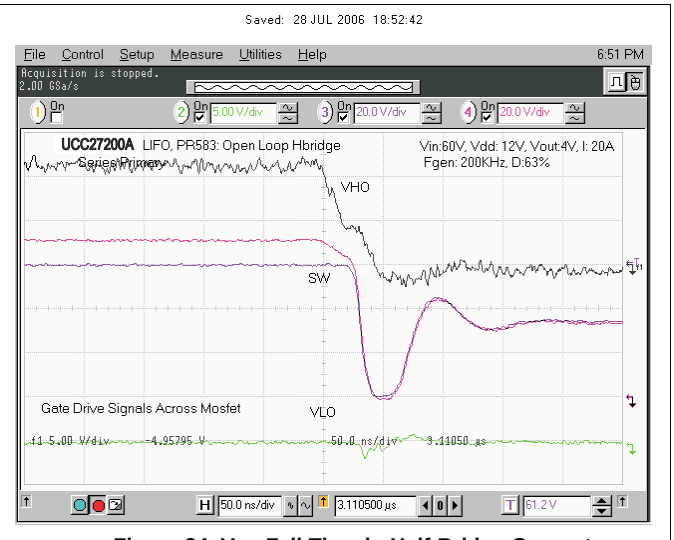


Figure 24. V_{HO} Fall Time in Half-Bridge Converter

8.2.2.3 Delay Matching and Narrow Pulse Widths

The total delays encountered in the PWM, driver and power stage need to be considered for a number of reasons, primarily delay in current limit response. Also to be considered are differences in delays between the drivers which can lead to various concerns depending on the topology. The sync-buck topology switching requires careful selection of dead-time between the high- and low-side switches to avoid 1) cross conduction and 2) excessive body diode conduction. Bridge topologies can be affected by a resulting volt-sec imbalance on the transformer if there is imbalance in the high and low side pulse widths in a steady state condition.

Narrow pulse width performance is an important consideration when transient and short circuit conditions are encountered. Although there may be relatively long steady state PWM output-driver-MOSFET signals, very narrow pulses may be encountered in 1) soft start, 2) large load transients, and 3) short circuit conditions.

The UCC27201A-Q1 driver offers excellent performance regarding high and low-side driver delay matching and narrow pulse width performance. The delay matching waveforms are shown in Figure 25 and Figure 26. The UCC27201A-Q1 driver narrow pulse performance is shown in Figure 27 and Figure 28.

Figure 25. V_{LO} and V_{HO} Rising Edge Delay Matching

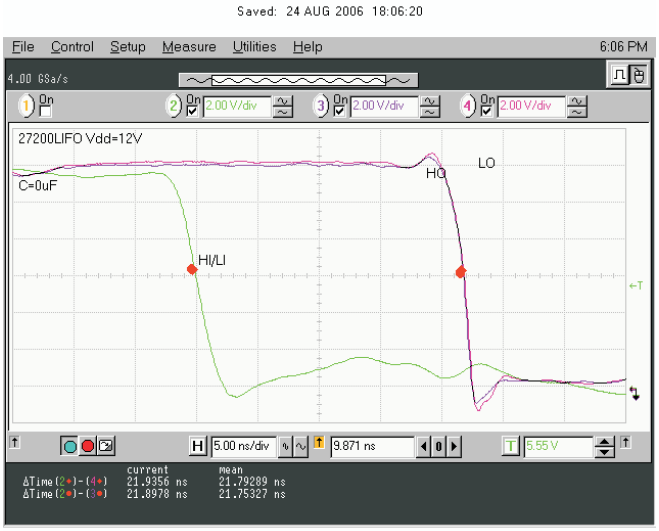


Figure 26. V_{LO} and V_{HO} Falling Edge Delay Matching

Figure 27. 20-ns Input Pulse Delay Matching

Figure 28. 10-ns Input Pulse Delay Matching

8.2.2.4 Boot Diode Performance

The UCC27201A-Q1 driver incorporates the bootstrap diode necessary to generate the high side bias internally. The characteristics of this diode are important to achieve efficient, reliable operation. The dc characteristics to consider are V_F and dynamic resistance. A low V_F and high dynamic resistance results in a high forward voltage during charging of the bootstrap capacitor. The UCC27201A-Q1 has a boot diode rated at 0.65-V V_F and dynamic resistance of 0.6 Ω for reliable charge transfer to the bootstrap capacitor. The dynamic characteristics to consider are diode recovery time and stored charge. Diode recovery times that are specified with no conditions can be misleading. Diode recovery times at no forward current (I_F) can be noticeably less than with forward current applied. The UCC27201A-Q1 boot diode recovery is specified at 20 ns at I_F = 20 mA, I_{REV} = 0.5 A. At 0 mA I_F, the reverse recovery time is 15 ns.

Another less obvious consideration is how the stored charge of the diode is affected by applied voltage. On every switching transition when the HS node transitions from low to high, charge is removed from the boot capacitor to charge the capacitance of the reverse biased diode. This is a portion of the driver power losses and reduces the voltage on the HB capacitor. At higher applied voltages, the stored charge of the UCC27201A-Q1 PN diode is often less than a comparable Schottky diode.

8.2.3 Application Curves

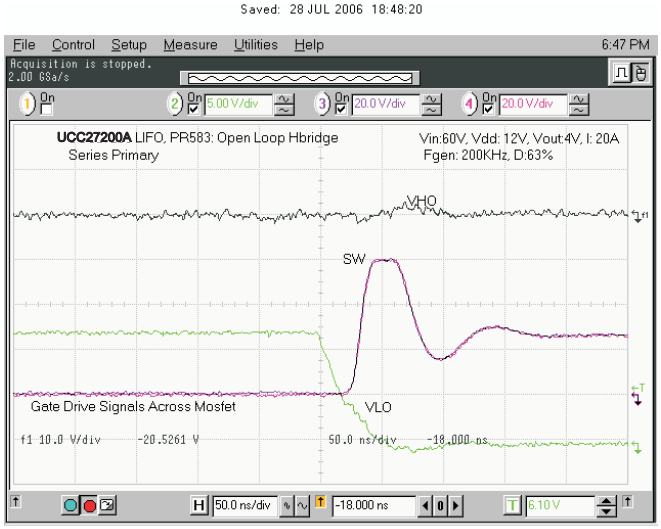


Figure 29. V_{LO} Fall Time in Half-Bridge Converter

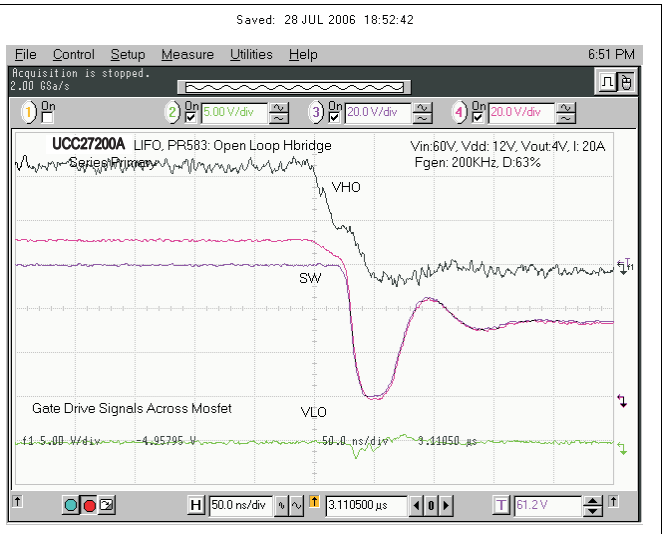


Figure 30. V_{HO} Fall Time in Half-Bridge Converter

9 Power Supply Recommendations

The bias supply voltage range for which the device is rated to operate is from 8 V to 17 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 17 V. The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD(hys).Therefore, ensuring that, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the V(OFF) threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the VDD pin voltage has exceeded above the V(ON) threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the HO pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the HO pin a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that a local bypass capacitor is provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends using a capacitor in the range 0.22 uF to 4.7 uF between VDD and GND. In a similar manner, the current pulses delivered by the LO pin are sourced from the HB pin. Therefore a 0.022-uF to 0.1-uF local decoupling capacitor is recommended between the HB and HS pins.

10 Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and V_{HB} (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA package as GND by connecting it to the VSS pin (GND). *Note: The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.*
- Use similar rules for the HS node as for GND for the high side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. 60 mil to 100 mil width is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node needs to be routed from one layer to another. For GND the number of vias needs to be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid L_I and H_I (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.
- Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

10.2 Layout Example

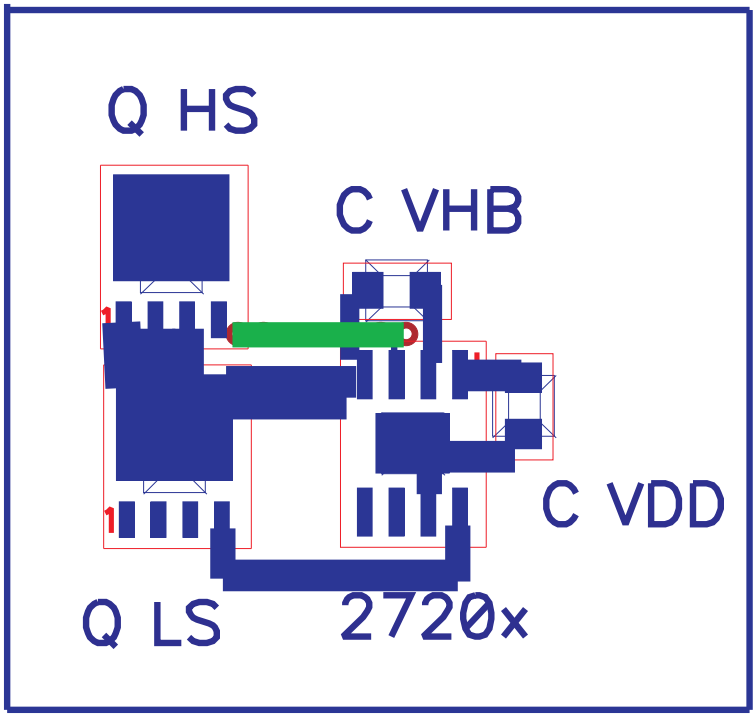


Figure 31. Example Component Placement

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

更多信息，请参见以下文档：

1. 《*QFN/SON PCB 连接应用报告*》（文献编号：SLUA271）
2. 《*PowerPAD™ 散热增强型封装*》（文献编号：SLMA002）
3. 《*PowerPAD™ 速成*》（文献编号：SLMA004）

11.2 商标

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All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27201AQDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	201AQ1	Samples
UCC27201AQDMKRQ1	ACTIVE	VSON	DMK	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC 27201AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

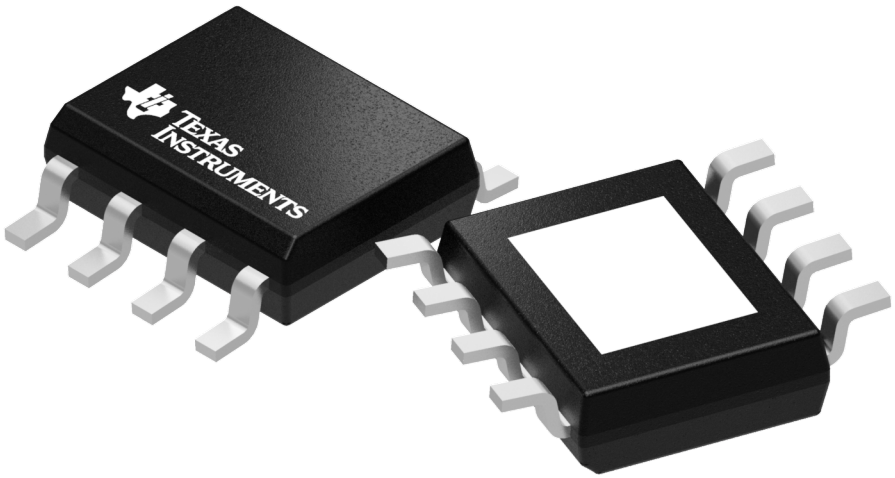
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

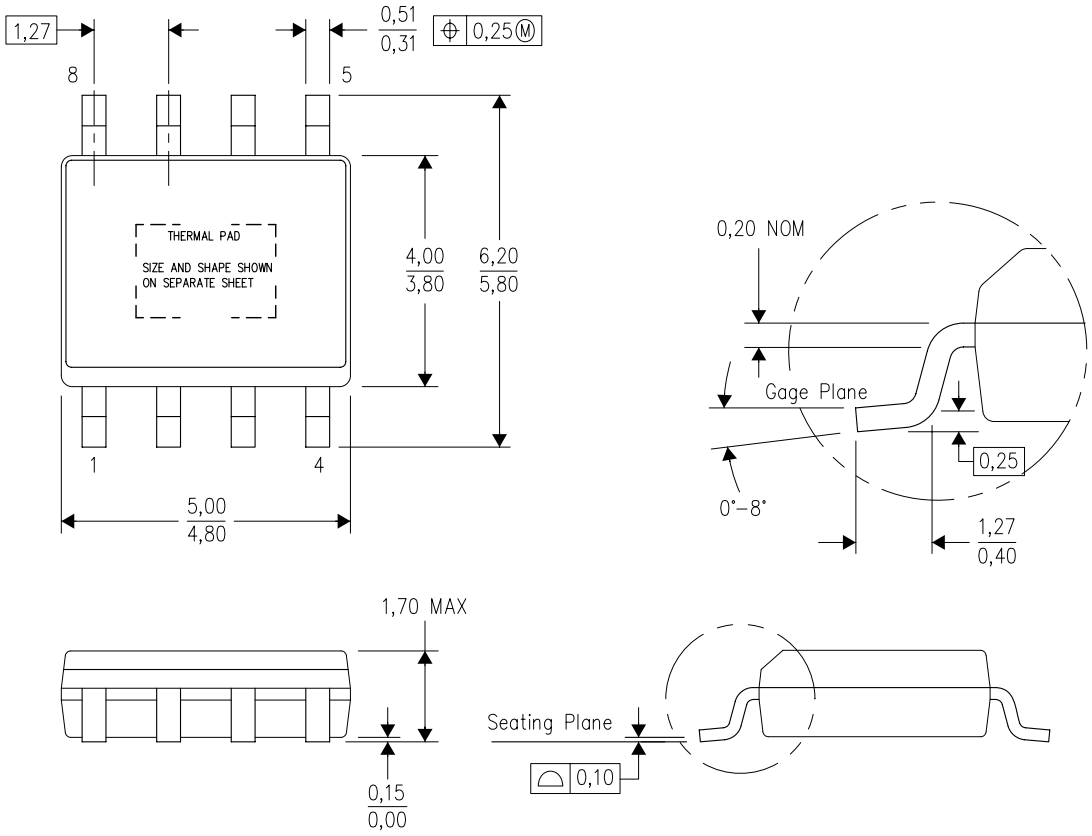
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

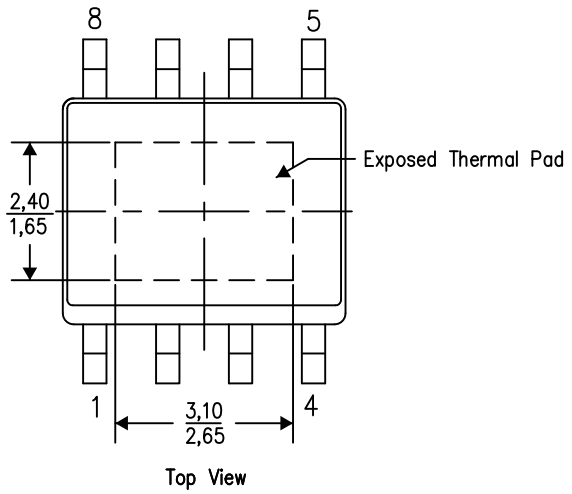
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



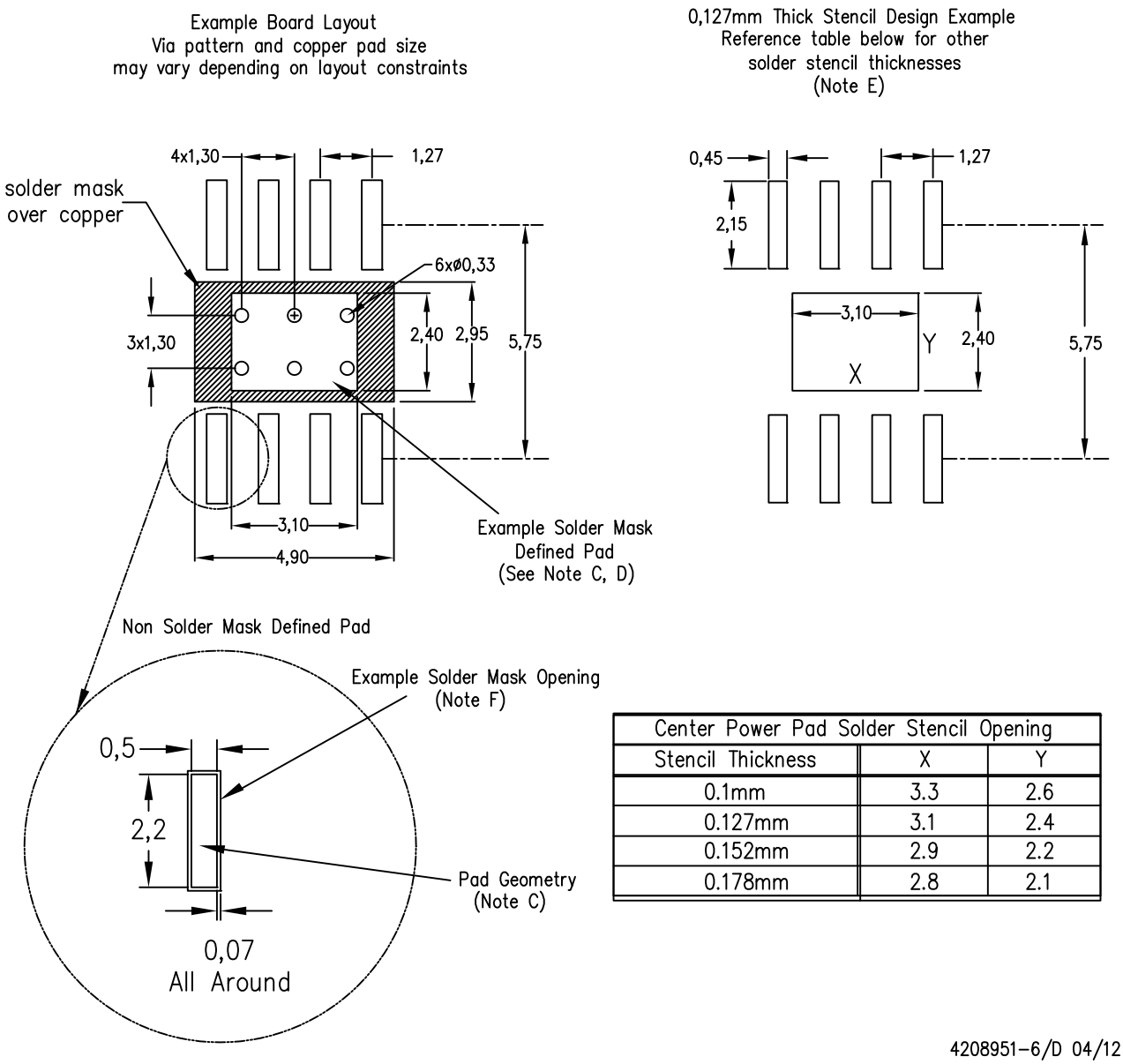
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

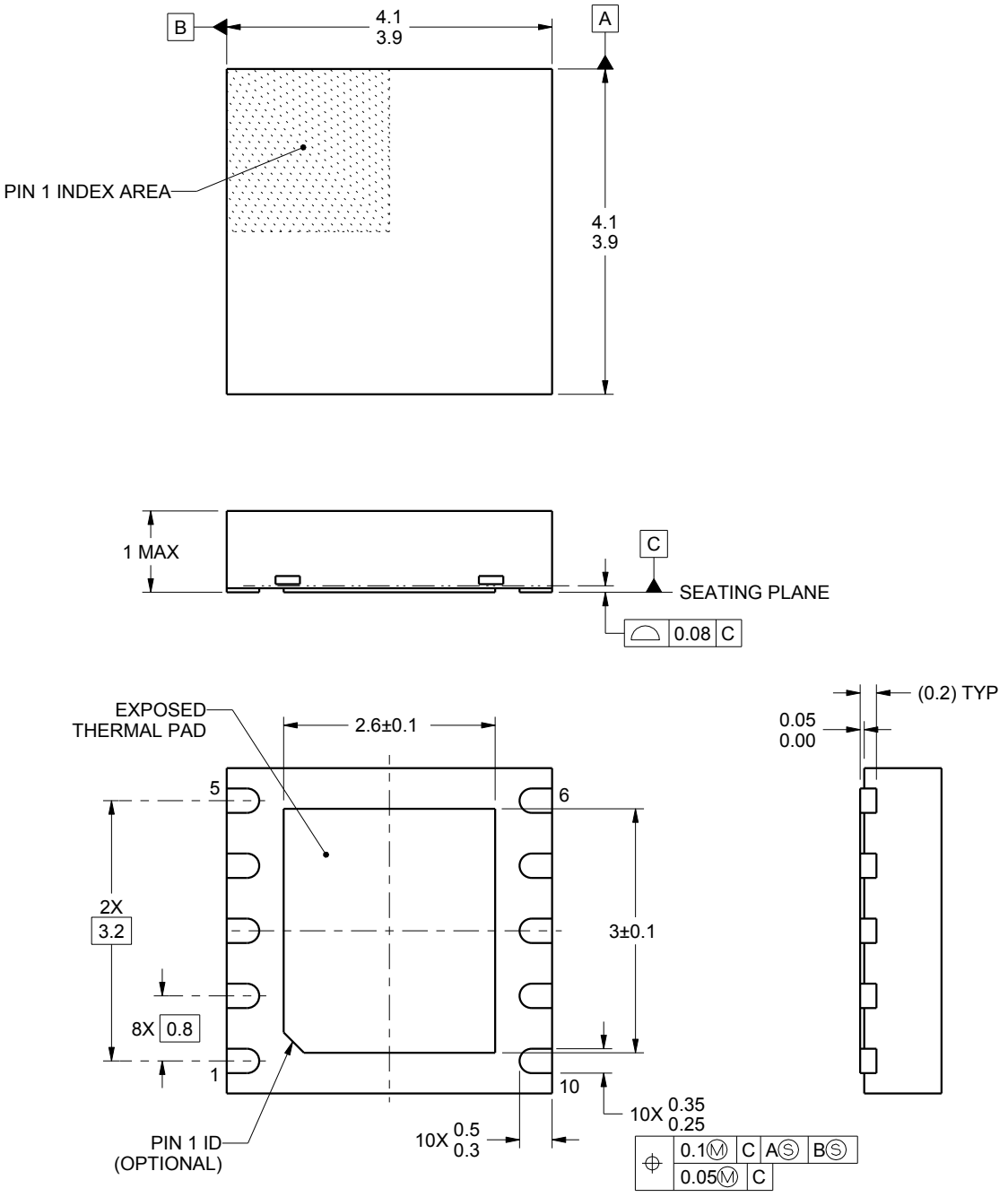
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DMK0010A

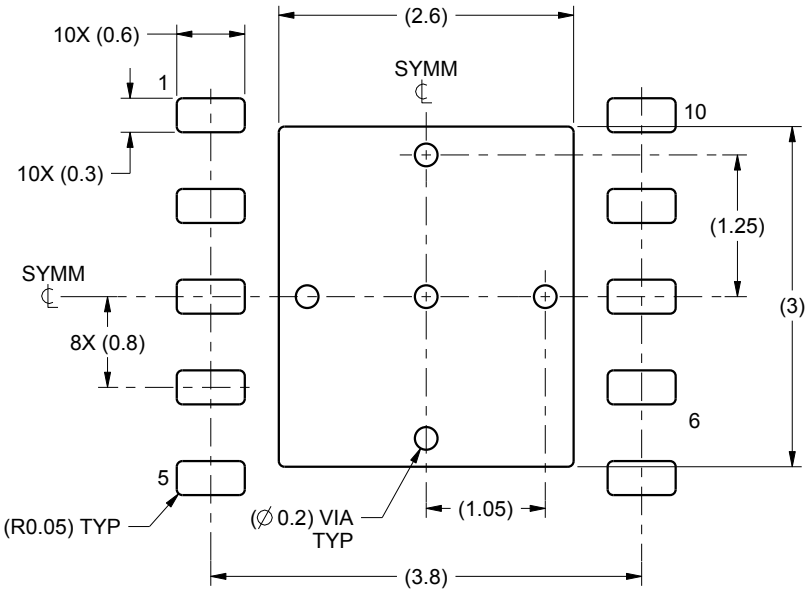
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

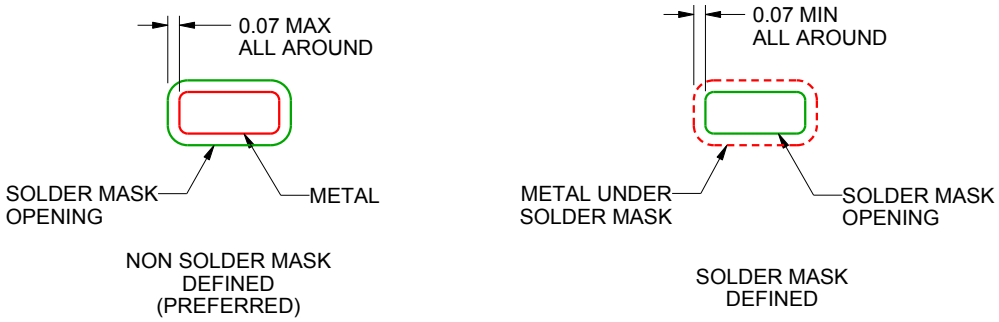


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

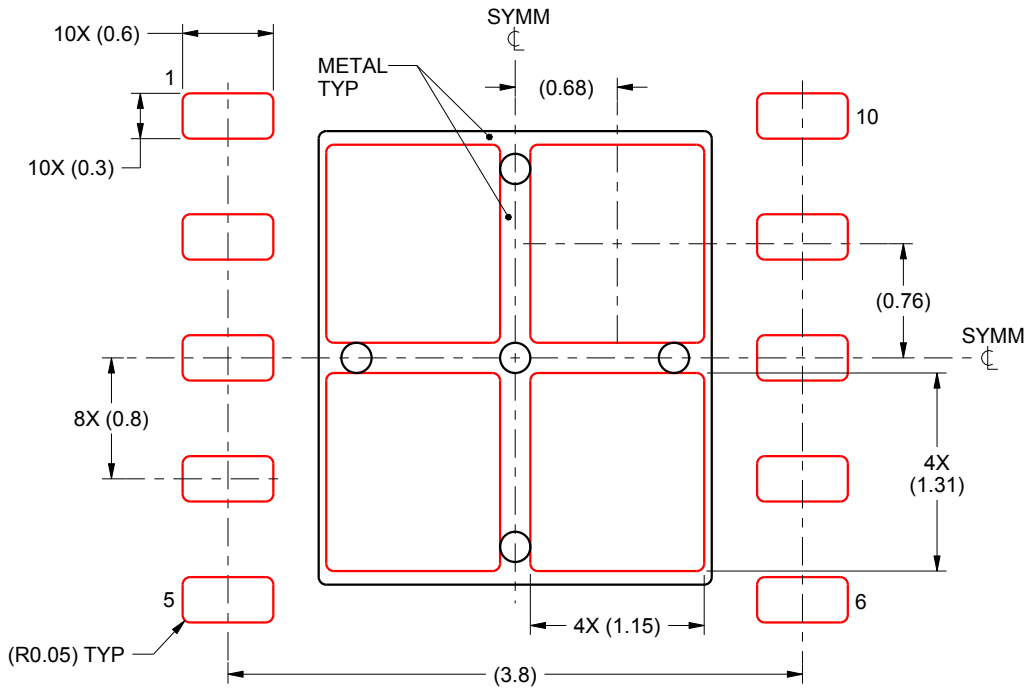


SOLDER MASK DETAILS

4222146/A 08/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4222146/A 08/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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