

# SN74LV1T02 单电源 2 输入正或非门 CMOS 逻辑电平转换器

## 1 特性

- $V_{CC}$  为 5V、3.3V、2.5V 和 1.8V 时单电源电压转换器
- 1.8V 至 5.5V 的工作电压范围
- 上行转换：
  - 1.8V  $V_{CC}$  时, 1.2V<sup>(1)</sup> 至 1.8V
  - 2.5V  $V_{CC}$  时, 1.5V<sup>(1)</sup> 至 2.5V
  - 3.3V  $V_{CC}$  时, 1.8V<sup>(1)</sup> 至 3.3V
  - 5.0V  $V_{CC}$  时, 3.3V 至 5.0V
- 下行转换：
  - 1.8V  $V_{CC}$  时, 3.3V 至 1.8V
  - 2.5V  $V_{CC}$  时, 3.3V 至 2.5V
  - 3.3V  $V_{CC}$  时, 5.0V 至 3.3V
- 逻辑输出以  $V_{CC}$  为基准
- 输出驱动：
  - 电压为 5V 时, 输出驱动为 8mA
  - 电压为 3.3V 时, 输出驱动为 7mA
  - 电压为 1.8V 时, 输出驱动为 3mA
- $V_{CC}$  为 3.3V 时, 特征频率高达 50MHz
- 输入引脚可耐受 5V 电压
- -40°C 至 125°C 工作温度范围
- 可采用无铅封装：SC-70 (DCK)

- 2mm x 2.1mm x 0.65mm (高度 1.1mm)

- 闩锁性能超过 250mA, 符合 JESD 17 规范
- 支持标准逻辑引脚排列
- 与 AUP1G 和 LVC1G 系列兼容的 CMOS 输出 B<sup>1</sup>

## 2 应用

- 电信
- 便携式应用
- 服务器
- PC 和笔记本电脑

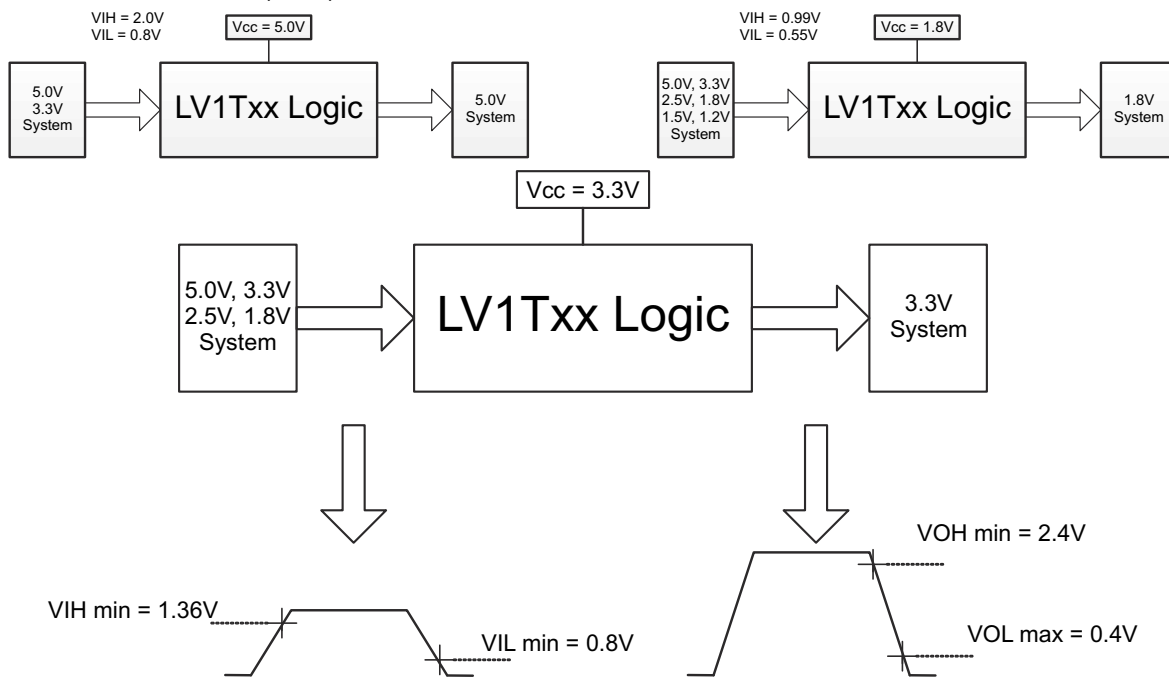
## 3 说明

SN74LV1T02 是一款具有较低输入阈值的单路 2 输入或非门, 可支持电压转换应用。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
SN74LV1T02	DBV (SOT-23-5)	2.90mm × 1.60mm
	DCK (SC70, 5)	2.00mm × 1.25mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



1.8V 至 3.3V 转换的开关阈值

<sup>1</sup> 请参考较低  $V_{CC}$  条件下的  $V_{IH}/V_{IL}$  和输出驱动。



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision A (February 2014) to Revision B (June 2022)</b>	<b>Page</b>
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Added ESD Ratings table, Thermal Information table, Typical Characteristics section, Pin Configuration and Functions section, Detailed Description section, Power Supply Recommendations section, Layout section, Receiving Notification of Documentation Updates section, and Community Resources section.....	5

<b>Changes from Revision * (December 2013) to Revision A (February 2014)</b>	<b>Page</b>
• 更新了文档格式.....	1
• Updated $V_{CC}$ values for $V_{IH}$ parameter in the Electrical Characteristics table.....	6

## 5 Related Products

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T04	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T17	DCK, DBV	Single Schmitt-Trigger Buffer Gate
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T34	DCK, DBV	Single Buffer Gate
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV1T126	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV4T125	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs

## 6 Pin Configuration and Functions

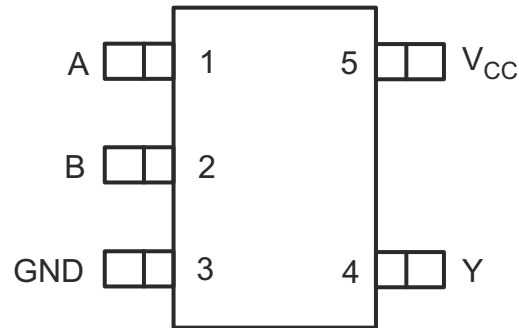


图 6-1. DCK or DBV Package, 5-Pin SC70 or SOT-23 (Top View)

表 6-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	G	Ground
Y	4	O	Output Y
V <sub>CC</sub>	5	P	Positive supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	- 0.5	7.0	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	- 0.5	7.0	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	- 0.5	4.6	V
	Voltage range applied to any output in the high or low state <sup>(2)</sup>	- 0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		- 20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current			±25 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	
		±2000	V
		Machine Model (MM), per JEDEC specification	
	±200		
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	
		±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	1.6	5.5	V	
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.8 V		-3	mA
		V <sub>CC</sub> = 2.5 V		-5	
		V <sub>CC</sub> = 3.3 V		-7	
		V <sub>CC</sub> = 5.0 V		-8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.8 V		3	mA
		V <sub>CC</sub> = 2.5 V		5	
		V <sub>CC</sub> = 3.3 V		7	
		V <sub>CC</sub> = 5.0 V		8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V		20	ns/V
		V <sub>CC</sub> = 3.3 V or 2.5 V		20	
		V <sub>CC</sub> = 5.0 V		20	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DBV	DCK	UNIT
		5 PINS	5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	206	252	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.8 V	0.94			1.0			V
		V <sub>CC</sub> = 2.0 V	1.02			1.03			
		V <sub>CC</sub> = 2.25 V to 2.5 V	1.135			1.18			
		V <sub>CC</sub> = 2.75 V	1.21			1.23			
		V <sub>CC</sub> = 3 V to 3.3 V	1.35			1.37			
		V <sub>CC</sub> = 3.6 V	1.47			1.48			
		V <sub>CC</sub> = 4.5 V to 5.0 V	2.02			2.03			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 2.0 V			0.58			0.55	V
		V <sub>CC</sub> = 2.25 V to 2.75 V			0.75			0.71	
		V <sub>CC</sub> = 3 V to 3.6 V			0.8			0.65	
		V <sub>CC</sub> = 4.5 V to 5.5 V			0.8			0.8	

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +125°C			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V <sub>OH</sub>	High-level output voltage	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1			V	
		1.65 V	1.28			1.21				
		1.8 V	1.5			1.45				
		2.3 V	2			1.93				
		2.5 V	2.25			2.15				
		3.0 V	2.78			2.7				
		3.0 V	2.6			2.49				
		3.3 V	2.9			2.8				
		4.5 V	4.2			4.1				
		4.5 V	4.1			3.95				
		5.0 V	4.6			4.5				
V <sub>OL</sub>	Low-level output voltage	1.65 V to 5.5 V	0.1			0.1			V	
		1.65 V	0.2			0.25				
		2.3 V	0.15			0.2				
		3.0 V	0.1			0.15				
		3.0 V	0.2			0.252				
		4.5 V	0.15			0.2				
		4.5 V	0.3			0.35				
I <sub>I</sub>	Input leakage current	A input; V <sub>I</sub> = 0 V or V <sub>CC</sub>	0 V, 1.8 V, 2.5 V, 3.3 V, 5.5 V			0.1			±1	μA
I <sub>CC</sub>	Static supply current	V <sub>I</sub> = 0 V or V <sub>CC</sub> , I <sub>O</sub> = 0; open on loading	5.0 V	1			10			μA
			3.3 V	1			10			
			2.5 V	1			10			
			1.8 V	1			10			
ΔI <sub>CC</sub>	Additional static supply current	One input at 0.3 V or 3.4 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	5.5 V			1.35			1.5	mA
		One input at 0.3 V or 1.1 V Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	1.8 V			10			10	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			2 10			2 10	pF
C <sub>o</sub>	Output capacitance	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			2.5			2.5	pF

## 7.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FREQUENCY (TYP)	V <sub>CC</sub>	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -65°C to 125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>pd</sub>	Any In	Y	DC to 50 MHz	5.0 V	15 pF	4	5	4	5	ns		
					30 pF	5.5	7.0	5.5	7.0			
				3.3 V	15 pF	4.8	5	5	5.5	ns		
					30 pF	5	5.5	5.5	6.5			
			DC to 25 MHz	2.5 V	15 pF	6	6.5	7	7.5	ns		
					30 pF	6.5	7.5	7.5	8.5			
				1.8 V	15 pF	10.5	11	11	12	ns		
					30 pF	12	13	12	14			

## 7.7 Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	f = 1 MHz and 10 MHz	1.8 V ± 0.15 V	14	pF
		2.5 V ± 0.2 V	14	
		3.3 V ± 0.3 V	14	
		5.5 V ± 0.5 V	14	

## 7.8 Typical Characteristics

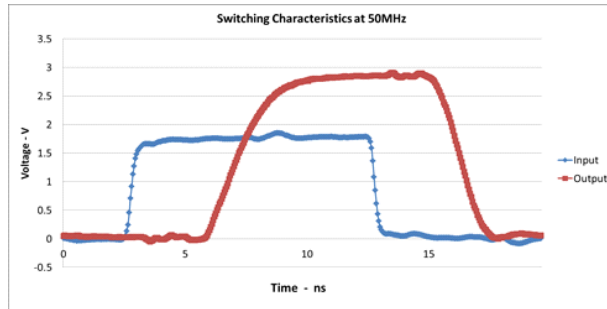


图 7-1. Excellent Signal Integrity  
(1.8 V to 3.3 V at 3.3-V V<sub>CC</sub>)

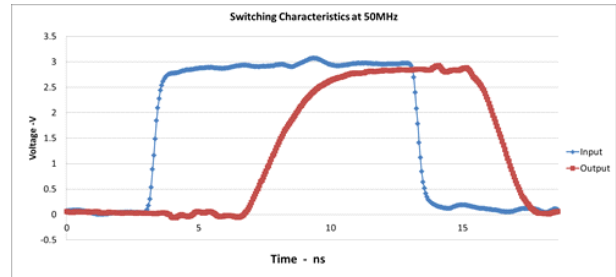


图 7-2. Excellent Signal Integrity  
(3.3 V to 3.3 V at 3.3-V V<sub>CC</sub>)

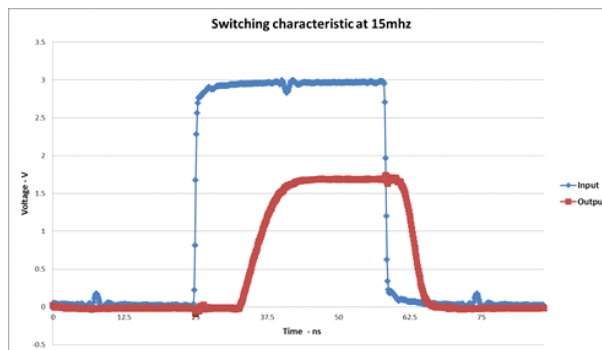
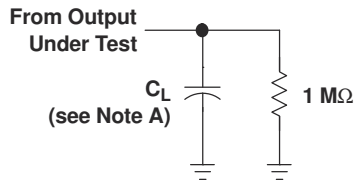


图 7-3. Excellent Signal Integrity  
(3.3 V to 1.8 V at 1.8-V V<sub>CC</sub>)

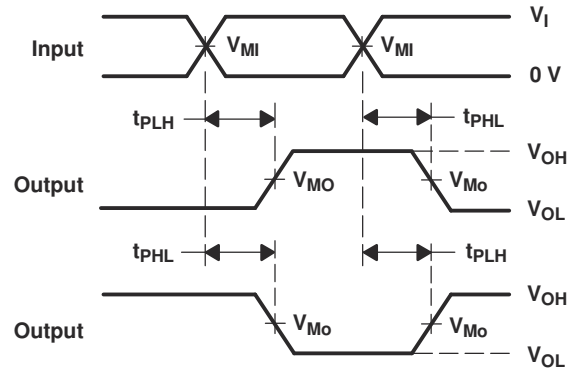


## 8 Parameter Measurement Information



LOAD CIRCUIT

	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_{MI}$	$V_I/2$	$V_I/2$
$V_{MO}$	$V_{CC}/2$	$V_{CC}/2$



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50\ \Omega$ , slew rate  $\geq 1$  V/ns.  
 C. The outputs are measured one at a time, with one transition per measurement.  
 D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

图 8-1. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

The SN74LV1T02 device is a low-voltage CMOS gate logic that operates at a wider voltage range for industrial, portable, telecom, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels. The input is designed with a lower threshold circuit to match 1.8 V input logic at  $V_{CC} = 3.3$  V and can be used in 1.8 V to 3.3 V level-up translation. In addition, the 5 V tolerant input pins enable down translation (that is, 3.3 V to 2.5 V output at  $V_{CC} = 2.5$  V). The wide  $V_{CC}$  range of 1.8 V to 5.5 V allows generation of desired output levels to connect to controllers or processors. The SN74LV1T02 device is designed with current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

### 9.2 Functional Block Diagram



图 9-1. Logic Diagram

### 9.3 Feature Description

#### 9.3.1 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as depicted in 图 9-2.

#### CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

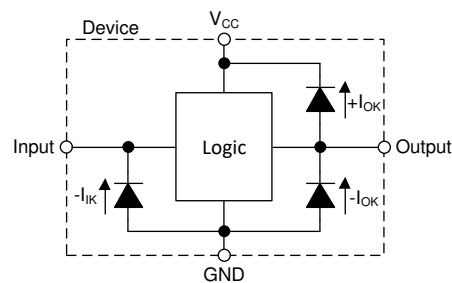


图 9-2. Electrical Placement of Clamping Diodes for Each Input and Output

#### 9.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 9.3.3 LVxT Enhanced Input Voltage

The SN74LV1T02 belongs to TI's LVxT family of Logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage ( $V_{CC}$ ), as described in the *Electrical Characteristics* table. To ensure proper functionality, input signals must remain at or below the specified  $V_{IH(MIN)}$  level for a HIGH input state, and at or below the specified  $V_{IL(MAX)}$  for a LOW input state. 图 9-3 shows the typical  $V_{IH}$  and  $V_{IL}$  levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-k $\Omega$  resistor is recommended and will typically meet all requirements.

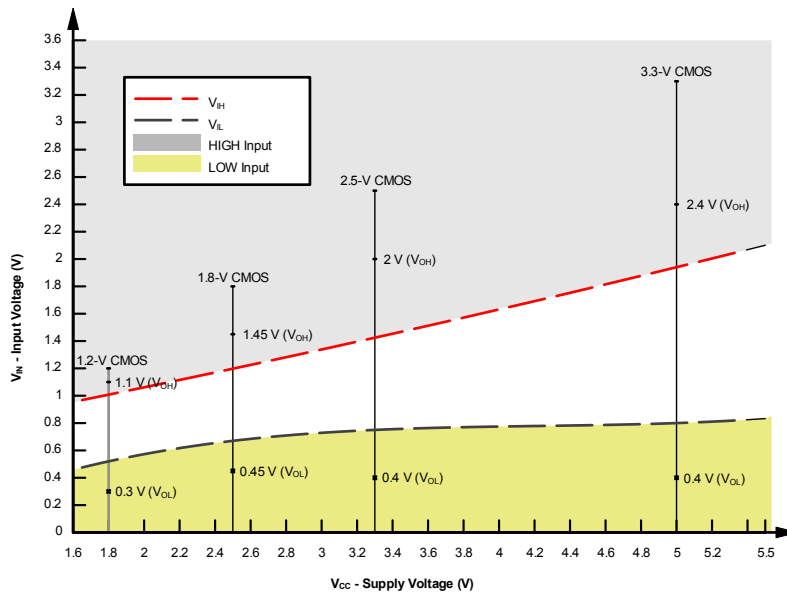


图 9-3. LVxT Input Voltage Levels

#### 9.3.3.1 Down Translation

Signals can be translated down using the SN74LV1T02. The voltage applied at the  $V_{CC}$  will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately  $V_{CC}$  in the HIGH state, and 0 V in the LOW state. Ensure that the input signals in the HIGH state are between  $V_{IH(MIN)}$  and 5.5 V, and input signals in the LOW state are lower than  $V_{IL(MAX)}$  as shown in 图 9-3.

For example, standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V  $V_{CC}$ . See 图 9-4.

**Down Translation Combinations:**

- 1.8-V  $V_{CC}$  – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V  $V_{CC}$  – Inputs from 3.3 V and 5.0 V
- 3.3-V  $V_{CC}$  – Inputs from 5.0 V

**9.3.3.2 Up Translation**

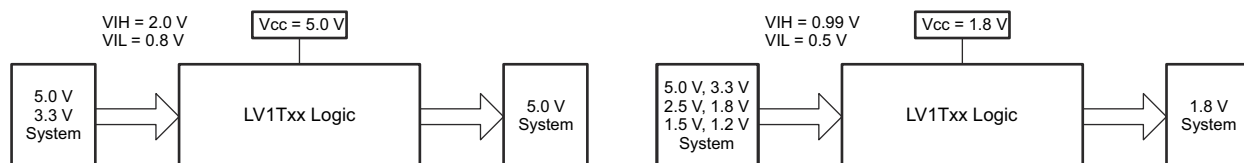
Input signals can be up translated using the SN74LV1T02. The voltage applied at  $V_{CC}$  will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately  $V_{CC}$  in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input high-state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a  $V_{IH(MIN)}$  of 3.5 V. For the SN74LV1T02,  $V_{IH(MIN)}$  with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

Ensure that the input signals in the HIGH state are above  $V_{IH(MIN)}$  and input signals in the LOW state are lower than  $V_{IL(MAX)}$  as shown in [图 9-4](#).

**Up Translation Combinations:**

- 1.8-V  $V_{CC}$  – Inputs from 1.2 V
- 2.5-V  $V_{CC}$  – Inputs from 1.8 V
- 3.3-V  $V_{CC}$  – Inputs from 1.8 V and 2.5 V
- 5.0-V  $V_{CC}$  – Inputs from 2.5 V and 3.3 V


**图 9-4. LVxT Up and Down Translation Example**
**9.4 Device Functional Modes**
**Function Table**

INPUT <sup>(1)</sup> (LOWER LEVEL INPUT)		OUTPUT <sup>(2)</sup> ( $V_{CC}$ CMOS)
A	B	Y
H	X	L
X	H	L
L	L	H
<b>SUPPLY <math>V_{CC} = 3.3 V</math></b>		
A	B	Y
$V_{IH(min)} = 1.35 V$ $V_{IL(max)} = 0.08 V$		$V_{OH(min)} = 2.9 V$ $V_{OL(max)} = 0.2 V$

- (1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance  
 (2) H = Driving High, L = Driving Low, Z = High Impedance State

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 12 Device and Documentation Support

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV1T02DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(NEB3, NEBJ, NEBS)	<a href="#">Samples</a>
SN74LV1T02DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NEB3	<a href="#">Samples</a>
SN74LV1T02DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(WB3, WBJ, WBS)	<a href="#">Samples</a>
SN74LV1T02DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		WB3	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

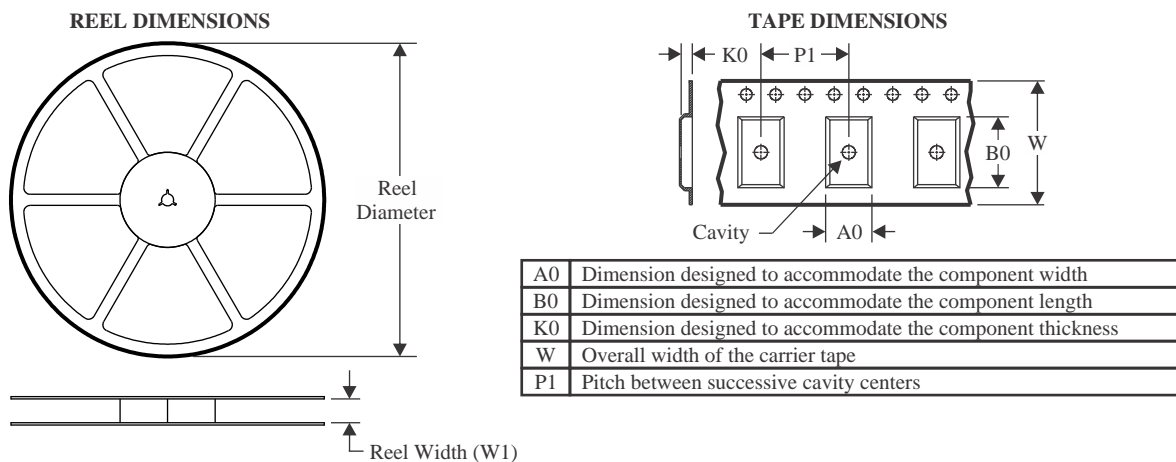
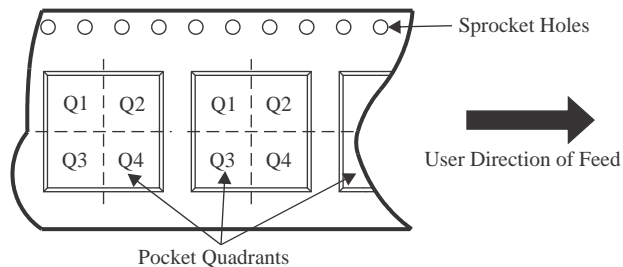
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV1T02DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LV1T02DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LV1T02DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LV1T02DBVRG4	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LV1T02DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LV1T02DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LV1T02DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LV1T02DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV1T02DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T02DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LV1T02DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T02DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T02DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LV1T02DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LV1T02DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LV1T02DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0

DCK (R-PDSO-G5)

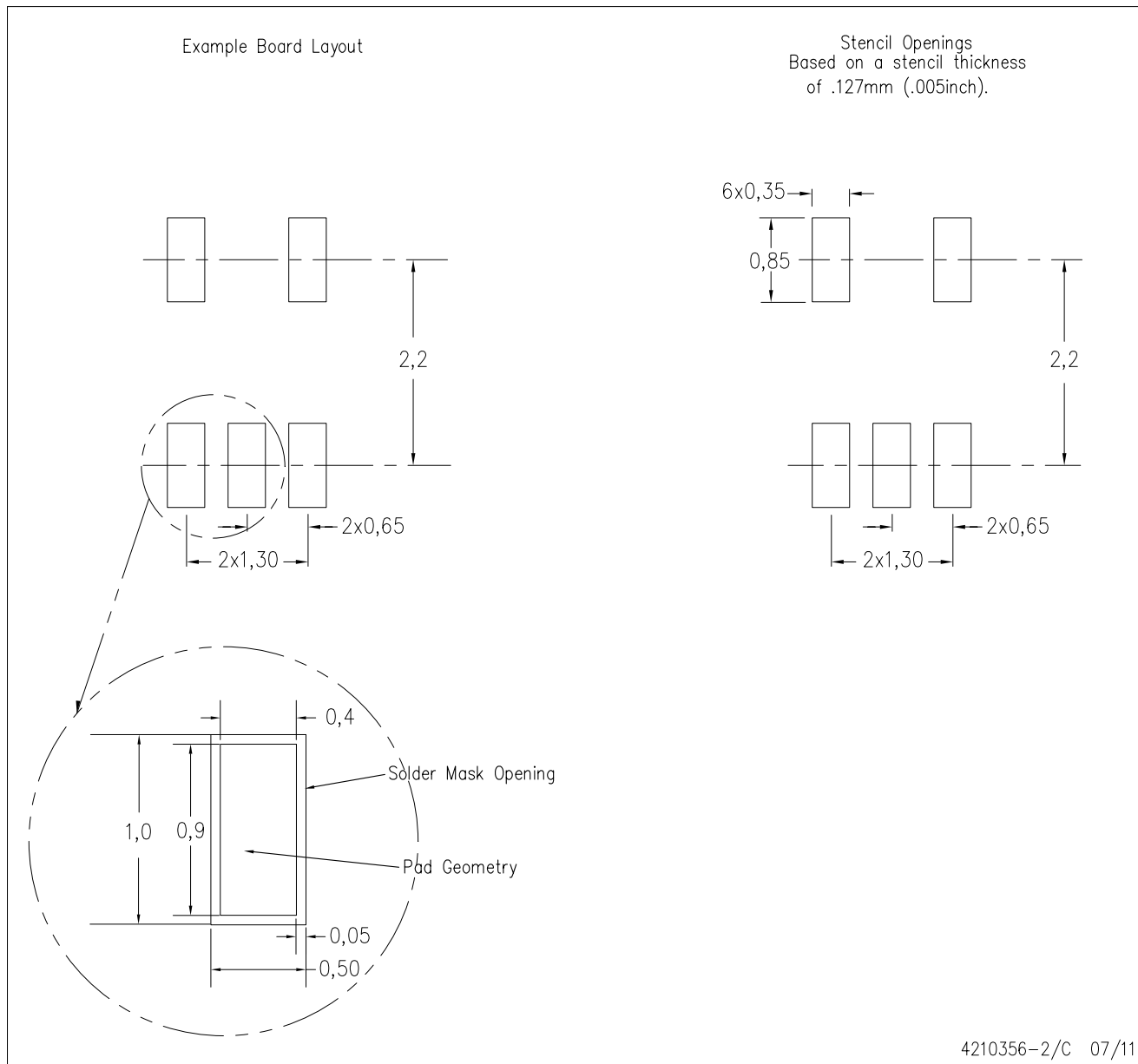
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

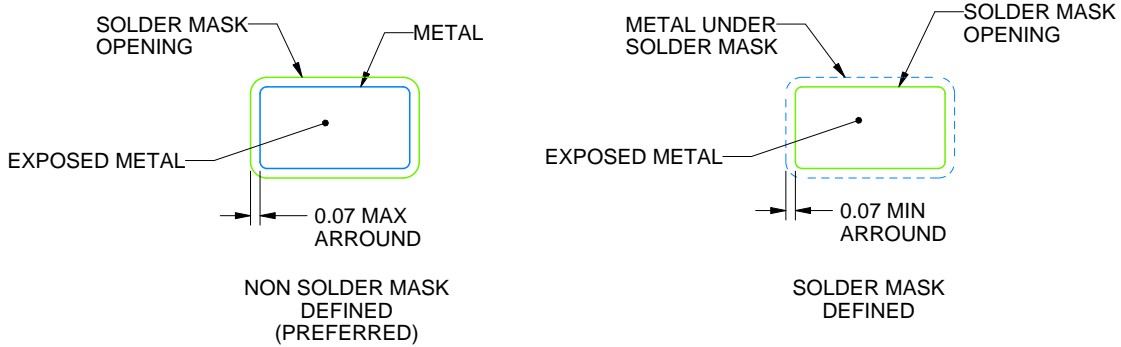
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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