DS90UR90xQ-Q1 5 至 65MHz 24 位彩色 FPD-Link II 串行器和解串器

1 特性

- 5 至 65MHz PCLK 支持（140Mbps 至 1.82Gbps）
- 交流耦合 STP 内部互联电缆长达 10 米
- 串行器和解串器上的集成终端
- @SPEED 链路 BIST 模式和报告引脚
- 可选 I^2C 兼容串行控制总线
- RGB888 + VS，HS，DE 支持
- 断电模式可最大程度地降低功率耗散
- 1.8V 或 3.3V 兼容 LVCMOS I/O 接口
- 汽车级产品：符合 AEC-Q100 2 级要求
- > 8kV 的 HBM 和 ISO 10605 ESD 额定值
- 向后兼容模式，用于与老一代器件一起运行
- 串行器 - **DS90UR905Q-Q1**
  - RGB888 + VS/HS/DE 串行化为 1 对 FPD-Link II
  - 随机发生器/扰频器 - 直流平衡数据流
  - 可选输出 VOD 和可调节去加重功能
- 解串器 - **DS90UR906Q-Q1**
  - FAST 随机数据锁定；无需参考时钟
  - 可调节输入接收器均衡
  - LOCK（实时链路状态）报告引脚
  - 输出并行总线的 EMI 最小化 (SSCG)
  - 输出压摆控制 (OS)

2 应用

- 汽车导航显示屏
- 汽车娱乐显示屏

3 说明

DS90UR90xQ-Q1 芯片组将并行 RGB 视频接口转换为单对高速串行化接口。该串行总线方案通过消除时钟和数据间的偏差，减少连接器引脚数量，减小互连线路的尺寸、重量和成本以及简化印刷电路板 (PCB) 总体布局布线等方式简化系统设计。此外，内部 DC 均衡解码用于支持 AC 耦合互连。

DS90UR905Q-Q1 串行器内嵌时钟，可均衡数据有效载荷并将信号电平转换为高速低压差分信令。多达 24 个输入连同 3 个视频控制信号被共同串行化。此器件支持全
24 位颜色或 18 位颜色和 6 个通用信号（例如，音频 I2S 应用）。

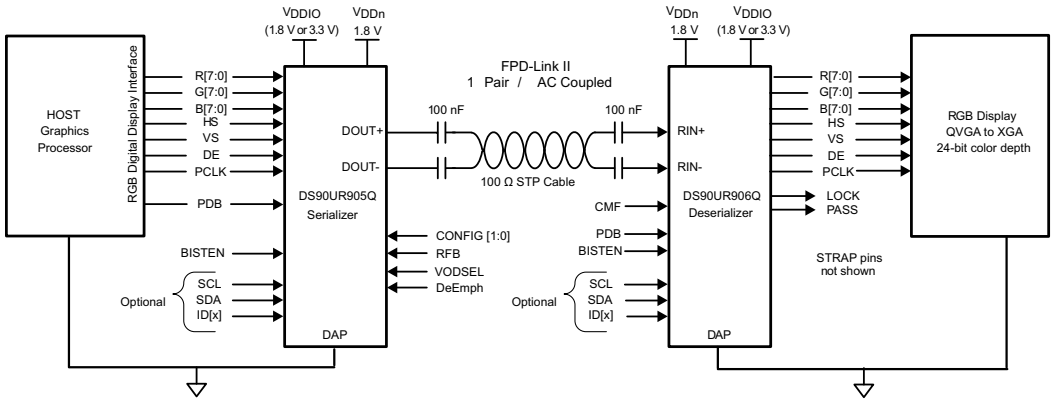
DS90UR906Q-Q1 解串器可恢复数据 (RGB) 和控制信号，并从串行数据流中提取时钟。DS90UR906Q-Q1 能够锁定传入数据流，无需使用训练序列或特殊的 SYNC（同步）模式，也不需要基准时钟。链路状态 (LOCK) 输出信号也由该芯片组提供。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DS90UR905Q-Q1	WQFN (48)	7.00mm x 7.00mm
DS90UR906Q-Q1	WQFN (60)	9.00mm x 9.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

703A I2C



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision H (July 2015) to Revision I — **Page**

- Fixed typo in power down supply current units - changed mA to uA ... 12

Changes from Revision G (April 2013) to Revision H — **Page**

- 添加了 *ESD 额定值*表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1

Changes from Revision F (January 2011) to Revision G — **Page**

- 已将美国国家半导体数据表的版面布局更改为 TI 格式 ... 1

Changes from Revision E (August 2010) to Revision F — **Page**

- Modified ESD to include IEC condition (330 Ohm, 150pF) ... 10
- Updated deserializer parameters: IDD1, IDDZ, IDDIOZ, IDDR, VOH, VOL, tROS, tRDC ... 11
- Updated Figure 14 and Figure 15 to reflect data measurement at VDDIO/2 ... 20
- Updated Figure 38 – C13 changed to 4.7uF ... 44

Changes from Revision D (May 2010) to Revision E — **Page**

- 删除了“数据随机生成和扰频”、“噪声裕度”以及“典型性能曲线”部分 ... 1
- 修改了订购信息，在 NSPN 列（替代 NSID 列）中添加了 NOPB 标识 ... 1
- Corrected *ESD Ratings* to IEC 61000 – 4 – 2 from ISO 10605 (duplication). ... 10

- Added RPU = 10k Ω condition for the *Serial Control Bus Characteristics* of tR and tF. 14

Changes from Revision C (March 2010) to Revision D **Page**

- DS90UR906Q-Q1 data sheet limits have been updated per characterization results 11
- Corrected register 5 from RFB to VODSEL and register 4 from VODSEL to RFB in Table 14 39

Changes from Revision B (Feburary 2010) to Revision C **Page**

- Added reference to soldering profile..... 10
- Added ESD CDM and ESD MM values..... 10
- Updated $R_{\theta A}$ value 11

Changes from Revision A (September 2009) to Revision B **Page**

- 删除了 IDDT3 和 IDDIOT3（随机模式），原因是其限制与检测板模式相同 1
- DS90UR905Q 数据表限制已根据特性结果更新为最终限制 1
- Updated DS90UR905Q-Q1 Typical Connection Diagram — Pin Control. Ref 30102044 5
- Updated DS90UR906Q-Q1 Pin Diagram: strap changes on pin11, pin14, and pin42 7
- Added strap to pin 11 “ OS_PCLK ” (Output Slew_PCLK) 7
- Changed strap pin 14 feature from “ RDS ” to “ OS_DATA ” (Output Slew_DATA) 7
- Added strap to pin 42 “ OP_LOW ” (Output LOW) 8
- Updated DS90UR906Q-Q1 Typical Connection Diagram — Pin Control. Ref 30102045 8
- Updated DS90UR906Q-Q1 Deserializer Pin Descriptions: RDS feature changed to OS_PCLK and OS_DATA. Added OP_LOW feature 8
- Created OP_LOW timing Figure 28. Ref 30102065 31
- Created OP_LOW timing Figure 29. Ref 30102066 32
- Updated Table 12: deleted ID[x] Address 7'b 110 1000 (h'68) (8'b 1101 0000 (h'D0)) 38
- Updated Table 13: deleted ID[x] Address 7'b 111 0000 (h'70) (8'b 1110 0000 (h'E0)) 39
- Changed Table 14 ADD \ 1 \ bit \ 6:0 \ ID[x]: deleted Device ID 7b'1101 00 (h'68). Only four (4) IDs will be available..... 39
- Changed Table 15: ADD \ 0 \ bit \ 6 \ OSS_SEL: “ OSS_SEL ” changed feature to “ OS_PCLK ” (Output Slew_PCLK). OSS_SEL moved to ADD \ 2 \ bit \ 6 \..... 40
- Changed Table 15: ADD \ 0 \ bit \ 5 \ RDS: changed “ RDS ” feature to OS_DATA (Output Slew_DATA) 40
- Changed Table 15: ADD \ 1\ bit \ 6:0 \ ID[x]: deleted Device ID 7b'1110 00 (h'70). Only four (4) IDs will be available. 40
- Changed Table 15: ADD \ 2 \ bit \ 7 \ Reserved: changed “ Reserved ” to “ OP_LOW ”..... 40
- Changed Table 15: ADD \ 2 \ bit \ 6 \ Reserved: changed “ Reserved ” to “ OSS_SEL ”..... 40

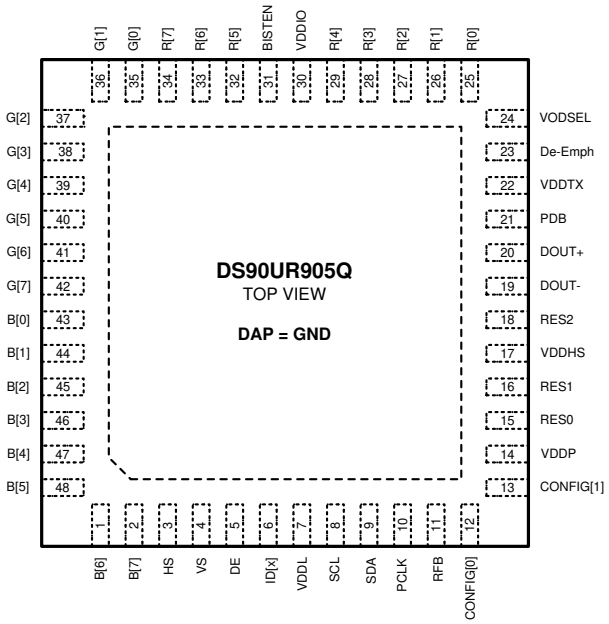
5 说明 （续）

串行传输通过用户可选择的去加重功能、差分输出电平选择 特性和接收器均衡实现优化。通过使用低压差分信令、接收器驱动强度控制和展频计时兼容性最大限度地减少了电磁干扰 (EMI)。解串器可配置为在其并行输出中生成展频时钟和数据。

DS90UR905Q-Q1 串行器采用 48 引脚超薄型四方扁平无引线封装 (WQFN) 封装，而 DS90UR906Q-Q1 解串器采用 60 引脚 WQFN 封装。两种器件可在 -40˚C 至 +105˚C 的汽车级 AEC-Q100 2 级温度范围内额定运行。

6 Pin Configuration and Functions

RHS Package
48-Pin WQFN
Top View



DS90UR905Q-Q1 Serializer Pin Functions(1)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
B[7:0]	2, 1, 48, 47, 46, 45, 44, 43	I, LVCMOS with pulldown	BLUE parallel interface data input pins (MSB = 7, LSB = 0)
DE	5	I, LVCMOS with pulldown	Data enable input Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the control signal filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the control signal filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
G[7:0]	42, 41, 40, 39, 38, 37, 36, 35	I, LVCMOS with pulldown	GREEN parallel interface data input pins (MSB = 7, LSB = 0)
HS	3	I, LVCMOS with pulldown	Horizontal Sync Input Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the control signal filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the control signal filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
PCLK	10	I, LVCMOS with pulldown	Pixel clock input Latch edge set by RFB function.
R[7:0]	34, 33, 32, 29, 28, 27, 26, 25	I, LVCMOS with pulldown	RED parallel interface data input pins (MSB = 7, LSB = 0)
VS	4	I, LVCMOS with pulldown	Vertical sync input Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.

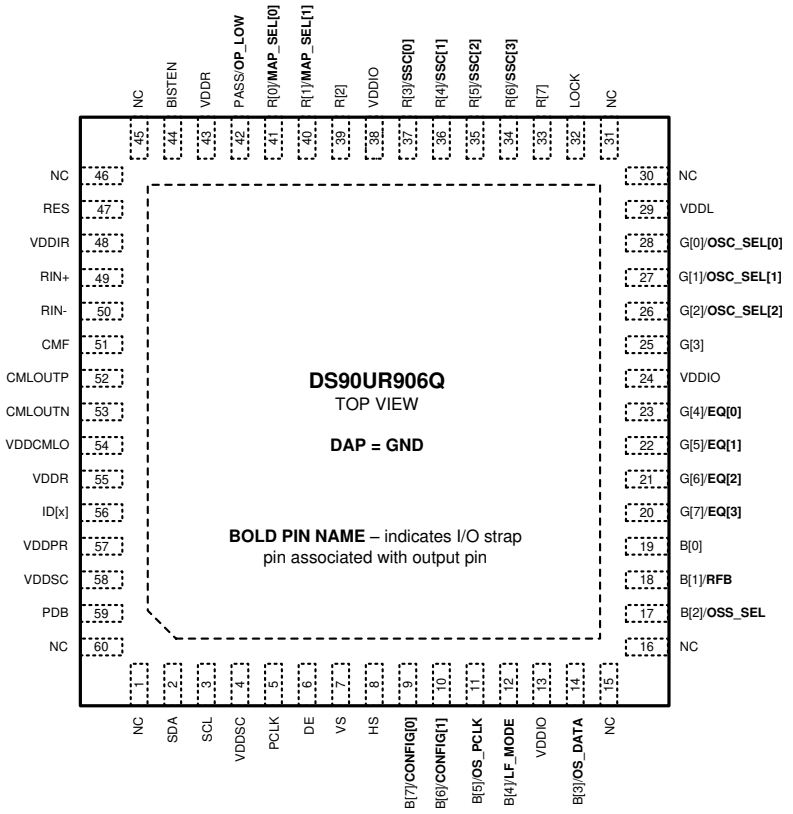
(1) 1 = HIGH, 0 = LOW

DS90UR905Q-Q1 Serializer Pin Functions(1) (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
CONTROL AND CONFIGURATION			
BISTEN	31	I, LVCMOS with pulldown	BIST mode — optional BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
CONFIG[1:0]	13, 12	I, LVCMOS with pulldown	Operating modes — pin or register control Determine the operating mode of the DS90UR905 and interfacing device. CONFIG[1:0] = 00: interfacing to DS90UR906Q-Q1, control signal filter DISABLED CONFIG[1:0] = 01: interfacing to DS90UR906Q-Q1, control signal filter ENABLED CONFIG[1:0] = 10: interfacing to DS90UR124, DS99R124 CONFIG[1:0] = 11: interfacing to DS90C124
De-Emph	23	I, Analog with pullup	De-emphasis control — pin or register control De-emph = open (float) - disabled To enable de-emphasis, tie a resistor from this pin to GND or control via register (see Table 2).
ID[x]	6	I, Analog	Serial control bus device ID address select — optional Resistor-to-ground and 10-kΩ pullup to 1.8-V rail (see Table 11).
PDB	21	I, LVCMOS with pulldown	Power-down mode input PDB = 1, serializer is enabled (normal operation). Refer to *Power Up Requirements and PDB Pin*. PDB = 0, serializer is powered down When the serializer is in the power-down state, the driver outputs (DOUT±) are both logic high, the PLL is shutdown, IDD is minimized. Control registers are RESET.
RES[2:0]	18, 16, 15	I, LVCMOS with pulldown	***Reserved*** - tie LOW
RFB	11	I, LVCMOS with pulldown	Pixel clock input latch edge select — pin or register control RFB = 1, parallel interface data and control signals are latched on the rising clock edge. RFB = 0, parallel interface data and control signals are latched on the falling clock edge.
SCL	8	I, LVCMOS	Serial control bus clock input - optional SCL requires an external pullup resistor to V_{DDIO}.
SDA	9	I/O, LVCMOS Open-Drain	Serial control bus data input/output - optional SDA requires an external pullup resistor V_{DDIO}.
VODSEL	24	I, LVCMOS with pulldown	Differential driver output voltage select — pin or register control VODSEL = 1, LVDS VOD is ±420 mV, 840 mVp-p (typical) — long cable / de-emp applications VODSEL = 0, LVDS VOD is 280 mV, 560 mVp-p (typical)
FPD-LINK II SERIAL INTERFACE			
DOUT+	20	O, LVDS	True output The output must be AC-coupled with a 100-nF capacitor.
DOUT-	19	O, LVDS	Inverting output The output must be AC-coupled with a 100-nF capacitor.
POWER AND GROUND(2)			
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 9 vias.
VDDHS	17	Power	TX high-speed logic power, 1.8 V ±5%
VDDL	7	Power	Logic power, 1.8 V ±5%
VDDP	14	Power	PLL power, 1.8 V ±5%
VDDIO	30	Power	LVCMOS I/O power, 1.8 V ±5% or 3.3 V ±10%
VDDTX	22	Power	Output Driver power, 1.8 V ±5%

(2) The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms, then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

NKB Package
60-Pin WQFN
Top View



DS90UR906Q-Q1 Deserializer Pin Functions (1)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
B[7:0]	9, 10, 11, 12, 14, 17, 18, 19	I, STRAP, O, LVCMOS	BLUE parallel interface data output pins (MSB = 7, LSB = 0) In power-down (PDB = 0), outputs are controlled by the OSS_SEL (see Table 6). These pins are inputs during power up (see *Deserializer Strap Input Pins*).
DE	6	O, LVCMOS	Data enable output In power down (PDB = 0), output is controlled by the OSS_SEL pin (see Table 6). Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the control signal filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the control signal filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
G[7:0]	20, 21, 22, 23, 25, 26, 27, 28	I, STRAP, O, LVCMOS	GREEN parallel interface data output pins (MSB = 7, LSB = 0) In power down (PDB = 0), outputs are controlled by the OSS_SEL (see Table 6). These pins are inputs during power up (see *Deserializer Strap Input Pins*).
HS	8	O, LVCMOS	Horizontal sync output In power down (PDB = 0), output is controlled by the OSS_SEL pin (see Table 6). Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the control signal filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the control signal filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.

(1) 1 = HIGH, 0 = LOW

DS90UR906Q-Q1 Deserializer Pin Functions(1) (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
LOCK	32	O, LVCMOS	LOCK status output LOCK = 1, PLL is Locked, outputs are active LOCK = 0, PLL is unlocked, RGB[7:0], HS, VS, DE and PCLK output states are controlled by OSS_SEL (see Table 6). May be used as link status or to flag when video data is active (ON/OFF).
PASS	42	O, LVCMOS	PASS output (BIST mode) PASS = 1, error free transmission PASS = 0, one or more errors were detected in the received payload Route to test point for monitoring, or leave open if unused.
PCLK	5	O, LVCMOS	Pixel clock output In power down (PDB = 0), output is controlled by the OSS_SEL pin (see Table 6). Strobe edge set by RFB function.
R[7:0]	33, 34, 35, 36, 37, 39, 40, 41	I, STRAP, O, LVCMOS	RED parallel interface data output pins (MSB = 7, LSB = 0) In power down (PDB = 0), outputs are controlled by the OSS_SEL (see Table 6). These pins are inputs during power up (see *Deserializer Strap Input Pins*).
VS	7	O, LVCMOS	Vertical sync output In power down (PDB = 0), output is controlled by the OSS_SEL pin (see Table 6). Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
CONTROL AND CONFIGURATION — STRAP PINS For a HIGH state, use a 10-kΩ pullup to V_{DDIO}; for a LOW state, the IO includes an internal pulldown. The STRAP pins are read upon power up and set device configuration. Pin Number listed along with shared RGB output name in square brackets.			
CONFIG[1:0]	10 [B6], 9 [B7]	STRAP I, LVCMOS with pulldown	Operating modes — pin or register control These pins determine the operating mode of the DS90UR906 and interfacing device. CONFIG[1:0] = 00: interfacing to DS90UR905Q-Q1, control signal filter DISABLED CONFIG[1:0] = 01: interfacing to DS90UR905Q-Q1, control signal filter ENABLED CONFIG[1:0] = 10: interfacing to DS90UR241 CONFIG[1:0] = 11: interfacing to DS90C241
EQ[3:0]	20 [G7], 21 [G6], 22 [G5], 23 [G4]	STRAP I, LVCMOS with pulldown	Receiver input equalization — pin or register control (see Table 3).
LF_MODE	12 [B4]	STRAP I, LVCMOS with pulldown	SSCG low-frequency mode — pin or register control Only required when SSCG is enabled, otherwise LF_MODE condition is a DON'T CARE (X). LF_MODE = 1, SSCG in low-frequency mode (PCLK = 5 to 20 MHz) LF_MODE = 0, SSCG in high-frequency mode (PCLK = 20 to 65 MHz)
MAP_SEL[1:0]	40 [R1], 41 [R0]	STRAP I, LVCMOS with pulldown	Bit mapping backward compatibility / DS90UR241 options — pin or register control Normal setting to b'00 (see Table 9).
OP_LOW	42 PASS	STRAP I, LVCMOS with pulldown	Outputs held LOW when LOCK = 1 — pin or register control See (2) OP_LOW = 1: all outputs are held LOW during power up until released by programming OP_LOW release / set register HIGH See (3) See Figure 30 and Figure 31. OP_LOW = 0: all outputs toggle normally as soon as LOCK goes HIGH (default).
OS_DATA	14 [B3]	STRAP I, LVCMOS with pulldown	Data output slew select — pin or register control OS_DATA = 1, increased DATA slew OS_DATA = 0, normal (default)
OSC_SEL[2:0]	26 [G2], 27 [G1], 28 [G0]	STRAP I, LVCMOS with pulldown	Oscillator select — pin or register control (see Table 7 and Table 8).
OS_PCLK	11 [B5]	STRAP I, LVCMOS with pulldown	PCLK output slew select — pin or register control OS_PCLK = 1, increased PCLK slew OS_PCLK = 0, normal (default)
OSS_SEL	17 [B2]	STRAP I, LVCMOS with pulldown	Output sleep state select — pin or register control See (4) OSS_SEL is used in conjunction with PDB to determine the state of the outputs in power down (Sleep) (see Table 6).

(2) It is not recommended to use any other strap options with this strap function
(3) Before the device is powered up, the outputs are in tri-state.
(4) OSS_SEL strap cannot be used if OP_LOW =1

DS90UR906Q-Q1 Deserializer Pin Functions(1) (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
RFB	18 [B1]	STRAP I, LVCMOS with pulldown	Pixel clock output strobe edge select — pin or register control RFB = 1, parallel interface data and control signals are strobed on the rising clock edge. RFB = 0, parallel interface data and control signals are strobed on the falling clock edge.
SSC[3:0]	34 [R6], 35 [R5], 36 [R4], 37 R[3]	STRAP I, LVCMOS with pulldown	Spread spectrum clock generation (SSCG) range select — pin or register control See Table 4 and Table 5.
CONTROL AND CONFIGURATION			
BISTEN	44	I, LVCMOS with pulldown	BIST enable input — optional BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
ID[x]	56	I, Analog	Serial control bus device ID address select — optional Resistor-to-ground and 10-kΩ pullup to 1.8-V rail (see Table 10).
NC	1, 15, 16, 30, 31, 45, 46, 60	—	Not connected Leave pin open (float)
PDB	59	I, LVCMOS with pulldown	Power-down mode input PDB = 1, deserializer is enabled (normal operation). Refer to *Power Up Requirements and PDB Pin*. PDB = 0, deserializer is in power down. When the deserializer is in the power-down state, the LVCMOS output state is determined by Table 6. Control Registers are RESET.
RES	47	I, LVCMOS with pulldown	***Reserved*** - tie LOW
SCL	3	I, LVCMOS	Serial control bus clock input — optional SCL requires an external pullup resistor to V_{DDIO}.
SDA	2	I/O, LVCMOS Open-Drain	Serial control bus data input/output — optional SDA requires an external pullup resistor to V_{DDIO}.
FPD-LINK II SERIAL INTERFACE			
CMF	51	I, Analog	Common-mode filter VCM center-tap is a virtual ground which may be AC coupled to ground to increase receiver common-mode noise immunity. Recommended value is 0.1 μF or higher.
CMLOUTN	53	O, LVDS	Test monitor pin — EQ waveform NC or connect to test point. Requires serial bus control to enable.
CMLOUTP	52	O, LVDS	Test monitor pin — EQ waveform NC or connect to test point. Requires serial bus control to enable.
RIN+	49	I, LVDS	True input. The input must be AC coupled with a 100-nF capacitor.
RIN-	50	I, LVDS	Inverting input. The input must be AC coupled with a 100-nF capacitor.
POWER AND GROUND(5)			
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 9 vias.
VDDCMLO	54	Power	RX high-speed logic power, 1.8 V ±5%
VDDL	29	Power	Logic power, 1.8 V ±5%
VDDIO	13, 24, 38	Power	LVCMOS I/O power, 1.8 V ±5% or 3.3 V ±10% (V_{DDIO})
VDDIR	48	Power	Input power, 1.8 V ±5%
VDDPR	57	Power	PLL power, 1.8 V ±5%
VDDR	43, 55	Power	RX high-speed logic power, 1.8 V ±5%
VDDSC	4, 58	Power	SSCG power, 1.8 V ±5%

(5) The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms, then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3).

		MIN	MAX	UNIT
Supply voltage – V_{DDn} (1.8 V)		–0.3	2.5	V
Supply voltage – V_{DDIO}		–0.3	4	V
LVCMOS I/O voltage		–0.3	VDDIO + 0.3	V
Receiver input voltage		–0.3	VDD + 0.3	V
Driver output voltage		–0.3	VDD + 0.3	V
Junction temperature			150	°C
48L RHS package	Maximum power dissipation capacity at 25°C		215	mW
	Derate above 25°C		$1/\theta_{JA}$	mW/°C
60L NKB package	Maximum power dissipation capacity at 25°C		470	mW
	Derate above 25°C		$1/\theta_{JA}$	mW/°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office or Distributors for availability and specifications.
(3) For soldering specifications see product folder at www.ti.com and SNOA549.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±8000	V
	Charged-device model (CDM), per AEC Q100-011		±1000	
	Machine Model (MM)		±250	
	ISO10605(2)	Air Discharge (D_{OUT+}, D_{OUT-})	≥±30000	
		Contact Discharge (D_{OUT+}, D_{OUT-})	≥±10000	
		Air Discharge (R_{IN+}, R_{IN-})	≥±30000	
		Contact Discharge (R_{IN+}, R_{IN-})	≥±10000	
	ISO10605(3)	Air Discharge (D_{OUT+}, D_{OUT-})	≥±15000	
		Contact Discharge (D_{OUT+}, D_{OUT-})	≥±10000	
		Air Discharge (R_{IN+}, R_{IN-})	≥±15000	
		Contact Discharge (R_{IN+}, R_{IN-})	≥±10000	
	IEC 61000-4-2(3)	Air Discharge (D_{OUT+}, D_{OUT-})	≥±25000	
		Contact Discharge (D_{OUT+}, D_{OUT-})	≥±8000	
		Air Discharge (R_{IN+}, R_{IN-})	≥±25000	
		Contact Discharge (R_{IN+}, R_{IN-})	≥±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) R_D = 2 kΩ, C_S = 150 pF or R_D = 2 kΩ, C_S = 330 pF or R_D = 330 Ω, C_S = 150 pF
(3) R_D = 330 Ω, C_S = 330 pF

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS supply voltage (V_{DDIO})	1.71	1.8	1.89	V
OR LVCMOS supply voltage (V_{DDIO})	3	3.3	3.6	
Operating free-air temperature (T_A)	−40	25	105	°C
PCLK clock frequency	5		65	MHz
Supply noise(1)			50	mV_{P-P}

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8-V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency on the serializer is less than 750 kHz. The deserializer on the other hand shows no error when the noise frequency is less than 400 kHz.

7.4 Thermal Information

THERMAL METRIC(1)		DS90UR905Q-Q1 RHS (WQFN) 48 PINS	DS90UR906Q-Q1 NKB (WQFN) 60 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	30.3	26.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(2)	11.5	9.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	6.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.3	6.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Based on nine thermal vias.

7.5 Serializer DC Electrical Characteristics

over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS		PIN / FREQ	MIN	TYP	MAX	UNIT
LVCMOS INPUT DC SPECIFICATIONS								
V_{IH}	High-level input voltage	V_{DDIO} = 3.0 to 3.6 V		R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, PDB, VODSEL, RFB, CONFIG[1:0],BISTEN	2.2		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89 V			0.65 × V_{DDIO}		V_{DDIO}	V
V_{IL}	Low-level input voltage	V_{DDIO} = 3.0 to 3.6 V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89 V			GND		0.35 × V_{DDIO}	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6 V		–15	±1	+15	µA
			V_{DDIO} = 1.7 to 1.89 V		–15	±1	+15	µA

(1) The Electrical Characteristics tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Serializer DC Electrical Characteristics (continued)

over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS		PIN / FREQ	MIN	TYP	MAX	UNIT
LVDS DRIVER DC SPECIFICATIONS								
V_{OD}	Differential output voltage	R_L = 100 Ω, De-emph = disabled, Figure 2	VODSEL = 0	DOUT+, DOUT–	±205	±280	±355	mV
			VODSEL = 1		±320	±420	±520	
V_{ODp-p}	Differential output voltage (DOUT+) – (DOUT-)		VODSEL = 0	DOUT+, DOUT–		560		mVp-p
			VODSEL = 1			840		
ΔV_{OD}	Output voltage unbalance	R_L = 100 Ω, De-emph = disabled, VODSEL = L		DOUT+, DOUT–		1	50	mV
V_{OS}	Offset voltage – single-ended at TP A and B, Figure 1	R_L = 100 Ω, De-emph = disabled	VODSEL = 0	DOUT+, DOUT–		1.65		V
			VODSEL = 1			1.575		
ΔV_{OS}	Offset voltage unbalance Single-ended at TP A and B, Figure 1	R_L = 100 Ω, De-emph = disabled		DOUT+, DOUT–		1		mV
I_{OS}	Output short circuit current	DOUT± = 0 V, De-emph = disabled	VODSEL = 0			–36		mA
R_T	Internal termination resistor				80	100	120	Ω
SUPPLY CURRENT								
I_{DDT1}	Serializer supply current (includes load current) R_L = 100 Ω, f = 65 MHz	Checker Board Pattern, De-emph = 3 KΩ VODSEL = H, Figure 9	V_{DD} = 1.89 V	All V_{DD} pins		75	85	mA
			V_{DDIO} = 1.89 V	V_{DDIO}		3	5	
I_{DDIOT1}			V_{DDIO} = 3.6 V			11	15	
I_{DDT2}		Checker Board Pattern, De-emph = 6 KΩ, VODSEL = L, Figure 9	V_{DD} = 1.89 V	All V_{DD} pins		65	75	mA
			V_{DDIO} = 1.89 V	V_{DDIO}		3	5	
I_{DDIOT2}			V_{DDIO} = 3.6 V			11	15	
I_{DDZ}	Serializer cupply current power down	PDB = 0 V , (All other LVCMOS Inputs = 0 V)	V_{DD} = 1.89 V	All V_{DD} pins		40	1000	µA
			V_{DDIO} = 1.89 V	V_{DDIO}		5	10	
I_{DDIOZ}			V_{DDIO} = 3.6 V			10	20	

7.6 Deserializer DC Electrical Characteristics

over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN / FREQ	MIN	TYP	MAX	UNIT
3.3 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 3.0 to 3.6 V							
V_{IH}	High-level input voltage		PDB, BISTEN	2.2		V_{DDIO}	V
V_{IL}	Low-level input voltage			GND		0.8	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO}		−15	±1	15	µA
V_{OH}	High-level output voltage	I_{OH} = −2 mA, OS_PCLK/DATA = L	R[7:0], G[7:0], B[7:0], HS,VS, DE, PCLK, LOCK, PASS	2.4	V_{DDIO}		V
V_{OL}	Low-level output voltage	I_{OL} = +2 mA, OS_PCLK/DATA = L	R[7:0], G[7:0], B[7:0], HS, VS, DE,PCLK, LOCK, PASS		GND	0.4	V
I_{OS}	Output short circuit current	V_{DDIO} = 3.3 V V_{OUT} = 0 V, OS_PCLK/DATA = L/H	PCLK		36		mA
	Output short circuit current	V_{DDIO} = 3.3 V V_{OUT} = 0 V, OS_PCLK/DATA = L/H	Deserializer Outputs		37		mA
I_{OZ}	TRI-STATE output current	PDB = 0 V, OSS_SEL = 0 V, V_{OUT} = H	Outputs	−15		15	µA

Deserializer DC Electrical Characteristics (continued)

over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN / FREQ	MIN	TYP	MAX	UNIT
1.8 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 1.71 to 1.89 V							
V_{IH}	High-level input voltage		PDB, BISTEN	1.235		V_{DDIO}	V
V_{IL}	Low-level input voltage			GND		0.595	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO}		−15	±1	15	µA
V_{OH}	High-level output voltage	I_{OH} = −2 mA, OS_PCLK/DATA = L/H	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, LOCK, PASS	V_{DDIO} − 0.45	V_{DDIO}		V
V_{OL}	Low-level output voltage	I_{OL} = +2 mA, OS_PCLK/DATA = L/H		GND		0.45	V
I_{OS}	Output short circuit current	VDDIO = 1.8 V V_{OUT} = 0 V, OS_PCLK/DATA = L/H	PCLK		18		mA
		VDDIO = 1.8 V V_{OUT} = 0 V, OS_PCLK/DATA = L/H	DATA		18		mA
I_{OZ}	TRI-STATE output current	PDB = 0 V, OSS_SEL = 0 V, V_{OUT} = 0 V or V_{DDIO}	Outputs	–15		15	µA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential input threshold high voltage	V_{CM} = +1.2 V (Internal V_{BIAS})	RIN+, RIN-	50			mV
V_{TL}	Differential input threshold low voltage			–50			mV
V_{CM}	Common-mode voltage, internal V_{BIAS}				1.2		V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO}		–15		15	µA
R_T	Internal termination resistor		RIN+, RIN-	80	100	120	Ω
CMLOUTP/N DRIVER OUTPUT DC SPECIFICATIONS – EQ TEST PORT							
V_{OD}	Differential output voltage	R_L = 100 Ω	CMLOUTP, CMLOUTN		542		mV
V_{OS}	Offset voltage Single-ended	R_L = 100 Ω			1.4		V
R_T	Internal termination resistor		CMLOUTP, CMLOUTN	80	100	120	Ω
SUPPLY CURRENT							
I_{DD1}	Deserializer supply current (includes load current)	Checker Board Pattern, OS_PCLK/DATA = H, EQ = 001, SSCG=ON CMLOUTP/N = enabled C_L = 4 pF, Figure 9	All V_{DD} pins		93	110	mA
I_{DDIO1}			V_{DDIO}		33	45	mA
					62	75	mA
I_{DDZ}	Deserializer supply current power down	PDB = 0 V, All other LVCMOS Inputs = 0 V	All V_{DD} pins		40	3000	µA
I_{DDIOZ}			V_{DDIO}		5	50	µA
					10	100	µA

7.7 DC and AC Serial Control Bus Characteristics

over 3.3-V supply and temperature ranges unless otherwise specified.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high-level voltage	SDA and SCL	2.2		V_{DDIO}	V
V_{IL}	Input low-level voltage	SDA and SCL	GND		0.8	V
V_{HY}	Input hysteresis			>50		mV
V_{OL}	Output low-level voltage(1)	SDA, IOL = 1.25 mA	0		0.4	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	–15		15	µA
C_{in}	Input capacitance	SDA or SCL		<5		pF

(1) Specification is ensured by characterization and is not tested in production.

7.8 Timing Requirements for DC and AC Serial Control Bus

over recommended operating supply and temperature ranges unless otherwise specified.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_R	SDA rise time – READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF		40		ns
t_F	SDA fall time – READ			25		ns
$t_{SU;DAT}$	Set-up time – READ			520		ns
$t_{HD;DAT}$	Hold up time – READ			55		ns
t_{SP}	Input filter			50		ns

7.9 Timing Requirements for Serializer PCLK

over recommended operating supply and temperature ranges unless otherwise specified.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{TCP}	Transmit input PCLK period	5 MHz to 65 MHz, Figure 4	15.38	T	200	ns
t_{TCIH}	Transmit input PCLK high time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit input PCLK low time		0.4T	0.5T	0.6T	ns
t_{CLKT}	PCLK input transition time		0.5		2.4	ns
SSC_{IN}	PCLK input – spread spectrum at PCLK = 65 MHz	fmod			35	kHz
		fdev			±2%	

7.10 Timing Requirements for Serial Control Bus

over 3.3-V supply and temperature ranges unless otherwise specified.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard Mode	>0		100	kHz
		Fast Mode	>0		400	kHz
t_{LOW}	SCL low period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL high period	Standard Mode	4			µs
		Fast Mode	0.6			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition, Figure 18	Standard Mode	4			us
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set-up time for a start or a repeated start condition, Figure 18	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD;DAT}$	Data hold time, Figure 18	Standard Mode	0		3.45	µs
		Fast Mode	0		0.9	µs
$t_{SU;DAT}$	Data set-up time, Figure 18	Standard Mode	250			ns
		Fast Mode	100			ns

Timing Requirements for Serial Control Bus (continued)

over 3.3-V supply and temperature ranges unless otherwise specified.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{SU;STO}$	Set-up time for STOP condition, Figure 18	Standard Mode	4			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus free time between STOP and START, Figure 18	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL and SDA rise time, Figure 18	Standard Mode			1000	µs
		Fast Mode			300	ns
t_f	SCL and SDA fall time, Figure 18	Standard Mode			300	ns
		Fast mode			300	ns

7.11 Switching Characteristics: Serializer

over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LHT}	Serializer output low-to-high transition time, Figure 3	R_L = 100 Ω, De-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100 Ω, De-emphasis = disabled, VODSEL = 1		200		ps
t_{HLT}	Serializer output high-to-low transition time, Figure 3	R_L = 100 Ω, De-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100 Ω, De-emphasis = disabled, VODSEL = 1		200		ps
t_{DIS}	Input data – set-up time, Figure 4	RGB[7:0], HS, VS, DE to PCLK	2			ns
t_{DIH}	Input data – hold time, Figure 4	PCLK to RGB[7:0], HS, VS, DE	2			ns
t_{XZD}	Serializer output active to OFF delay, Figure 6 (1)			8	15	ns
t_{PLD} (2)	Serializer PLL lock time, Figure 5 (1)(3)	R_L = 100 Ω		1.4	10	ms
t_{SD}	Serializer delay – latency, Figure 7 (1)	R_L = 100 Ω		144 × T	145 × T	ns
t_{DJIT}	Serializer output total jitter, Figure 8	R_L = 100 Ω, De-Emph = disabled, RANDOM pattern, PCLK = 65 MHz		0.28		UI (4)
		R_L = 100 Ω, De-Emph = disabled, RANDOM pattern, PCLK = 43 MHz		0.27		UI
		R_L = 100 Ω, De-Emph = disabled, RANDOM pattern, PCLK = 5 MHz		0.35		UI
λ_{STXBW}	Serializer jitter transfer Function –3-dB bandwidth	PCLK = 65 MHz		3		MHz
		PCLK = 43 MHz		2.3		MHz
		PCLK = 20 MHz		1.3		MHz
		PCLK = 5 MHz		650		kHz
δ_{STX}	Serializer jitter transfer function peaking	PCLK = 65 MHz		0.838		dB
		PCLK = 43 MHz		0.825		dB
		PCLK = 20 MHz		0.826		dB
		PCLK = 5 MHz		0.278		dB

(1) Specification is ensured by characterization and is not tested in production.
(2) t_{PLD} is the time required by the serializer to obtain lock when exiting power-down state with an active PCLK.
(3) When the serializer output is at TRI-STATE the deserializer will lose PLL lock. Resynchronization / Relock must occur before data transfer require t_{PLD}
(4) UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / [28 × PCLK]). The UI scales with PCLK frequency.

7.12 Switching Characteristics: Deserializer

over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETERS		TEST CONDITIONS	PIN / FREQ	MIN	TYP	MAX	UNIT
t_{RCP}	PCLK output period	$t_{RCP} = t_{TCP}$	PCLK	15.38	T	200	ns
t_{RDC}	PCLK output duty cycle	SSCG=OFF, 5–65 MHz	PCLK	43%	50%	57%	
		SSCG=ON, 5–20 MHz		35%	59%	65%	
		SSCG=ON, 20–65 MHz		40%	53%	60%	
t_{CLH}	LVCMOS Low-to-high transition time, Figure 10	V_{DDIO} = 1.8 V, C_L = 4 pF	PCLK/RGB[7:0], HS, VS, DE		2.1		ns
		V_{DDIO} = 3.3 V, C_L = 4 pF			2.0		ns
t_{CHL}	LVCMOS High-to-low transition time, Figure 10	V_{DDIO} = 1.8 V C_L = 4 pF, OS_PCLK/DATA = L	PCLK/RGB[7:0], HS, VS, DE		1.6		ns
		V_{DDIO} = 3.3 V C_L = 4 pF, OS_PCLK/DATA = H			1.5		ns
t_{ROS}	Data valid before PCLK – set-up time Figure 14	V_{DDIO} = 1.71 to 1.89 V or 3.0 to 3.6 V C_L = 4pF (lumped load)	RGB[7:0], HS, VS, DE	0.27	0.45		T
t_{ROH}	Data valid after PCLK – hold time Figure 14	V_{DDIO} = 1.71 to 1.89 V or 3.0 to 3.6 V C_L = 4pF (lumped load)	RGB[7:0], HS, VS, DE	0.4	0.55		T
t_{DDLT} (1)	Deserializer lock time, Figure 13	SSC[3:0] = 0000 (OFF) (2)	PCLK = 5 MHz		3		ms
		SSC[3:0] = 0000 (OFF) (2)	PCLK = 65 MHz		4		ms
		SSC[3:0] = ON (2)	PCLK = 5 MHz		30		ms
		SSC[3:0] = ON (2)	PCLK = 65 MHz		6		ms
t_{DD}	Deserializer delay – latency, Figure 11	SSC[3:0] = 0000 (OFF) (2)			139 × T	140 × T	ns
t_{DPJ}	Deserializer period jitter	SSC[3:0] = OFF (3) (4) (5)	PCLK = 5 MHz		975	1700	ps
			PCLK = 10 MHz		500	1000	ps
			PCLK = 65 MHz		550	1250	ps
t_{DCCJ}	Deserializer cycle-to-cycle jitter	SSC[3:0] = OFF (6) (7) (5)	PCLK = 5 MHz		675	1150	ps
			PCLK = 10 MHz		375	900	ps
			PCLK = 65 MHz		500	1150	ps
t_{IJT}	Deserializer input jitter tolerance, Figure 16	EQ = OFF, SSCG = OFF, PCLK = 65 MHz	for jitter freq < 2 MHz		0.9		UI
			for jitter freq > 6 MHz		0.5		UI
BIST Mode							
t_{PASS}	BIST PASS valid time, BISTEN = 1, Figure 17				1	10	µs
SSCG Mode							
f_{DEV}	Spread spectrum clocking deviation frequency	Under typical conditions	PCLK = 5 to 65 MHz, SSC[3:0] = ON	±0.5%		±2%	
f_{MOD}	Spread spectrum clocking modulation frequency	Under typical conditions	PCLK = 5 to 65 MHz, SSC[3:0] = ON	8		100	kHz

(1) t_{DDLT} is the time required by the deserializer to obtain lock when exiting power-down state with an active PCLK.
(2) t_{PLD} is the time required by the serializer to obtain lock when exiting power-down state with an active PCLK.
(3) t_{DPJ} is the maximum amount the period is allowed to deviate over many samples.
(4) Specification is ensured by characterization and is not tested in production.
(5) Specification is ensured by design and is not tested in production.
(6) Specification is ensured by characterization and is not tested in production.
(7) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.

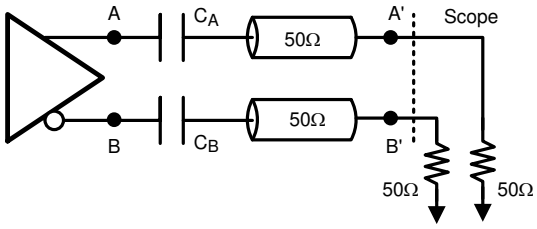


Figure 1. Serializer Test Circuit

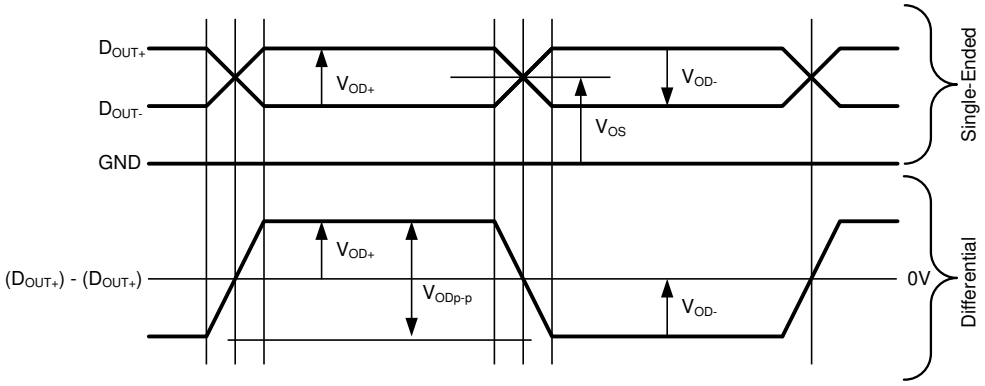


Figure 2. Serializer Output Waveforms

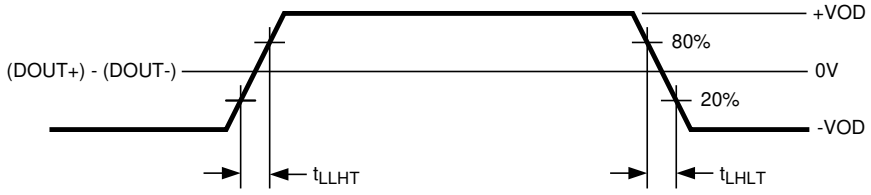


Figure 3. Serializer Output Transition Times

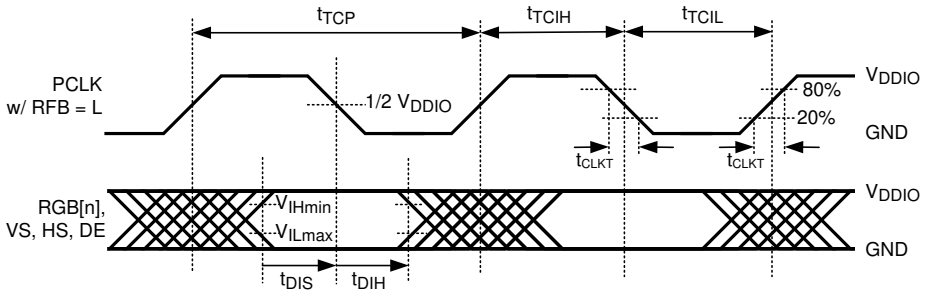


Figure 4. Serializer Input PCLK Waveform and Set and Hold Times

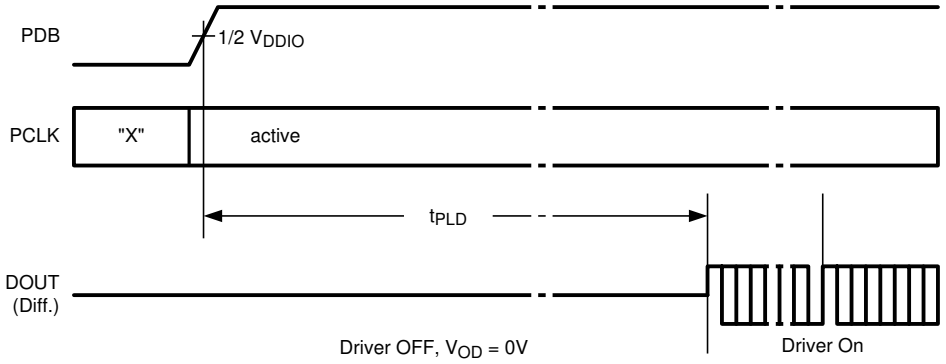


Figure 5. Serializer Lock Time

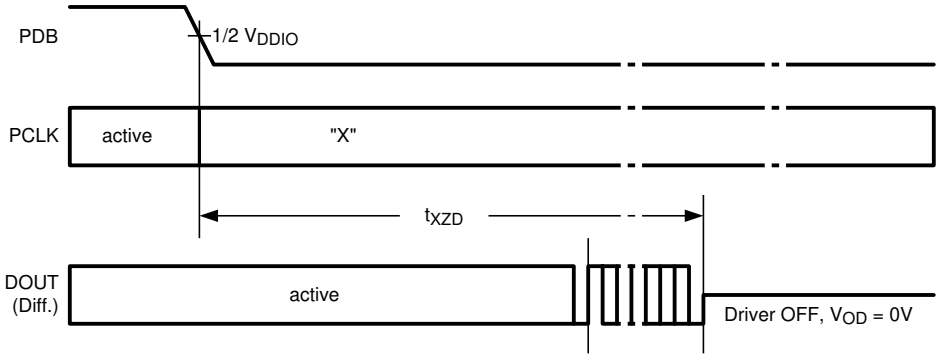


Figure 6. Serializer Disable Time

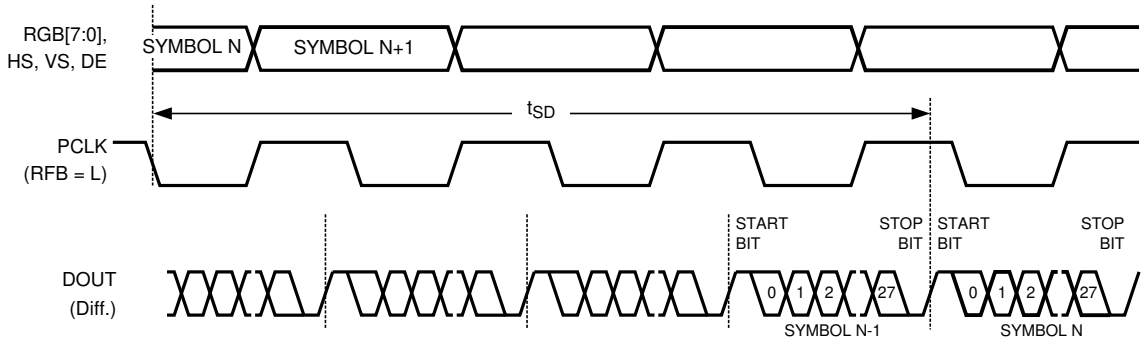


Figure 7. Serializer Latency Delay

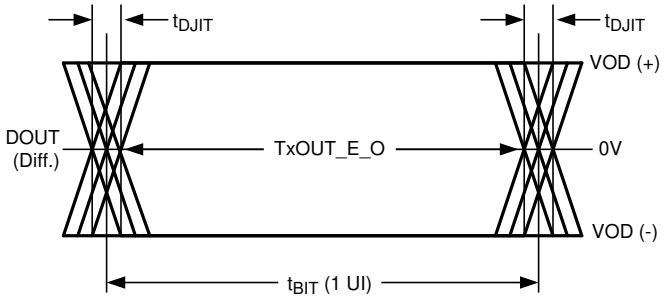


Figure 8. Serializer Output Jitter

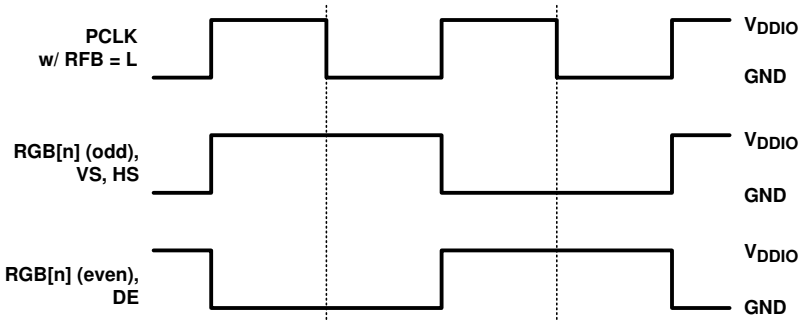


Figure 9. Checkerboard Data Pattern

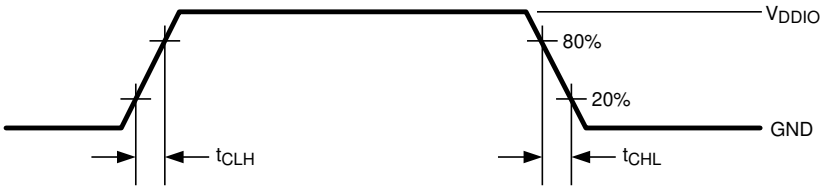


Figure 10. Deserializer LVCMOS Transition Times

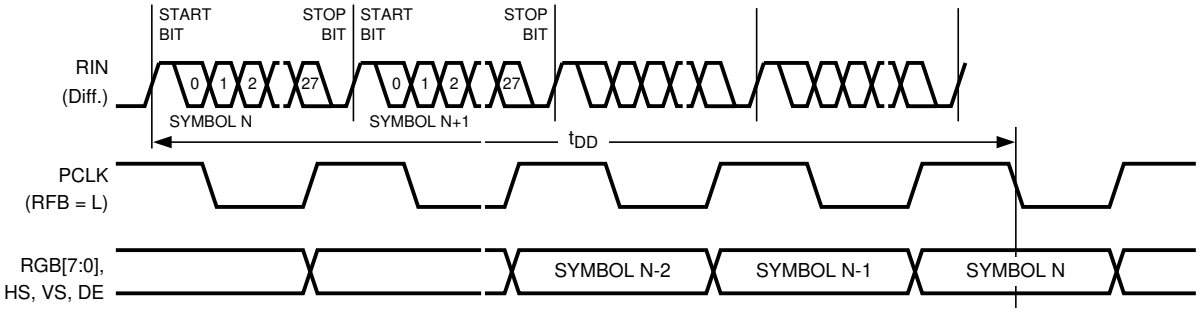


Figure 11. Deserializer Delay – Latency

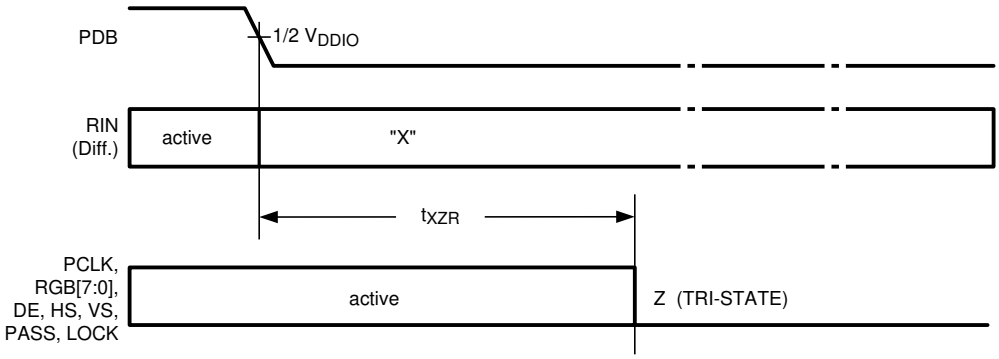


Figure 12. Deserializer Disable Time (OSS_SEL = 0)

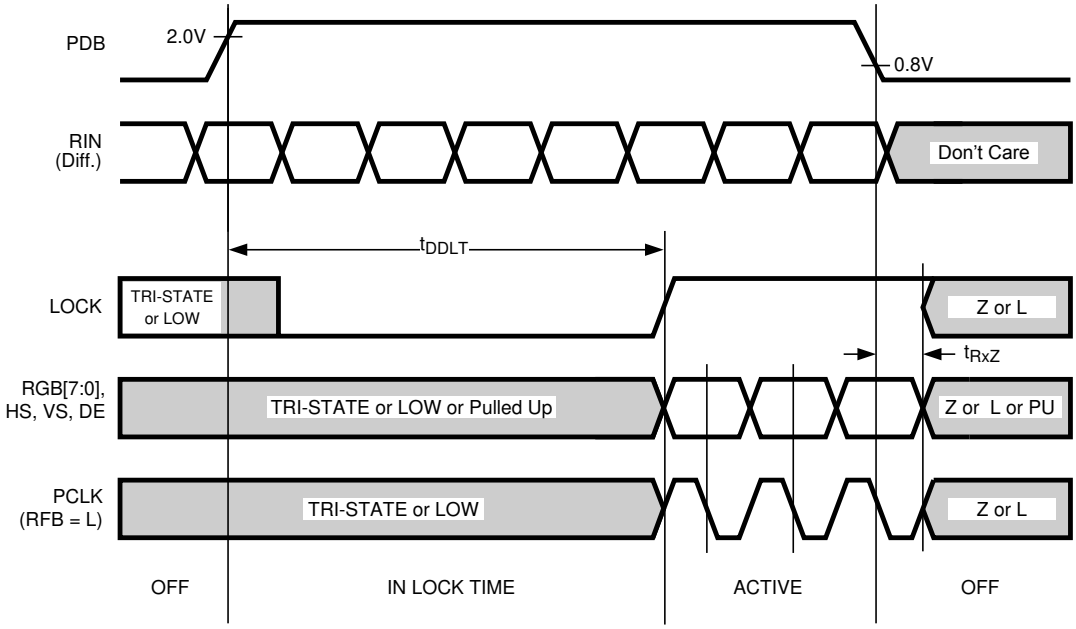


Figure 13. Deserializer PLL Lock Times and PDB TRI-STATE Delay

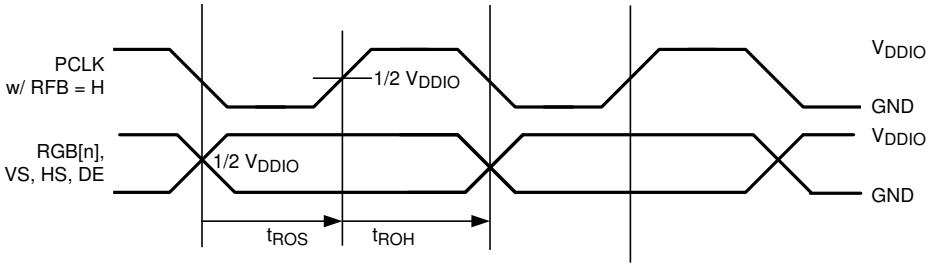


Figure 14. Deserializer Output Data Valid (Set-up and Hold) Times With SSCG = Off

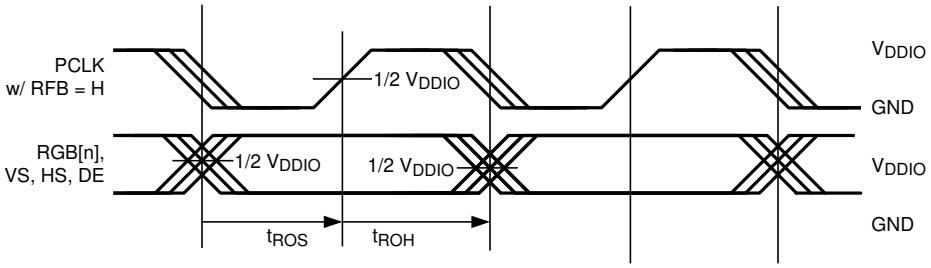


Figure 15. Deserializer Output Data Valid (Set-up and Hold) Times With SSCG = On

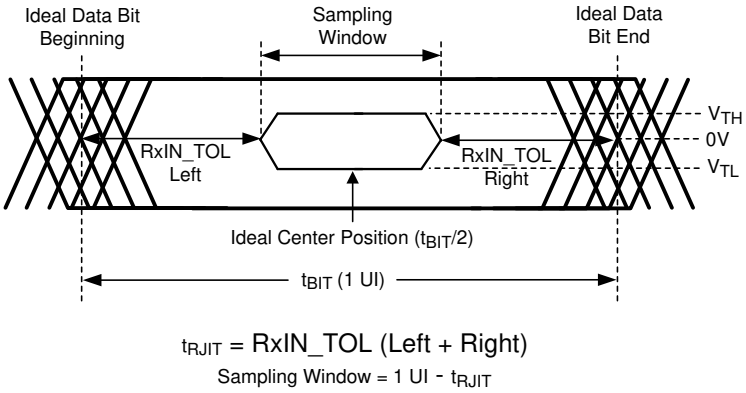


Figure 16. Receiver Input Jitter Tolerance

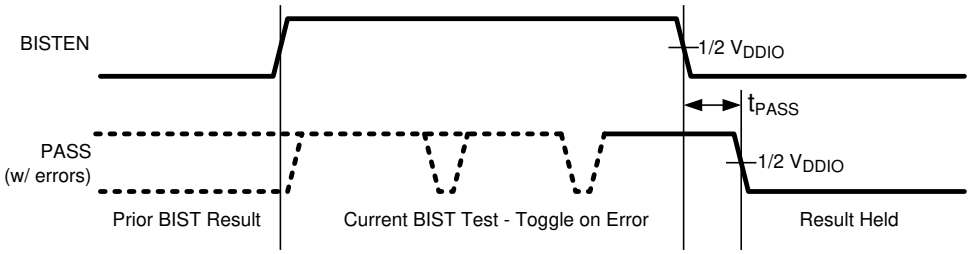


Figure 17. BIST PASS Waveform

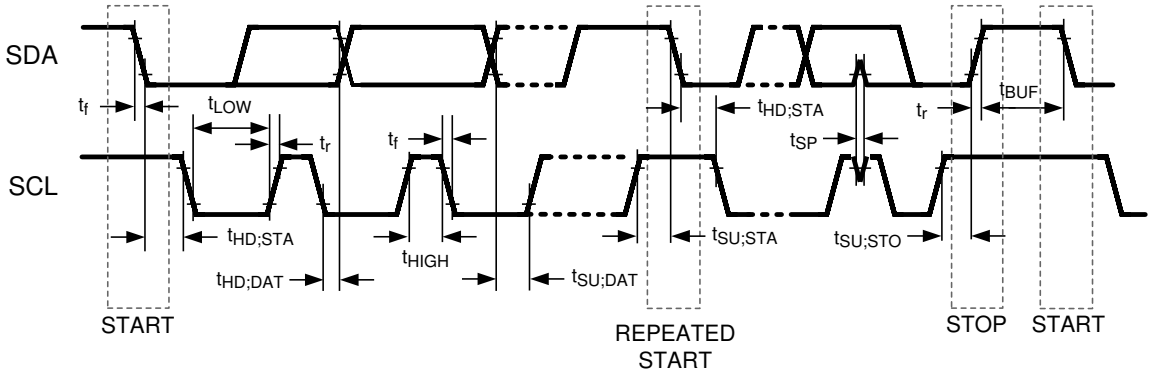


Figure 18. Serial Control Bus Timing Diagram

7.13 Typical Characteristics

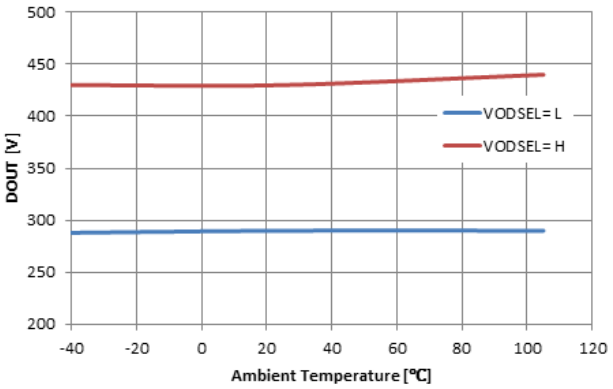


Figure 19. Differential Output Voltage vs Ambient Temperature

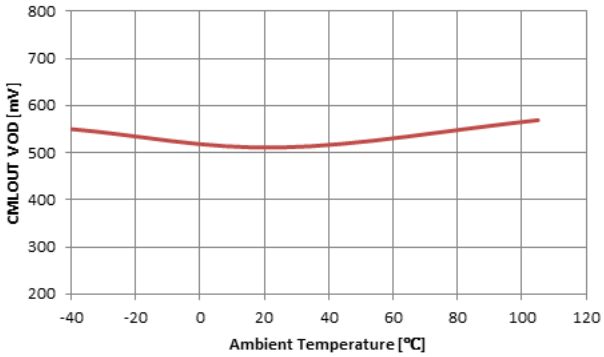


Figure 20. CMLOUT VOD vs Ambient Temperature

8 Detailed Description

8.1 Overview

The DS90UR90xQ-Q1 chipset transmits and receives 27-bits of data (24-high speed color bits and 3 low speed video control signals) over a single serial FPD-Link II pair operating at 140Mbps to 1.82Gbps. The serial stream also contains an embedded clock, video control signals and the DC-balance information which enhances signal quality and supports AC coupling. The pair is intended for use with each other but is backward-compatible with previous generations of FPD-Link II as well.

The deserializer can attain lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic *plug and lock* performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream providing a parallel LVCMOS video bus to the display.

The DS90UR90xQ-Q1 chipset can operate in 24-bit color depth (with VS,HS,DE encoded in the DCA bit) or in 18-bit color depth (with VS, HS, DE encoded in DCA or mapped into the high-speed data bits). In 18–bit color applications, the three video signals maybe sent encoded via the DCA bit (restrictions apply) or sent as data bits along with three additional general-purpose signals.

Functional Block Diagrams shows the diagrams for the chipsets.

8.2 Functional Block Diagrams

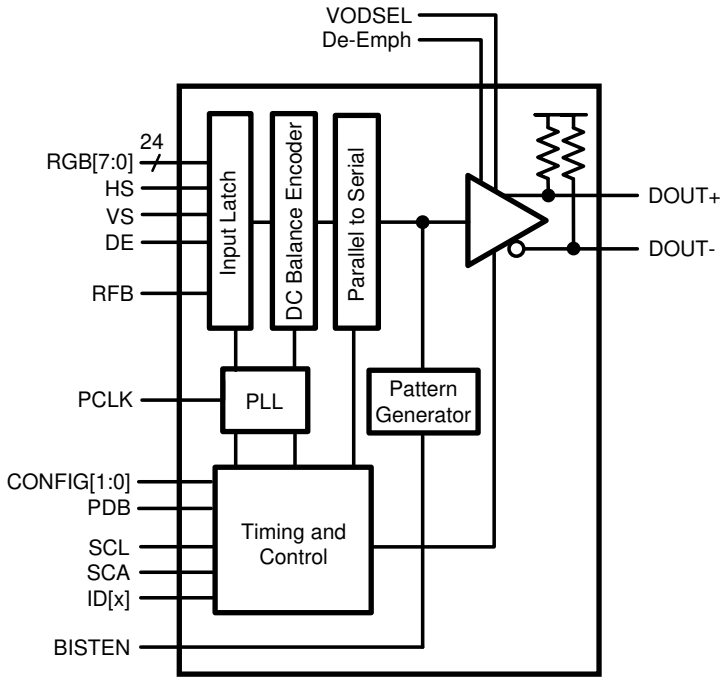


Figure 21. DS90UR905Q-Q1 – Serializer

Functional Block Diagrams (continued)

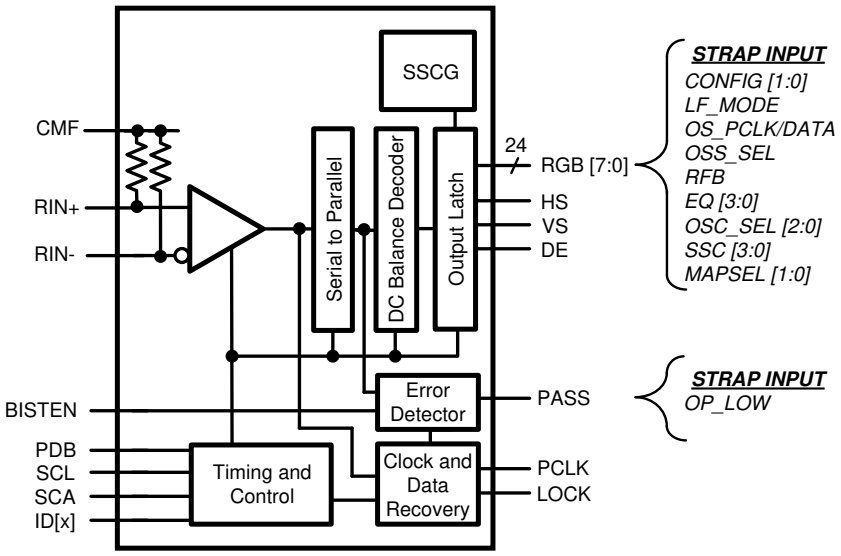


Figure 22. DS90UR906Q-Q1 – Deserializer

8.3 Feature Description

8.3.1 Data Transfer

The DS90UR90xQ-Q1 chipset will transmit and receive a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. b[23:0] contain the scrambled RGB data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream and can also contain encoded control (VS, HS, DE). Both DCA and DCB coding schemes are generated by the serializer and decoded by the deserializer automatically. Figure 23 illustrates the serial stream per PCLK cycle.

NOTE

The figure only illustrates the bits but does not actually represent the bit location as the bits are scrambled and balanced continuously.

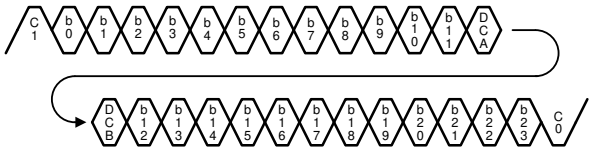


Figure 23. FPD-Link II Serial Stream (DS90UR90xQ-Q1)

Feature Description (continued)

8.3.2 Video Control Signal Filter — Serializer and Deserializer

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled:
  - DE and HS: Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled:
  - DE and HS: Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS: Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals (see Figure 24).

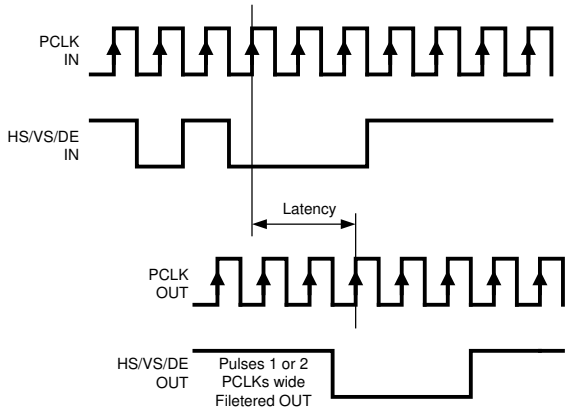


Figure 24. Video Control Signal Filter Waveform

8.3.3 Serializer Functional Description

The serializer converts a wide parallel input bus to a single serial output data stream, and also acts as a signal generator for the chipset Built-In Self Test (BIST) mode. The device can be configured via external pins or through the optional serial control bus. The serializer features enhance signal quality on the link by supporting: a selectable VOD level, a selectable de-emphasis signal conditioning and also the FPD-Link II data coding that provides randomization, scrambling, and DC balancing of the video data. The serializer includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and also the system spread spectrum PCLK support. The serializer features power saving features with a sleep mode, auto stop clock feature, and optional LVCMOS (1.8 V) parallel bus compatibility.

See also the Functional Description of the chipset's serial control bus and BIST modes.

8.3.3.1 EMI Reduction Features

8.3.3.1.1 Serializer Spread Spectrum Compatibility

The serializer PCLK is capable of tracking spread spectrum clocking (SSC) from a host source. The PCLK will accept spread spectrum tracking up to 35 kHz modulation and ±0.5, ±1 or ±2% deviations (center spread). The maximum conditions for the PCLK input are: a modulation frequency of 35 kHz and amplitude deviations of ±2% (4% total).

Feature Description (continued)

8.3.3.2 Signal Quality Enhancers

8.3.3.2.1 Serializer VOD Select (VODSEL)

The serializer differential output voltage may be increased by setting the VODSEL pin High. When VODSEL is Low, the VOD is at the standard (default) level. When VODSEL is High, the DC VOD is increased in level. The increased VOD is useful in extremely high noise environments and also on extra long cable length applications. When using de-emphasis it is recommended to set VODSEL = H to avoid excessive signal attenuation especially with the larger de-emphasis settings. This feature may be controlled by the external pin or by register.

Table 1. Differential Output Voltage

INPUT	EFFECT	
VODSEL	VOD (mV)	VOD (mVp-p)
H	±420	840
L	±280	560

8.3.3.2.2 Serializer De-Emphasis (De-Emph)

The De-Emph pin controls the amount of de-emphasis beginning one full bit time after a logic transition that the serializer drives. This is useful to counteract loading effects of long or lossy cables. This pin should be left open for standard switching currents (no de-emphasis) or if controlled by register. De-emphasis is selected by connecting a resistor on this pin to ground, with R value between 0.5 kΩ to 1 MΩ, or by register setting. When using De-Emphasis, TI recommends to set VODSEL = H.

Table 2. De-Emphasis Resistor Value

RESISTOR VALUE (KΩ)	DE-EMPHASIS SETTING
Open	Disabled
0.6	–12 dB
1.0	–9 dB
2.0	–6 dB
5.0	–3 dB

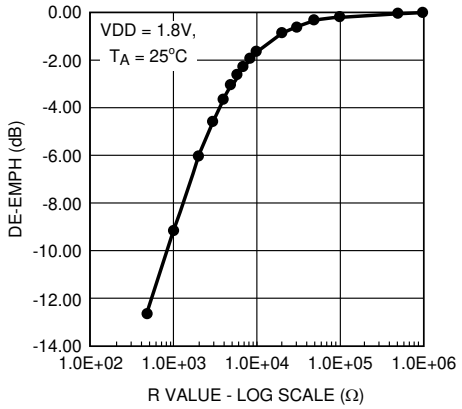


Figure 25. De-Emph vs. R value

8.3.3.3 Power-Saving Features

8.3.3.3.1 Serializer Power-down Feature (PDB)

The serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin is controlled by the host and is used to save power, disabling the link when the display is not needed. In the power-down mode, the high-speed driver outputs are both pulled to VDD and present a 0-V VOD state.

NOTE

In power down, the optional Serial Bus Control Registers are **RESET**.

8.3.3.3.2 Serializer Stop Clock Feature

The serializer will enter a low power SLEEP state when the PCLK is stopped. A STOP condition is detected when the input clock frequency is less than 3 MHz. The clock should be held at a static LOW or HIGH state. When the PCLK starts again, the Ser will then lock to the valid input PCLK and then transmits the RGB data to the deserializer.

NOTE

In STOP CLOCK SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

8.3.3.3.3 1.8-V or 3.3-V VDDIO Operation

The serializer parallel bus and serial bus interface can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for host compatibility. The 1.8 V levels will offer lower noise (EMI) and also a system power savings.

8.3.3.4 Serializer Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the data is latched on. If RFB is High, input data is latched on the Rising edge of the PCLK. If RFB is Low, input data is latched on the Falling edge of the PCLK. serializer and deserializer maybe set differently. This feature may be controlled by the external pin or by register.

8.3.3.5 Optional Serial Bus Control

See *Optional Serial Bus Control*.

8.3.3.6 Optional BIST Mode

See *Built-In Self Test (BIST)*.

8.3.4 Deserializer Functional Description

The deserializer converts a single input serial data stream to a wide parallel output bus, and also provides a signal check for the chipset Built-In Self Test (BIST) mode. The device can be configured via external pins and strap pins or through the optional serial control bus. The deserializer features enhance signal quality on the link by supporting: an equalizer input and also the FPD-Link II data coding that provides randomization, scrambling, and DC balanacing of the data. The deserializer includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and also the output spread spectrum clock generation (SSCG) support. The deserializer features power saving features with a power-down mode, and optional LVCMOS (1.8 V) interface compatibility.

8.3.4.1 Signal Quality Enhancers

8.3.4.1.1 Deserializer Input Equalizer Gain (EQ)

The deserializer can enable receiver input equalization of the serial stream to increase the eye opening to the deserializer input.

NOTE

This function cannot be seen at the RxIN± input but can be observed at the serial test port (CMLOUTP/N) enabled through the Serial Bus control registers. The equalization feature may be controlled by the external pin or by register.

Table 3. Receiver Equalization Configuration Table

INPUTS				EFFECT
EQ3	EQ2	EQ1	EQ0	
L	L	L	H	≈1.5 dB
L	L	H	H	≈3 dB
L	H	L	H	≈4.5 dB
L	H	H	H	≈6 dB
H	L	L	H	≈7.5 dB
H	L	H	H	≈9 dB
H	H	L	H	≈10.5 dB
H	H	H	H	≈12 dB
X	X	X	L	OFF(1)

(1) Default Setting is EQ = Off

8.3.4.2 EMI Reduction Features

8.3.4.2.1 Deserializer Output Slew (OS_PCLK/DATA)

The parallel bus outputs (RGB[7:0], VS, HS, DE and PCLK) of the deserializer feature a selectable output slew. The DATA (RGB[7:0], VS, HS, DE) are controlled by strap pin or register bit OS_DATA. The PCLK is controlled by strap pin or register bit OS_PCLK. When the OS_PCLK/DATA = HIGH, the maximum slew rate is selected. When the OS_PCLK/DATA = LOW, the minimum slew rate is selected. Use the higher slew rate setting when driving longer traces or a heavier capacitive load.

8.3.4.2.2 Deserializer Common-Mode Filter Pin (CMF) — Optional

The deserializer provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 0.1-µF capacitor may be connected to this pin to Ground.

8.3.4.2.3 Deserializer SSCG Generation — Optional

The deserializer provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2.0% (4% total) at up to 35kHz modulations nominally are available (see Table 4). This feature may be controlled by external STRAP pins or by register.

Table 4. SSCG Configuration (LF_MODE = L) — Deserializer Output

SSC[3:0] INPUTS LF_MODE = L (20 to 65 MHz)				RESULT	
SSC3	SSC2	SSC1	SSC0	FDEV (%)	FMOD (kHz)
L	L	L	L	Off	Off
L	L	L	H	±0.5	PCLK/2168
L	L	H	L	±1.0	
L	L	H	H	±1.5	
L	H	L	L	±2.0	
L	H	L	H	±0.5	PCLK/1300
L	H	H	L	±1.0	
L	H	H	H	±1.5	
H	L	L	L	±2.0	
H	L	L	H	±0.5	PCLK/868
H	L	H	L	±1.0	
H	L	H	H	±1.5	
H	H	L	L	±2.0	

Table 4. SSCG Configuration (LF_MODE = L) — Deserializer Output (continued)

SSC[3:0] INPUTS LF_MODE = L (20 to 65 MHz)				RESULT	
SSC3	SSC2	SSC1	SSC0	FDEV (%)	FMOD (kHz)
H	H	L	H	±0.5	PCLK/650
H	H	H	L	±1.0	
H	H	H	H	±1.5	

Table 5. SSCG Configuration (LF_MODE = H) — Deserializer Output

SSC[3:0] INPUTS LH_MODE = H (5 to 20 MHz)				RESULT	
SSC3	SSC2	SSC1	SSC0	FDEV (%)	FMOD (kHz)
L	L	L	L	Off	Off
L	L	L	H	±0.5	PCLK/620
L	L	H	L	±1.0	
L	L	H	H	±1.5	
L	H	L	L	±2.0	
L	H	L	H	±0.5	PCLK/370
L	H	H	L	±1.0	
L	H	H	H	±1.5	
H	L	L	L	±2.0	
H	L	L	H	±0.5	PCLK/258
H	L	H	L	±1.0	
H	L	H	H	±1.5	
H	H	L	L	±2.0	
H	H	L	H	±0.5	PCLK/192
H	H	H	L	±1.0	
H	H	H	H	±1.5	

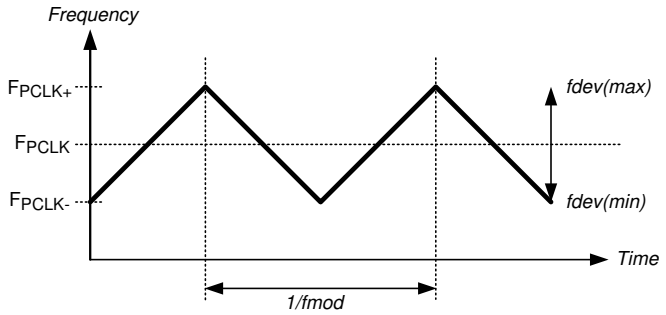


Figure 26. SSCG Waveform

8.3.4.2.4 1.8-V or 3.3-V VDDIO Operation

The deserializer parallel bus and Serial Bus Interface can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for target (Display) compatibility. The 1.8-V levels will offer a lower noise (EMI) and also a system power-savings.

8.3.4.3 Power-Saving Features

8.3.4.3.1 Deserializer Power-Down Feature (PDB)

The deserializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the system to save power, disabling the deserializer when the display is not needed. An auto detect mode is also available. In this mode, the PDB pin is tied High and the deserializer will enter power down when the serial stream stops. When the serial stream starts up again, the deserializer will lock to the input stream and assert the LOCK pin and output valid data. In power-down mode, the Data and PCLK output states are determined by the OSS_SEL status.

NOTE

In power down, the optional Serial Bus Control Registers are **RESET**.

8.3.4.3.2 Deserializer Stop Stream SLEEP Feature

The deserializer will enter a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the deserializer will then lock to the incoming signal and recover the data.

NOTE

In STOP STREAM SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

8.3.4.4 Deserializer CLOCK-DATA RECOVERY STATUS FLAG (LOCK) and OUTPUT STATE SELECT (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK goes from TRI-STATE to LOW (depending on the value of the OSS_SEL setting). After the DS90UR906Q-Q1 completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and PCLK outputs. The PCLK output is held at its current state at the change from OSC_CLK (if this is enabled via OSC_SEL) to the recovered clock (or vice versa).

If there is a loss of clock from the input serial stream, LOCK is driven Low and the state of the RGB/VS/HS/DE outputs are based on the OSS_SEL setting (STRAP PIN configuration or register).

8.3.4.5 Deserializer Oscillator Output (Optional)

The deserializer provides an optional PCLK output when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by the external pin or by register (see Table 7 and Table 8).

Table 6. OSS_SEL and PDB Configuration — Deserializer Outputs (1)

INPUTS			OUTPUTS			
SERIAL INPUT	PDB	OSS_SEL	PCLK	RGB/HS/VS/DE	LOCK	PASS
X	L	X	Z	Z	Z	Z
Static	H	L	L	L	L	L
Static	H	H	Z	Z*	L	L
Active	H	X	Active	Active	H	H

(1) If pin is strapped HIGH, output will be pulled up

Table 7. OSC (Oscillator) Mode — Deserializer Output(1)

INPUTS	OUTPUTS			
EMBEDDED PCLK	PCLK	RGB/HS/VS/DE	LOCK	PASS
NOTE *	OSC Output	L	L	L
Present	Toggling	Active	H	H

(1) Absent and OSC_SEL ≠ 000

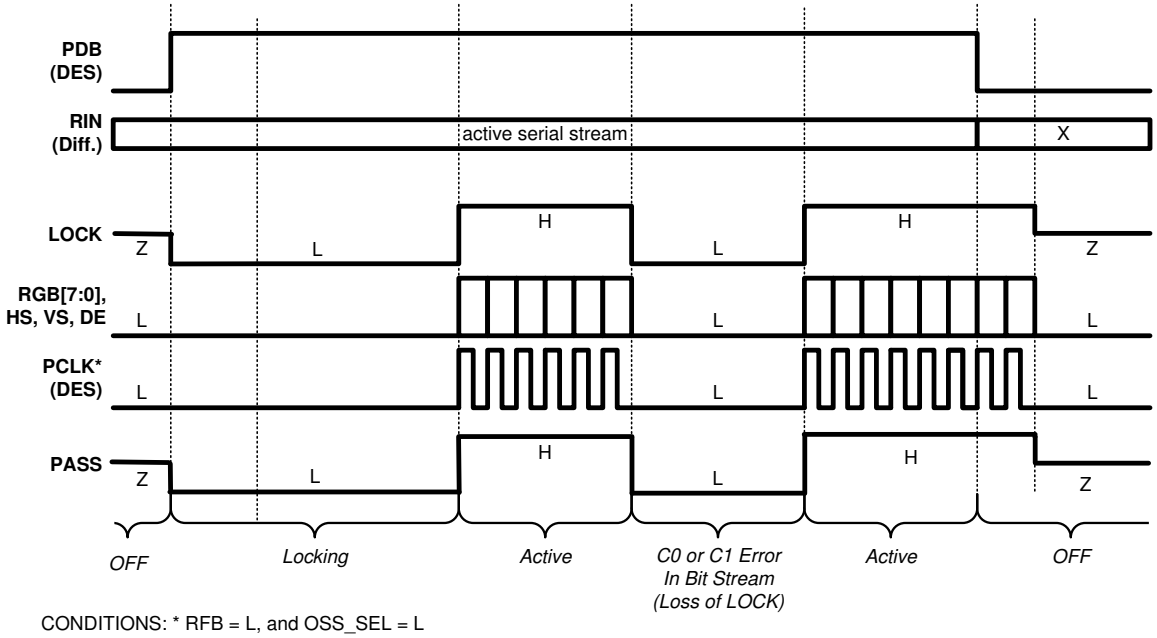


Figure 27. Deserializer Outputs With Output State Select Low (OSS_SEL = L)

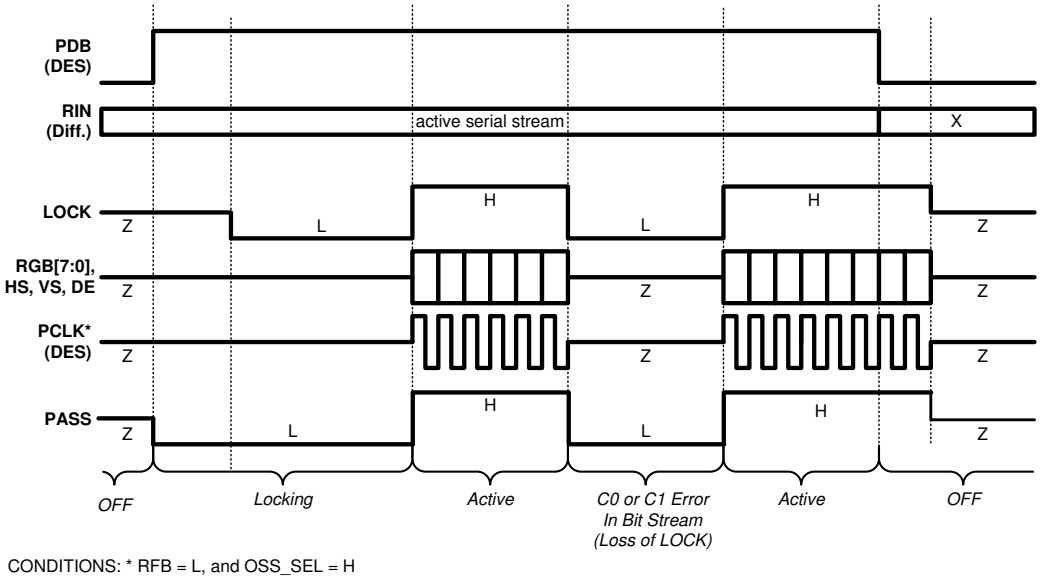
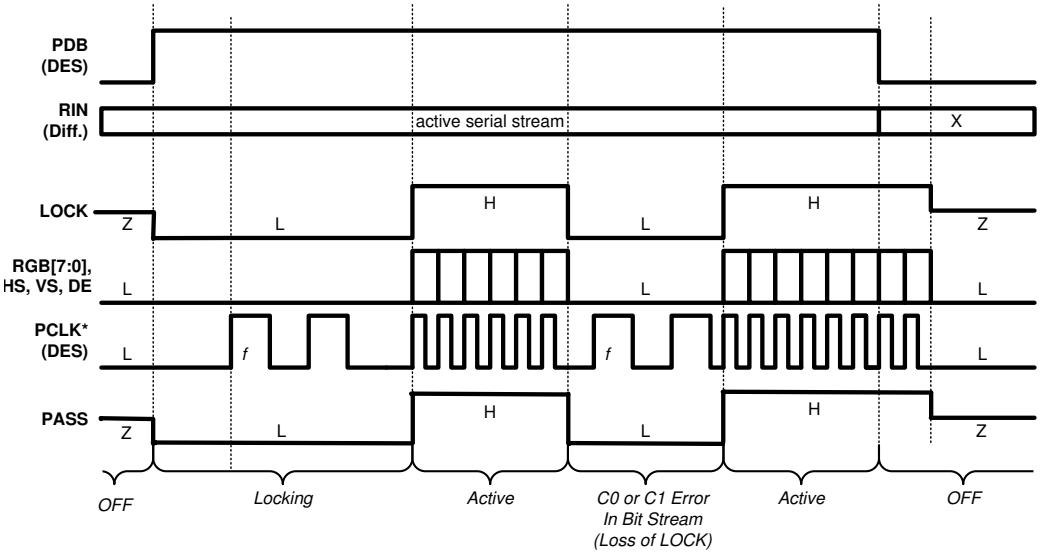


Figure 28. Deserializer Outputs With Output State Select High (OSS_SEL = H)

Table 8. OSC_SEL (Oscillator) Configuration

OSC_SEL[2:0] INPUTS			PCLK OSCILLATOR OUTPUT
OSC_SEL2	OSC_SEL1	OSC_SEL0	
L	L	L	Off – Feature Disabled – Default
L	L	H	50 MHz ±40%
L	H	L	25 MHz ±40%
L	H	H	16.7 MHz ±40%
H	L	L	12.5 MHz ±40%
H	L	H	10 MHz ±40%
H	H	L	8.3 MHz ±40%
H	H	H	6.3 MHz ±40%



CONDITIONS: * RFB = L, OSS_SEL = H , and OSC_SEL not equal to 000.

Figure 29. Deserializer Outputs with Output State High and PCLK Output Oscillator Option Enabled

8.3.4.6 Deserializer OP_LOW (Optional)

The OP_ LOW feature is used to hold the LVCMOS outputs (except the LOCK output) at a LOW state. The user must toggle the OP_LOW Set / Reset register bit to release the outputs to the normal toggling state.

NOTE

The release of the outputs can only occur when LOCK is HIGH. When the OP_LOW feature is enabled, anytime LOCK = LOW, the LVCMOS outputs will toggle to a LOW state again. The OP_ LOW strap pin feature is assigned to output PASS pin 42.

Restrictions on other straps:

1. Other straps should not be used in order to keep RGB[7:0], HS, VS, DE, and PCLK at a true LOW state. Other features should be selected through I^2C.
2. OSS_SEL function is not available when O/P_LOW is tied H.

Outputs RGB[7:0], HSYNC, VSYNC, DE, and PCLK are in TRI-STATE before PDB toggles HIGH because the OP_LOW strap value has not been recognized until the DS90UR906Q-Q1 powers up. Figure 30 shows the user controlled release of OP_LOW and automatic reset of OP_LOW set on the falling edge of LOCK. Figure 31 shows the user controlled release of OP_LOW and manual reset of OP_LOW set.

NOTE

Manual reset of OP_LOW can only occur when LOCK is H.

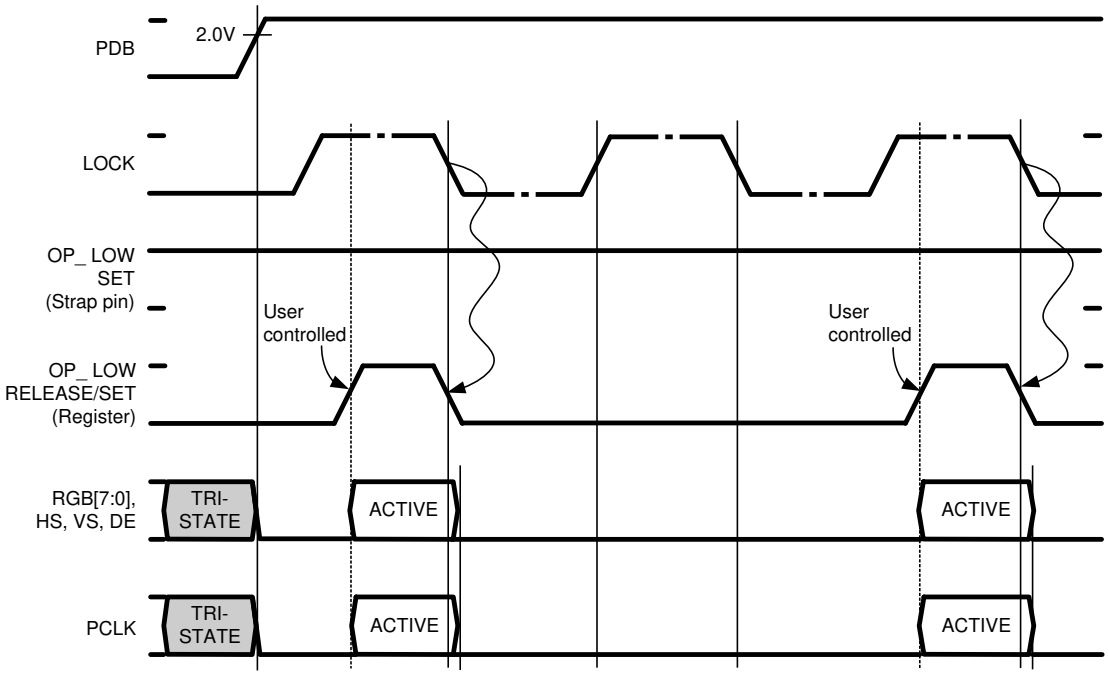


Figure 30. OP_LOW Auto Set

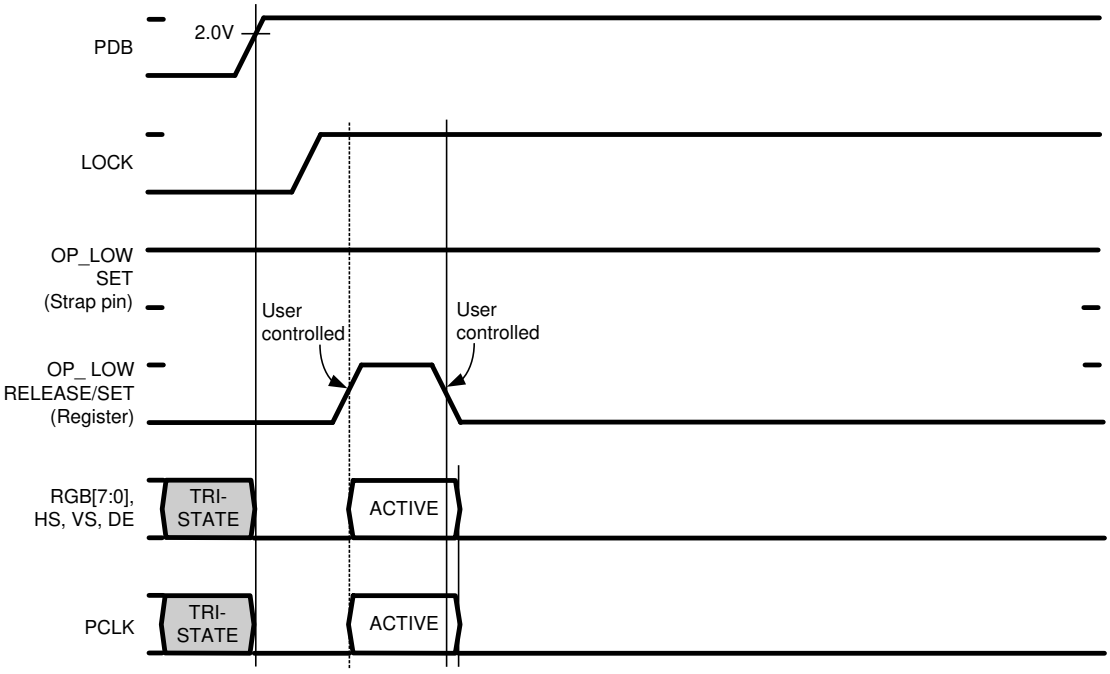


Figure 31. OP_LOW Manual Set/Reset

8.3.4.7 Deserializer Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the data is strobed on. If RFB is High, output data is strobed on the Rising edge of the PCLK. If RFB is Low, data is strobed on the Falling edge of the PCLK. This allows for inter-operability with downstream devices. The deserializer output does not need to use the same edge as the serializer input. This feature may be controlled by the external pin or by register.

8.3.4.8 Deserializer Control Signal Filter (Optional)

The deserializer provides an optional Control Signal (VS, HS, DE) filter that monitors the three video control signals and eliminates any pulses that are 1 or 2 PCLKs wide. Control signals must be 3 pixel clocks wide (in its HIGH or LOW state, regardless of which state is active). This is set by the CONFIG[1:0] or by the Control Register. This feature may be controlled by the external pin or by Register.

8.3.4.9 Deserializer Low Frequency Optimization (LF_Mode)

This feature may be controlled by the external pin or by Register.

8.3.4.10 Deserializer Map Select

This feature may be controlled by the external pin or by register.

Table 9. Map Select Configuration

INPUTS		Effect
MAPSEL1	MAPSEL0	
L	L	Bit 4, Bit 5 on LSB **DEFAULT**
L	H	LSB 0 or 1
H	H or L	LSB 0

8.3.4.11 Deserializer Strap Input Pins

Configuration of the device maybe done through configuration input pins and the STRAP input pins, or through the Serial Control Bus. The STRAP input pins share select parallel bus output pins. They are used to load in configuration values during the initial power-up sequence of the device. Only a pullup on the pin is required when a HIGH is desired. By default the pad has an internal pulldown, and will bias Low by itself. The recommended value of the pullup is 10 kΩ to V_{DDIO}; open (NC) for Low, no pulldown is required (internal pulldown). If using the Serial Control Bus, no pullups are required.

8.3.4.12 Optional Serial Bus Control

See *Optional Serial Bus Control*.

8.3.4.13 Optional BIST Mode

See *Built-In Self Test (BIST)*.

8.3.5 Built-In Self Test (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only a input clock is required along with control to the serializer and deserializer BISTEN input pins. The Ser outputs a test pattern (PRBS7) and drives the link at speed. The deserializer detects the PRBS7 pattern and monitors it for errors. A PASS output pin toggles to flag any payloads that are received with 1 to 24 errors. Upon completion of the test, the result of the test is held on the PASS output until reset (new BIST test or power down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. During the BIST duration the deserializer data outputs toggle with a checkerboard pattern.

Inter-operability is supported between this FPD-Link II device and all FPD-Link II generations (Gen 1, 2, 3). See *Sample BIST Sequence* for entering BIST mode and control.

8.3.5.1 Sample BIST Sequence

See Figure 32 for the BIST mode flow diagram.

Step 1: Place the DS90UR905Q-Q1 serializer in BIST Mode by setting serializer BISTEN = H. For the DS90UR905Q-Q1 serializer or DS99R421 FPD-Link II serializer BIST Mode is enabled through the BISTEN pin. For the DS90C241 serializer or DS90UR241 serializer, BIST mode is enetered by setting all the input data of the device to LOW state. A PCLK is required for all the serializer options. When the deserializer detects the BIST mode pattern and command (DCA and DCB code) the RGB and control signal outputs are shut off.

Step 2: Place the DS90UR906Q-Q1 deserializer in BIST mode by setting the BISTEN = H. The deserializer is now in the BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data and the final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the serializer BISTEN input is set Low. The Link returns to normal operation.

Figure 33 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or Rx Equalization).

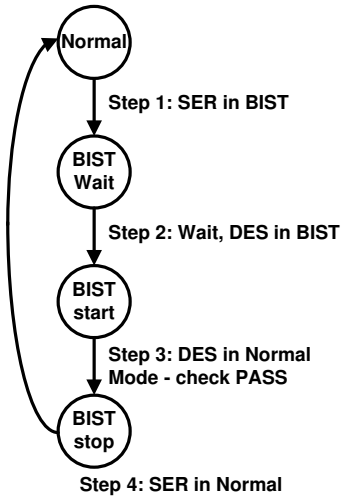


Figure 32. BIST Mode Flow Diagram

8.3.5.2 BER Calculations

It is possible to calculate the approximate Bit Error Rate (BER). The following is required:

- Pixel Clock Frequency (MHz)
- BIST Duration (seconds)
- BIST test Result (PASS)

The BER is less than or equal to one over the product of 24 times the PCLK rate times the test duration. If we assume a 65-MHz PCLK, a 10 minute (600 seconds) test, and a PASS, the BERT is ≤ 1.07 × 10E-12.

The BIST mode runs a check on the data payload bits. The LOCK pin also provides a link status. It the recovery of the C0 and C1 bits does not reconstruct the expected clock signal, the LOCK pin will switch Low. The combination of the LOCK and At-Speed BIST PASS pin provides a powerful tool for system evaluation and performance monitoring.

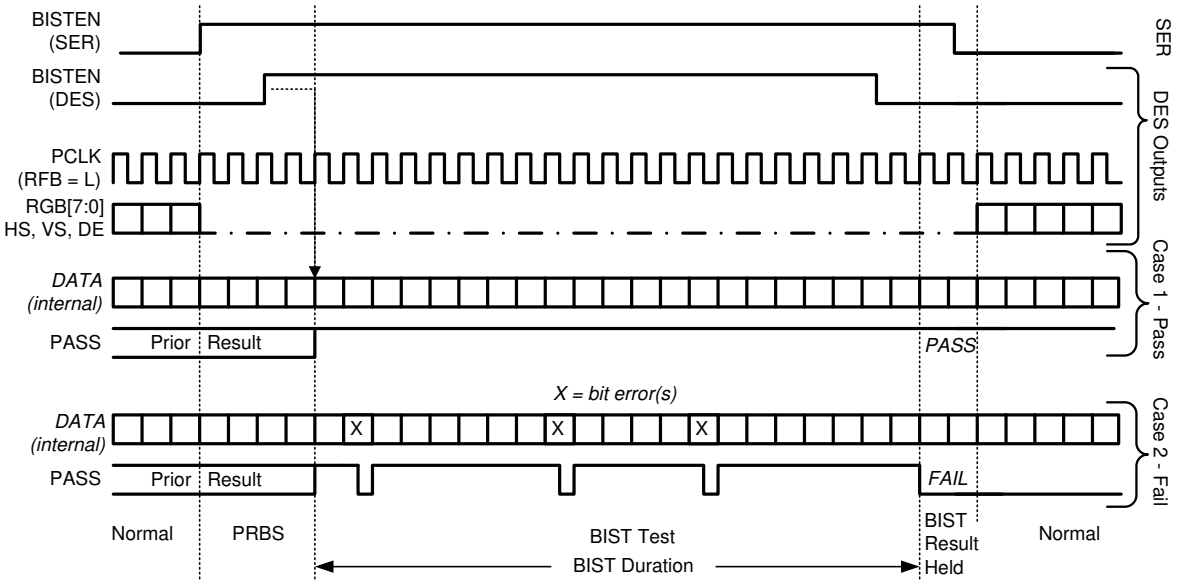


Figure 33. BIST Waveforms

8.3.6 Optional Serial Bus Control

The serializer and deserializer may also be configured by the use of a serial control bus that is I^2C protocol compatible. By default, the I^2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable or allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus since multiple addresses are supported (see Figure 34).

The serial bus is comprised of three pins. The SCL is a serial bus clock Input. The SDA is the serial bus data input/output signal. Both SCL and SDA signals require an external pullup resistor to V_{DDIO}. For most applications a 4.7-k pullup resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

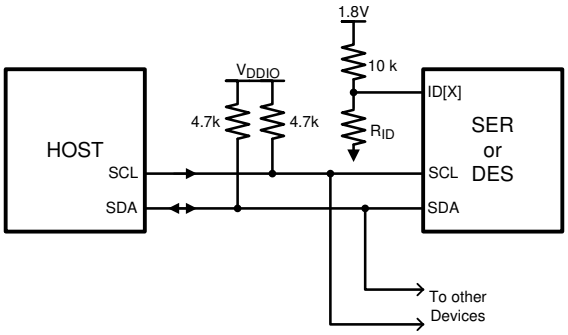


Figure 34. Serial Control Bus Connection

The third pin is the ID[X] pin. This pin sets one of four possible device addresses. Two different connections are possible. The pin may be pulled to V_{DD} (**1.8V, NOT V_{DDIO}**) with a 10 kΩ resistor; or a 10-kΩ pullup resistor (to V_{DD}**1.8V, NOT V_{DDIO}**) and a pulldown resistor of the recommended value to set other three possible addresses may be used. See Table 10 for the serializer and Table 11 for the deserializer. Do not tie ID[x] directly to VSS.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH (see Figure 35).

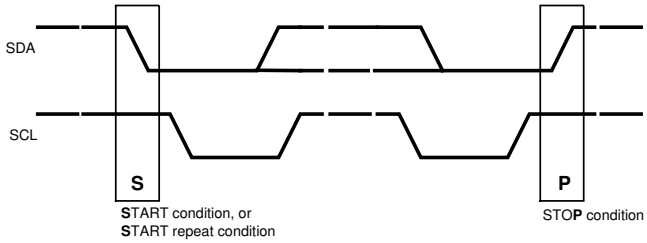


Figure 35. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 36 and a WRITE is shown in Figure 37.

NOTE

During initial power-up, a delay of 10 ms will be required before the I^2C will respond.

If the Serial Bus is not required, the three pins may be left open (NC).

Table 10. ID[x] Resistor Value – DS90UR905Q-Q1 Serializer

RESISTOR RID(1) kΩ (5% TOL)	ADDRESS 7'b	ADDRESS 8'b 0 APPENDED (WRITE)
0.47	7b' 110 1001 (h'69)	8b' 1101 0010 (h'D2)
2.7	7b' 110 1010 (h'6A)	8b' 1101 0100 (h'D4)
8.2	7b' 110 1011 (h'6B)	8b' 1101 0110 (h'D6)
Open	7b' 110 1110 (h'6E)	8b' 1101 1100 (h'DC)

(1) RID ≠ 0 Ω, do not connect directly to VSS (GND), this is not a valid address.

Table 11. ID[x] Resistor Value – DS90UR906Q-Q1 Deserializer

RESISTOR RID(1) kΩ (5% TOL)	ADDRESS 7'b	ADDRESS 8'b 0 APPENDED (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

(1) RID ≠ 0 Ω, do not connect directly to VSS (GND), this is not a valid address.

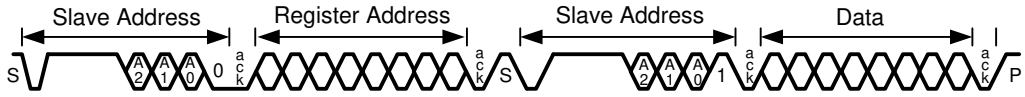


Figure 36. Serial Control Bus — READ

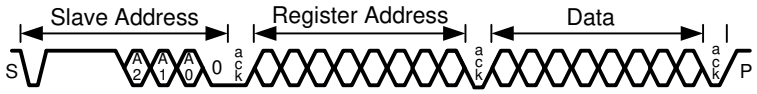


Figure 37. Serial Control Bus — WRITE

8.4 Device Functional Modes

8.4.1 Serializer and Deserializer Operating Modes and Backward Compatibility (CONFIG[1:0])

The DS90UR90xQ-Q1 chipset is also backward-compatible with previous generations of FPD-Link II. Configuration modes are provided for backwards compatibility with the DS90C241 / DS90C124 FPD-Link II Generation 1, and also the DS90UR241 / DS90UR124 FPD-Link II Generation 2 chipset by setting the respective mode with the CONFIG[1:0] pins on the serializer or deserializer as shown in Table 12 and Table 13. The selection also determine whether the Video Control Signal filter feature is enabled or disabled in Normal mode. This feature may be controlled by pin or by Register.

Table 12. DS90UR905Q-Q1 Serializer Modes

CONFIG1	CONFIG0	MODE	DESERIALIZER DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS90UR906Q-Q1
L	H	Normal Mode, Control Signal Filter enabled	DS90UR906Q-Q1
H	L	Backwards-Compatible GEN2	DS90UR124, DS99R124
H	H	Backwards-Compatible GEN1	DS90C124

Table 13. DS90UR906Q Deserializer Modes

CONFIG1	CONFIG0	MODE	SERIALIZER DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS90UR905Q-Q1
L	H	Normal Mode, Control Signal Filter enabled	DS90UR905Q-Q1
H	L	Backwards-Compatible GEN2	DS90UR241
H	H	Backwards-Compatible GEN1	DS90C241

8.5 Register Maps

Table 14. SERIALIZER — Serial Bus Control Registers

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
0	0	Serializer Config 1	7	R/W	0	***Reserved***	***Reserved***
			6	R/W	0	***Reserved***	***Reserved***
			5	R/W	0	VODSEL	0: Low 1: High
			4	R/W	0	RFB	0: Data latched on Falling edge of PCLK 1: Data latched on Rising edge of PCLK
			3:2	R/W	00	CONFIG	00: Control Signal Filter Disabled 01: Control Signal Filter Enabled 10: DS90UR124, DS99R124 Mode 11: DS90C124 Mode
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG	0: Configurations set from control pins 1: Configuration set from registers (except I2C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[x] Pin 1: Address from Register
			6:0	R/W	1101000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1101 001 (h'69) 7b '1101 010 (h'6A) 7b '1101 011 (h'6B) 7b '1101 110 (h'6E) All other addresses are ***Reserved***.
2	2	De-Emphasis Control	7:5	R/W	000	De-E Setting	000: set by external Resistor 001: –1 dB 010: –2 dB 011: –3.3 dB 100: –5 dB 101: –6.7 dB 110: –9 dB 111: –12 dB
			4	R/W	0	De-E EN	0: De-Emphasis Enabled 1: De-Emphasis Disabled
			3:0	R/W	000	***Reserved***	***Reserved***

Table 15. DESERIALIZER — Serial Bus Control Registers

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
0	0	Deserializer Config 1	7	R/W	0	LFMODE	0: 20 to 65 MHz Operation 1: 5 to 20 MHz Operation
			6	R/W	0	OS_PCLK	0: Normal PCLK Output Slew 1: Increased PCLK Slew
			5	R/W	0	OS_DATA	0: Normal DATA OUTPUT Slew 1: Increased Data Slew
			4	R/W	0	RFB	0: Data strobed on Falling edge of PCLK 1: Data strobed on Rising edge of PCLK
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: Backwards-Compatible (DS90UR241) 11: Backwards-Compatible (DS90C241)
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG Control	0: Configurations set from control pins / STRAP pins 1: Configurations set from registers (except I2C_ID)
1	1	Slave ID	7	R/W	0		0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1110000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1110 001 (h'71) 7b '1110 010 (h'72) 7b '1110 011 (h'73) 7b '1110 110 (h'76) All other addresses are ***Reserved***.
2	2	Deserializer Features 1	7	R/W	0	OP_LOW Release/Set	0: set outputs state LOW (except LOCK) 1: release output LOW state, outputs toggling normally Note: This register only works during LOCK = 1.
			6	R/W	0	OSS_SEL	Output Sleep State Select 0: PCLK/RGB[7:0]/HS/VS/DE = L, LOCK = Normal, PASS = H 1: PCLK/RGB[7:0]/HS/VS/DE = Tri-State, LOCK = Normal, PASS = H
			5:4	R/W	00	MAP_SEL	Special for Backwards-Compatible Mode 00: bit 4, 5 on LSB 01: LSB zero if all data is zero; one if any data is one 10: LSB zero 11: LSB zero
			3	R/W	0	OP_LOW strap bypass	0: strap will determine whether OP_LOW feature is ON or OFF 1: Turns OFF OP_LOW feature
			2:0	R/W	00	OSC_SEL	000: OFF 001: 50 MHz ±40% 010: 25 MHz ±40% 011: 16.7 MHz ±40% 100: 12.5 MHz ±40% 101: 10 MHz ±40% 110: 8.3 MHz ±40% 111: 6.3 MHz ±40%

Table 15. DESERIALIZER — Serial Bus Control Registers (continued)

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
3	3	Deserializer Features 2	7:5	R/W	000	EQ Gain	000: ≈1.625 dB 001: ≈3.25 dB 010: ≈4.87 dB 011: ≈6.5 dB 100: ≈8.125 dB 101: ≈9.75 dB 110: ≈11.375 dB 111: ≈13 dB
			4	R/W	0	EQ Enable	0: EQ = disabled 1: EQ = enabled
			3:0	R/W	0000	SSC	**IF LF_MODE = 0, then**: 000: SSCG OFF 0001: fdev = ±0.5%, fmod = PCLK/2168 0010: fdev = ±1.0%, fmod = PCLK/2168 0011: fdev = ±1.5%, fmod = PCLK/2168 0100: fdev = ±2.0%, fmod = PCLK/2168 0101: fdev = ±0.5%, fmod = PCLK/1300 0110: fdev = ±1.0%, fmod = PCLK/1300 0111: fdev = ±1.5%, fmod = PCLK/1300 1000: fdev = ±2.0%, fmod = PCLK/1300 1001: fdev = ±0.5%, fmod = PCLK/868 1010: fdev = ±1.0%, fmod = PCLK/868 1011: fdev = ±1.5%, fmod = PCLK/868 1100: fdev = ±2.0%, fmod = PCLK/868 1101: fdev = ±0.5%, fmod = PCLK/650 1110: fdev = ±1.0%, fmod = PCLK/650 1111: fdev = ±1.5%, fmod = PCLK/650 **IF LF_MODE = 1, then**: 000: SSCG OFF 0001: fdev = ±0.5%, fmod = PCLK/620 0010: fdev = ±1.0%, fmod = PCLK/620 0011: fdev = ±1.5%, fmod = PCLK/620 0100: fdev = ±2.0%, fmod = PCLK/620 0101: fdev = ±0.5%, fmod = PCLK/370 0110: fdev = ±1.0%, fmod = PCLK/370 0111: fdev = ±1.5%, fmod = PCLK/370 1000: fdev = ±2.0%, fmod = PCLK/370 1001: fdev = ±0.5%, fmod = PCLK/258 1010: fdev = ±1.0%, fmod = PCLK/258 1011: fdev = ±1.5%, fmod = PCLK/258 1100: fdev = ±2.0%, fmod = PCLK/258 1101: fdev = ±0.5%, fmod = PCLK/192 1110: fdev = ±1.0%, fmod = PCLK/192 1111: fdev = ±1.5%, fmod = PCLK/192
4	4	CMLOUT Config	7	R/W	0	Repeater Enable	0: Output CMLOUTP/N = disabled 1: Output CMLOUTP/N = enabled
			6:0	R/W	0000000	***Reserved***	***Reserved***

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Display Application

The DS90UR90xQ-Q1 chipset is intended for interface between a host (graphics processor) and a display. It supports an 24-bit color depth (RGB888) and up to 1024 × 768 display formats. In a RGB888 application, 24 color bits (R[7:0], G[7:0], B[7:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link with PCLK rates from 5 to 65 MHz. The chipset may also be used in 18-bit color applications. In this application three to six general-purpose signals may also be sent from host to display.

The deserializer is expected to be located close to its target device. The interconnect between the deserializer and the target device is typically in the 1 to 3 inch separation range. The input capacitance of the target device is expected to be in the 5 to 10 pF range. Care should be taken on the PCLK output trace as this signal is edge sensitive and strobes the data. It is also assumed that the fanout of the deserializer is one. If additional loads need to be driven, a logic buffer or mux device is recommended.

9.1.2 Live Link Insertion

The serializer and deserializer devices support live pluggable applications. The automatic receiver lock to random data "plug & go" hot insertion capability allows the DS90UR906Q-Q1 to attain lock to the active data stream during a live insertion event.

9.1.3 Alternate Color / Data Mapping

Color Mapped data Pin names are provided to specify a recommended mapping for 24-bit Color Applications. Seven [7] is assumed to be the MSB, and Zero [0] is assumed to be the LSB. While this is recommended it is not required. When connecting to earlier generations of FPD-Link II serializer and deserializer devices, a color mapping review is recommended to ensure the correct connectivity is obtained. Table 16 provides examples for interfacing to 18-bit applications with or without the video control signals embedded. The DS90UR906Q-Q1 deserializer also provides additional flexibility with the MAP_SEL feature as well.

Table 16. Alternate Color / Data Mapping

18-BIT RGB	18-BIT RGB	24-BIT RGB	905 PIN NAME	906 PIN NAME	24-BIT RGB	18-BIT RGB	18-BIT RGB
LSB R0	GP0	RO	RO	R0	R0	GP0	LSB R0
R1	GP1	R1	R1	R1	R1	GP1	R1
R2	R0	R2	R2	R2	R2	R0	R2
R3	R1	R3	R3	R3	R3	R1	R3
R4	R2	R4	R4	R4	R4	R2	R4
MSB R5	R3	R5	R5	R5	R5	R3	MSB R5
LSB G0	R4	R6	R6	R6	R6	R4	LSB G0
G1	R5	R7	R7	R7	R7	R5	G1
G2	GP2	G0	G0	G0	G0	GP2	G2
G3	GP3	G1	G1	G1	G1	GP3	G3
G4	GO	G2	G2	G2	G2	G0	G4
MSB G5	G1	G3	G3	G3	G3	G1	MSB G5
LSB B0	G2	G4	G4	G4	G4	G2	LSB0
B1	G3	G5	G5	G5	G5	G3	B1
B2	G4	G6	G6	G6	G6	G4	B2

Application Information (continued)

Table 16. Alternate Color / Data Mapping (continued)

18-BIT RGB	18-BIT RGB	24-BIT RGB	905 PIN NAME	906 PIN NAME	24-BIT RGB	18-BIT RGB	18-BIT RGB
B3	G5	G7	G7	G7	G7	G5	B3
B4	GP4	B0	B0	B0	B0	GP4	B4
MSB B5	GP5	B1	B1	B1	B1	GP5	MSB B5
HS	B0	B2	B2	B2	B2	B0	HS
VS	B1	B3	B3	B3	B3	B1	VS
DE	B2	B4	B4	B4	B4	B2	DE
GP0	B3	B5	B5	B5	B5	B3	GP0
GP1	B4	B6	B6	B6	B6	B4	GP1
GP2	B5	B7	B7	B7	B7	B5	GP2
GND	HS	HS	HS	HS	HS	HS	GND
GND	VS	VS	VS	VS	VS	VS	GND
GND	DE	DE	DE	DE	DE	DE	GND
Scenario 3 (1)	**Scenario 2 (2)**	**Scenario 1 (3)**	**905 Pin Name**	**906 Pin Name**	**Scenario 1 (3)**	**Scenario 2 (2)**	**Scenario 3 (1)**

(1) Scenario 3 supports an 18-bit RGB color mapping, 3 un-embedded video control signals, and up to three general-purpose signals.
(2) Scenario 2 supports an 18-bit RGB color mapping, 3 embedded video control signals, and up to six general-purpose signals.
(3) Scenario 1 supports the 24-bit RGB color mapping, along with the 3 embedded video control signals. This is the native mode for the chipset.

9.2 Typical Applications

9.2.1 DS90UR905Q-Q1 Typical Connection

Figure 38 shows a typical application of the DS90UR905Q-Q1 serializer in Pin control mode for a 65 MHz 24-bit Color Display Application. The LVDS outputs require 100-nF AC-coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1 µF capacitors and a 4.7-µF capacitor should be used for local device bypassing. System GPO (General-Purpose Output) signals control the PDB and BISTEN pins. In this application the RFB pin is tied Low to latch data on the falling edge of the PCLK. The application assumes the companion deserializer (DS90UR906Q-Q1) therefore the configuration pins are also both tied Low. In this example the cable is long, therefore the VODSEL pin is tied High and a De-Emphasis value is selected by the resistor R1. The interface to the host is with 1.8-V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8-V rail. The Optional Serial Bus Control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

Typical Applications (continued)

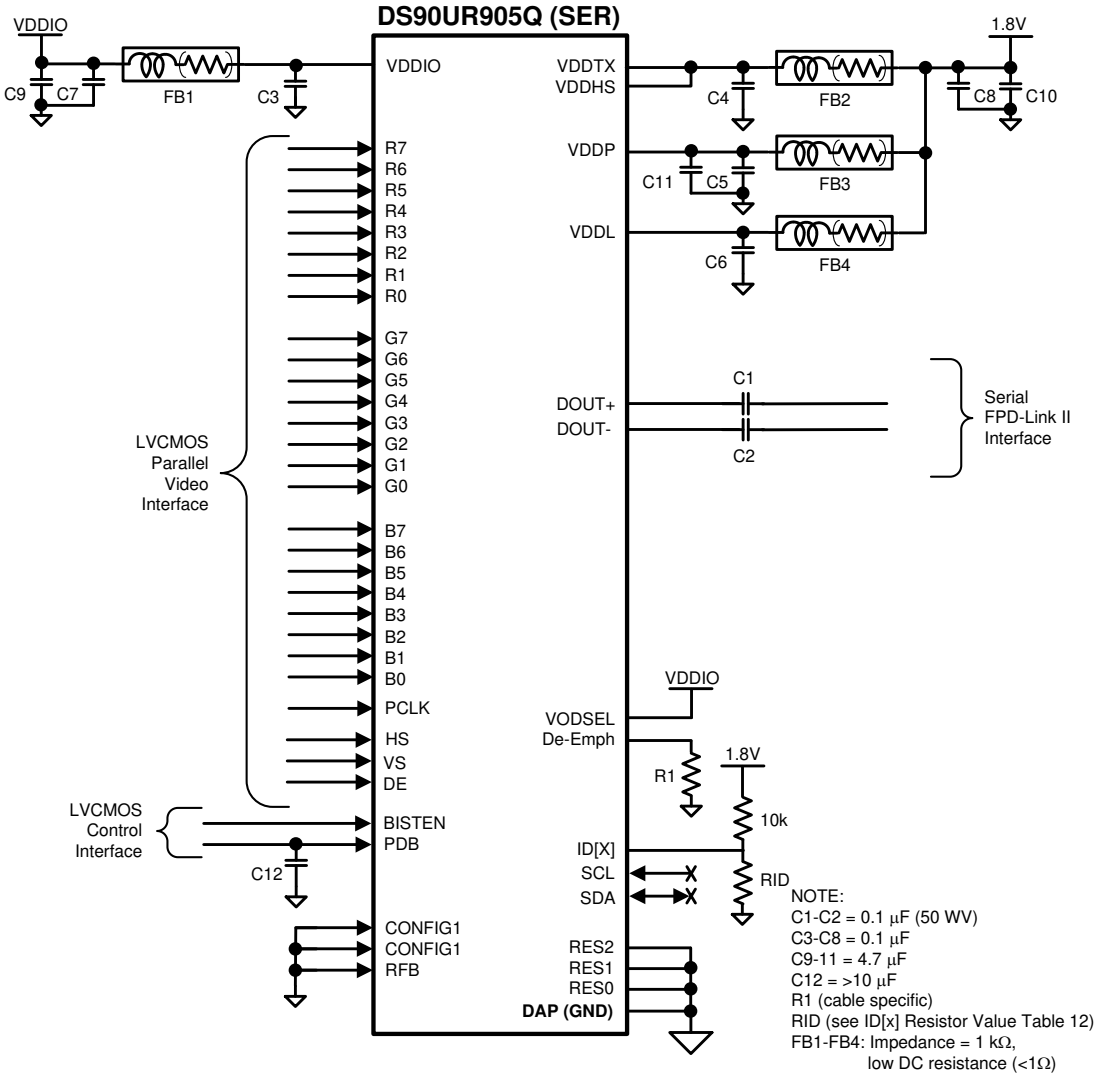


Figure 38. DS90UR905Q-Q1 Typical Connection Diagram – Pin Control

9.2.1.1 Design Requirements

For this example, use the parameters listed in Table 17.

Table 17. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
VDDIO	1.8 V to 3.3 V
VDDL, VDDP, VDDHS, VDDTX	1.8 V
AC-Coupling Capacitor for DOUT±	100 nF

9.2.1.2 Detailed Design Procedure

The DOUT± outputs require 100-nF AC-coupling capacitors to the line. The power supply filter capacitors are placed near the power supply pins. A smaller capacitance capacitor should be located closer to the power supply pins.

The VODSEL pin is tied to VDDIO for the long cable application. The De-Emph pin may connect a resistor to ground. Refer to Table 2. The PDB and BISTEN pins are assumed controlling by a microprocessor. The PDB has to be LOW state until all power supply voltages reach the final voltage. The RFB pin is tied Low to latch data on the falling edge of the PCLK, High for the rising clock edge. The CNFIG[1:0] pins are set depending on operating modes and backward compatibility. The SCL, SDA and ID[x] pins are left open when these Serial Bus Control pins are unused. The RES[2:0] pins and DAP should be tied to ground.

9.2.1.3 Application Curves

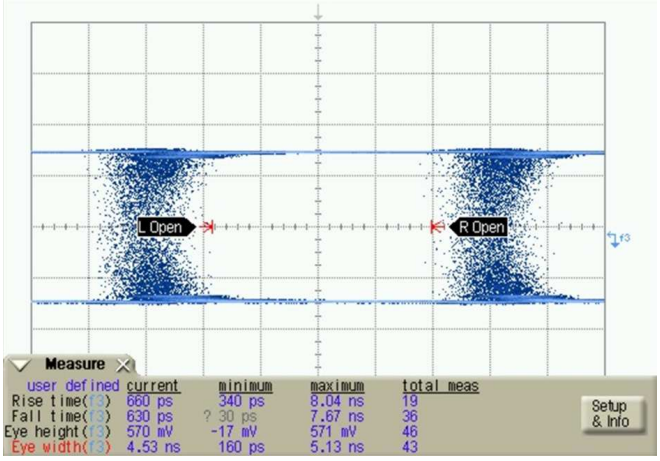


Figure 39. Eye Diagram at PCLK = 5 MHz

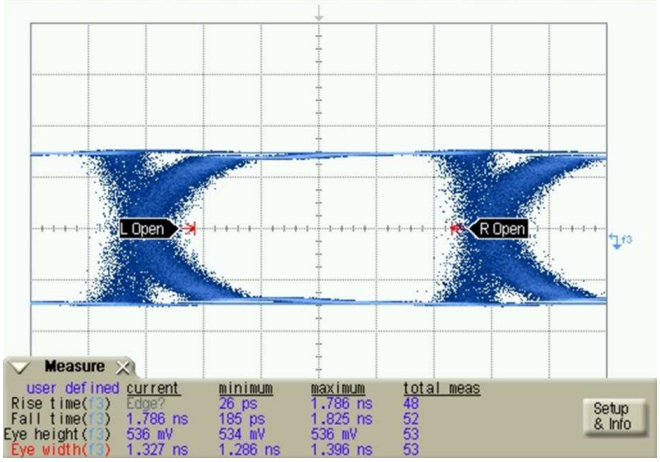


Figure 40. Eye Diagram at PCLK = 20 MHz

9.2.2 DS90UR906Q-Q1 Typical Connection

Figure 41 shows a typical application of the DS90UR906Q-Q1 deserializer in Pin/STRAP control mode for a 65-MHz 24-bit Color Display Application. The LVDS inputs utilize 100-nF coupling capacitors to the line and the receiver provides internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, seven 0.1-µF capacitors and two 4.7-µF capacitors should be used for local device bypassing. System GPO (General-Purpose Output) signals control the PDB and the BISTEN pins. In this application the RRFB pin is tied Low to strobe the data on the falling edge of the PCLK.

Since the device in the Pin/STRAP mode, four 10-kΩ pullup resistors are used on the parallel output bus to select the desired device features. CONFIG[1:0] is set to 01'b for Normal Mode and Control Signal Filter ON, this is accomplished with the STRAP pullup on B7. The receiver input equalizer is also enabled and set to provide 7.5 dB of gain, this is accomplished with EQ[3:0] set to 1001'b with STRAP pullups on G4 and G7. To reduce parallel bus EMI, the SSCG feature is enabled and set to 30 kHz and ±1% with SSC[3:0] set to 0010'b and a STRAP pullup on R4. The desired features are set with the use of the four pullup resistors.

The interface to the target display is with 3.3V LVCMOS levels, thus the VDDIO pin is connected to the 3.3 V rail. The optional Serial Bus Control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

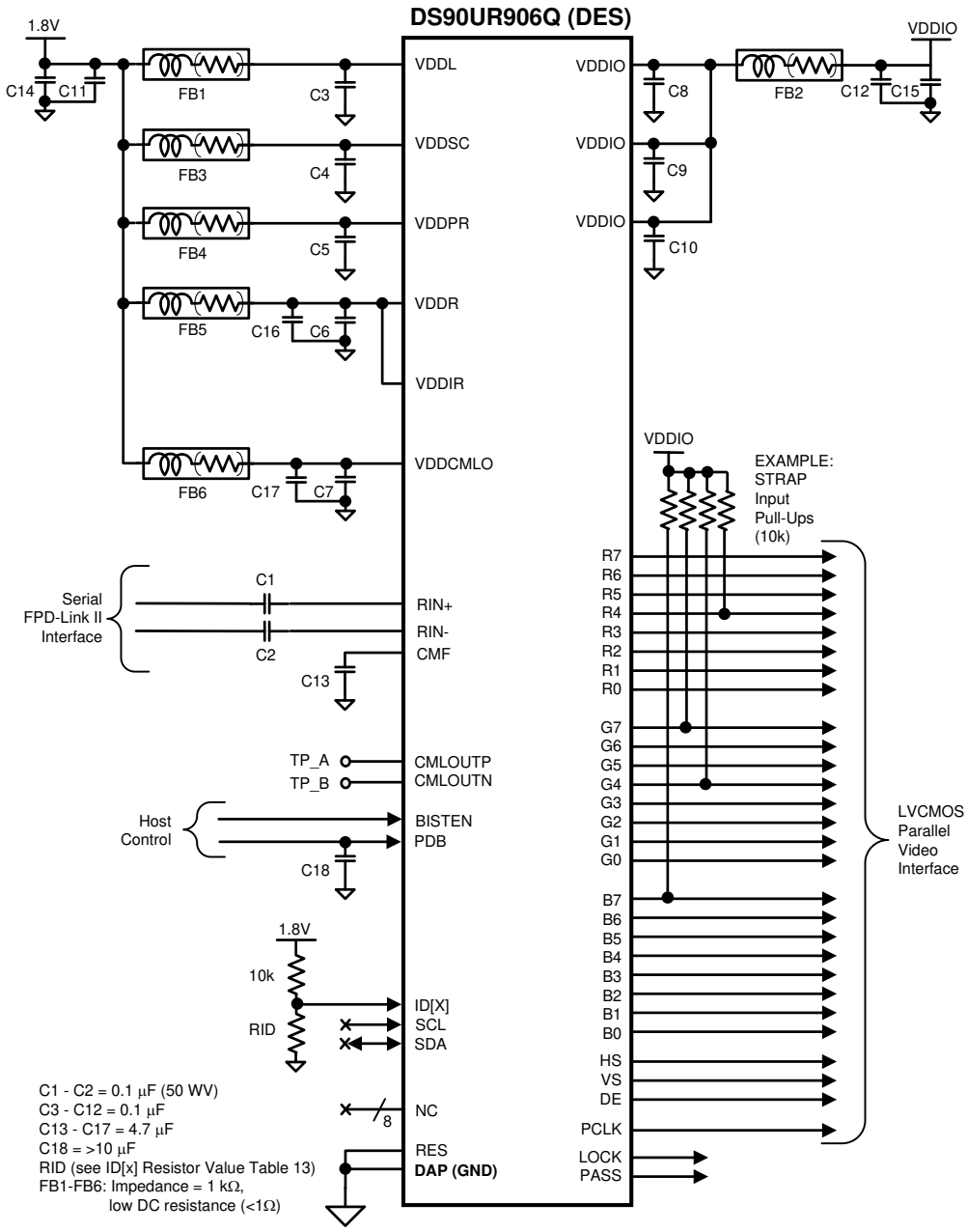


Figure 41. DS90UR906Q-Q1 Typical Connection Diagram — Pin Control

9.2.2.1 Design Requirements

For this example, use the parameters listed in Table 18.

Table 18. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
VDDIO	1.8 V to 3.3 V
VDDL, VDDSC, VDDPR, VDDR, VDDIR, VDDCMLO	1.8 V
AC-Coupling Capacitor for DOUT±	100 nF

9.2.2.2 Detailed Design Procedure

The RIN± input require 100-nF AC-coupling capacitors to the line. The power supply filter capacitors are placed near the power supply pins. A smaller capacitance capacitor should be located closer to the power supply pins.

The device has twenty-two Control and Configuration pins which are called STARTP pins. These pins include an internal pulldown. For a HIGH state, use a 10-KΩ resistor pulled up to VDDIO.

The PDB and BISTEN pins are assumed controlling by a microprocessor. The PDB has to be LOW state until all power supply voltages reach the final voltage. The SCL, SDA and ID[x] pins are left open when these Serial Bus Control pins are unused.

The RES pins and DAP should be tied to ground.

9.2.2.3 Application Curves

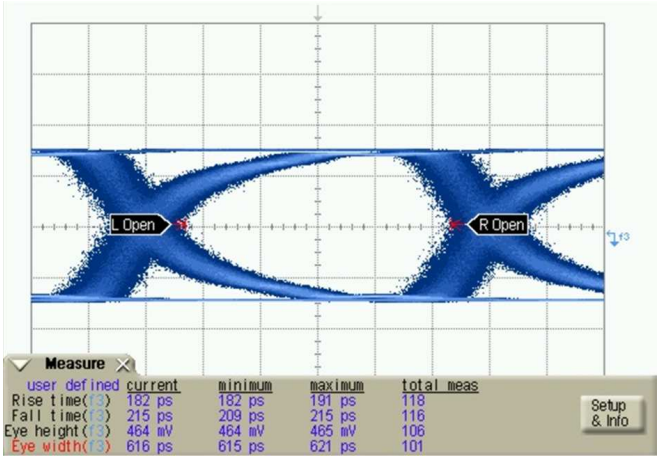


Figure 42. Eye Diagram at PCLK = 45 MHz

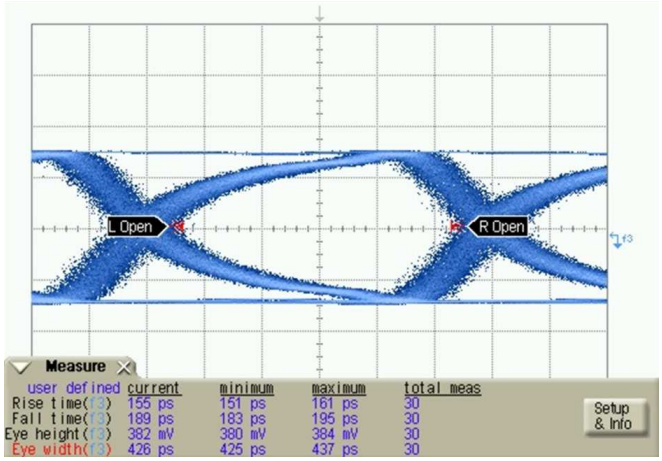


Figure 43. Eye Diagram at PCLK = 65 MHz

10 Power Supply Recommendations

10.1 Power Up Requirements and PDB Pin

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO}, it is recommended to use a 10-kΩ pullup and a > 10 µF capacitor to GND to delay the PDB input signal.

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2 µF to 10 µF range. Voltage rating of the tantalum capacitors should be at least 5× the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50 µF to 100 µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in *Leadless Leadframe Package (LLP) Application Report* (SNOA401).

11.1.1 Transmission Media

The serializer and deserializer chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The serializer and deserializer provide internal terminations providing a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

Layout Guidelines (continued)

11.1.2 LVDS Interconnect Guidelines

See AN-1108 *Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and AN-905 *Transmission Line RAPIDESIGNER Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S, 2S, 3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: www.ti.com/lvds

11.2 Layout Example

Figure 44 and Figure 45 show the PCB layout example derived from the layout design of the DS90UR905Q-Q1 and DS90UR906Q-Q1 Evaluation Boards. The graphic and layout description are used to determine both proper routing and proper solder techniques for designing the board.

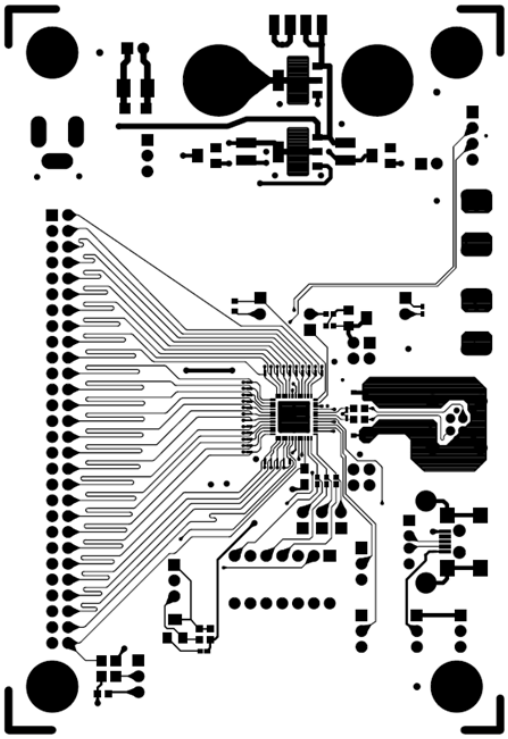


Figure 44. DS90UR905Q-Q1 Serializer Example Layout

Layout Example (continued)

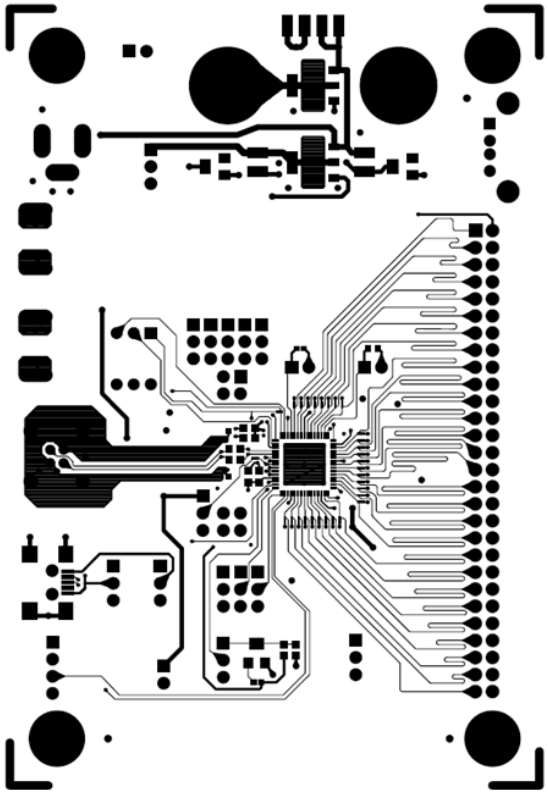


Figure 45. DS90UR906Q-Q1 Deserializer Example Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- AN-1108《*无引线框架封装 (LLP) 应用报告*》（文献编号：SNOA401）
- 《*通道链路 PCB 和互连设计指南*》（文献编号：SNLA008）
- 《AN-905 *传输线路 RAPIDESIGNER 操作和 应用 指南*》 (SNLA035)

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **19.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
DS90UR905Q-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DS90UR906Q-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UR905QSQ/NOPB	ACTIVE	WQFN	RHS	48	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR905QSQ	Samples
DS90UR905QSQE/NOPB	ACTIVE	WQFN	RHS	48	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR905QSQ	Samples
DS90UR905QSQX/NOPB	ACTIVE	WQFN	RHS	48	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR905QSQ	Samples
DS90UR906QSQ/NOPB	ACTIVE	WQFN	NKB	60	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR906QSQ	Samples
DS90UR906QSQE/NOPB	ACTIVE	WQFN	NKB	60	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR906QSQ	Samples
DS90UR906QSQX/NOPB	ACTIVE	WQFN	NKB	60	2000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR906QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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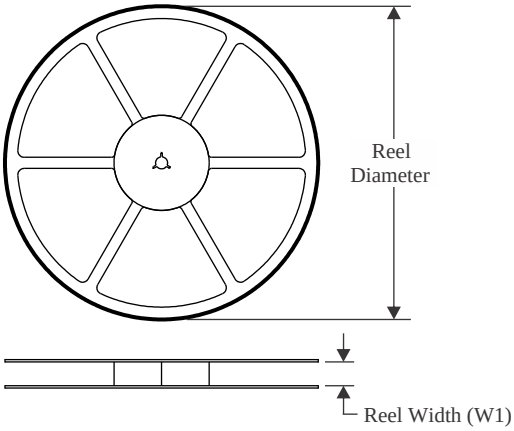
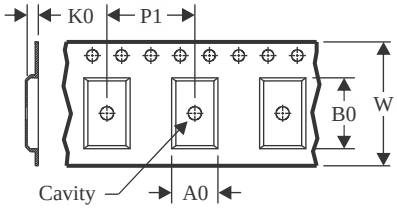
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

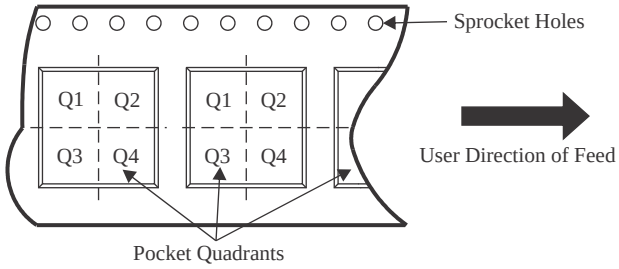


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

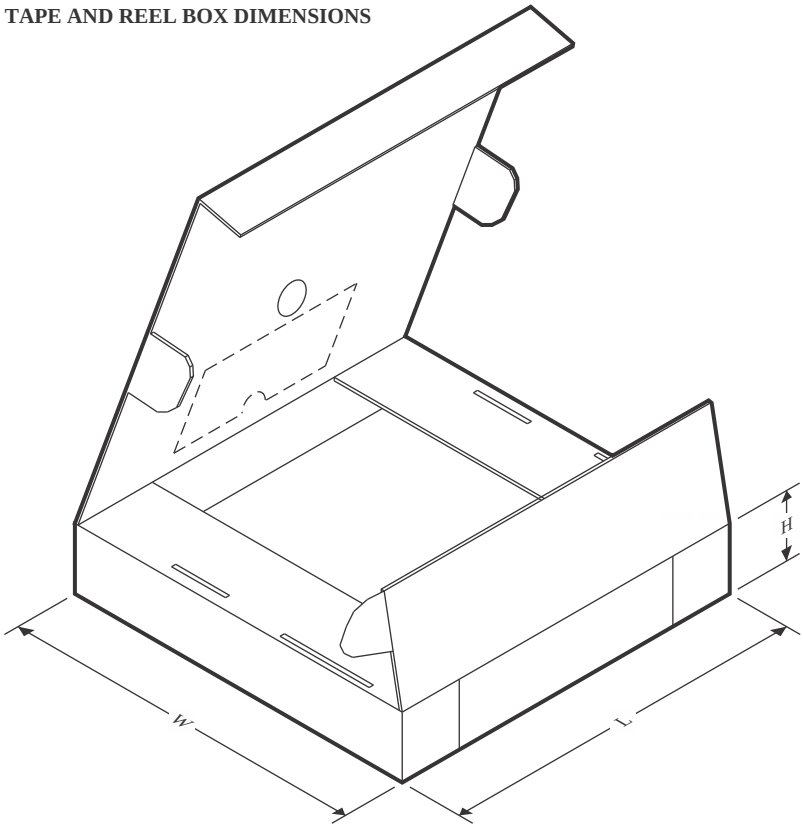
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UR905QSQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UR905QSQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UR905QSQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UR906QSQ/NOPB	WQFN	NKB	60	1000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UR906QSQE/NOPB	WQFN	NKB	60	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UR906QSQX/NOPB	WQFN	NKB	60	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

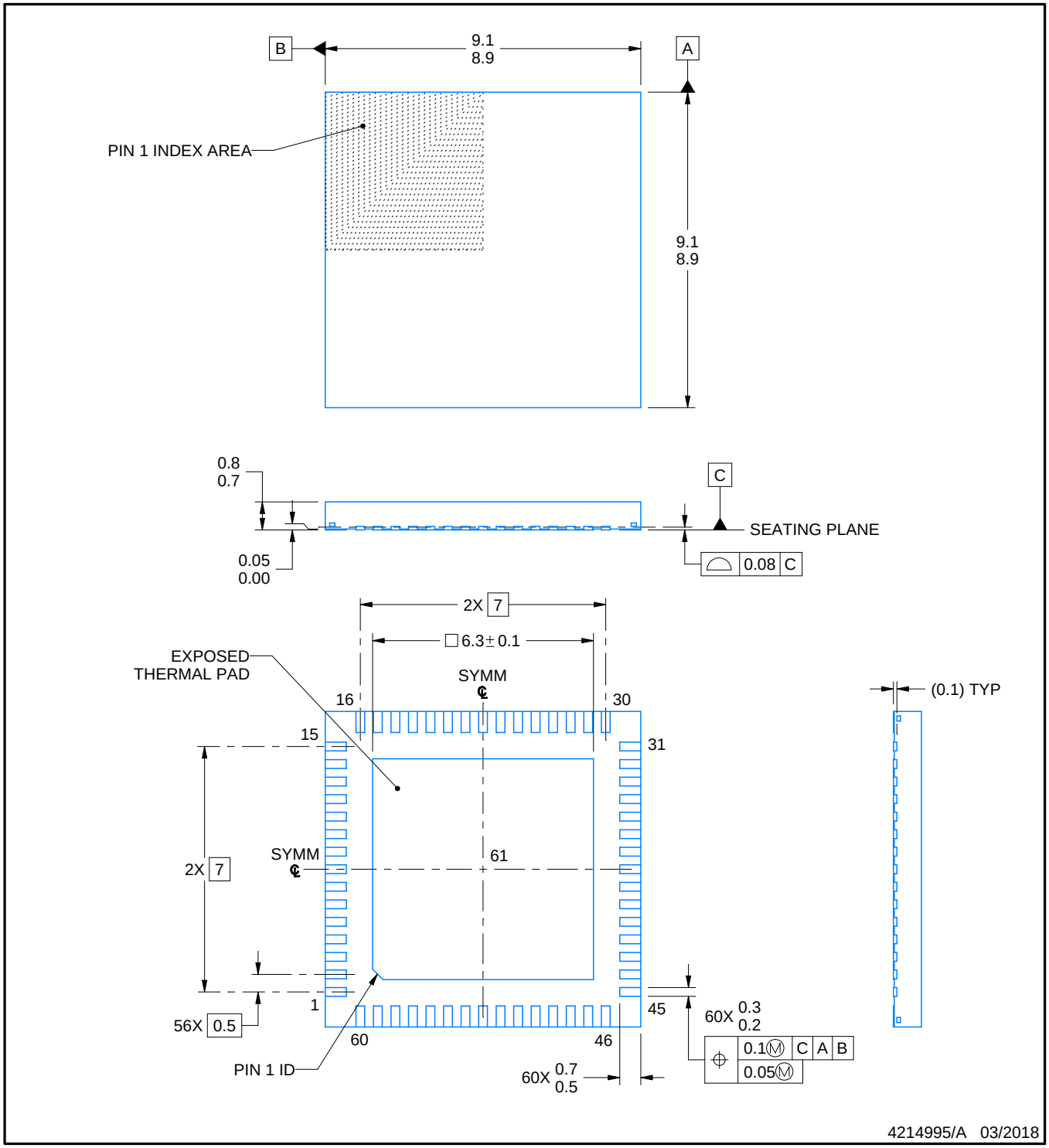
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UR905QSQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	35.0
DS90UR905QSQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS90UR905QSQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	35.0
DS90UR906QSQ/NOPB	WQFN	NKB	60	1000	356.0	356.0	35.0
DS90UR906QSQE/NOPB	WQFN	NKB	60	250	208.0	191.0	35.0
DS90UR906QSQX/NOPB	WQFN	NKB	60	2000	356.0	356.0	35.0

NKB0060B

PACKAGE OUTLINE

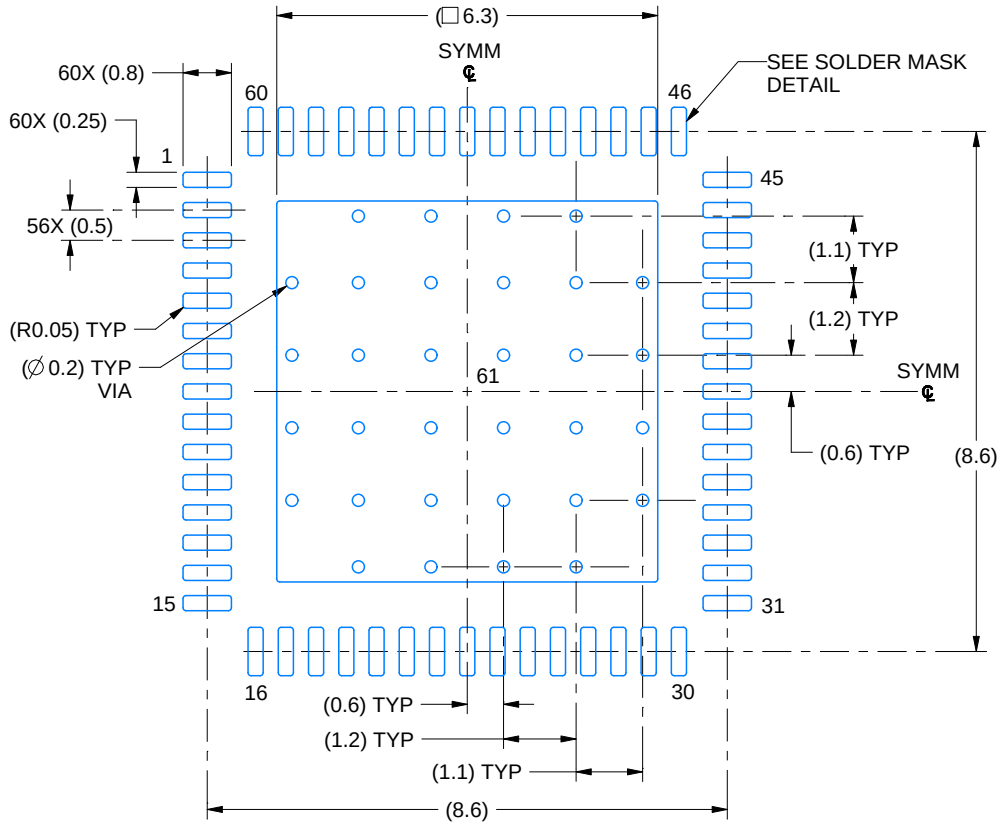
VQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

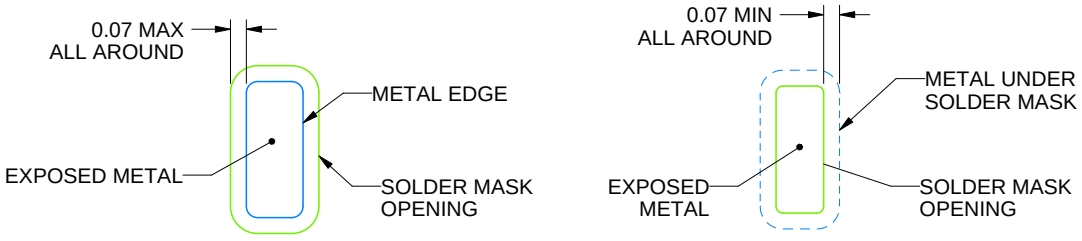


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

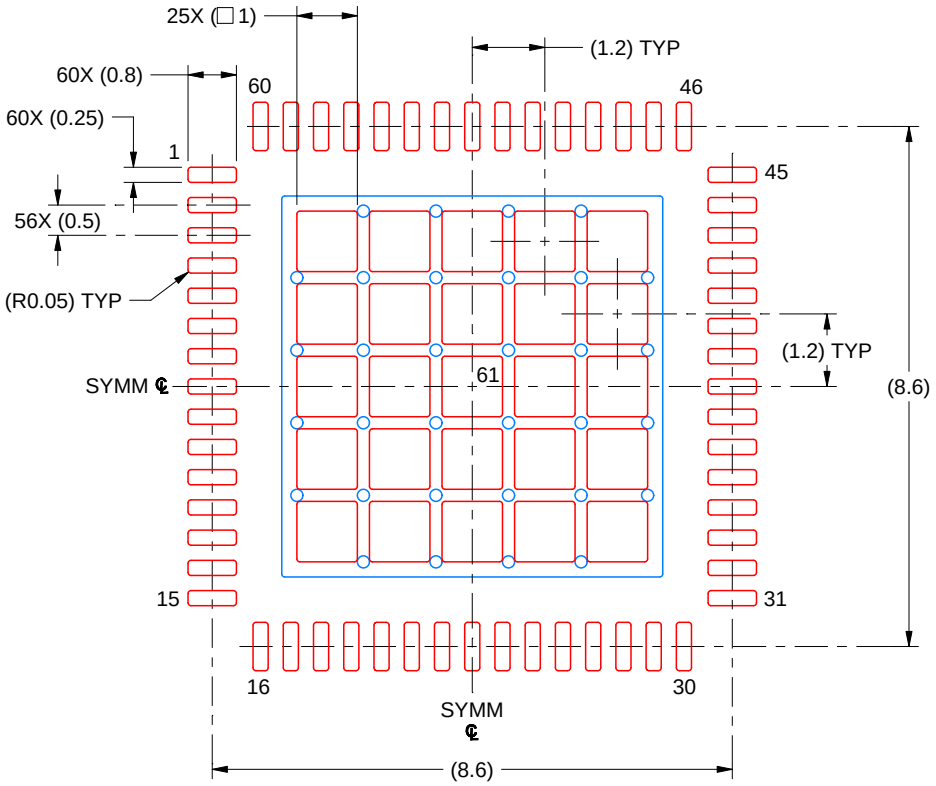


SOLDER MASK DETAILS

4214995/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

EXPOSED PAD 61
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4214995/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

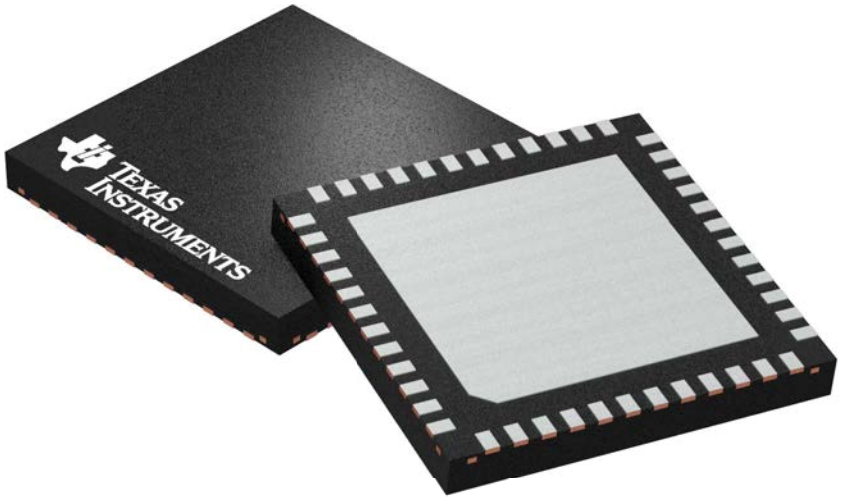
GENERIC PACKAGE VIEW

RHS 48

WQFN - 0.8 mm max height

7 x 7 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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