

SN74LV164A 8 位并行输出串行移位寄存器

1 特性

- V_{CC} 工作电压范围为 2V 至 5.5V
- 5V 时 t_{pd} 最大值为 10.5 ns
- V_{OLP} (输出接地反弹) 典型值
小于 0.8V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时)
- V_{OHV} (输出 V_{OH} 下冲) 典型值
大于 2.3V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时)
- I_{off} 支持带电插入、局部关断模式以及后驱动保护
- 所有端口上均支持以混合模式电压运行
- 闩锁性能超过 250mA, 符合 JESD 17 规范

2 应用

- IP 路由器
- 企业交换机
- 门禁和安全：门禁键盘和生物辨识
- 智能仪表：电力线通信

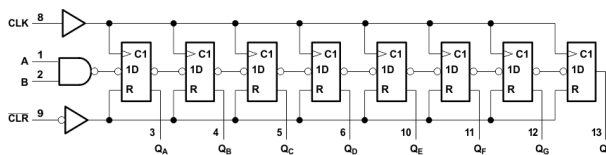
3 说明

SN74LV164A 器件是 8 位并行输出串行移位寄存器，专为 2V 至 5.5V V_{CC} 运行而设计。

封装信息⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV164A	D (SOIC, 14)	8.65 mm × 3.91 mm
	DB (SSOP, 14)	6.20 mm × 5.30 mm
	DGV (TVSOP, 14)	3.60 mm × 4.40 mm
	NS (SOP, 14)	10.30 mm × 5.30 mm
	PW (TSSOP, 14)	5.00 mm × 4.40 mm
	RGY (VQFN, 14)	3.50 mm × 3.50 mm
	BQA (WQFN, 14)	3.00 mm × 2.50 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

逻辑图 (正逻辑)



Table of Contents

1 特性	1	8 Detailed Description	11
2 应用	1	8.1 Overview.....	11
3 说明	1	8.2 Functional Block Diagram.....	11
4 Revision History	2	8.3 Feature Description.....	11
5 Pin Configuration and Functions	3	8.4 Device Functional Modes.....	11
6 Specifications	4	9 Application and Implementation	12
6.1 Absolute Maximum Ratings ⁽¹⁾	4	9.1 Application Information.....	12
6.2 ESD Ratings.....	4	9.2 Typical Application.....	12
6.3 Recommended Operating Conditions.....	5	10 Power Supply Recommendations	14
6.4 Thermal Information.....	5	11 Layout	15
6.5 Electrical Characteristics.....	6	11.1 Layout Guidelines.....	15
6.6 Timing Requirements: $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	6	11.2 Layout Example.....	15
6.7 Timing Requirements: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	12 Device and Documentation Support	16
6.8 Timing Requirements: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	7	12.1 接收文档更新通知.....	16
6.9 Switching Characteristics: $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	7	12.2 支持资源.....	16
6.10 Switching Characteristics: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	7	12.3 Trademarks.....	16
6.11 Switching Characteristics: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	12.4 Electrostatic Discharge Caution.....	16
6.12 Noise Characteristics ⁽¹⁾	8	12.5 术语表.....	16
6.13 Operating Characteristics.....	8	13 Mechanical, Packaging, and Orderable Information	16
6.14 Typical Characteristics.....	9		
7 Parameter Measurement Information	10		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (February 2015) to Revision J (December 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的格式.....	1

Changes from Revision H (April 2005) to Revision I (February 2015)	Page
• 添加了引脚配置和功能部分、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

5 Pin Configuration and Functions

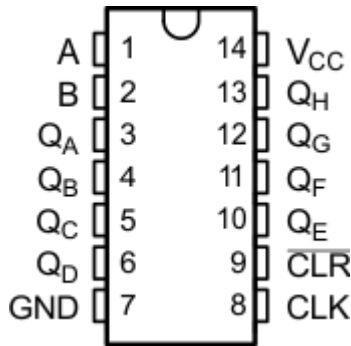


图 5-1. D, DB, DGV, NS, or PW Package 14-PIN SOIC, SSOP, TVSOP, SOP, or TSSOP Top View

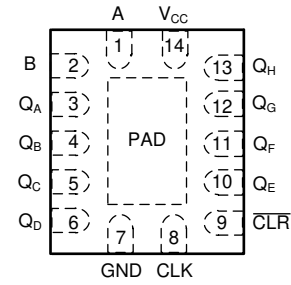


图 5-2. RGY or BQA Package 14-PIN VQFN or WQFN Top View

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	A	I	Serial input A
2	B	I	Serial input B
3	Q _A	O	Output A
4	Q _B	O	Output B
5	Q _C	O	Output C
6	Q _D	O	Output D
7	GND	—	Ground pin
8	CLK	I	Storage clock
9	$\overline{\text{CLR}}$	I	Storage clear
10	Q _E	O	Output E
11	Q _F	O	Output F
12	Q _G	O	Output G
13	Q _H	O	Output H
11	Q _H '	O	Q _H inverted
14	V _{CC}	—	Power pin
-	PAD	—	Thermal Pad ⁽²⁾

(1) I = input, O = output

(2) RGY and BQA packages only

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
V _I	Input voltage ⁽²⁾	-0.5	7	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V _O	Output voltage ⁽²⁾ ⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-20 mA
I _{OK}	Output clamp current	V _O < 0		-50 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25 mA
	Continuous current through V _{CC} or GND			±50 mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74LV164A		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	μA
		V _{CC} = 2.3 V to 2.7 V	-2	mA
		V _{CC} = 3 V to 3.6 V	-6	
		V _{CC} = 4.5 V to 5.5 V	-12	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 2.3 V to 2.7 V	2	mA
		V _{CC} = 3 V to 3.6 V	6	
		V _{CC} = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200	ns/V
		V _{CC} = 3 V to 3.6 V	100	
		V _{CC} = 4.5 V to 5.5 V	20	
T _A	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV164A						UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	92.6	104.4	126.7	89.3	120.2	54.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	53.9	57	50	46.9	48.9	67	
R _{θJB}	Junction-to-board thermal resistance	46.8	51.7	59.6	48	61.9	30.5	
ψ _{JT}	Junction-to-top characterization parameter	18.9	18.6	5.8	13.7	5.7	2.3	
ψ _{JB}	Junction-to-board characterization parameter	46.6	51.2	58.9	47.7	61.3	30.5	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	11.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LV164A –40°C to 85°C			SN74LV164A –40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V				0.1			V
	I _{OL} = 2 mA	2.3 V				0.4			
	I _{OL} = 6 mA	3 V				0.44			
	I _{OL} = 12 mA	4.5 V				0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V				±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5				20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0				5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.2			2.2			pF

6.6 Timing Requirements: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

			T _A = 25°C		SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CL _R low	6		6.5		6.5		ns
		CLK high or low	6.5		7.5		7.5		
t _{su}	Setup time	Data before CLK↑	6.5		8.5		8.5		ns
		CL _R inactive	3		3		3		
t _h	Hold time	Data after CLK↑	–0.5		0		0		ns

6.7 Timing Requirements: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			T _A = 25°C		SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CL _R low	5		5		5		ns
		CLK high or low	5		5		5		
t _{su}	Setup time	Data before CLK↑	5		6		6		ns
		CL _R inactive	2.5		2.5		2.5		
t _h	Hold time	Data after CLK↑	0		0		0		ns

6.8 Timing Requirements: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

			$T_A = 25^\circ\text{C}$		SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time	Data before CLK \uparrow	4.5		4.5		4.5		ns
		$\overline{\text{CLR}}$ inactive	2.5		2.5		2.5		
t_h	Hold time	Data after CLK \uparrow	1		1		1		ns

6.9 Switching Characteristics: $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	55 ⁽¹⁾	105 ⁽¹⁾		50		50		MHz
			$C_L = 50\text{ pF}$	45	85		40		40		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$		9.2 ⁽¹⁾	17.6 ⁽¹⁾	1	20	1	21	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			8.6 ⁽¹⁾	16 ⁽¹⁾	1	18	1	18.5	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$		11.5	21.1	1	24	1	25	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			10.8	19.5	1	22	1	22.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Switching Characteristics: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	80 ⁽¹⁾	155 ⁽¹⁾		65		65		MHz
			$C_L = 50\text{ pF}$	50	120		45		45		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$		6.4 ⁽¹⁾	12.8 ⁽¹⁾	1	15	1	16	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			6 ⁽¹⁾	12.8 ⁽¹⁾	1	15	1	16	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$		8.3	16.3	1	18.5	1	19.5	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			7.9	16.3	1	18.5	1	19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.11 Switching Characteristics: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	125 ⁽¹⁾	220 ⁽¹⁾		105		95		MHz
			$C_L = 50\text{ pF}$	85	165		75		65		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$		4.5 ⁽¹⁾	9 ⁽¹⁾	1	10.5	1	11.5	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			4.2 ⁽¹⁾	8.6 ⁽¹⁾	1	10	1	11	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$		6	11	1	12.5	1	13	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			5.8	10.6	1	12.5	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.12 Noise Characteristics⁽¹⁾

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		SN74LV164A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.28	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.22	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.09		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$	$f = 10\text{ MHz}$	3.3 V	48.1	pF
				5 V	47.5	

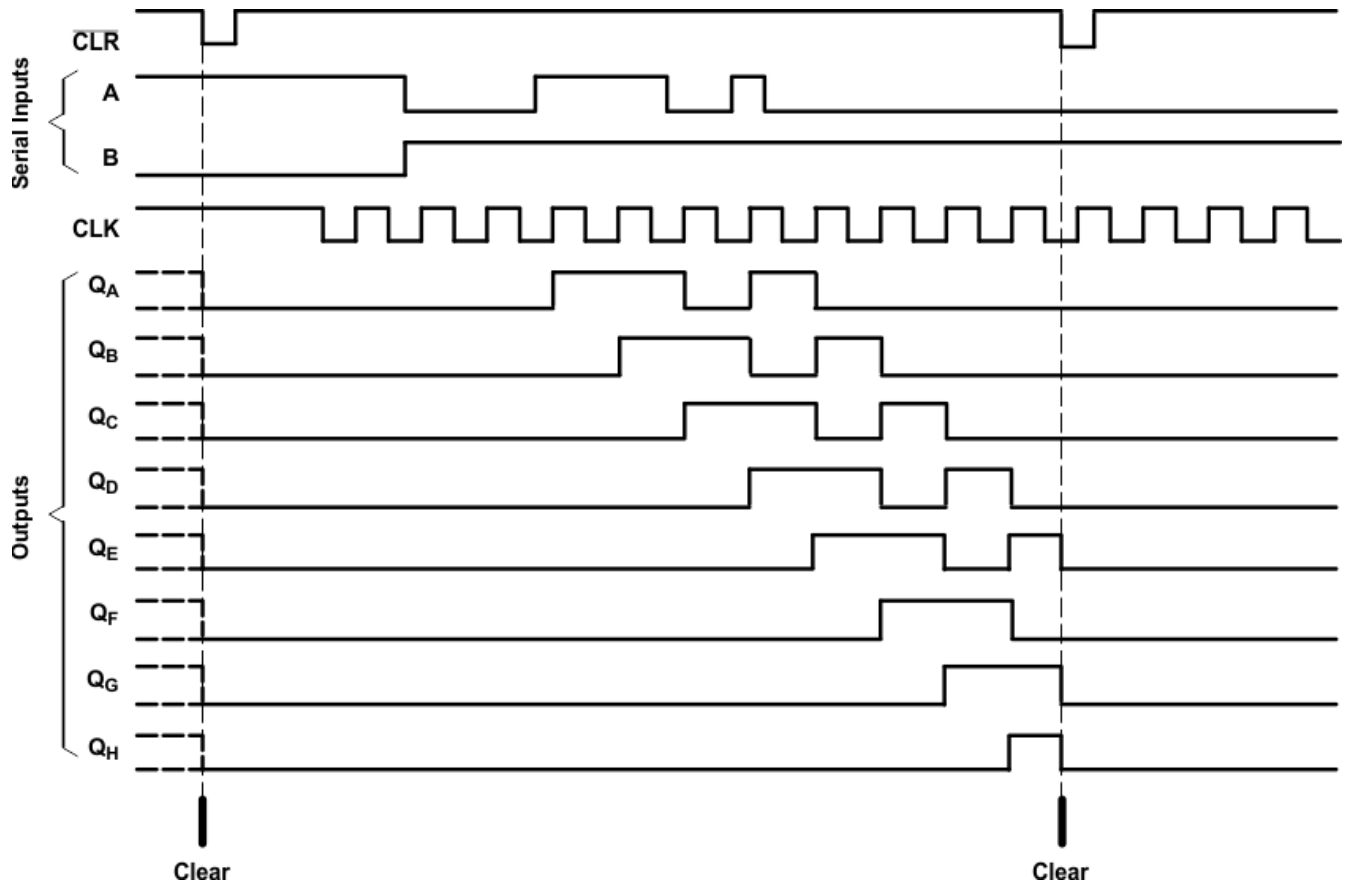


图 6-1. Typical Clear, Shift, and Clear Sequences

6.14 Typical Characteristics

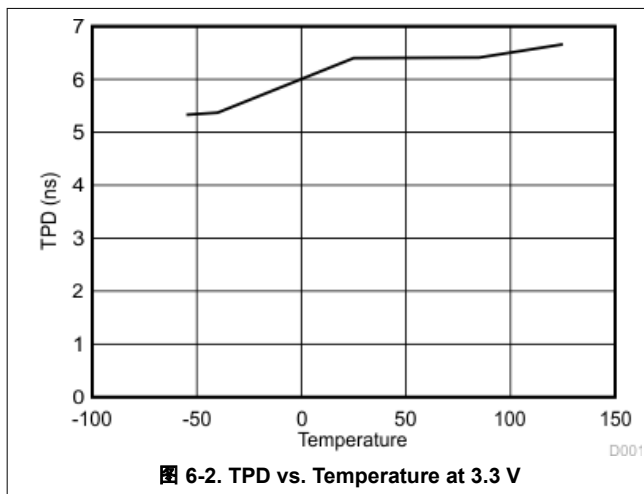


图 6-2. TPD vs. Temperature at 3.3 V

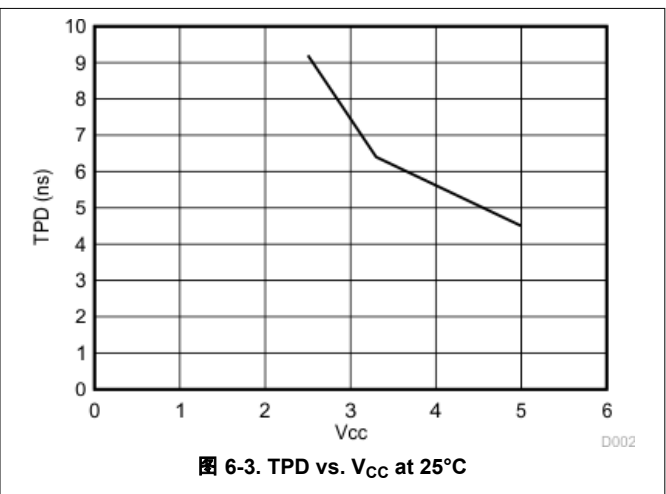
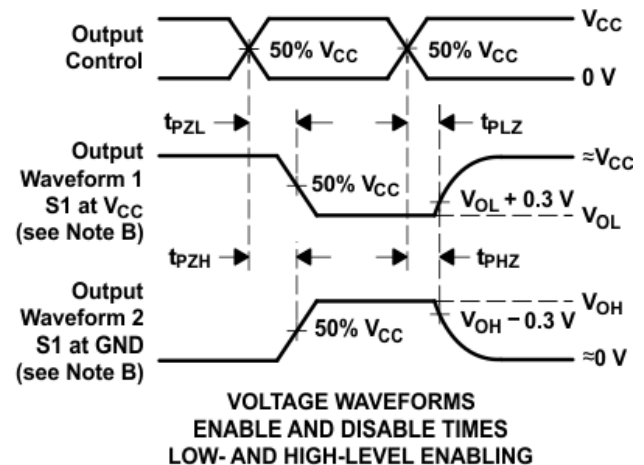
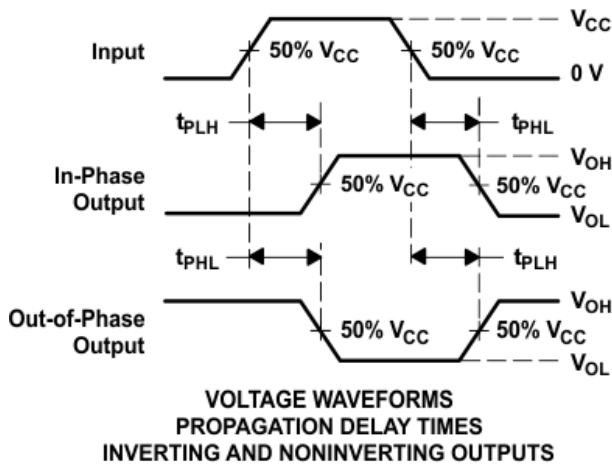
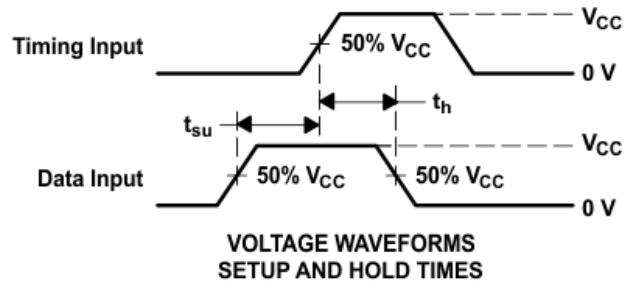
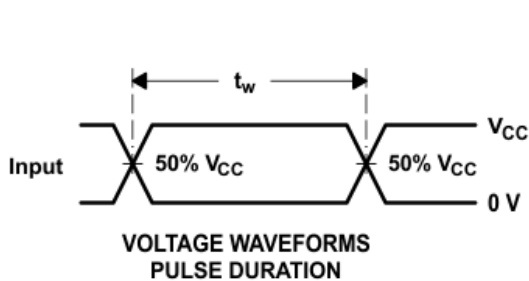
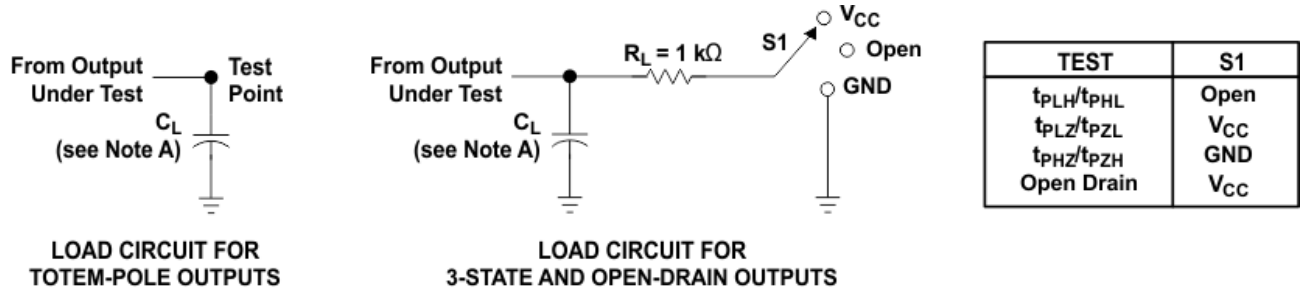


图 6-3. TPD vs. V_{CC} at 25°C

7 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

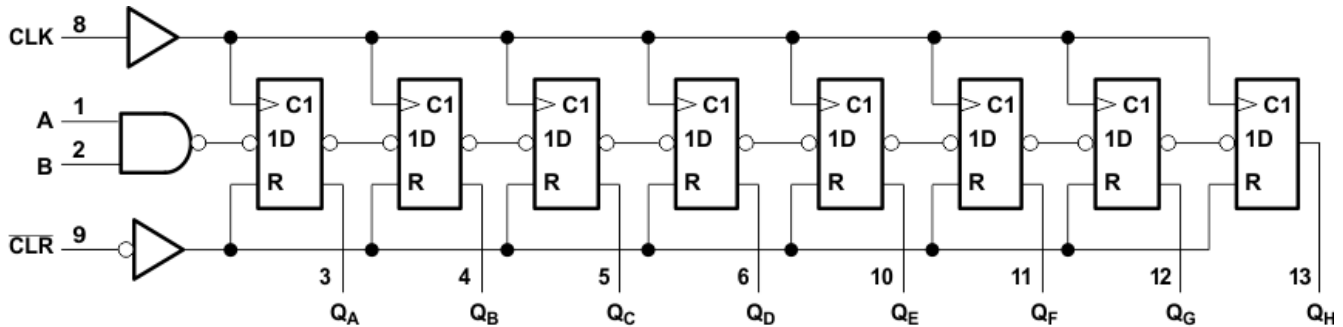
8 Detailed Description

8.1 Overview

The SNx4LV164A devices are 8-bit parallel-out serial shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices feature NAND-gated serial (A and B) inputs and an asynchronous clear (\overline{CLR}) input. The gated serial inputs permit complete control over incoming data, as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The wide operating range allows the device to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

表 8-1. Function Table⁽¹⁾⁽²⁾

INPUTS				OUTPUTS			
CLR	CLK	A	B	Q _A	Q _B	...	Q _H
L	X	X	X	L	L		L
H	L	X	X	Q _{A0}	Q _{B0}		Q _{H0}
H	↑	H	H	H	Q _{An}		Q _{Gn}
H	↑	L	X	L	Q _{An}		Q _{Gn}
H	↑	X	L	L	Q _{An}		Q _{Gn}

- (1) Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
- (2) Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a 1-bit shift.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN74LV164A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

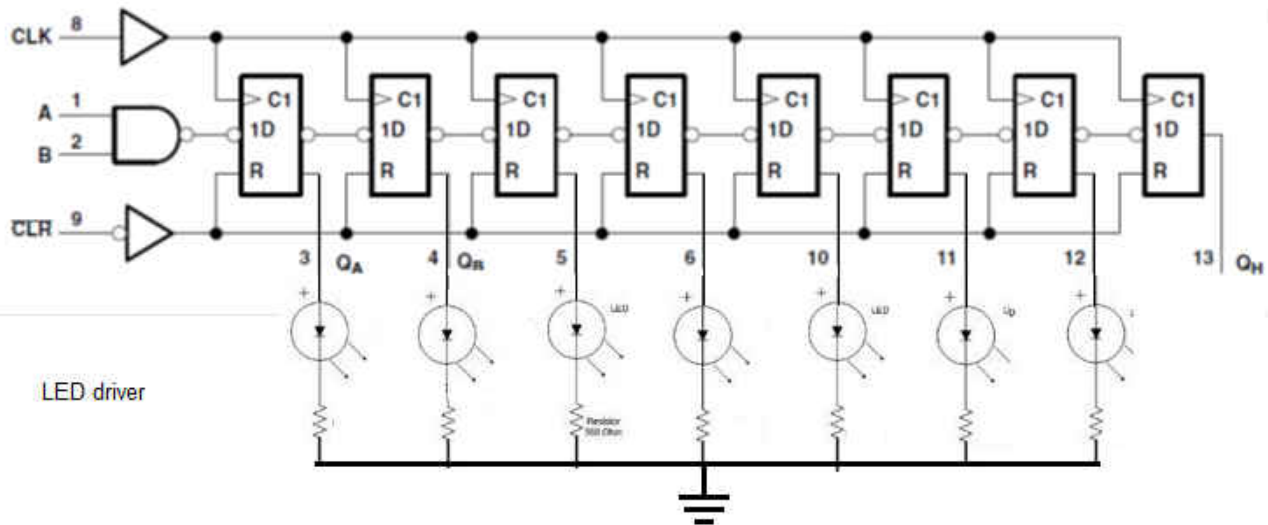


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in [# 6.3](#).
 - Specified high and low level. See $(V_{IH}$ and $V_{IL})$ in [# 6.3](#).
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended output conditions:
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves

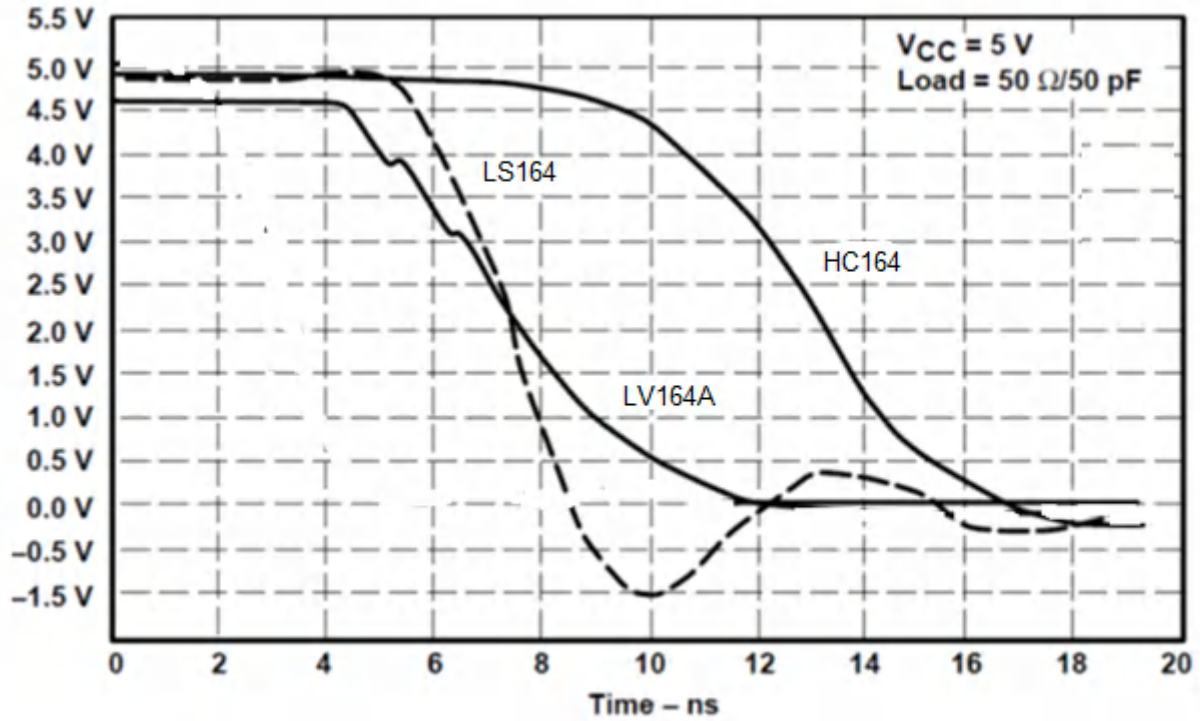


图 9-2. Switching Characteristics Comparison

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [# 6.3](#). Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01- μF or 0.022- μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

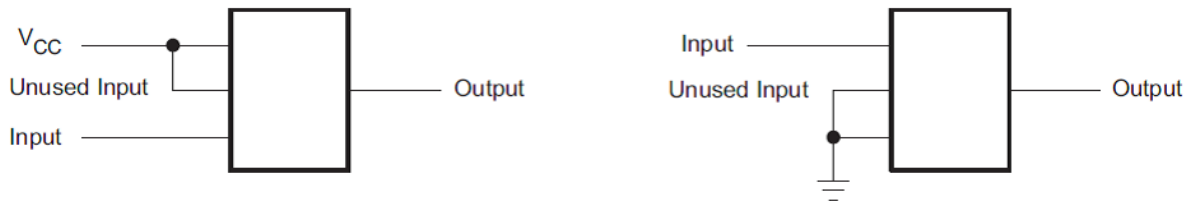


图 11-1. Layout Example

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV164ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVA164	Samples
SN74LV164AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV164A	Samples
SN74LV164APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV164A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV164A :

- Automotive : [SN74LV164A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV164ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LV164ADBDR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV164ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV164ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV164ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV164APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV164APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV164ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV164ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LV164ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV164ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV164ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV164ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV164APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV164APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LV164ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV164AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LV164APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LV164APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

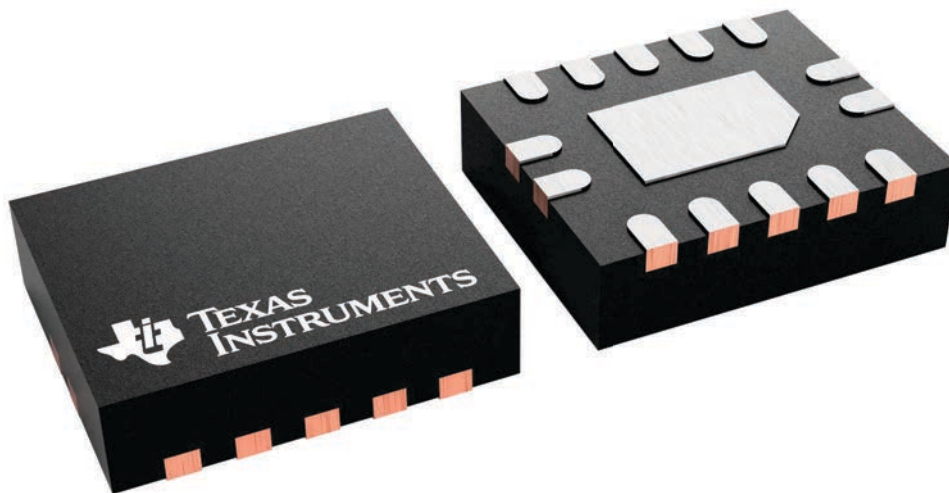
BQA 14

WQFN - 0.8 mm max height

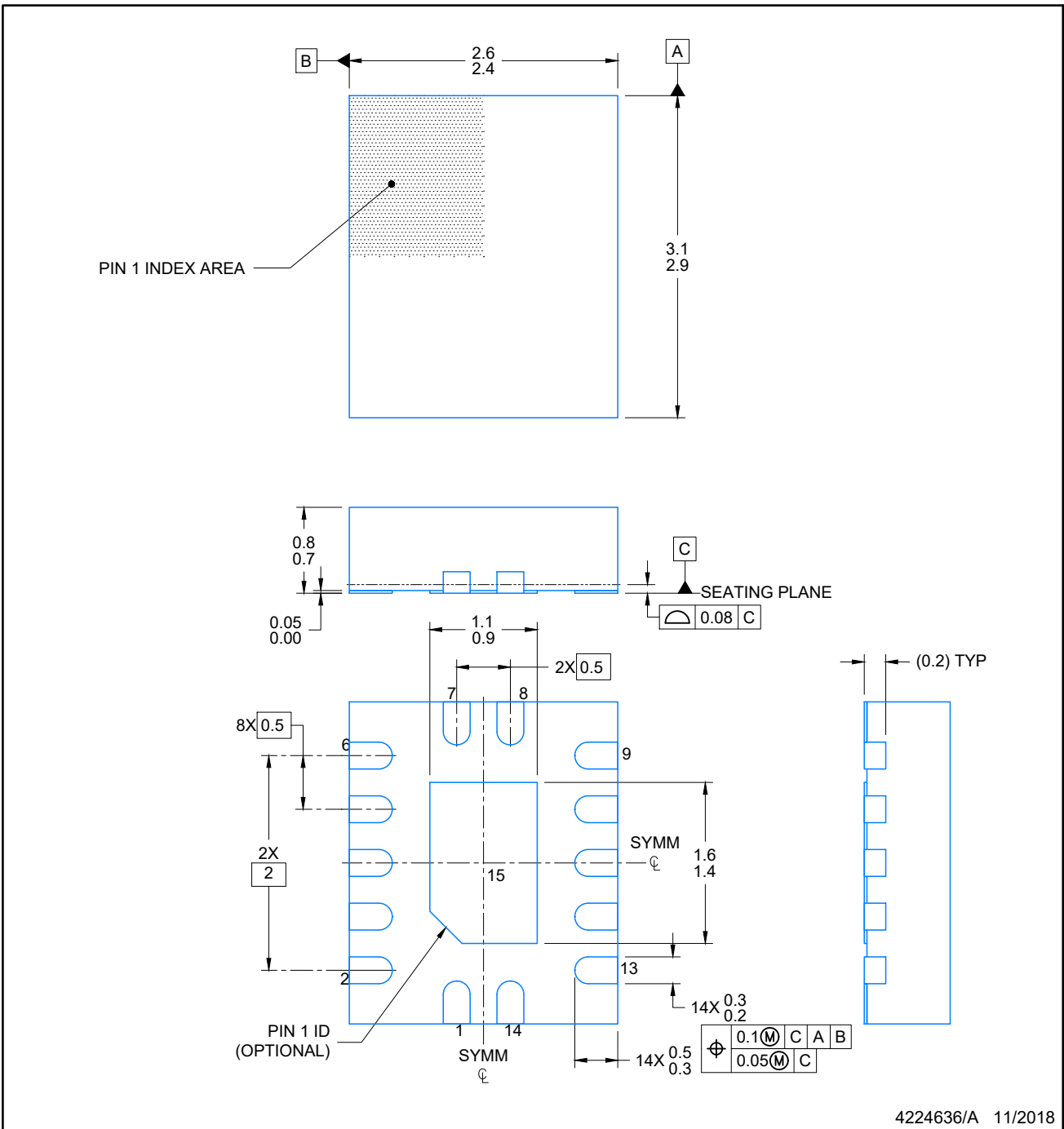
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

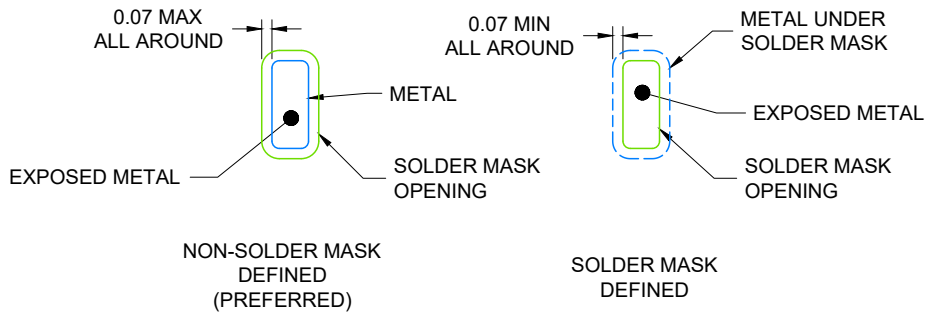
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司