低功耗三通道和四通道数字隔离器

查询样品: ISO7631FM, ISO7631FC, ISO7641FC

特性

- 信号发送速率：**150Mbps**（**M** 级），**25Mbps**（**C** 级）
- 具有集成噪声滤波器（**C** 级）的稳健设计
- 低功耗、每通道典型 I_{CC}（**3.3V** 电源）：
  - **ISO7631FM**：在 **10Mbps** 时为 **2mA**
  - **ISO7631FC**：**10Mbps** 时为 **1.5mA**
  - **ISO7641FC**：在 **10Mbps** 时为 **1.3 mA**
- 极低的 $I_{CC\_disable}$（**C** 级）
- 低传播延迟：典型值为 **7ns**（**M** 级）
- 在故障安全模式下输出默认为低电平状态
- 宽温度范围：**-40°C** 至 **125°C**
- **50KV/μs** 典型瞬态抗扰度
- 使用 SiO_2 绝缘隔栅实现长使用寿命
- 在 **2.7V**（**M** 级），**3.3V** 和 **5V** 电源和逻辑电平下运行
- 宽体小外形尺寸集成电路 **(SOIC)-16** 封装

应用范围

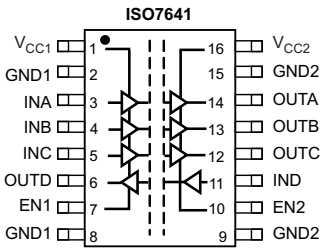
- 是下列应用中光耦合器的替代产品：
  - 工业现场总线 **(Fieldbus)**
    - **Profibus** 现场总线
    - **Modbus** 串行通信协议
    - **DeviceNet**™ 数据总线
  - 伺服器控制接口
  - 电机控制
  - 电源
  - 电池组

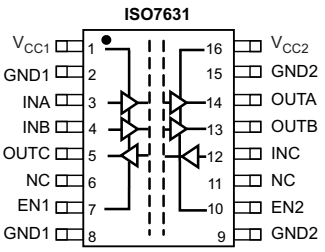
安全及管理批准

- 符合 **UL1577** 的 **1** 分钟 **2500** V_{RMS}（已批准）
- 针对 **DIN EN 60747-5-2**（**VDE 0884** 修订版本 **2**）标准的 **4242** V_{PK}**VDE** 额定值，**1414** V_{PK}工作电压（已批准）
- **CSA** 组件接受通知 **5A**（已批准）
- 针对 **EN/UL/CSA 60950-1** 和 **EN/UL/CSA 61010-1**（已获批准）符合 **TUV** 标准的 **3000** V_{RMS} 增强隔离

说明

ISO7631F 和 ISO7641F 提供符合 VDE 规范的高达 4242 V_{PK} 的电流隔离。 ISO7631F 具有 3 个通道，其中 2 个正向和 1 个反向通道，而 ISO7641F 具有 4 个通道，其中 3 个正向通道和 1 个反向通道。 后缀 F 说明在故障安全情况下输出默认为低电平状态（参见 Table 1）。 M 级器件是具有快速传播延迟且数据速率可达 150Mbps 的高速隔离器，而 C 级器件在低功耗下的数据速率可高达 25Mbps 且具有针对易于产生噪音应用的集成滤波器。 建议将 C 级器件用于低速应用，在此类应用中需要抑制持续时间少于 6ns 的输入噪声脉冲或者应用中的低功耗十分重要。





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

说明（继续）

每个隔离通道都有一个由二氧化硅 (SiO_2) 绝缘隔栅分开的逻辑输入和输出缓冲器。 与隔离电源配合使用，这些器件可防止数据总线或者其它电路上的噪声电流进入本地接地或者干扰或损坏敏感电路。 此器件具有 TTL 输入阈值并可在 2.7V（M 级），3.3V 和 5V 电源供电的情况下运行。 当由 3.3V 或者 2.7V 电源供电时，所有输入均可耐受 5V 电压。

PIN DESCRIPTIONS

PIN			I/O	DESCRIPTION
NAME	ISO7641	ISO7631		
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
IND	11	-	I	Input, channel D
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	5	O	Output, channel C
OUTD	6	-	O	Output, channel D
EN1	7	7	I	Enables (when input is High or Open) or Disables (when input is Low) OUTD of ISO7641 and OUTC of ISO7631
EN2	10	10	I	Enables (when input is High or Open) or Disables (when input is Low) OUTA, OUTB, and OUTC of ISO7641 Enables (when input is High or Open) or Disables (when input is Low) OUTA and OUTB of ISO7631
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	–	Power supply, V_{CC2}
GND1	2,8	2,8	–	Ground connection for V_{CC1}
GND2	9,15	9,15	–	Ground connection for V_{CC2}
NC	-	6,11	-	No Connect pins are floating with no internal connection

Table 1. FUNCTION TABLE(1)

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	L
PD	PU	X	H or Open	L
PD	PU	X	L	Z
PU	PD	X	X	Undetermined

(1) PU = Powered Up(V_{CC} ≥ 2.7 V); PD = Powered Down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	PACKAGE	INPUT THRESHOLD	DATA RATE and FILTER	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7631FM	4242 V_{PK} / 2500 V_{RMS} (1)	DW-16	1.5 V TTL (CMOS Compatible)	150 Mbps, No Noise Filter	2 Forward, 1 Reverse	ISO7631FM	ISO7631FMDW (rail)
							ISO7631FMDWR (reel)
ISO7631FC				25 Mbps, Integrated Noise Filter	2 Forward, 1 Reverse	ISO7631FC	ISO7631FCDW (rail)
							ISO7631FCDWR (reel)
ISO7641FC					3 Forward, 1 Reverse	ISO7641FC	ISO7641FCDW (rail)
							ISO7641FCDWR (reel)

(1) See the Regulatory Information table for detailed isolation ratings.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER				VALUE		UNIT
				MIN	MAX	
Supply voltage(2)	V_{CC1}, V_{CC2}			–0.5	6	V
Voltage	INx, OUTx, ENx			–0.5	6	V
Output Current, I_O					±15	mA
Electrostatic discharge	Human Body Model	ESDA, JEDEC JS-001-2012	All pins		±4	kV
	Field-Induced Charged Device Model	JEDEC JESD22-C101E			±1.5	kV
	Machine Model	JEDEC JESD22-A115-A			±200	V
Maximum junction temperature, T_J					150	°C
Storage temperature, T_{STG}				-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			MIN	TYP	MAX	UNIT
Supply voltage	V_{CC1}, V_{CC2}	M-Grade	2.7		5.5	V
		C-Grade	3		5.5	
High-level output current	I_{OH}		-4			mA
Low-level output current	I_{OL}				4	mA
High-level input voltage	V_{IH}		2		V_{CC}	V
Low-level input voltage	V_{IL}		0		0.8	V
Input pulse duration	t_{ui}	M-Grade: ≥3V-Operation	6.67			ns
		M-Grade: <3V-Operation	10			
		C-Grade: ≥3V-Operation	40			
Signaling rate	1 / t_{ui}	M-Grade: ≥3V-Operation	0		150	Mbps
		M-Grade: <3V-Operation	0		100	
		C-Grade: ≥3V-Operation	0		25	
Junction temperature	T_J		-40		136	°C
Ambient temperature	T_A		-40	25	125	°C

THERMAL INFORMATION

THERMAL METRIC(1)			ISO76xx	UNITS
			DW (16 Pins)	
θ_{JA}	Junction-to-ambient thermal resistance		72	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance		38	
θ_{JB}	Junction-to-board thermal resistance		39	
ψ_{JT}	Junction-to-top characterization parameter		9.4	
ψ_{JB}	Junction-to-board characterization parameter		n/a	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance		n/a	
P_D	Maximum Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF Input a 75 MHz 50% duty cycle square wave	399	mW

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：ZHCA543）。

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CCx} (1) – 0.8	4.8		V_{CCx} (1) – 0.8	4.7		V
		I_{OH} = –20 µA; see Figure 1	V_{CCx} (1) – 0.1	5		V_{CCx} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4		0.3	0.5	V
		I_{OL} = 20 µA; see Figure 1		0	0.1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450			450		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	75		25	75		kV/µs

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	3.5	7	10.5	11	17	28	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2			3	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2			3	
		Opposite-direction Channels			3			4	
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5			13	
t_r	Output signal rise time	See Figure 1		1.6			2.8		ns
t_f	Output signal fall time			1			2.9		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		5	16		8	20	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			5	16		7	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			4	16		11000	22000 (4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			4	16		8	20	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5			9		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

SUPPLY CURRENT

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F			**M-Grade**			**C-Grade**			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.5	4		1.1	1.9	mA
I_{CC2}				3.7	5.4		1.5	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.6	4.1		1.8	2.7	
I_{CC2}				3.8	5.5		2.6	3.9	
I_{CC1}	10 Mbps			3.3	4.5		2.7	3.7	
I_{CC2}				4.9	6.6		3.9	5.3	
I_{CC1}	25 Mbps			4.5	6		4.1	5.4	
I_{CC2}				6.8	9		5.9	7.8	
I_{CC1}	150 Mbps			15	19.5	Not Applicable			
I_{CC2}				22	30				
ISO7641F						**C-Grade**			
I_{CC1}	Disable	EN1 = EN2 = 0 V					1.2	2.1	mA
I_{CC2}							1.6	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					1.8	2.8	
I_{CC2}							3.1	4.2	
I_{CC1}	10 Mbps						3	4	
I_{CC2}							4.9	6.1	
I_{CC1}	25 Mbps						4.8	6	
I_{CC2}							7.7	9.5	

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7641F				M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.8	4.8		V_{CC1} – 0.8	4.7		V
			OUTx on V_{CC2} (3.3V) side	V_{CC2} - 0.4	3		V_{CC2} - 0.6	2.9		
		I_{OH} = –20 µA; see Figure 1	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.1	5		V_{CC1} – 0.1	5		
			OUTx on V_{CC2} (3.3V) side	V_{CC2} – 0.1	3.3		V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1			0.2	0.4		0.3	0.5	V
		I_{OL} = 20 µA; see Figure 1			0	0.1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430			430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4		25	50		25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	8	13	11	18	32	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2			3.5	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2.5			4.5	
		Opposite-direction Channels			3.5			5.5	
$t_{sk(pp)}$(3)	Part-to-part skew time				6			15	
t_r	Output signal rise time	See Figure 1		2			3.6		ns
t_f	Output signal fall time			1.2			3.3		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		6.5	17		9	20	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			6.5	17		8	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			5.5	17		11000	22000(4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			5.5	17		10	30	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5			8.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

SUPPLY CURRENT

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			C-Grade			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.5	4		1.1	1.9	mA
I_{CC2}				2.7	3.7		0.7	1.3	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.6	4.1		1.8	2.7	
I_{CC2}				2.8	3.8		1.8	2.6	
I_{CC1}	10 Mbps			3.3	4.5		2.7	3.7	
I_{CC2}				3.5	4.6		2.6	3.5	
I_{CC1}	25 Mbps			4.5	6		4.1	5.4	
I_{CC2}				4.7	5.9		3.8	5	
I_{CC1}	150 Mbps			15	19.5	Not Applicable			
I_{CC2}				14.6	19				
ISO7641F						**C-Grade**			
I_{CC1}	Disable	EN1 = EN2 = 0 V					1.2	2.1	mA
I_{CC2}							0.8	1.3	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					1.8	2.8	
I_{CC2}							2	2.9	
I_{CC1}	10 Mbps						3	4	
I_{CC2}							3.2	4.1	
I_{CC1}	25 Mbps						4.8	6	
I_{CC2}							5.1	7	

ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3V ± 10% and V_{CC2} at 5V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7641F				M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.4	3		V_{CC1}-0.6	2.9		V
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.8	4.8		V_{CC2}–0.8	4.7		
		I_{OH} = –20 µA; see Figure 1	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.1	3.3		V_{CC1}–0.1	3.3		
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.1	5		V_{CC2}–0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1			0.2	0.4		0.3	0.5	V
		I_{OL} = 20 µA; see Figure 1			0	0.1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430			430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4		25	50		25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3 V ± 10% and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	7.5	12.5	11	18.5	32	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2			2.5	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2.5			4.5	
		Opposite-direction Channels			3.5			5.5	
$t_{sk(pp)}$(3)	Part-to-part skew time				6			15	
t_r	Output signal rise time	See Figure 1		1.7			2.9		ns
t_f	Output signal fall time			1.1			2.9		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		5.5	17		8	20	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			5.5	17		7	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			4.5	17		11000	22000(4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			4.5	17		8	30	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5			7.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

SUPPLY CURRENT

V_{CC1} at 3.3V ± 10% and V_{CC2} at 5V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F			**M-Grade**			**C-Grade**			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.8	2.8		0.6	1.1	mA
I_{CC2}				3.7	5.4		1.5	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.9	2.9		1.2	1.8	
I_{CC2}				3.8	5.5		2.6	3.9	
I_{CC1}	10 Mbps			2.4	3.4		1.8	2.6	
I_{CC2}				4.9	6.6		3.9	5.3	
I_{CC1}	25 Mbps			3.2	4.2		2.7	3.6	
I_{CC2}				6.8	9		5.9	7.8	
I_{CC1}	150 Mbps			9.3	12.5	Not Applicable			
I_{CC2}				22	30				
ISO7641F						**C-Grade**			
I_{CC1}	Disable	EN1 = EN2 = 0 V					0.7	1.1	mA
I_{CC2}							1.6	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					1.2	1.9	
I_{CC2}							3.1	4.2	
I_{CC1}	10 Mbps						2	2.8	
I_{CC2}							4.9	6.1	
I_{CC1}	25 Mbps						3.1	4	
I_{CC2}							7.7	9.5	

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CCx}(1) – 0.4	3		V_{CCx}(1) – 0.6	2.9		V
		I_{OH} = –20 µA; see Figure 1	V_{CCx}(1) – 0.1	3.3		V_{CCx}(1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4		0.3	0.5	V
		I_{OL} = 20 µA; see Figure 1		0	0.1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			425			425		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	50		25	50		kV/µs

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	8.5	14	12	23	35	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2			3	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			3			5	
		Opposite-direction Channels			4			6	
$t_{sk(pp)}$(3)	Part-to-part skew time				6.5			16	
t_r	Output signal rise time	See Figure 1		2			3.7		ns
t_f	Output signal fall time			1.3			3.4		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		6.5	17		9	20	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			6.5	17		8	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			5.5	17		11000	22000(4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			5.5	17		10	30	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.2			7.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

SUPPLY CURRENT

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			C-Grade			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.8	2.8		0.6	1.1	mA
I_{CC2}				2.7	3.7		0.7	1.3	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.9	2.9		1.2	1.8	
I_{CC2}				2.8	3.8		1.8	2.6	
I_{CC1}	10 Mbps			2.4	3.4		1.8	2.6	
I_{CC2}				3.5	4.6		2.6	3.5	
I_{CC1}	25 Mbps			3.2	4.2		2.7	3.6	
I_{CC2}				4.7	5.9		3.8	5	
I_{CC1}	150 Mbps			9.3	12.5	Not Applicable			
I_{CC2}				14.6	19				
ISO7641F						**C-Grade**			
I_{CC1}	Disable	EN1 = EN2 = 0 V					0.7	1.1	mA
I_{CC2}							0.8	1.3	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					1.2	1.9	
I_{CC2}							2	2.9	
I_{CC1}	10 Mbps						2	2.8	
I_{CC2}							3.2	4.1	
I_{CC1}	25 Mbps						3.1	4	
I_{CC2}							5.1	7	

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 2.7 V(1) (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CC}(2) – 0.5	2.4		V
		I_{OH} = –20 µA; see Figure 1	V_{CC}(2) – 0.1	2.7		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			350		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	50		kV/µs

(1) Only M-Grade devices are recommended for operation down to 2.7 V supplies. For 2.7 V-operation, max data rate is 100 Mbps.
(2) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	5	8	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$				2.5	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			4	
		Opposite-direction Channels			5	
$t_{sk(pp)}$(3)	Part-to-part skew time				8	
t_r	Output signal rise time	See Figure 1		2.3		ns
t_f	Output signal fall time			1.8		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		8	18	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			8	18	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			7	18	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			7	18	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		8.5		µs

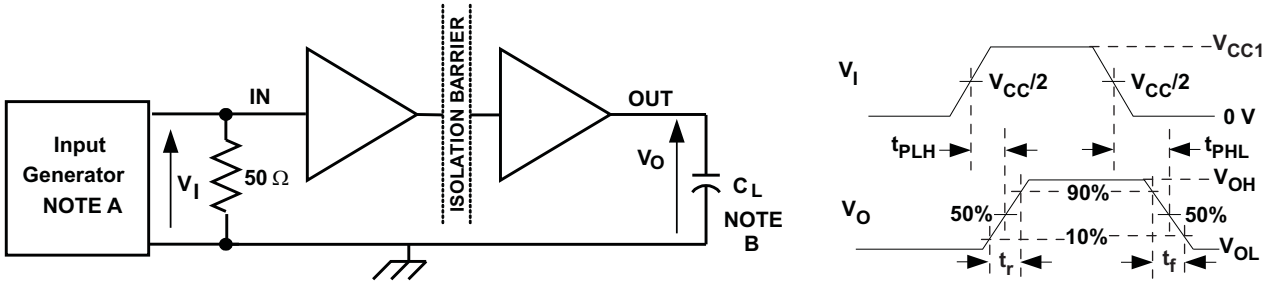
(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

SUPPLY CURRENT

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.5	2.4	mA
I_{CC2}				2.2	3.2	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.6	2.5	
I_{CC2}				2.3	3.2	
I_{CC1}	10 Mbps			2	2.9	
I_{CC2}				3	3.9	
I_{CC1}	25 Mbps			2.7	3.7	
I_{CC2}				3.9	4.9	
I_{CC1}	100 Mbps			5.7	6.8	
I_{CC2}				8.6	12	

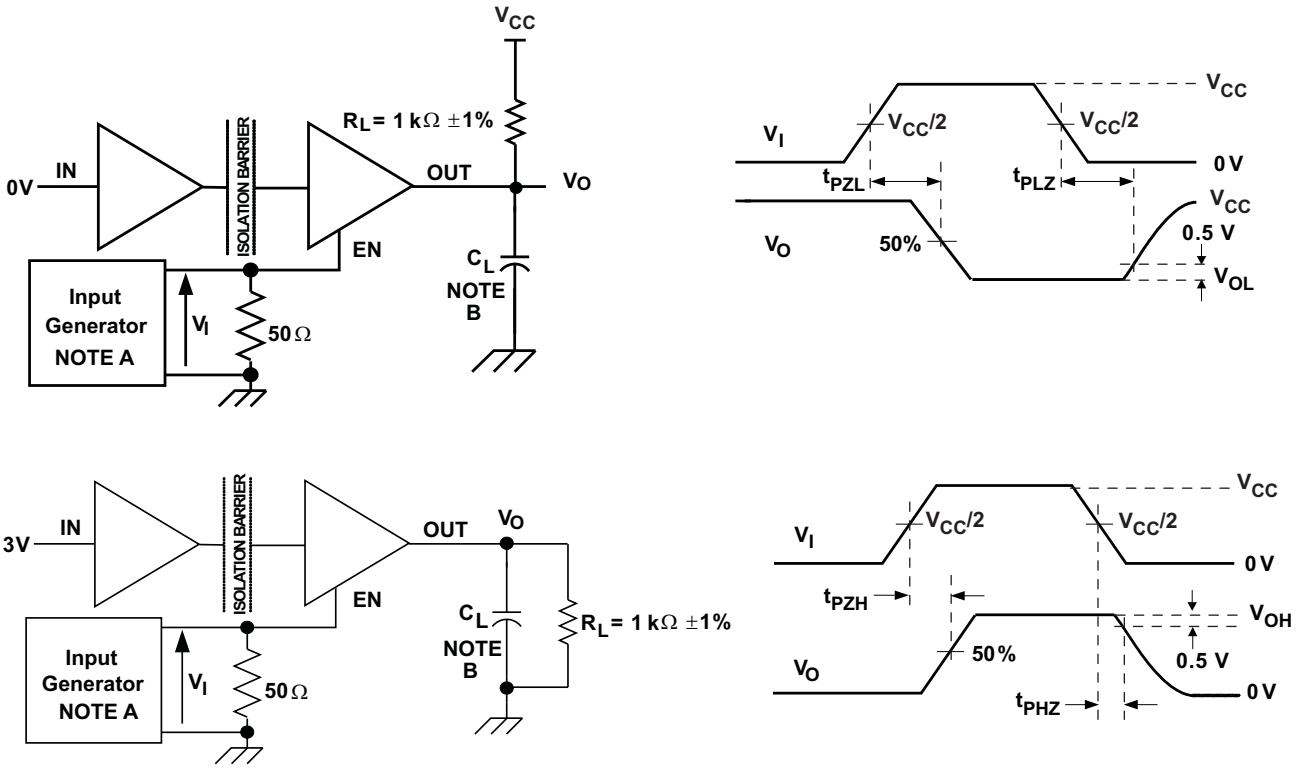
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristics Test Circuit and Voltage Waveforms

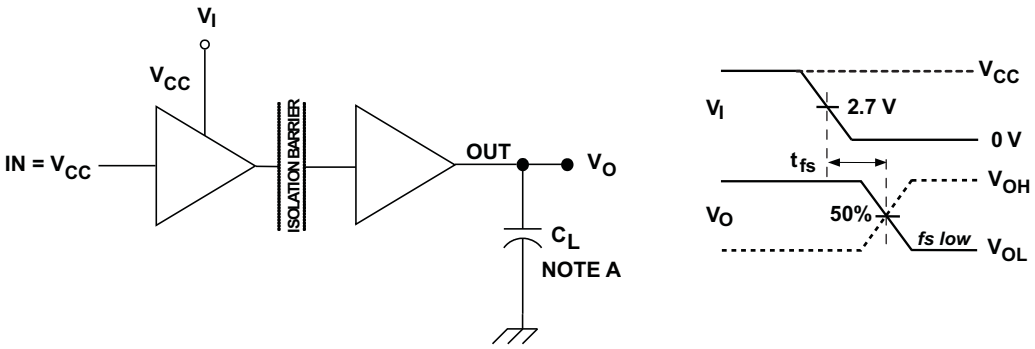


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

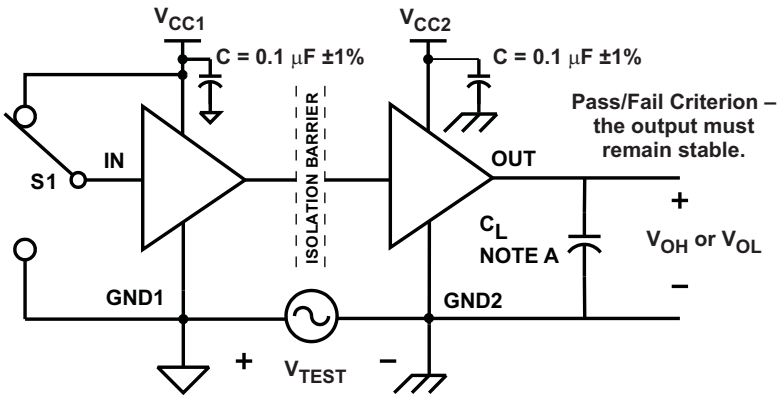
Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

IEC INSULATION AND SAFETY-RELATED SPECIFICATIONS FOR DW-16 PACKAGE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.3			mm
L(I02) (1)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.014			mm
R_{IO} (2)	Isolation resistance, Input to Output	V_{IO} = 500 V, T_A < 100°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		$>10^{11}$		
C_{IO} (2)	Barrier capacitance, Input to Output	V_I = 0.4 sin (2πft), f = 1MHz		2		pF
C_I (3)	Input capacitance	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1MHz, V_{CC} = 5 V		2		pF

(1) Per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.
(3) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

Table 2. DIN EN 60747-5-2 (VDE 0884 TEIL 2) INSULATION CHARACTERISTICS (1) over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		1414	V_{PEAK}
V_{PR}	Input-to-output test voltage	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	1697	V_{PEAK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, 100% Production test $V_{PR} = V_{IORM}$ x 1.875, t = 1 s Partial discharge < 5 pC	2652	
V_{IOTM}	Maximum transient overvoltage	$V_{TEST} = V_{IOTM}$ t = 60 sec (Qualification) t = 1 sec (100% Production)	4242	V_{PEAK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 3. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation classification	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–III
	Rated mains voltage ≤ 1000 V_{RMS}	I–II

REGULATORY INFORMATION

VDE	TUV	CSA	UL
Certified according to DIN EN 60747-5-2	Certified according to EN/UL/CSA 60950-1 and 61010-1	Approved under CSA Component Acceptance Notice #5A	Recognized under 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK} Maximum Working Voltage, 1414 V_{PK}	3000 V_{RMS} Reinforced Insulation, 400 V_{RMS} maximum working voltage 3000 V_{RMS} Basic Insulation, 600 V_{RMS} maximum working voltage	4242 V_{PK} Insulation	Single Protection, 2500 V_{RMS} (1)
File Number: 40016131	Certificate Number: U8V 13 09 77311 010	File Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 72 °C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			316	mA
			θ_{JA} = 72 °C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			482	
			θ_{JA} = 72 °C/W, V_I = 2.7V, T_J = 150°C, T_A = 25°C			643	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

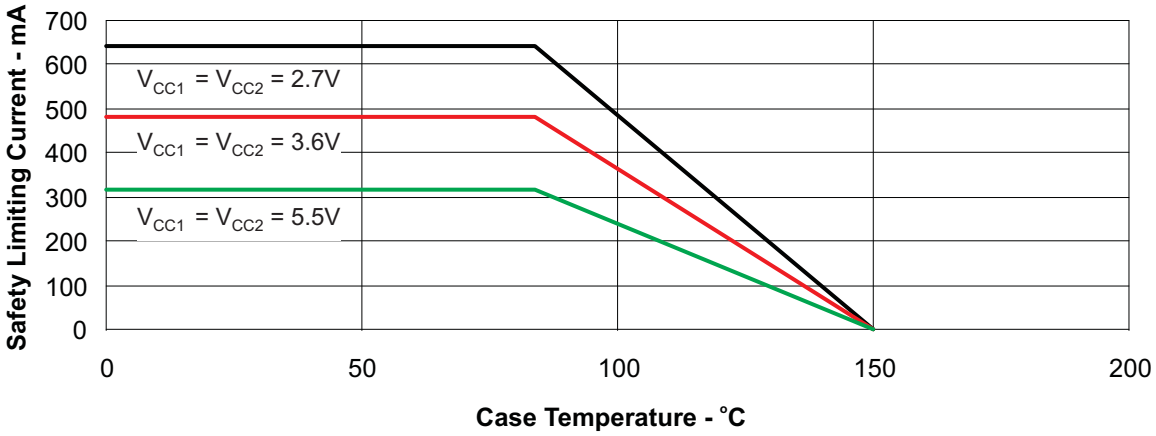


Figure 5. DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5-2

APPLICATION INFORMATION

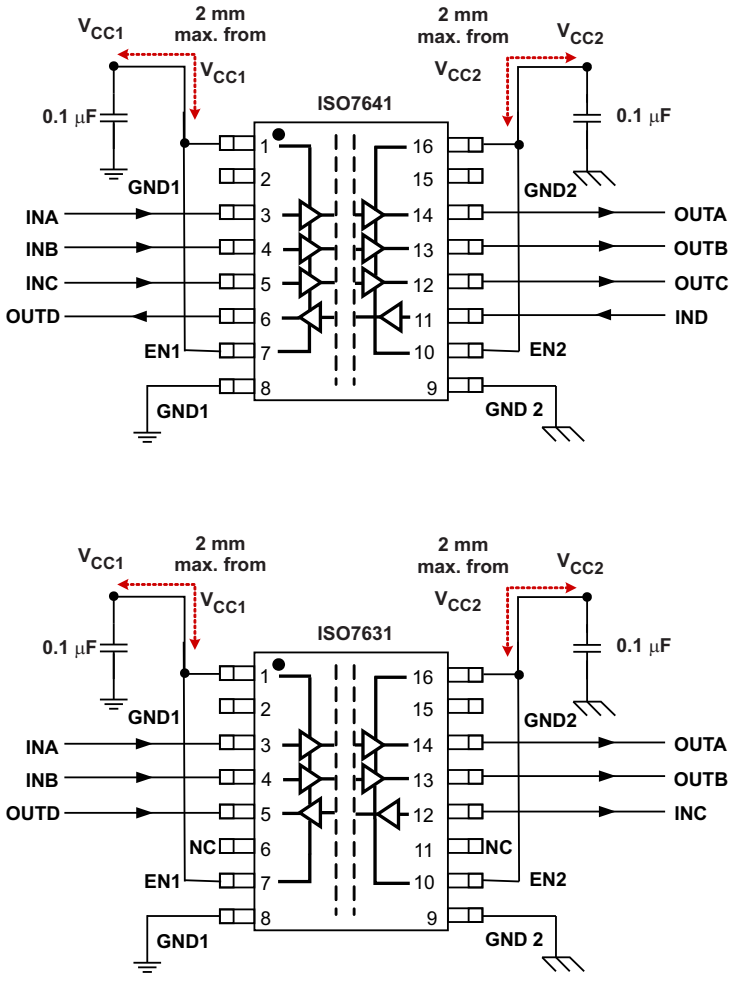


Figure 6. Typical ISO7641 and ISO7631 Application Circuit

Note: For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

TYPICAL SUPPLY CURRENT EQUATIONS

(Calculated based on room temperature and typical Silicon process)

ISO7631FM:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 1.8072 + 0.0244 \times f + 0.0016 \times f \times C_L$

$I_{CC2} = 2.4625 + 0.0252 \times f + 0.0033 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 5V$

$I_{CC1} = 2.3183 + 0.04 \times f + 0.0025 \times f \times C_L$

$I_{CC2} = 3.2582 + 0.0403 \times f + 0.0049 \times f \times C_L$

ISO7631FC:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 1.1762 + 0.0325 \times f + 0.0017 \times f \times C_L$

$I_{CC2} = 1.5285 + 0.0299 \times f + 0.0033 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 5V$

$I_{CC1} = 1.6001 + 0.0528 \times f + 0.0025 \times f \times C_L$

$I_{CC2} = 2.2032 + 0.0475 \times f + 0.005 \times f \times C_L$

ISO7641FC:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 1.2162 + 0.0462 \times f + 0.0017 \times f \times C_L$

$I_{CC2} = 1.8054 + 0.0411 \times f + 0.005 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 5V$

$I_{CC1} = 1.6583 + 0.0757 \times f + 0.0025 \times f \times C_L$

$I_{CC2} = 2.5008 + 0.0655 \times f + 0.0076 \times f \times C_L$

I_{CC1} and I_{CC2} are typical supply currents measured in mA; f is data rate measured in Mbps; C_L is the capacitive load on each channel measured in pF.

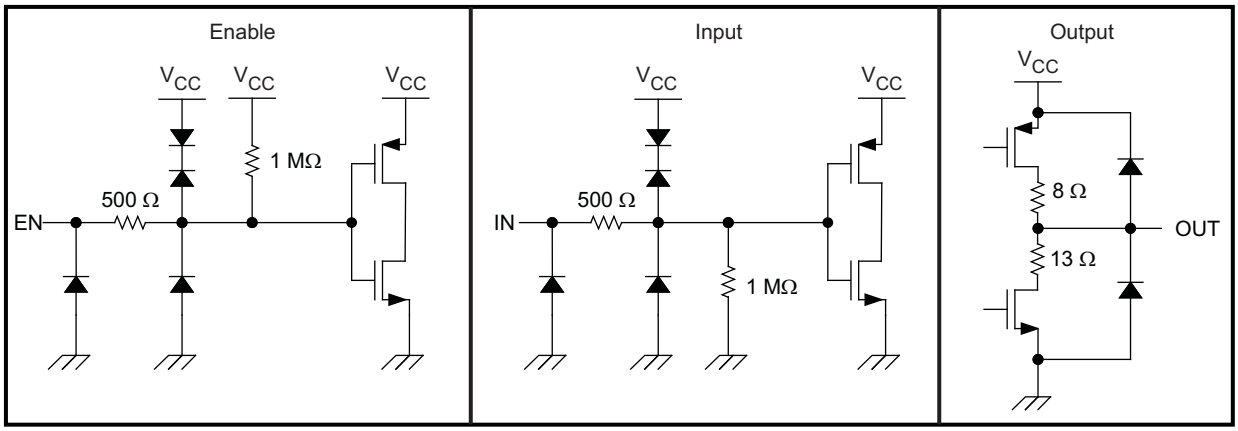


Figure 7. Device I/O Schematics

TYPICAL CHARACTERISTICS

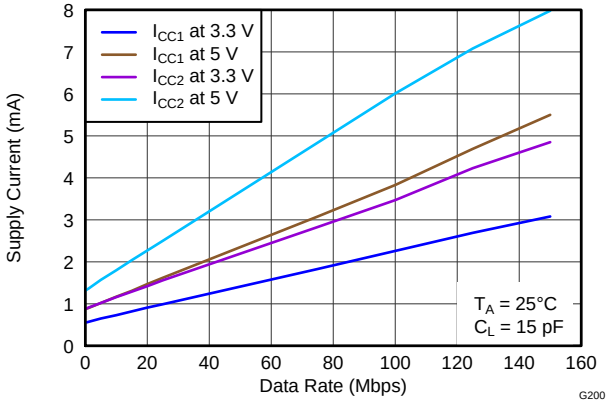


Figure 8. ISO7631FM Supply Current Per Channel vs Data Rate

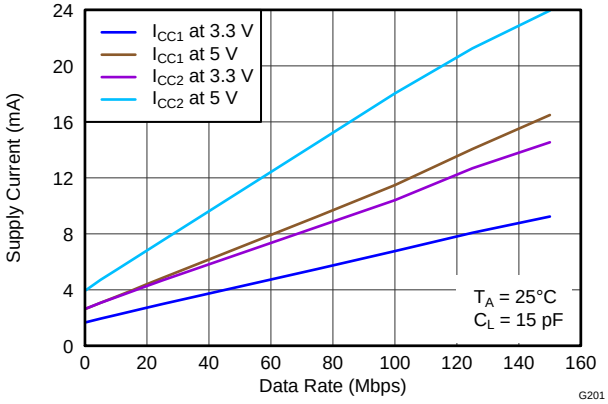


Figure 9. ISO7631FM Supply Current For All Channels vs Data Rate

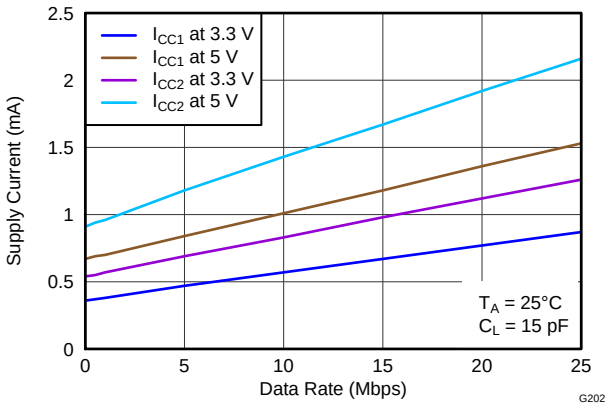


Figure 10. ISO7631FC Supply Current Per Channel vs Data Rate

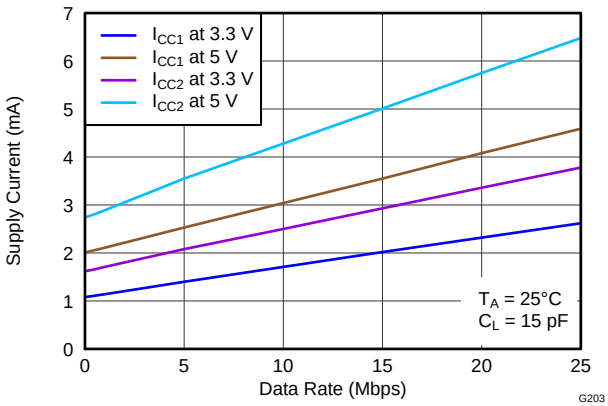


Figure 11. ISO7631FC Supply Current For All Channels vs Data Rate

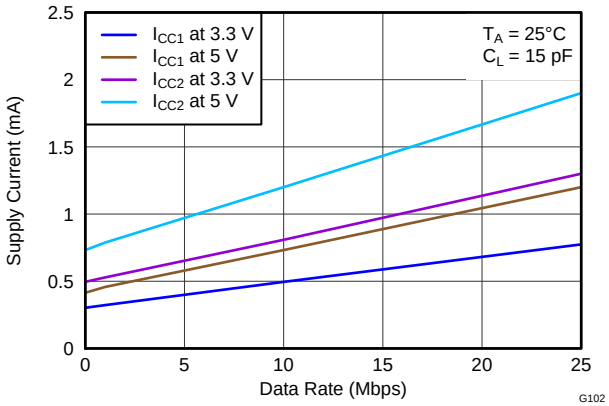


Figure 12. ISO7641FC Supply Current Per Channel vs Data Rate

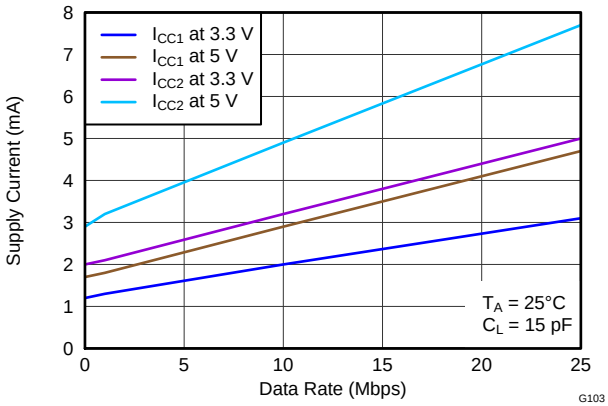


Figure 13. ISO7641FC Supply Current For All Channels vs Data Rate

TYPICAL CHARACTERISTICS (continued)

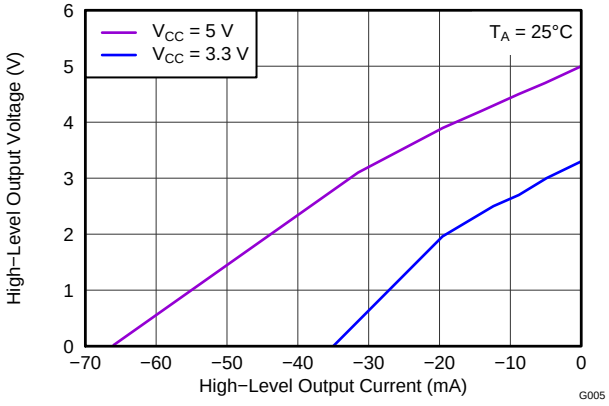


Figure 14. M-Grade High-Level Output Voltage vs High-Level Output Current

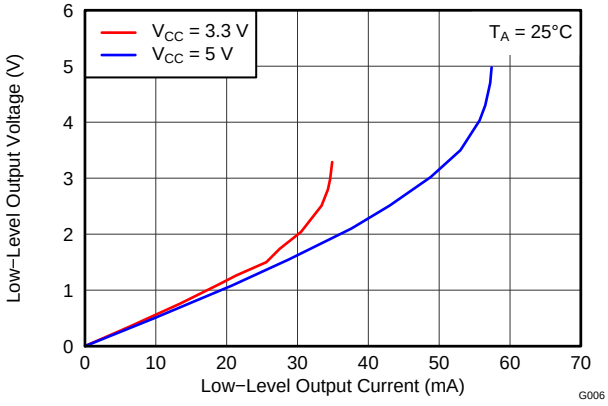


Figure 15. M-Grade Low-Level Output Voltage vs Low-Level Output Current

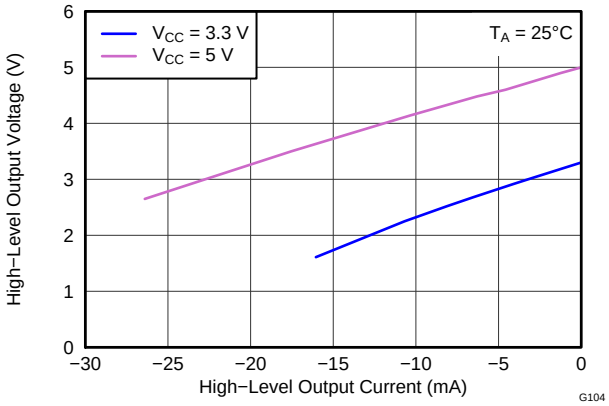


Figure 16. C-Grade High-Level Output Voltage vs High-Level Output Current

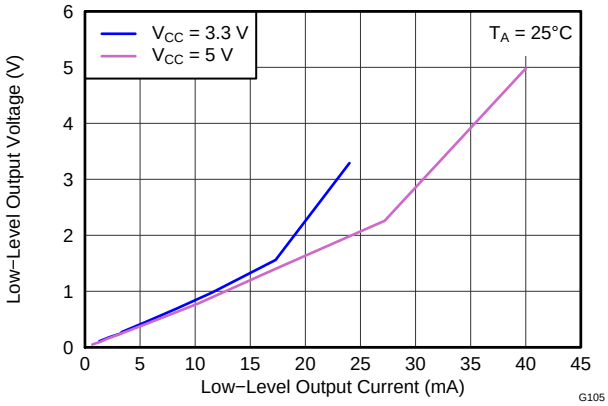


Figure 17. C-Grade Low-Level Output Voltage vs Low-Level Output Current

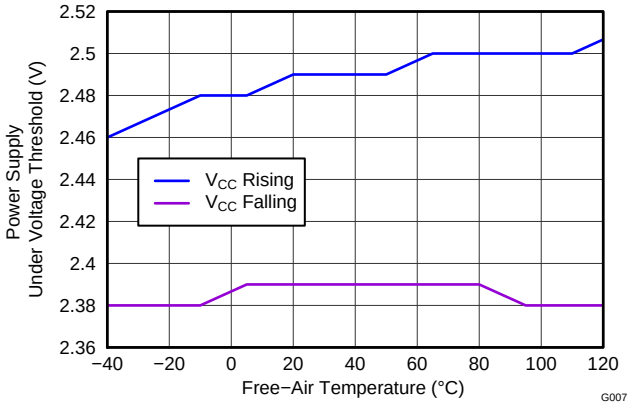


Figure 18. V_{CC} Undervoltage Threshold vs Free Air Temperature

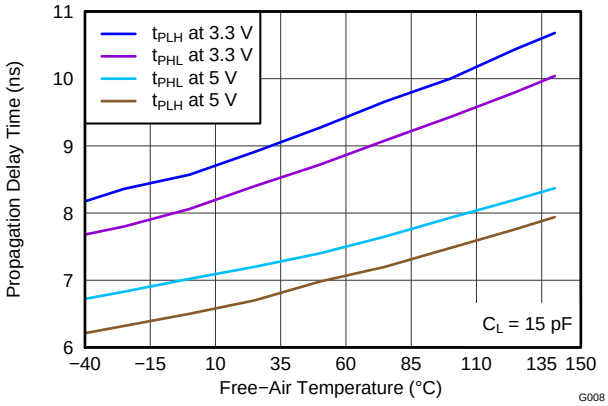


Figure 19. M-Grade Propagation Delay Time vs Free Air Temperature

TYPICAL CHARACTERISTICS (continued)

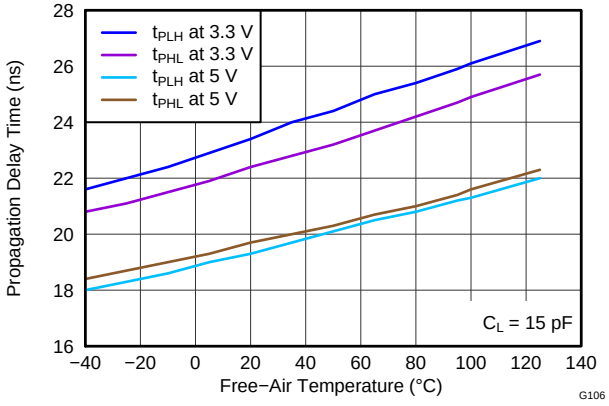


Figure 20. C-Grade Propagation Delay Time vs Free Air Temperature

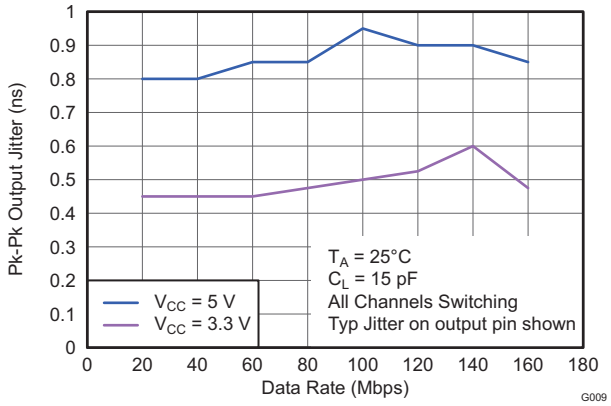


Figure 21. M-Grade Output Jitter vs Data Rate

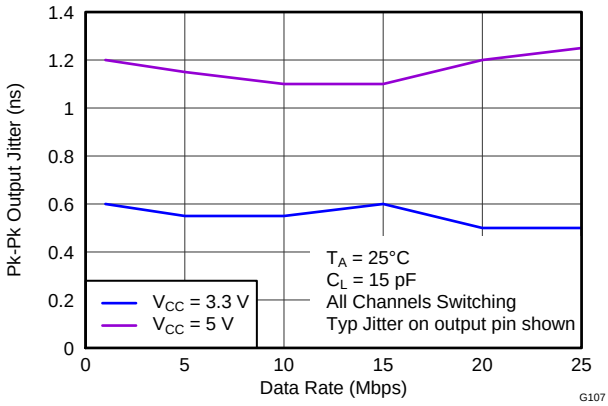


Figure 22. C-Grade Output Jitter vs Data Rate

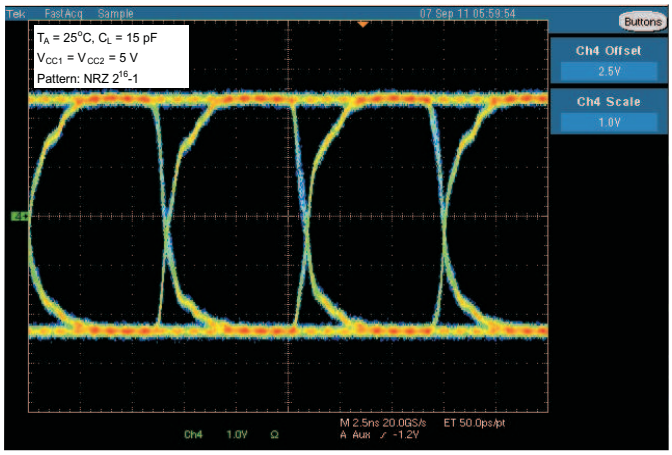


Figure 23. M-Grade Typical Eye Diagram at 150 Mbps, 5 V Operation

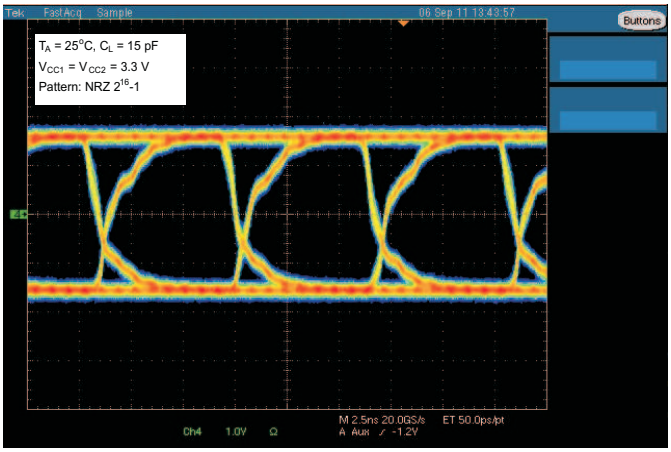


Figure 24. M-Grade Typical Eye Diagram at 150 Mbps, 3.3 V Operation

TYPICAL CHARACTERISTICS (continued)

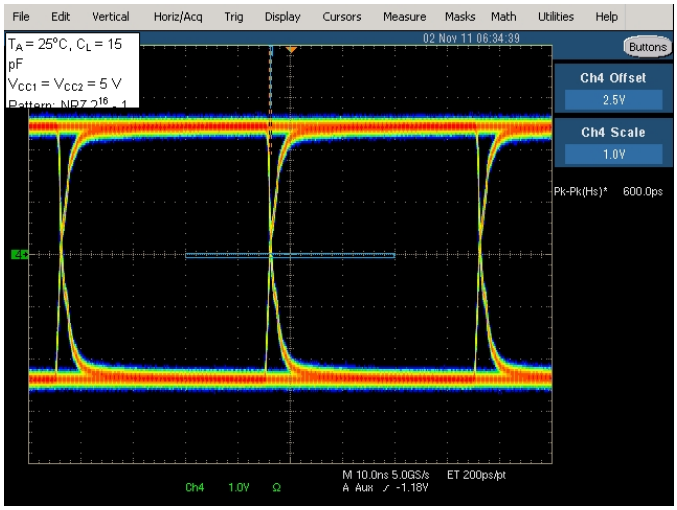


Figure 25. C-Grade Typical Eye Diagram at 25 Mbps, 5 V Operation

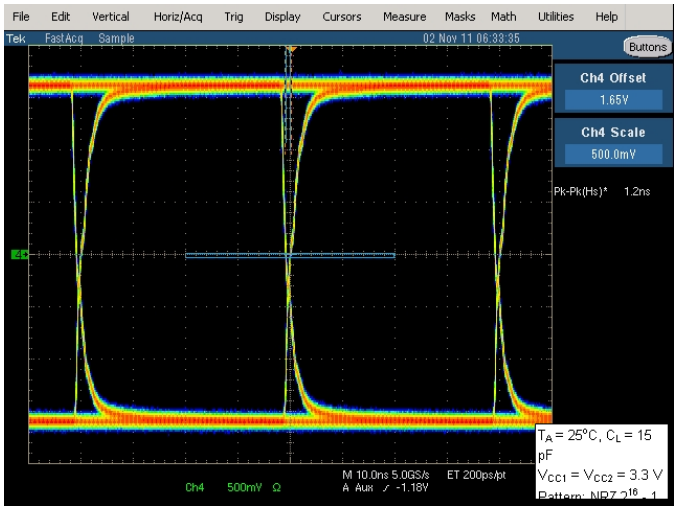


Figure 26. C-Grade Typical Eye Diagram at 25 Mbps, 3.3 V Operation

REVISION HISTORY

Changes from Original (September 2012) to Revision A **Page**

- 将说明文本从：“输入噪声脉冲持续时间少于 10ns 的应用。。。。。。” 改为：“输入噪声脉冲持续时间少于 6ns 的应用。。。。。。” 1
- Changed Input PU in the Function table From: Z To: 'Undetermined 2
- Added note "Product Preview" to ISO7640FC in the Available Options table 3

Changes from Revision A (September 2012) to Revision B **Page**

- 将安全特性从：针对 DIN EN 60747-5-2（VDE 0884 修订版本 2）标准的 4000 V_{PK}VDE 额定值改为：针对 DIN EN 60747-5-2（VDE 0884 修订版本 2）标准的 4242 V_{PK}VDE 额定值 1
- Changed the V_{IOTM} SPECIFICATION From: 4000 V_{PEAK} to 4242 V_{PEAK} 17
- Changed the REGULATORY INFORMATION table: 4242 V_{PK} To: 4000 V_{PK} 18

Changes from Revision B (April 2013) to Revision C **Page**

- 已从页面顶部删除器件图 1
- 已删除器件编号 ISO7640FC 1
- 已删除特性 ISO7640FC：10Mbps 时为 1.1mA 1
- 已添加安全特性：针对 EN/UL/CSA 60950-1 和 EN/UL/CSA 61010-1（已获批准）符合 TUV 标准的 3000 V_{RMS} 增强隔离 1
- 已更改说明 1
- 已删除 ISO7640 引脚分配图 1
- Deleted ISO7640FC from the Available Options table 3
- Changed The ISO7631FC Rated Isolation values in the Available Options table 3
- Added the TUV column to the REGULATORY INFORMATION table 18
- Deleted the ISO7640 circuit from the APPLICATION INFORMATION section 19
- Deleted ISO7640FC from the TYPICAL SUPPLY CURRENT EQUATIONS section 20
- Deleted Graph ISO7640FC Supply Current Per Channel vs Data Rate 21
- Deleted Graph ISO7640FC Supply Current For All Channels vs Data Rate 21

Changes from Revision C (August 2013) to Revision D **Page**

- Changed the REGULATORY INFORMATION table, TUV column From: Certificate Number: U8V 13 07 77311 009 To: Certificate Number: U8V 13 09 77311 010 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7631FCDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7631FC	Samples
ISO7631FCDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7631FC	Samples
ISO7631FMDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7631FM	Samples
ISO7631FMDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7631FM	Samples
ISO7641FCDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FC	Samples
ISO7641FCDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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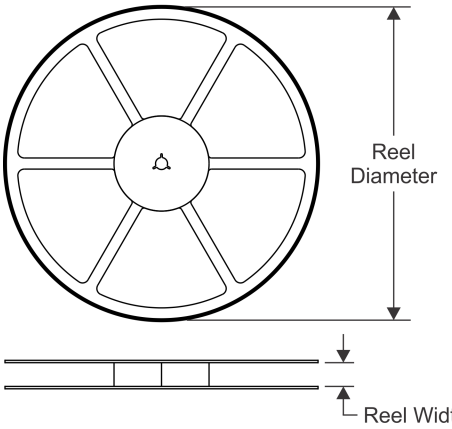
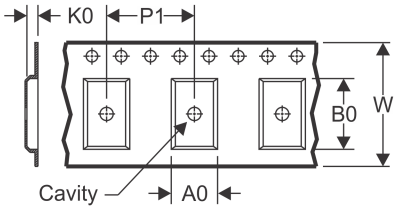
TAPE AND REEL INFORMATION

REEL DIMENSIONS

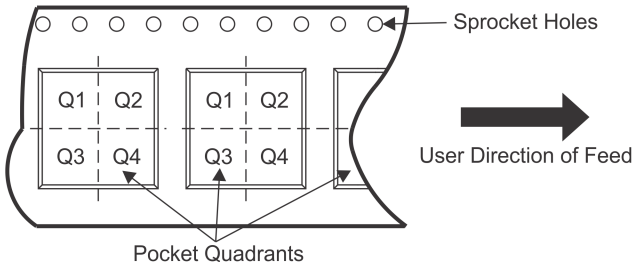


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

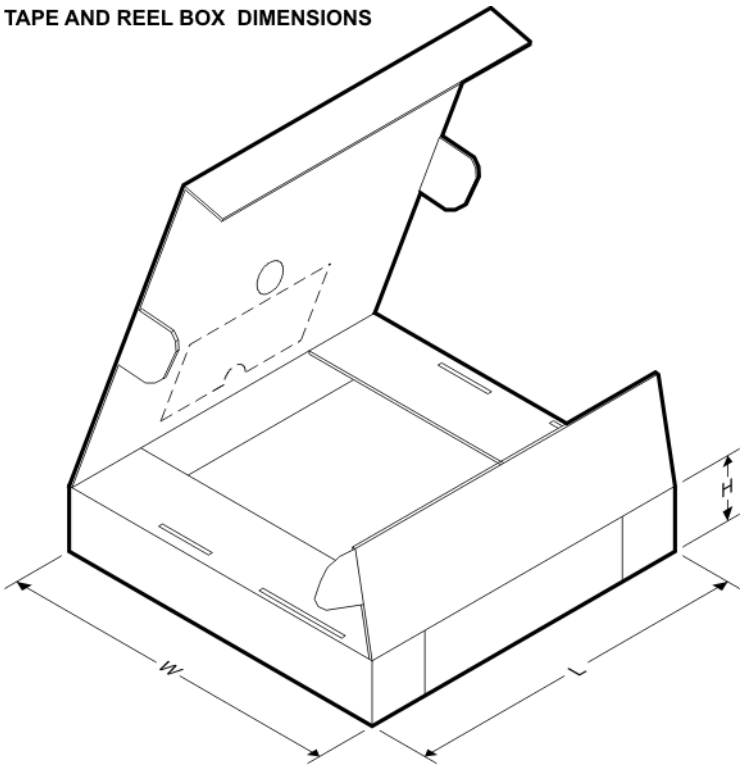
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7631FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7631FMDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7641FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

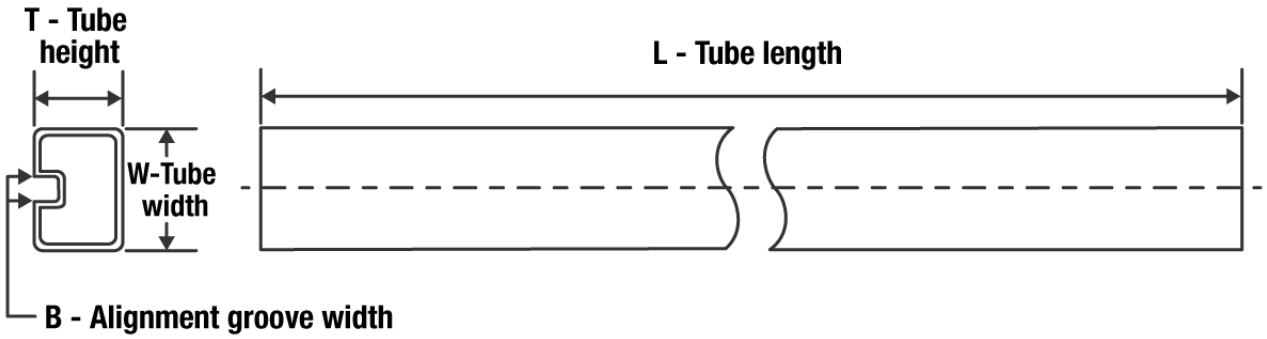
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7631FCDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7631FMDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7641FCDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7631FCDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7631FMDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7641FCDW	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

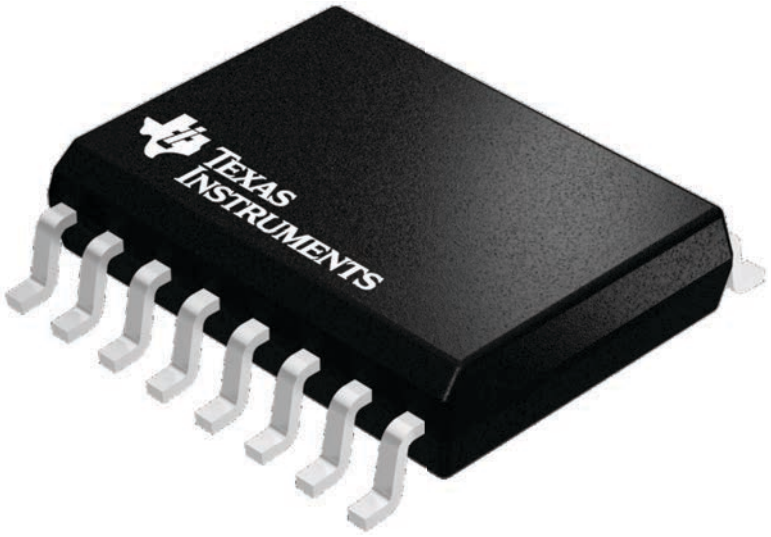
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

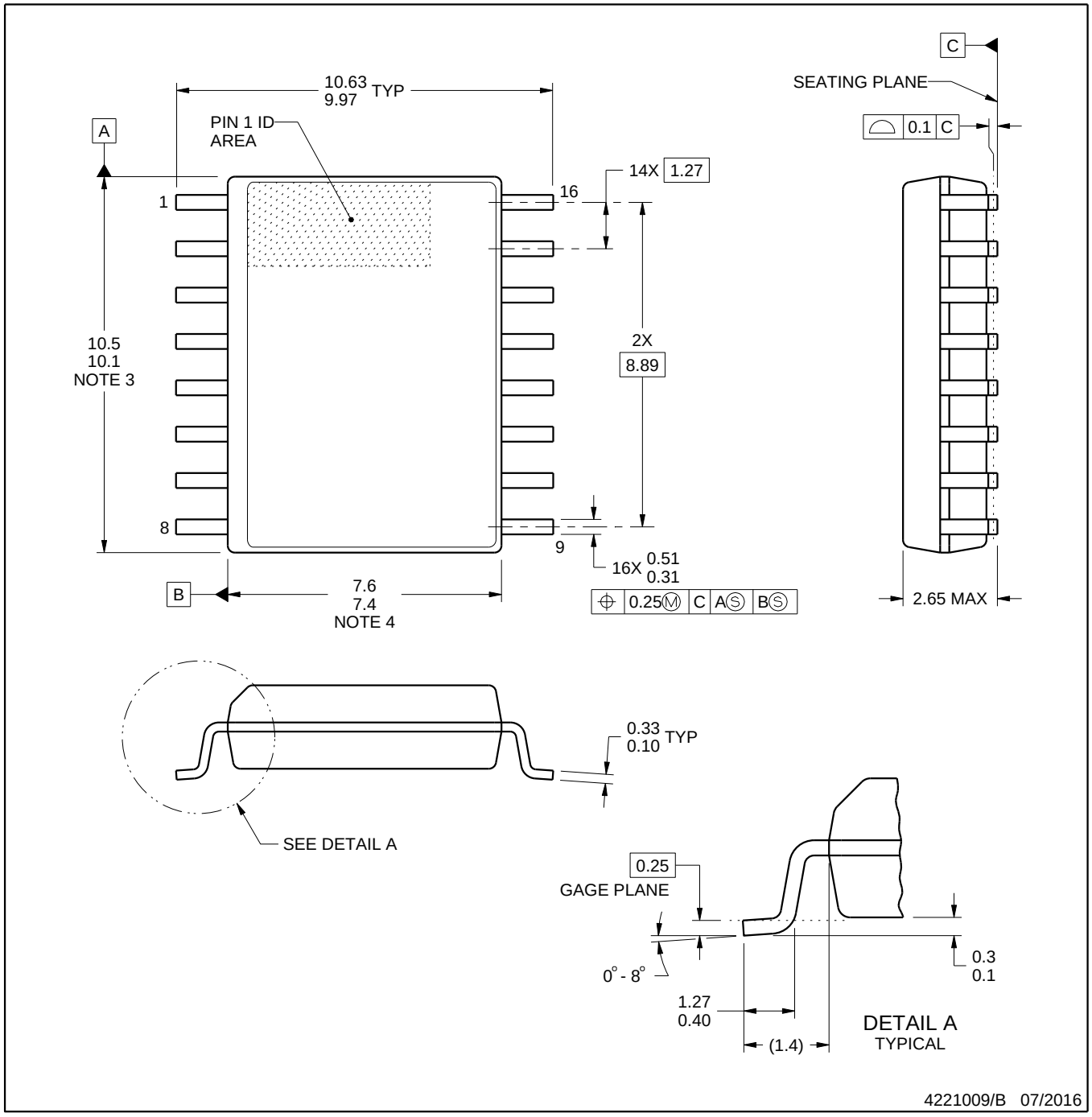
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



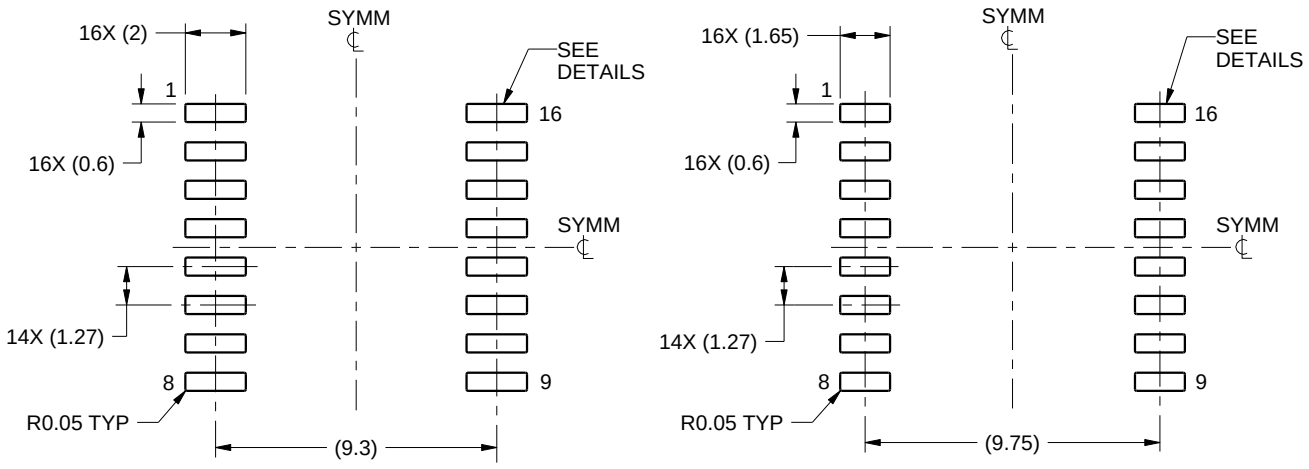
4224780/A

SOIC



NOTES:

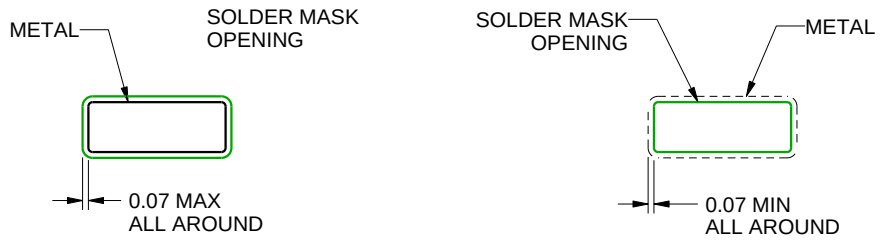
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

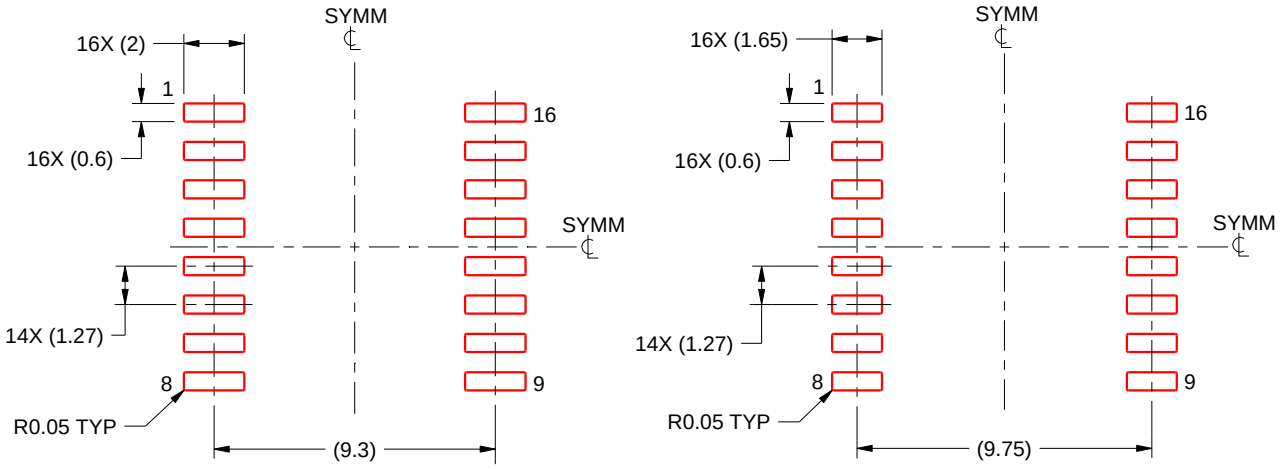
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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