具有 ±15kV IEC ESD 保护功能的 3V 至 5.5V 单通道 RS-232 1Mbits 线路驱动器和接收器

1 特性

- 为 RS-232 引脚提供 ESD 保护
  - ±15kV 人体放电模型 (HBM)
  - ±8kV IEC 61000-4-2 接触放电
  - ±15kV IEC 61000-4-2 气隙放电
- 由 3V 至 5.5V V_{CC} 电源供电
- 速率高达 1Mbit/s
- 低待机电流 ...1 μA（典型值）
- 外部电容器 ...4 × 0.1 μF
- 接受 5V 逻辑输入及 3.3V 电源
- 使用人体放电模型 (HBM) 时，RS-232 总线引脚 ESD 保护大于 ±15kV
- 自动断电功能可自动禁用驱动器以节省能耗

2 应用

- 工业 PC
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- PDA
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

3 说明

SN65C3221E 和 SN75C3221E 包含一个线路驱动器、一个线路接收器和一个具有引脚对引脚（串行端口连接引脚，包括 GND）±15kV IEC ESD 保护功能的双电荷泵电路。这些器件可在异步通信控制器和串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。

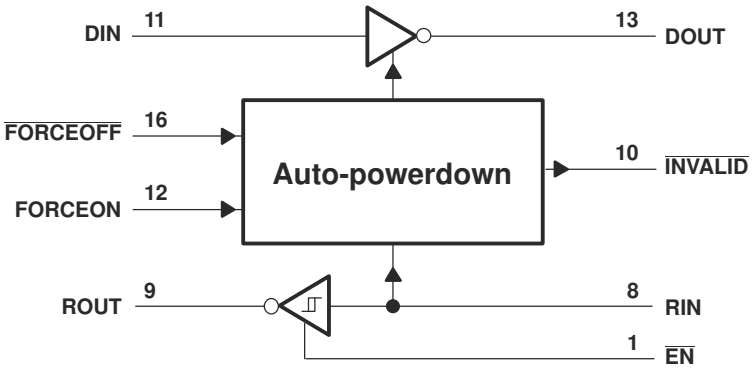
这些器件以高达 1Mbit/s 的数据信号传输速率运行，驱动器输出压摆率为 24V/μs 至 150V/μs。

串行端口处于非活动状态时，可提供灵活的电源管理控制选项。当 FORCEON 为低电平且 $\overline{\text{FORCEOFF}}$ 为高电平时，自动断电功能启用。在这种运行模式下，如果器件在接收器输入端未感应到有效的 RS-232 信号，则会禁用驱动器输出。如果 $\overline{\text{FORCEOFF}}$ 设定为低电平且 $\overline{\text{EN}}$ 为高电平，则驱动器和接收器均关闭，且电源电流降低至 1 μA。断开串行端口的连接或关闭外围驱动器会导致发生自动断电情况。当 FORCEON 和 $\overline{\text{FORCEOFF}}$ 均为高电平时可禁用自动断电。启用自动断电的情况下，向接收器输入施加有效信号时，器件会自动激活。$\overline{\text{INVALID}}$ 输出会通知用户接收器输入端是否存在 RS-232 信号。如果接收器输入电压大于 2.7V 或小于 -2.7V，或者介于 -0.3V 至 0.3V 之间的时间少于 30 μs，则 $\overline{\text{INVALID}}$ 为高电平（有效数据）。如果接收器输入电压在 -0.3V 至 0.3V 之间的时间超过 30 μs，则 $\overline{\text{INVALID}}$ 为低电平（无效数据）。有关接收器输入电平的信息，请参阅图 8-5。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
SNx5C3221E	SSOP (DB) 16	6.20mm x 5.30mm
	TSSOP (DW) 16	10.3mm x 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2009) to Revision C (July 2021)	Page
• 更改了*应用* 列表	1
• 删除了“订购信息”表	1
• 添加了*器件信息* 表	1
• Added the *Pin Configuration and Functions*	4
• Removed the thermal information from *Absolute Maximum Ratings*table and moved the thermal information to its own table	5
• Added a table note for PW package of SN65C3221E regarding the minimum capacitance in *ESD Ratings - IEC Specifications* table	5
• Changed thermal information for PW package of SN65C3221E. Added additional thermal information for other packages	6
• Added the *Detailed Desctipiton* section	13

5 Device Comparison Table

表 5-1. 1-Mbit/s RS-232 Parts

PART NO.	TEMPERATURE RANGE	DRIVER NO.	RECEIVER NO.	ESD	SUPPLY V_{CC} (V)	FEATURE	PIN/PACKAGE
SN65C3221E	–40°C to 85°C	1	1	±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Auto powerdown	16-pin SOIC, SSOP, TSSOP
SN65C3232E		2	2	±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
MAX3227I		1	1	±8-kV Air-Gap, ±8-k V Contact, ±15-kV HBM	3.3 or 5	Auto powerdown plus, ready signal	16-pin SSOP
SN65C3221		1	1	±15-kV HBM	3.3 or 5	Auto powerdown	16-pin SOIC, SSOP, TSSOP
SN65C3223		2	2	±15-kV HBM	3.3 or 5	Auto powerdown, enable signal	20-pin SOIC, SSOP, TSSOP
SN65C3222		2	2	±15-kV HBM	3.3 or 5	Enable, powerdown signal	20-pin SOIC, SSOP, TSSOP
SN65C3232		2	2	±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
SN65C3238		5	3	±15-kV HBM	3.3 or 5	Auto powerdown plus	28-pin SOIC, SSOP, TSSOP
SN65C3243		3	5	±15-kV HBM	3.3 or 5	Auto powerdown	28-pin SOIC, SSOP, TSSOP
SN75C3221E	0°C to 70°C	1	1	±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Auto powerdown	16-pin SOIC, SSOP, TSSOP
SN75C3232E		2	2	±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
MAX3227C		1	1	±8-kV Air-Gap, ±8-kV Contact, ±15-kV HBM	3.3 or 5	Auto powerdown plus, ready signal	16-pin SSOP
SN75C3221		1	1	±15-kV HBM	3.3 or 5	Auto powerdown	16-pin SOIC, SSOP, TSSOP
SN75C3223		2	2	±15-kV HBM	3.5 or 5	Auto powerdown, enable signal	20-pin SOIC, SSOP, TSSOP
SN75C3222		2	2	±15-kV HBM	3.3 or 5	Enable, powerdown signal	20-pin SOIC, SSOP, TSSOP
SN75C3232		2	2	±15-kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
SN75C3238		5	3	±15-kV HBM	3.3 or 5	Auto powerdown plus	28-pin SOIC, SSOP, TSSOP
SN75C3243		3	5	±15-kV HBM	3.3 or 5	Auto powerdown	28-pin SOIC, SSOP, TSSOP

6 Pin Configuration and Functions

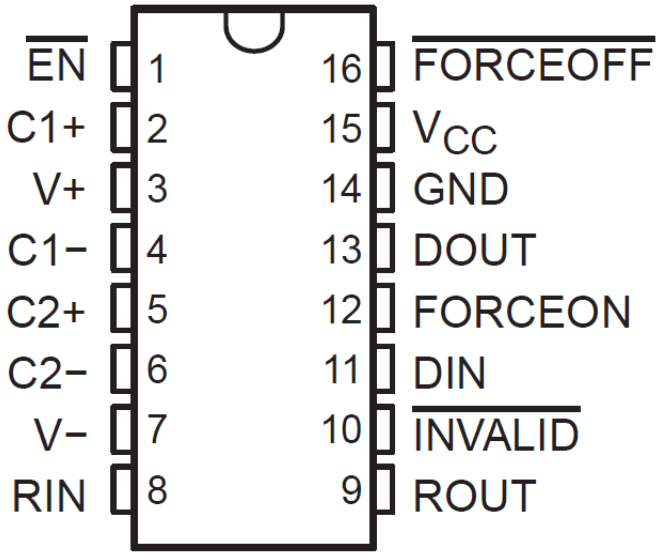


图 6-1. DB or PW Package
Top View

表 6-1. Pin Configurations

PIN			DESCRIPTION
NAME	NO	I/O	
$\overline{EN}$	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
C1+	2	—	Positive terminals of the voltage-doubler charge-pump capacitors
V+	3	O	5.5-V supply generated by the charge pump
C1 –	4	—	Negative terminals of the voltage-doubler charge-pump capacitors
C2+	5	—	Positive terminals of the voltage-doubler charge-pump capacitors
C2 –	6	—	Negative terminals of the voltage-doubler charge-pump capacitors
V –	7	O	– 5.5-V supply generated by the charge pump
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
$\overline{INVALID}$	10	O	Invalid output pin. Output low when all RIN inputs are unpowered.
DIN	11	I	Driver input
FORCEON	12	I	Automatic power-down control input
DOUT	13	O	RS-232 driver output
GND	14	—	Ground
V_{CC}	15	—	3-V to 5.5-V supply voltage
$\overline{FORCEOFF}$	16	I	Automatic power-down control input

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Driver ($\overline{FORCEOFF}$, FORCEON, $\overline{EN}$)	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
		Receiver ($\overline{INVALID}$)	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	DOUT, RIN	±15000	V
			All other pins	±3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge (1)	RIN and DOUT pins only	±8000	V
		IEC 61000-4-2 Air Discharge (1)	RIN and DOUT pins only	±15000	

(1) For the PW package of SN65C3221E only, a minimum of 1-µF capacitor is required between VCC and GND to meet the specified IEC-ESD level.

7.4 Recommended Operating Conditions

See 图 10-1. see (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			– 25		25	V
T_A	Operating free-air temperature		SN65C3221E	– 40		85	°C
			SN75C3221E	0		70	

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

7.5 Thermal Information

THERMAL METRIC[1]		SN65C3221E		SN75C3221E		UNIT
		PW (TSSOP)	DB (SSOP)	PW (TSSOP)	DB (SSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.9	82	108	82	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	45.7	41.1	45.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.2	44.4	51.4	44.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.2	11.0	3.9	11.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.6	43.8	50.9	43.8	°C/W

7.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 10-1)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
I_I	Input leakage current	$\overline{FORCEOFF}$, FORCEON, $\overline{EN}$			±0.01	±1	μA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	μA
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	μA

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

7.7 Driver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 10-1)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND		5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}		– 5	– 5.4		V
I_{IH}	High-level input current	V_I = V_{CC}				±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	μA
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V			±35	±90	
r_o	Output resistance	V_{CC}, V+, and V – = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND	V_O = ±12 V,	V_{CC} = 3 V to 3.6 V			±25	μA
			V_O = ±10 V,	V_{CC} = 4.5 V to 5.5 V			±25	

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

7.8 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 10-1)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
Maximum data rate (see 图 8-1)		R_L = 3 kΩ	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ,	See 图 8-2		100		ns
SR(tr)	Slew rate, transition region (see 图 8-1)	V_{CC} = 3.3 V,	R_L = 3 kΩ to 7 kΩ,	C_L = 150 pF to 1000 pF	18		150	V/μs

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

7.9 Receiver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 10-1)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6 V	V_{CC} – 0.1 V		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.5		V
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = 0 V		±0.05	±10	μA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

7.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 10-1)

PARAMETER		TEST CONDITIONS(1)	TYP(2)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 图 8-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See 图 8-3	150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 图 8-4	200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See 图 8-4	200	ns
$t_{sk(p)}$	Pulse skew(3)	See 图 8-3	50	ns

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

7.11 Auto-powerdown Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = –1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

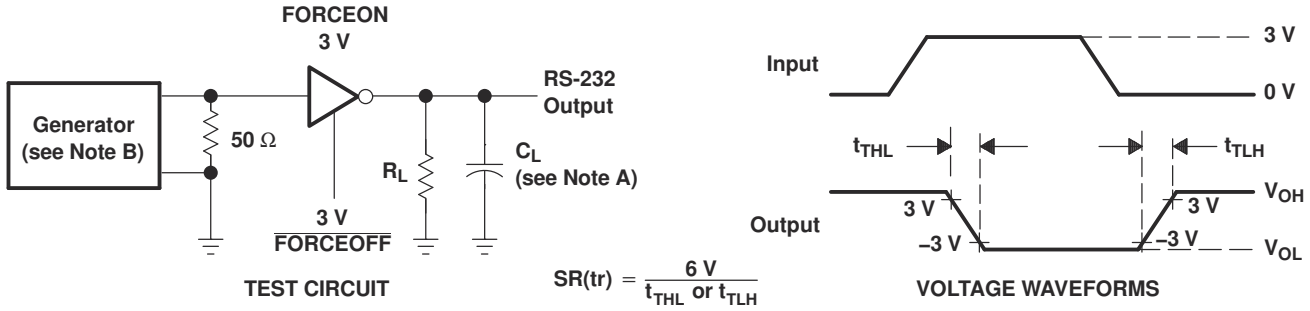
7.12 Switching Characteristics: Auto-powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-5)

PARAMETER		TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

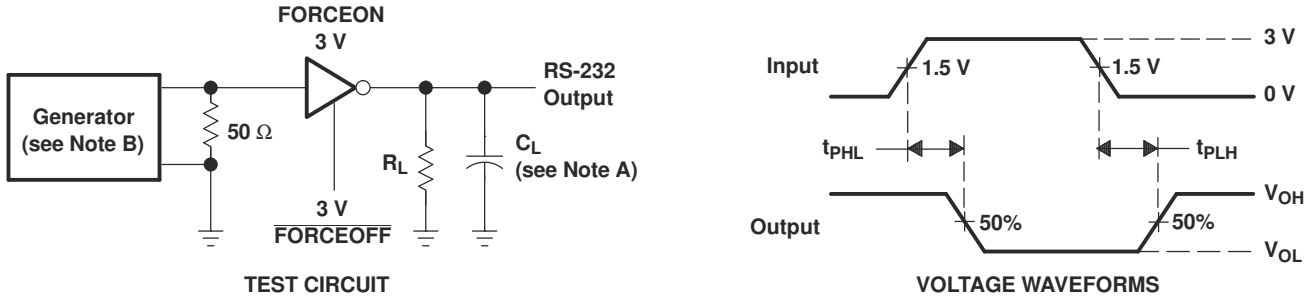
(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

8 Parameter Measurement Information



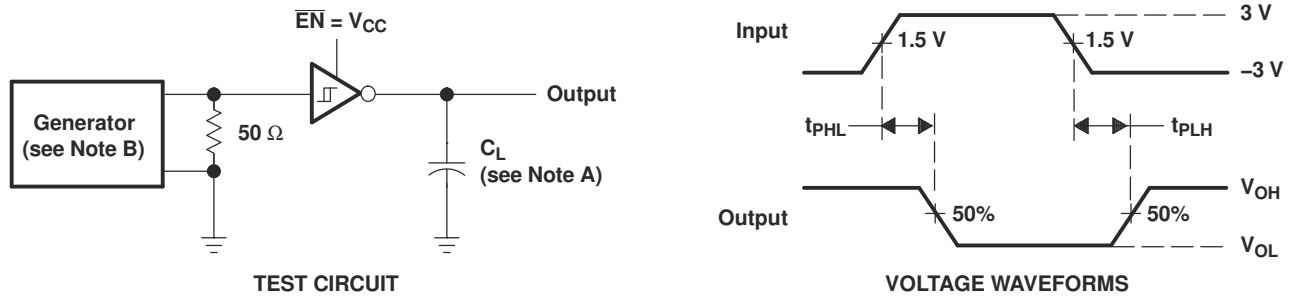
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

图 8-1. Driver Slew Rate



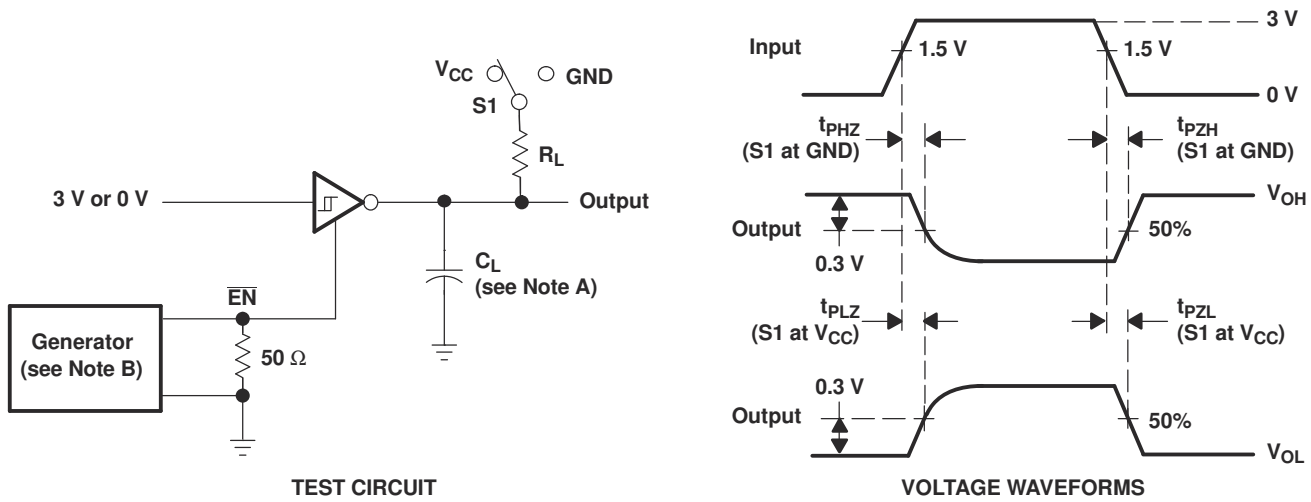
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

图 8-2. Driver Pulse Skew



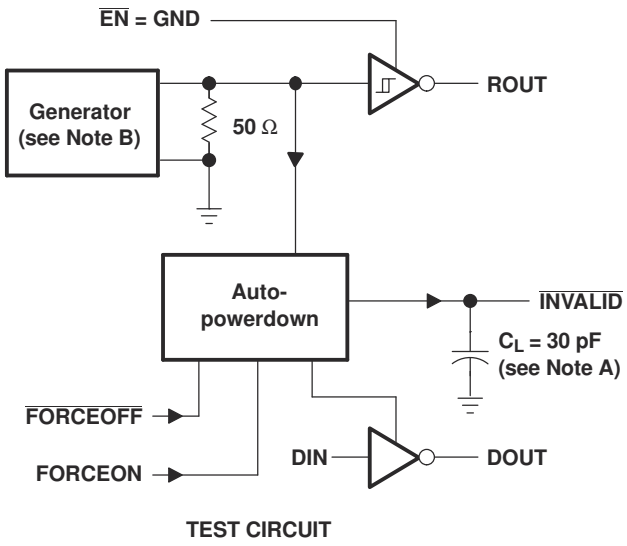
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

图 8-3. Receiver Propagation Delay Times

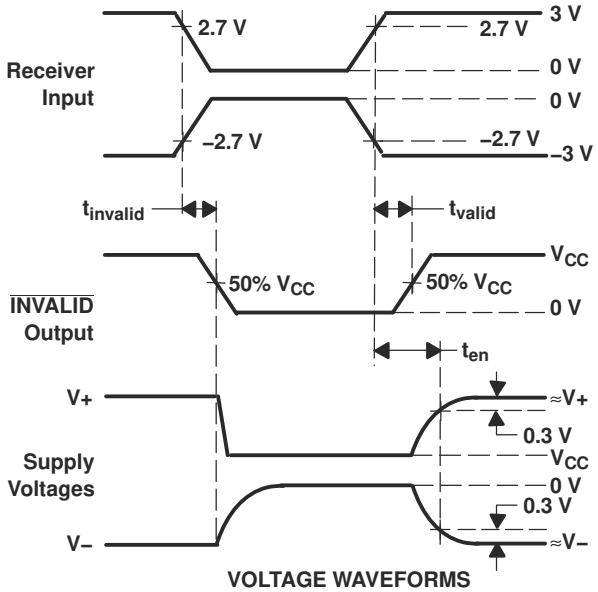


NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

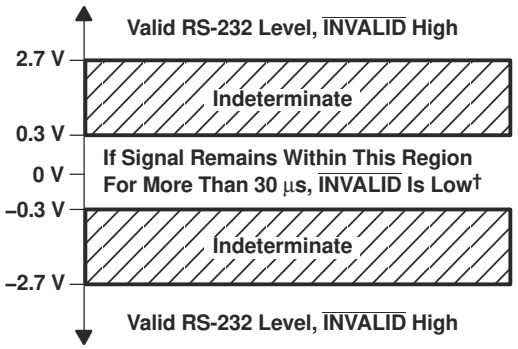
图 8-4. Receiver Enable and Disable Times



TEST CIRCUIT



VOLTAGE WAVEFORMS



† Auto-powerdown disables drivers and reduces supply current to 1 µA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

图 8-5. INVALID Propagation Delay Times and Driver Enabling Time

9 Detailed Description

9.1 Device Functional Modes

表 9-1. Each Driver

INPUTS(1)				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 9-2. Each Receiver

INPUTS(1)			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

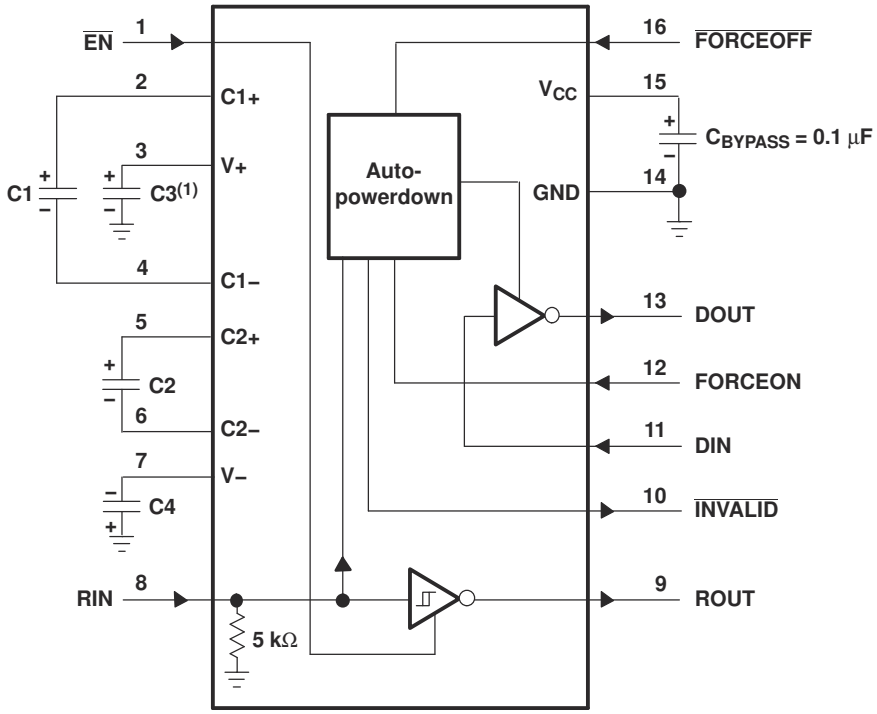
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

10 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

图 10-1. Typical Operating Circuit and Capacitor Values

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C3221EDB	ACTIVE	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E	Samples
SN65C3221EDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E	Samples
SN65C3221EPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU221E	Samples
SN75C3221EDB	ACTIVE	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MY221E	Samples
SN75C3221EDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MY221E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

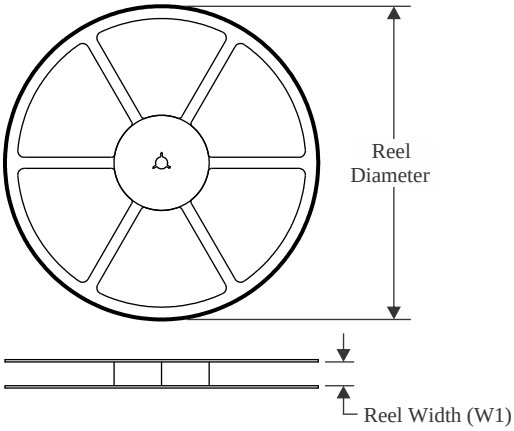
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

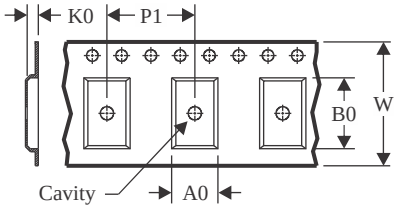
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

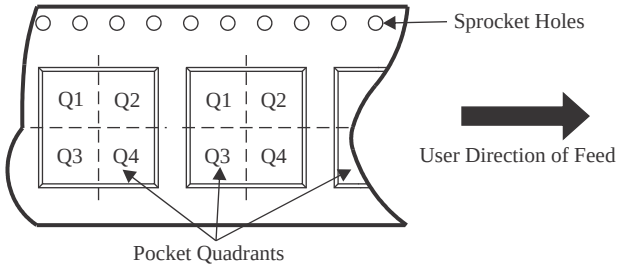


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

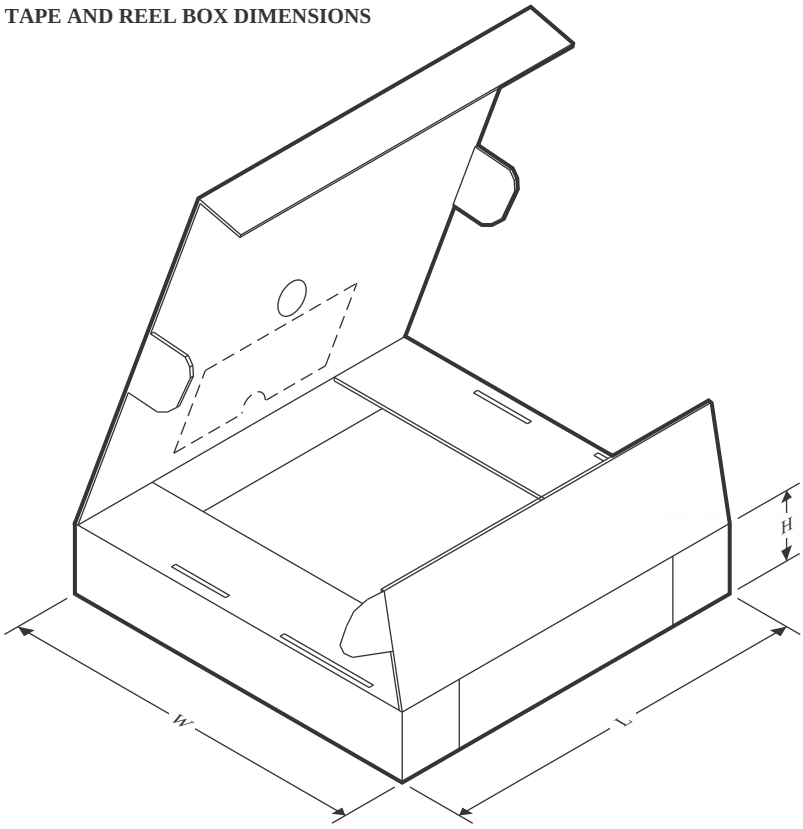
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3221EDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN65C3221EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75C3221EDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

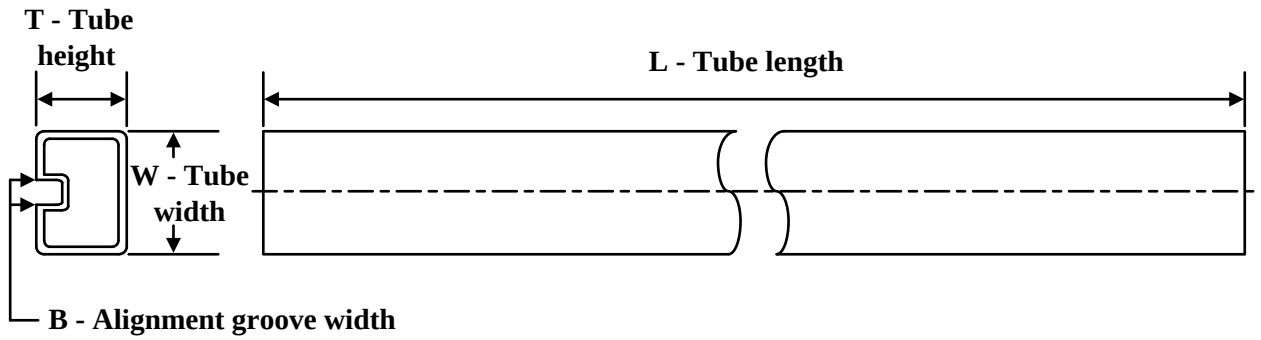
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3221EDBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN65C3221EPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN75C3221EDBR	SSOP	DB	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

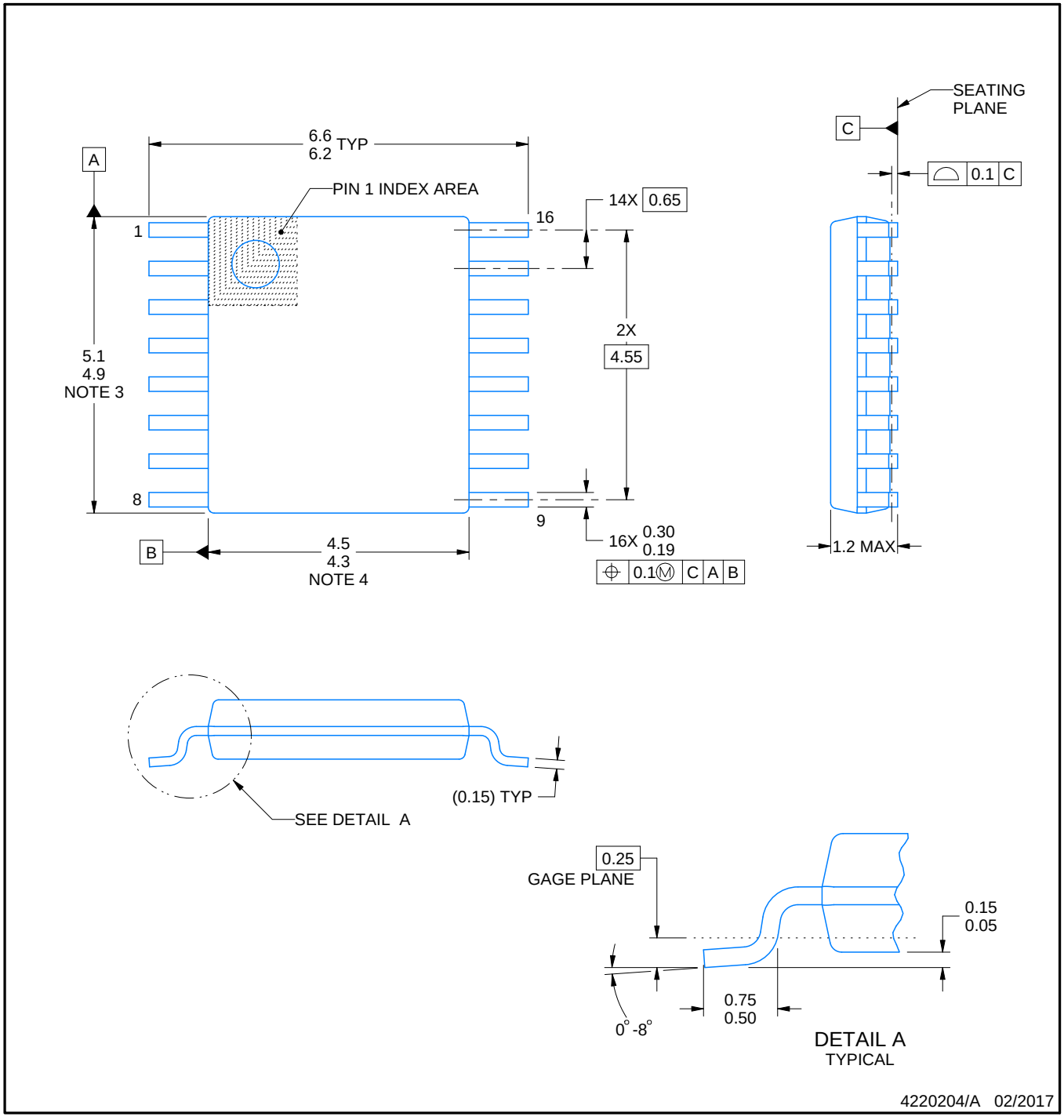
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65C3221EDB	DB	SSOP	16	80	530	10.5	4000	4.1
SN75C3221EDB	DB	SSOP	16	80	530	10.5	4000	4.1

PACKAGE OUTLINE

PW0016A

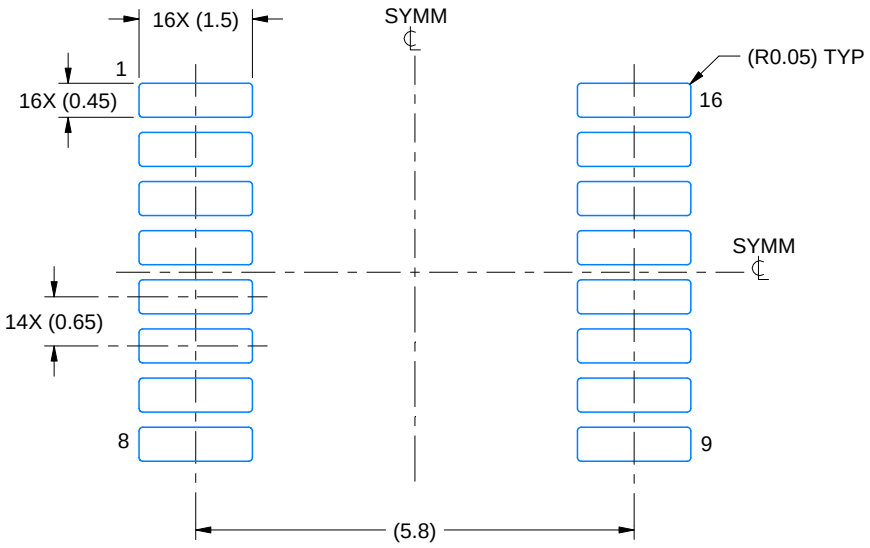
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

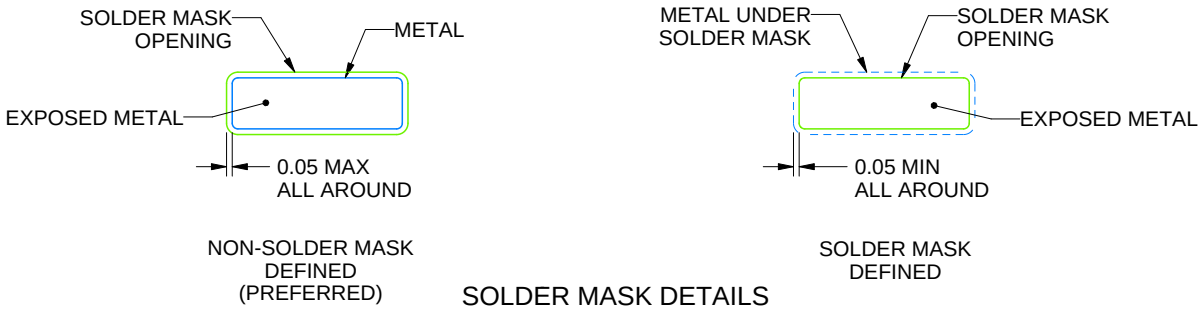


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

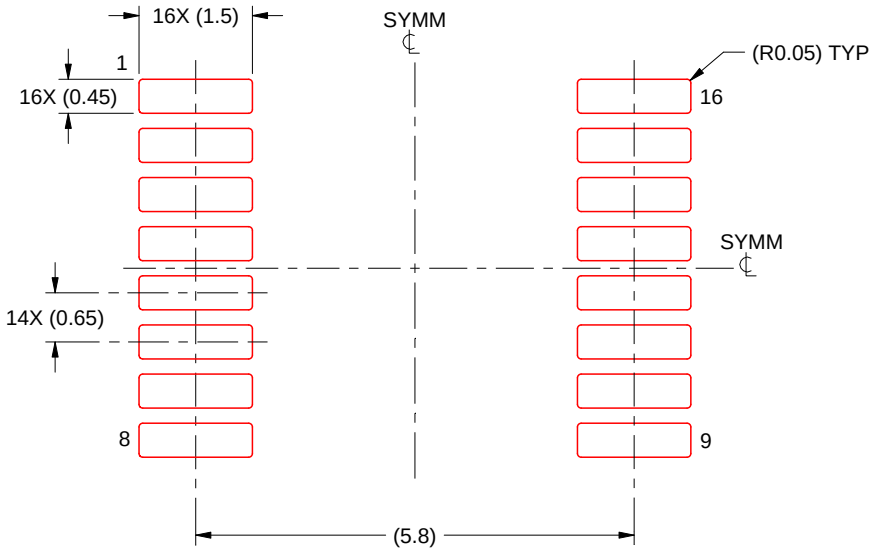


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

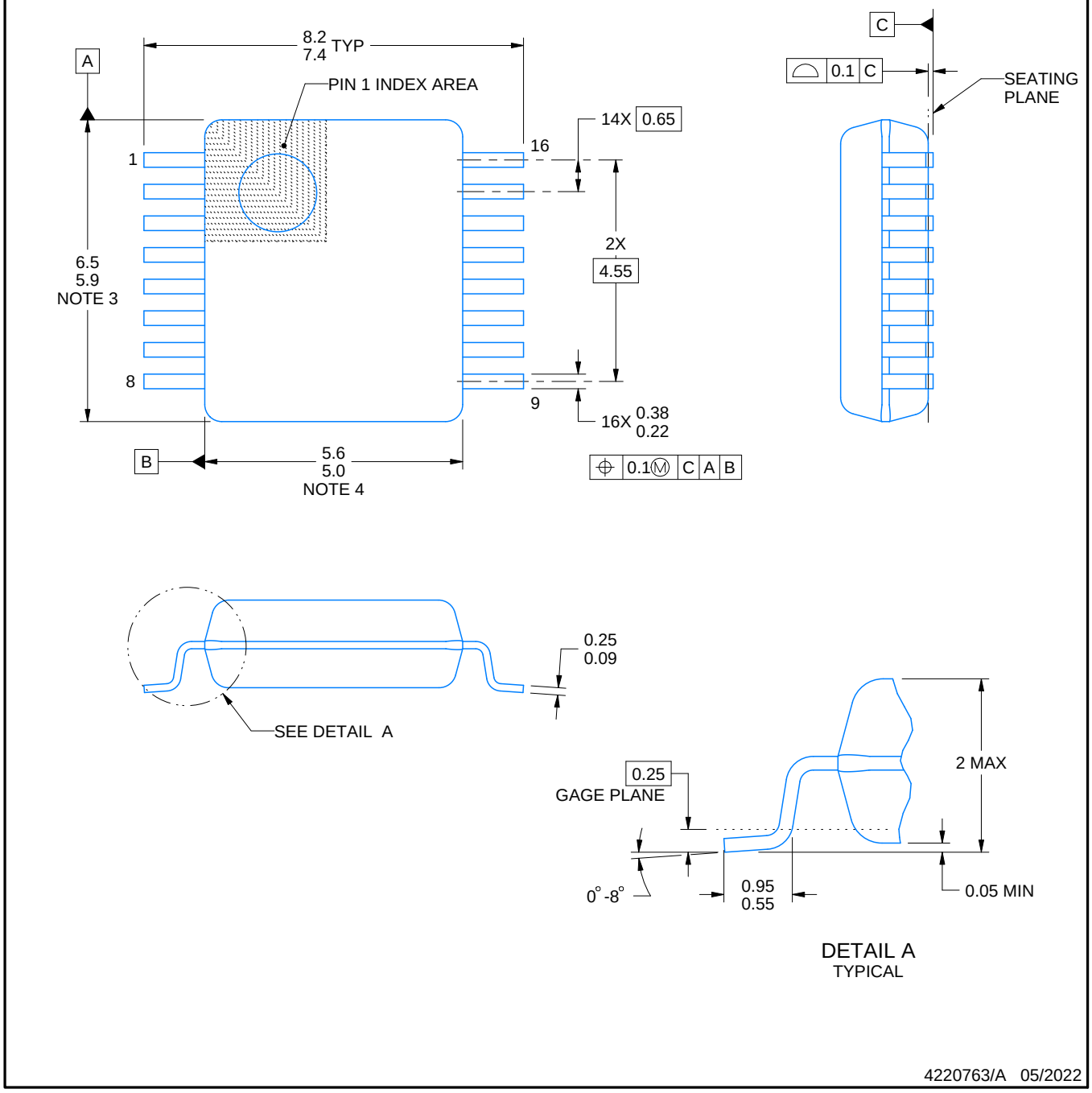
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

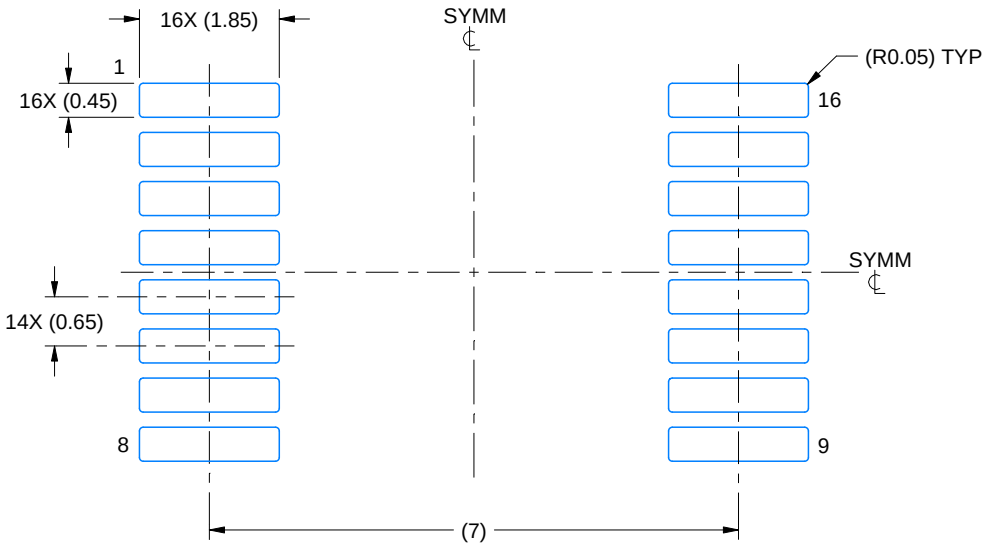
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

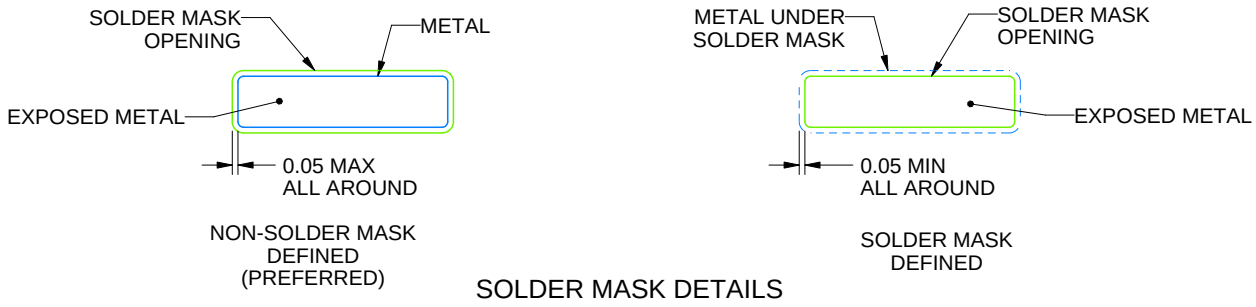


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

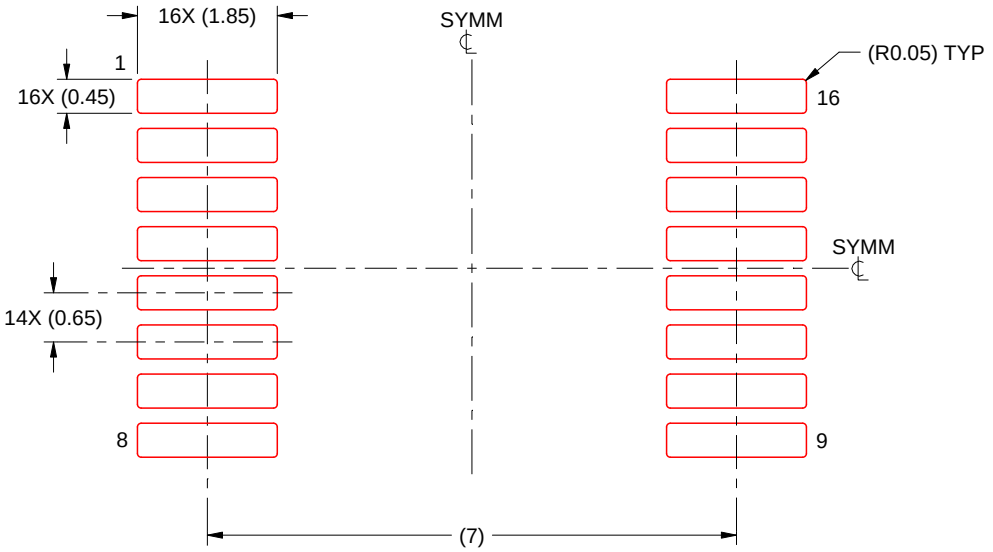


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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