

## DS90CF563/DS90CF564 LVDS 18-Bit Color Flat Panel Display (FPD) Link - 65 MHz

Check for Samples: [DS90CF563](#), [DS90CF564](#)

### FEATURES

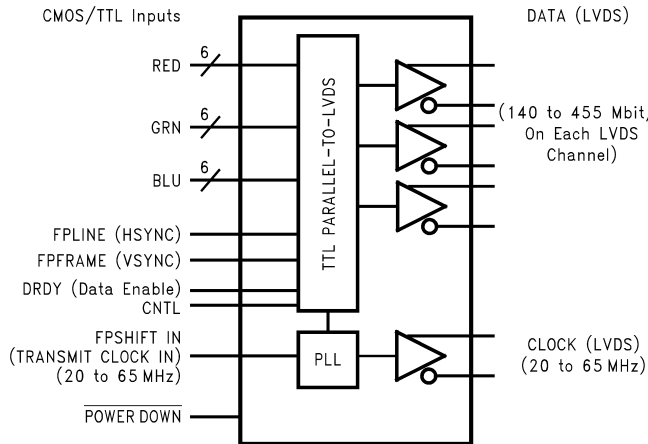
- 20 to 65 MHz Shift Clk Support
- Up to 171 Mbytes/s Bandwidth
- Cable Size is Reduced to Save Cost
- 290 mV Swing LVDS Devices for Low EMI
- Low Power CMOS Design (< 550 mW typ)
- Power-down Mode Saves Power (< 0.25 mW)
- PLL Requires No External Components
- Low Profile 48-Lead TSSOP Package
- Falling Edge Data Strobe
- Compatible with TIA/EIA-644 LVDS Standard
- Single Pixel Per Clock XGA (1024 x 768)
- Supports VGA, SVGA, XGA and Higher
- 1.3 Gbps Throughput

### DESCRIPTION

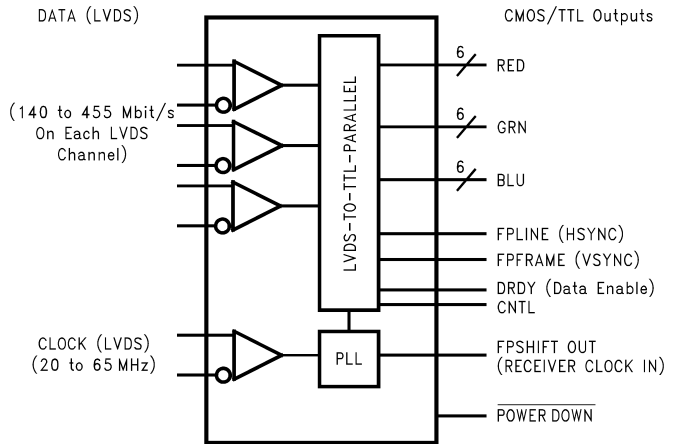
The DS90CF563 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CF564 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 171 Mbytes per second. These devices are offered with falling edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

### Block Diagram



**Figure 1. DS90CF563**  
DS90CF563MTD is no longer available.



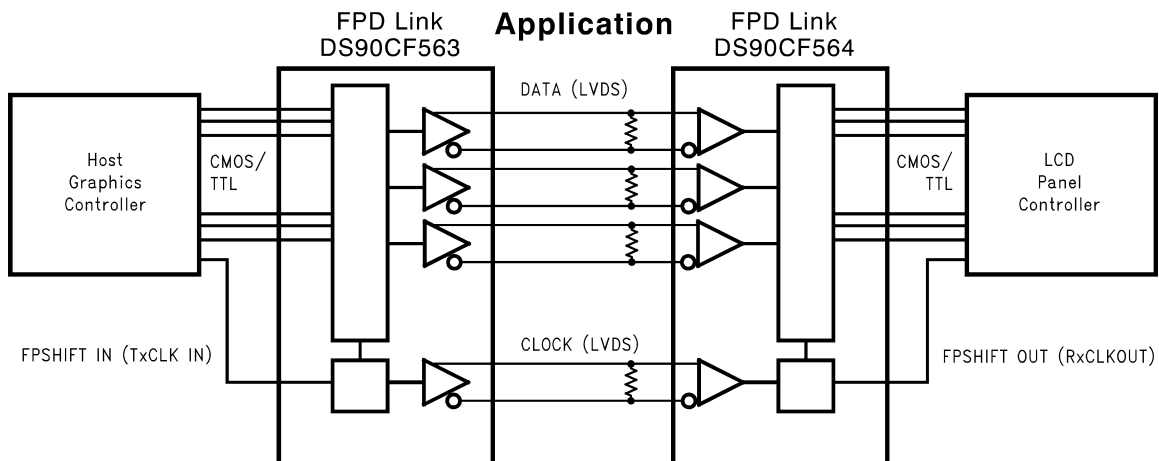
**Figure 2. DS90CF564**  
See Package Number DGG0048A



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### Application



### Absolute Maximum Ratings<sup>(1)(2)</sup>

Supply Voltage ( $V_{CC}$ )	-0.3V to +6V		
CMOS/TTL Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )		
CMOS/TTL Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )		
LVDS Receiver Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )		
LVDS Driver Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )		
LVDS Output Short Circuit Duration	Continuous		
Junction Temperature	+150°C		
Storage Temperature	-65°C to +150°C		
Lead Temperature (Soldering, 4 sec)	+260°C		
Maximum Package Power Dissipation @ +25°C	DGG0048A (TSSOP) Package:	DS90CF563	1.98W
		DS90CF564	1.89W
	Package Derating:	DS90CF563	16 mW/°C above +25°C
		DS90CF564	15 mW/°C above +25°C

This device does not meet 2000V ESD rating<sup>(3)</sup>.

- (1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (2) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The "Electrical Characteristics" specify conditions for device operation.
- (3) ESD Rating: HBM (1.5 kΩ, 100 pF) PLL  $V_{CC} \geq 1000V$  All other pins  $\geq 2000V$  EIAJ (0Ω, 200 pF)  $\geq 150V$

### Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage ( $V_{CC}$ )	4.75	5.0	5.25	V
Operating Free Air Temperature ( $T_A$ )	-10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage ( $V_{CC}$ )			100	mV <sub>P-P</sub>

### Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS/TTL DC SPECIFICATIONS</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Low Level Input Voltage		GND		0.8	V
$V_{OH}$	High Level Output Voltage	$I_{OH} = -0.4$ mA	3.8	4.9		V
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 2$ mA		0.1	0.3	V

## Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18 \text{ mA}$		-0.7 9	-1.5	V	
$I_{IN}$	Input Current	$V_{IN} = V_{CC}, \text{GND}, 2.5\text{V}$ or $0.4\text{V}$		$\pm 5.1$	$\pm 10$	$\mu\text{A}$	
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0\text{V}$			-120	$\text{mA}$	
<b>LVDS DRIVER DC SPECIFICATIONS</b>							
$V_{OD}$	Differential Output Voltage	$R_L = 100\Omega$	250	290	450	mV	
$\Delta V_{OD}$	Change in $V_{OD}$ between Complementary Output States				35	mV	
$V_{CM}$	Common Mode Voltage		1.1	1.25	1.37 5	V	
$\Delta V_{CM}$	Change in $V_{CM}$ between Complementary Output States				35	mV	
$V_{OH}$	High Level Output Voltage			1.3	1.6	V	
$V_{OL}$	Low Level Output Voltage		0.9	1.01		V	
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0\text{V}, R_L = 100\Omega$		-2.9	-5	$\text{mA}$	
$I_{OZ}$	Output TRI-STATE Current	Power Down = $0\text{V}$ , $V_{OUT} = 0\text{V}$ or $V_{CC}$		$\pm 1$	$\pm 10$	$\mu\text{A}$	
<b>LVDS RECEIVER DC SPECIFICATIONS</b>							
$V_{TH}$	Differential Input High Threshold	$V_{CM} = +1.2\text{V}$			+100	mV	
$V_{TL}$	Differential Input Low Threshold		-100			mV	
$I_{IN}$	Input Current	$V_{IN} = +2.4\text{V}$	$V_{CC} = 5.5\text{V}$		$\pm 10$	$\mu\text{A}$	
		$V_{IN} = 0\text{V}$			$\pm 10$	$\mu\text{A}$	
<b>TRANSMITTER SUPPLY CURRENT</b>							
$I_{CCTW}$	Transmitter Supply Current, Worst Case	$R_L = 100\Omega, C_L = 5 \text{ pF}$ , Worst Case Pattern (Figure 3, Figure 5)	$f = 32.5 \text{ MHz}$		49	63	$\text{mA}$
			$f = 37.5 \text{ MHz}$		51	64	$\text{mA}$
			$f = 65 \text{ MHz}$		70	84	$\text{mA}$
$I_{CCTG}$	Transmitter Supply Current, 16 Grayscale	$R_L = 100\Omega, C_L = 5 \text{ pF}$ , 16 Grayscale Pattern (Figure 4, Figure 5)	$f = 32.5 \text{ MHz}$		40	55	$\text{mA}$
			$f = 37.5 \text{ MHz}$		41	55	$\text{mA}$
			$f = 65 \text{ MHz}$		55	67	$\text{mA}$
$I_{CCTZ}$	Transmitter Supply Current, Power Down	Power Down = Low			1	25	$\mu\text{A}$
<b>RECEIVER SUPPLY CURRENT</b>							
$I_{CCRW}$	Receiver Supply Current, Worst Case	$C_L = 8 \text{ pF}$ , Worst Case Pattern (Figure 3, Figure 6)	$f = 32.5 \text{ MHz}$		64	77	$\text{mA}$
			$f = 37.5 \text{ MHz}$		70	85	$\text{mA}$
			$f = 65 \text{ MHz}$		110	140	$\text{mA}$
$I_{CCRG}$	Receiver Supply Current, 16 Grayscale	$C_L = 8 \text{ pF}$ , 16 Grayscale Pattern (Figure 4, Figure 6)	$f = 32.5 \text{ MHz}$		35	55	$\text{mA}$
			$f = 37.5 \text{ MHz}$		37	55	$\text{mA}$
			$f = 65 \text{ MHz}$		55	67	$\text{mA}$
$I_{CCRZ}$	Receiver Supply Current, Power Down	Power Down = Low			1	10	$\mu\text{A}$

## Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 5)		0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 5)		0.75	1.5	ns
TCIT	TxCLK IN Transition Time (Figure 7)			8	ns
TCCS	TxOUT Channel-to-Channel Skew <sup>(1)</sup> (Figure 8)			350	ps

(1) This limit based on bench characterization.

## Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V <sub>CC</sub> = 5.0V (Figure 11)	3.5		8.5	ns	
TCIP	TxCLK IN Period (Figure 9)	15	T	50	ns	
TCIH	TxCLK IN High Time (Figure 9)	0.35T	0.5T	0.65T	ns	
TCIL	TxCLK IN Low Time (Figure 9)	0.35T	0.5T	0.65T	ns	
TSTC	TxIN Setup to TxCLK IN (Figure 9)	f = 65 MHz	5	3.5	ns	
THTC	TxIN Hold to TxCLK IN (Figure 9)		2.5	1.5	ns	
TPDD	Transmitter Powerdown Delay (Figure 20)			100	ns	
TPLLS	Transmitter Phase Lock Loop Set (Figure 13)			10	ms	
TPPos0	Transmitter Output Pulse Position 0 (Figure 15)		-0.30	0	0.30	ns
TPPos1	Transmitter Output Pulse Position 1		1.70	1/7 T <sub>clk</sub>	2.50	ns
TPPos2	Transmitter Output Pulse Position 2		3.60	2/7 T <sub>clk</sub>	4.50	ns
TPPos3	Transmitter Output Pulse Position 3		5.90	3/7 T <sub>clk</sub>	6.75	ns
TPPos4	Transmitter Output Pulse Position 4		8.30	4/7 T <sub>clk</sub>	9.00	ns
TPPos5	Transmitter Output Pulse Position 5		10.40	5/7 T <sub>clk</sub>	11.10	ns
TPPos6	Transmitter Output Pulse Position 6		12.70	6/7 T <sub>clk</sub>	13.40	ns

## Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units	
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 6)		2.5	4.0	ns	
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 6)		2.0	3.5	ns	
RCOP	RxCLK OUT Period		15	T	50	ns
RCOH	RxCLK OUT High Time	f = 65 MHz	7.8	9	ns	
RCOL	RxCLK OUT Low Time	f = 65 MHz	3.8	5	ns	
RSRC	RxOUT Setup to RxCLK OUT	f = 65 MHz	2.5	4.2	ns	
RHRC	RxOUT Hold to RxCLK OUT	f = 65 MHz	4.0	5.2	ns	
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V <sub>CC</sub> = 5.0V (Figure 12)		6.4		10.7	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 14)			10	ms	
RSKM	RxIN Skew Margin <sup>(1)</sup> (Figure 16)	V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C	600		ps	
RPDD	Receiver Powerdown (Figure 19)			1	μs	

- (1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output skew (TCCS) and the setup and hold time (internal data sampling window), allowing for LVDS cable skew dependent on type/length and source clock (TxCLK IN) jitter.

$$RSKM \geq \text{cable skew (the, length)} + \text{source clock jitter (cycle to cycle)}$$

AC Timing Diagrams

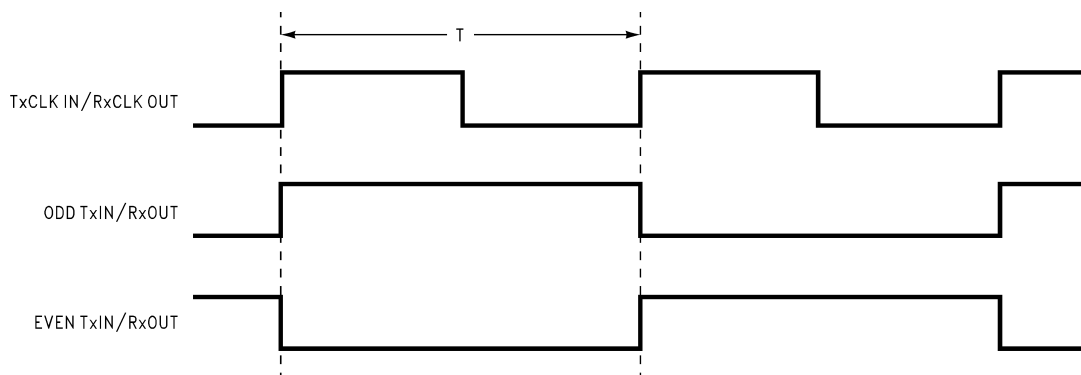
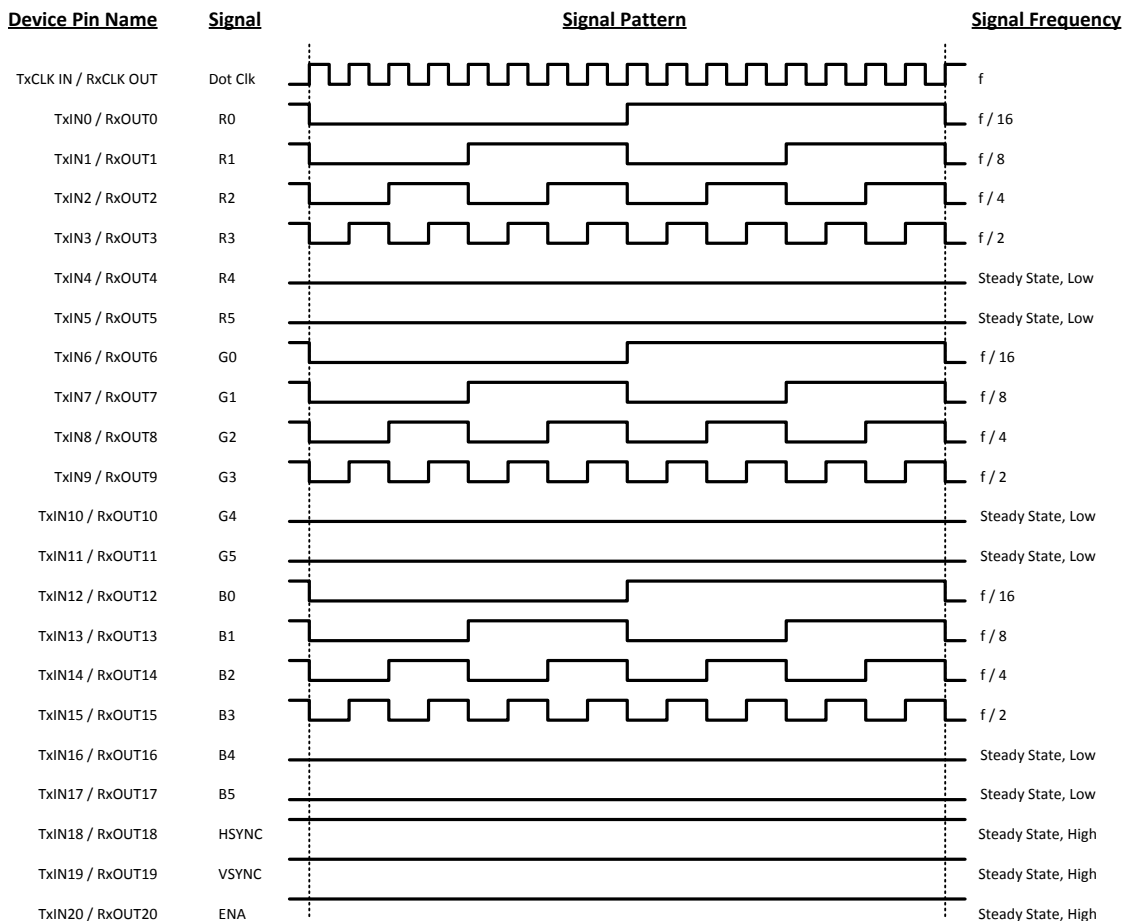


Figure 3. "Worst Case" Test Pattern



- (1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.
- (2) The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
- (3) Figure 3 and Figure 4 show a falling edge data strobe (TxCLK IN/RxCLK OUT).
- (4) Recommended pin to signal mapping. Customer may choose to define differently.

Figure 4. "16 Grayscale" Test Pattern

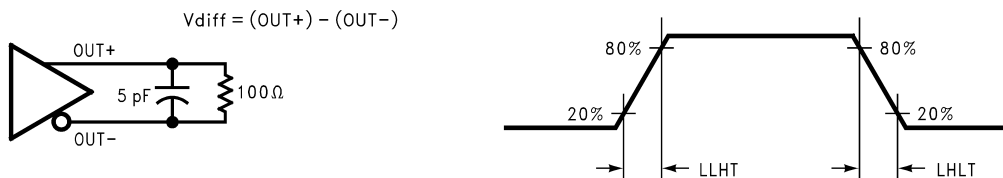


Figure 5. DS90CF563 (Transmitter) LVDS Output Load and Transition Times



Figure 6. DS90CF564 (Receiver) CMOS/TTL Output Load and Transition Times

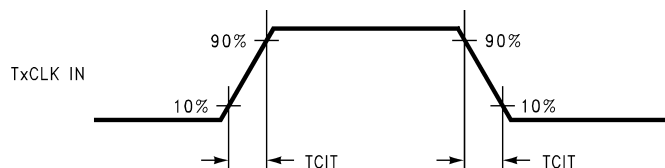
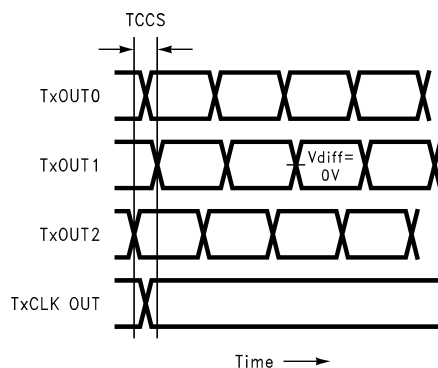


Figure 7. DS90CF563 (Transmitter) Input Clock Transition Time



**Note:** Measurements at  $V_{diff} = 0V$   
**Note:** TCSS measured between earliest and latest LVDS edges.  
**Note:** TxCLK Differential High→Low Edge

Figure 8. DS90CF563 (Transmitter) Channel-to-Channel Skew and Pulse Width

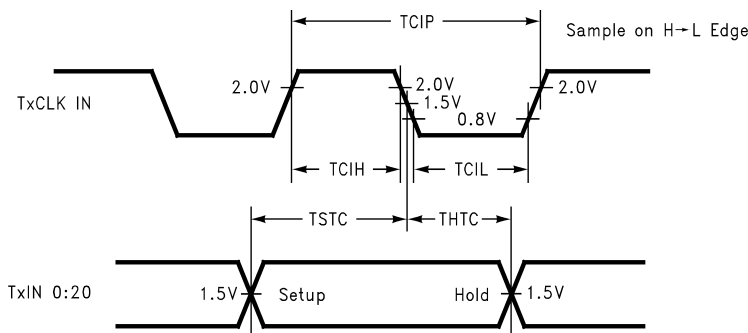


Figure 9. DS90CF563 (Transmitter) Setup/Hold and High/Low Times

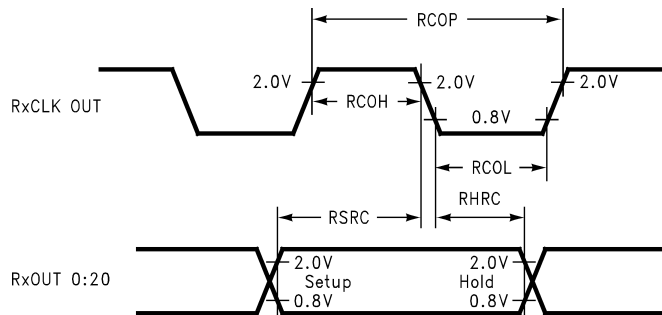


Figure 10. DS90CF564 (Receiver) Clock In to Clock Out Delay

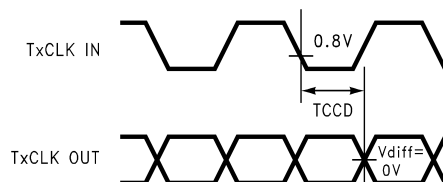


Figure 11. DS90CF563 (Transmitter) Clock In to Clock Out Delay

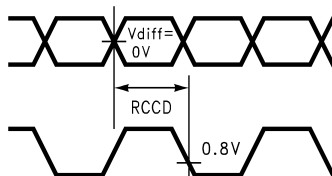


Figure 12. DS90CF564 (Receiver) Clock In to Clock Out Delay

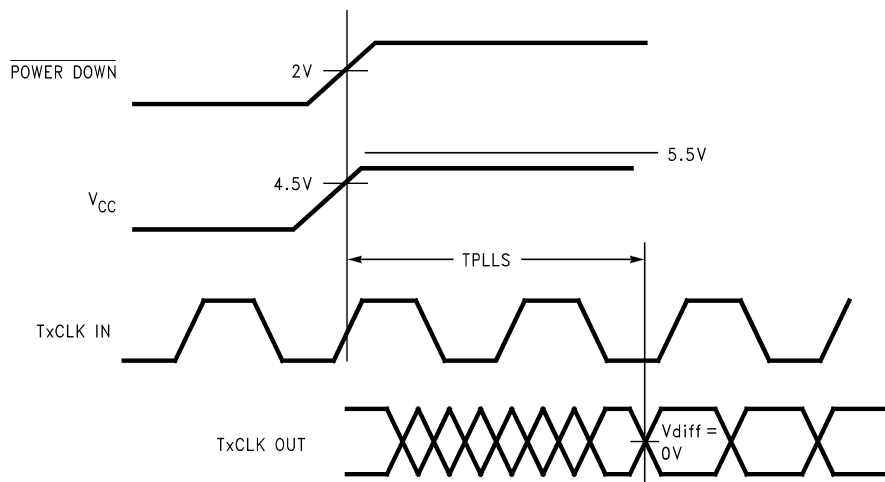


Figure 13. DS90CF563 (Transmitter) Phase Lock Loop Set Time

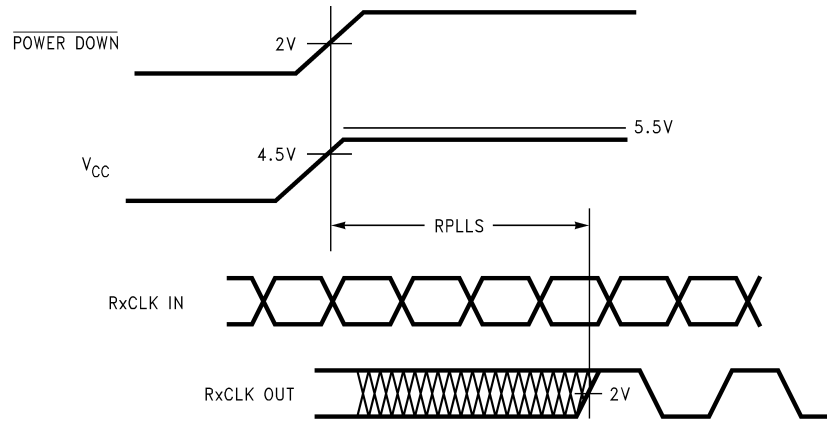


Figure 14. DS90CF564 (Receiver) Phase Lock Loop Set Time

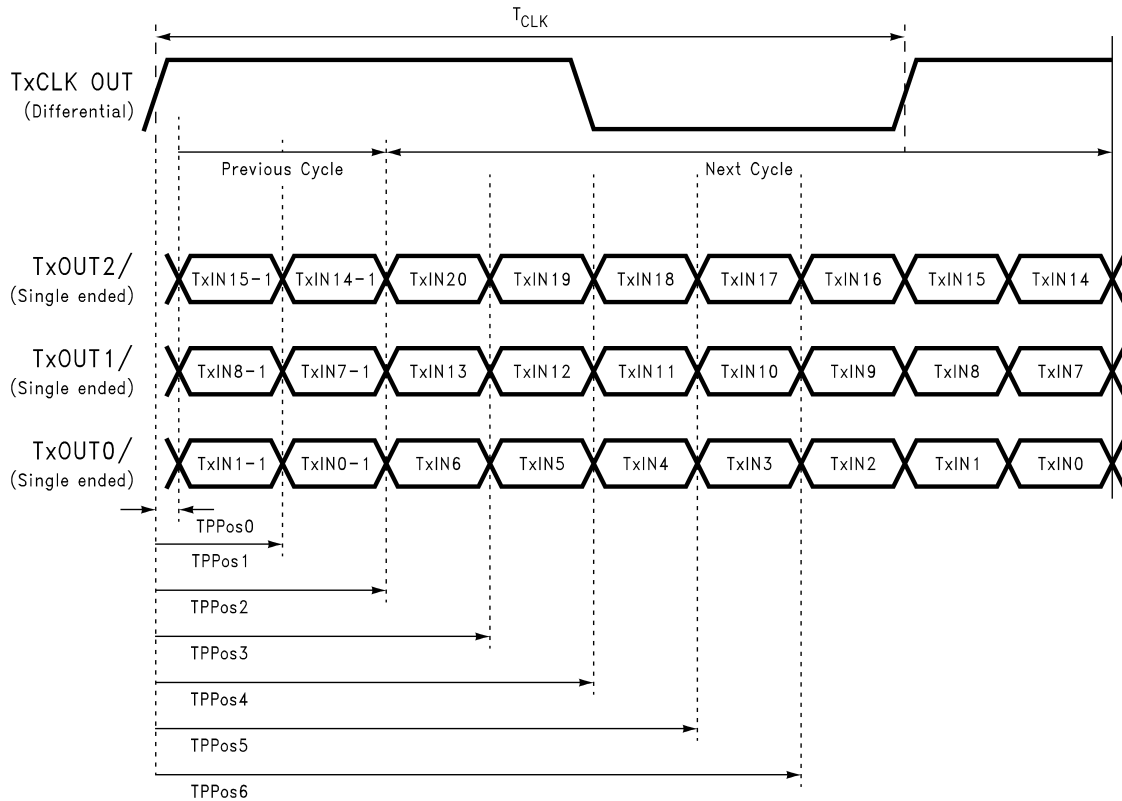
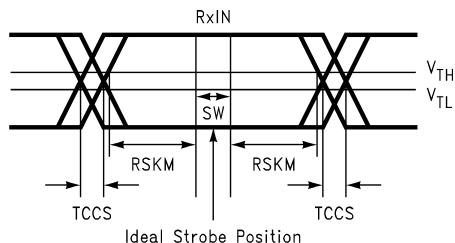


Figure 15. Transmitter LVDS Output Pulse Position Measurement





SW—Setup and Hold Time (Internal Data Sampling Window)  
 TCCS—Transmitter Output Skew  
 $RSKM \geq \text{Cable Skew (type, length)} + \text{Source Clock Jitter (cycle to cycle)}$   
 Cable Skew—typically 10 ps–40 ps per foot

Figure 16. Receiver LVDS Input Skew Margin

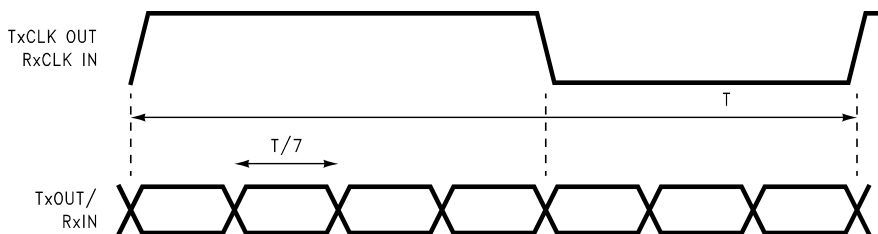


Figure 17. Seven Bits of LVDS in One Clock Cycle

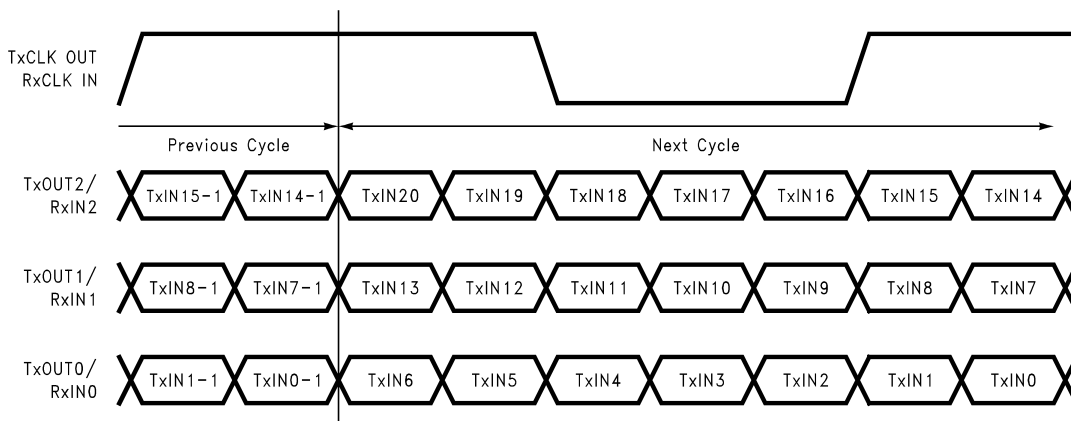


Figure 18. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CF563)

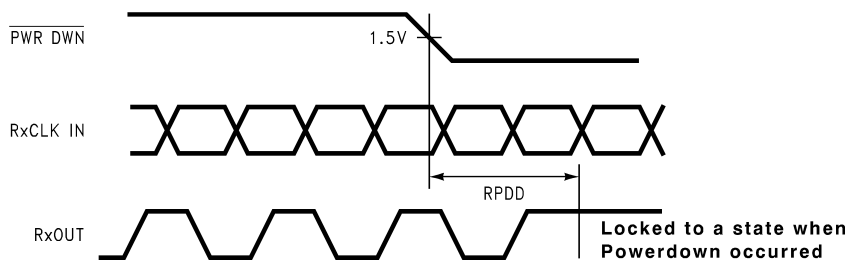


Figure 19. Receiver Powerdown Delay

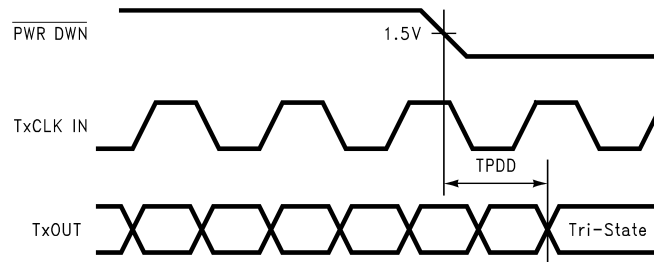


Figure 20. Transmitter Powerdown Delay

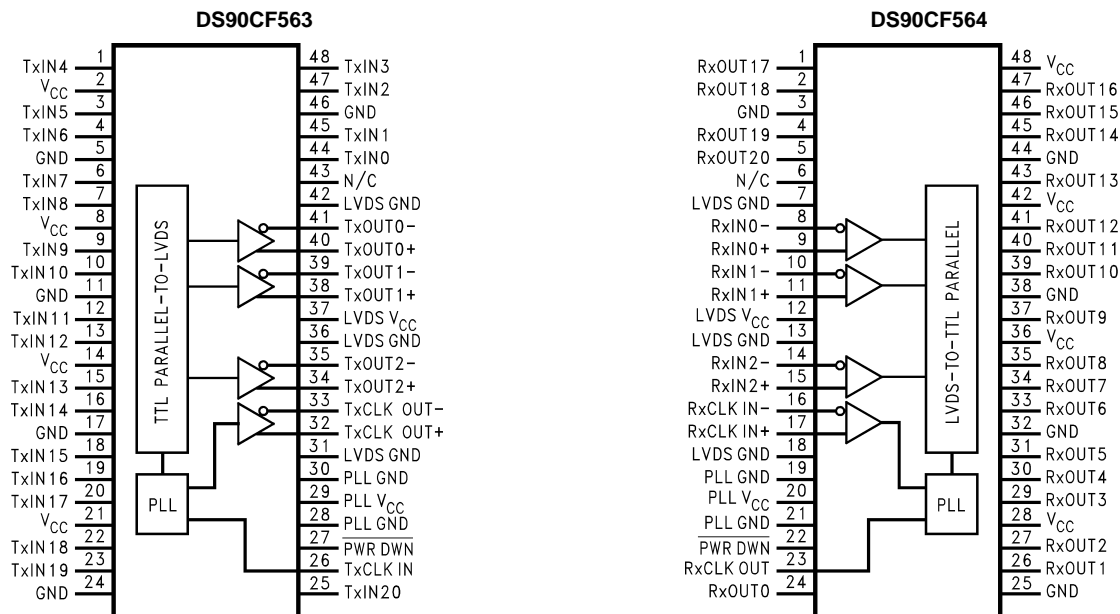
**DS90CF563 Pin Descriptions—FPD Link Transmitter**

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable)
TxOUT+	O	3	Positive LVDS differential data output
TxOUT-	O	3	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT-	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V <sub>CC</sub>	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V <sub>CC</sub>	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

**DS90CF564 Pin Descriptions—FPD Link Receiver**

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs
RxIN-	I	3	Negative LVDS differential data inputs
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY(also referred to as HSYNC, VSYNC, Data Enable)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN-	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) maintains the receiver outputs in the previous state
V <sub>CC</sub>	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V <sub>CC</sub>	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs



**Connection Diagram**



## REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format .....	11

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CF564MTD/NOPB	ACTIVE	TSSOP	DGG	48	38	RoHS & Green	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF564MTD >B	
DS90CF564MTDX/NOPB	ACTIVE	TSSOP	DGG	48	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF564MTD >B	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CF564MTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CF564MTDX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0

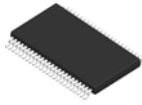


**TUBE**


\*All dimensions are nominal

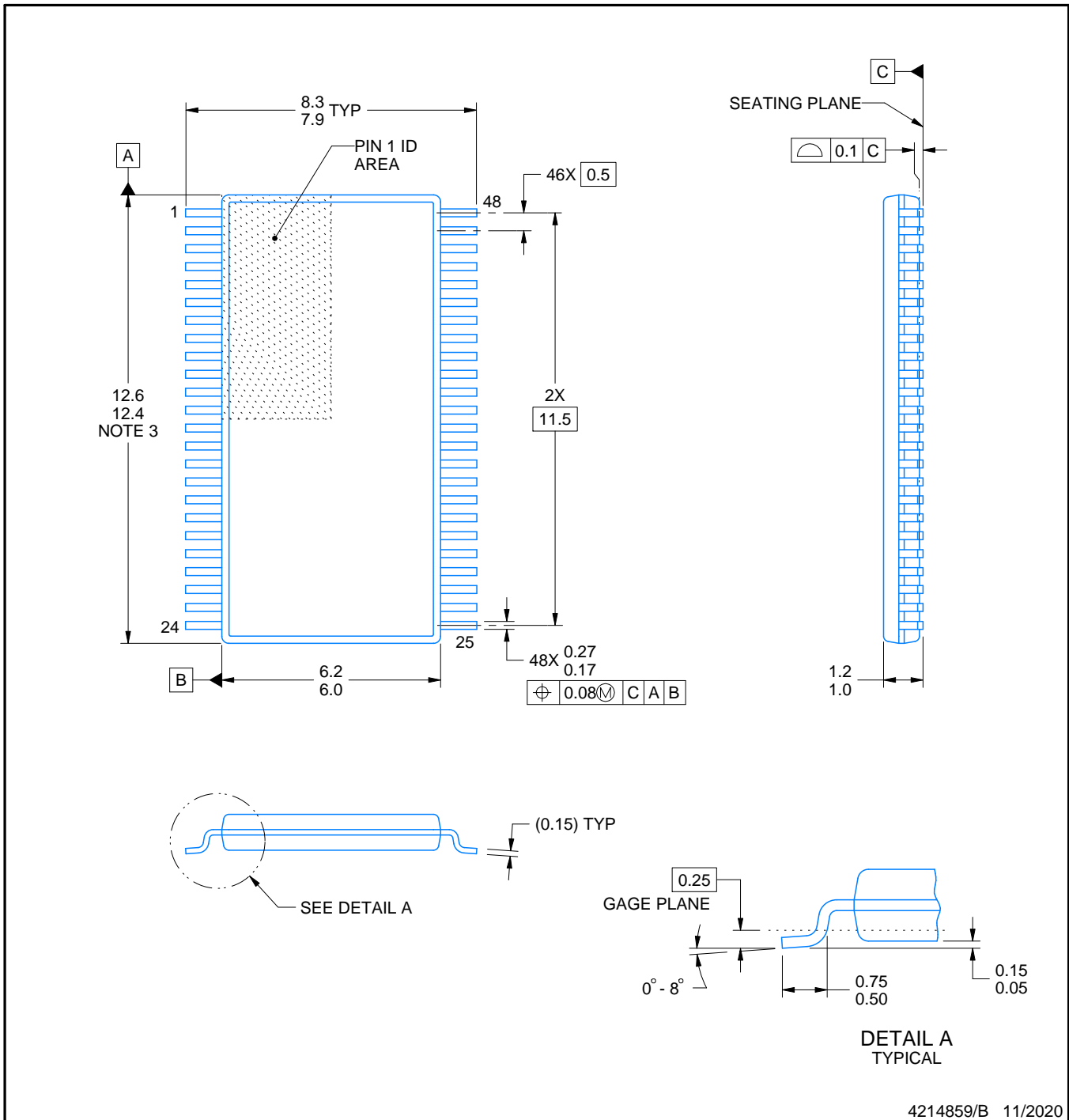
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS90CF564MTD/NOPB	DGG	TSSOP	48	38	495	10	2540	5.79

DGG0048A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4214859/B 11/2020

NOTES:

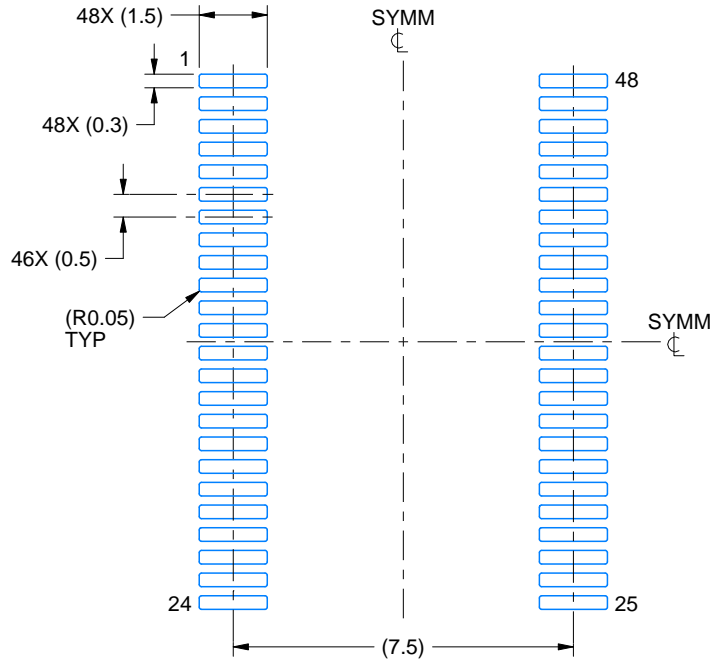
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

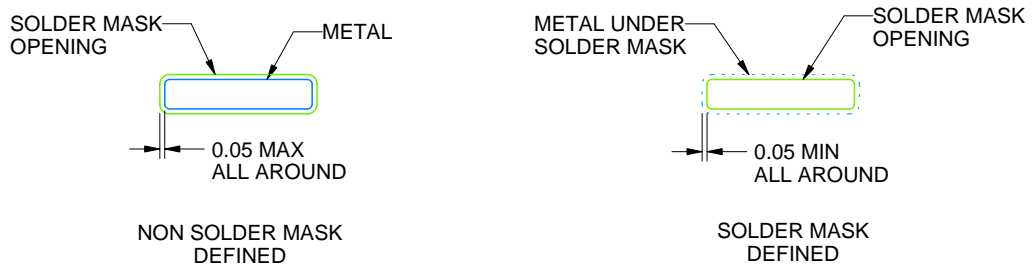
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

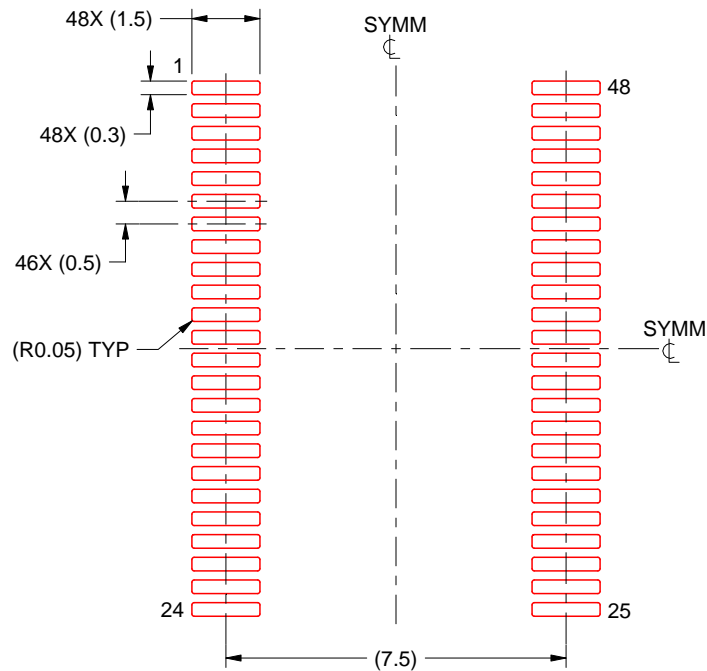
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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