HD3SS212 5.4Gbps DisplayPort 1.2 2 选 1 差动开关

1 特性

- 与Displayport 1.2的电气标准兼容
- 2:1开关支持的最高数据速率为5.4Gbps
- 支持热插拔检测(HPD)开关
- 在5.4 GHz上宽-3dB差分带宽(BW)
- 出色的动态特性（2.7GHz情况下）
  - 串扰 = -50dB
  - 隔音 = -22dB
  - 插入损耗 = –1.4dB
  - 回波损耗 = –11dB
  - 最大位到位失真 = 4ps
- 漏极电源电压电压(VDD)运行范围3.3V ± 10%
- 小型 5mm x 5mm x 1mm，48 焊球 u*BGA 封装方式
- 输出使能 (OE) 引脚禁用开关以省电
- 功耗
  - HD3SS212 < 10mW（待机功耗 < 30µW，此时，OE = L）在整个文档内将

2 应用

- 需要 DP 和 PCI Express 的 主板 应用
- 台式电脑
- 笔记本电脑
- 底座

3 说明

HD3SS212 是一款高速无源开关，能够在应用中将两个完全 DisplayPort 4 通道端口从两个源之一切换到一个目标位置。对于 DisplayPort 应用， HD3SS212 还支持在辅助 (AUX) 和热插拔检测 (HPD) 信号间切换。HPD 路径是一个缓冲器，此缓冲器在 HPDC 线路上要求一个 125kΩ 下拉电阻。

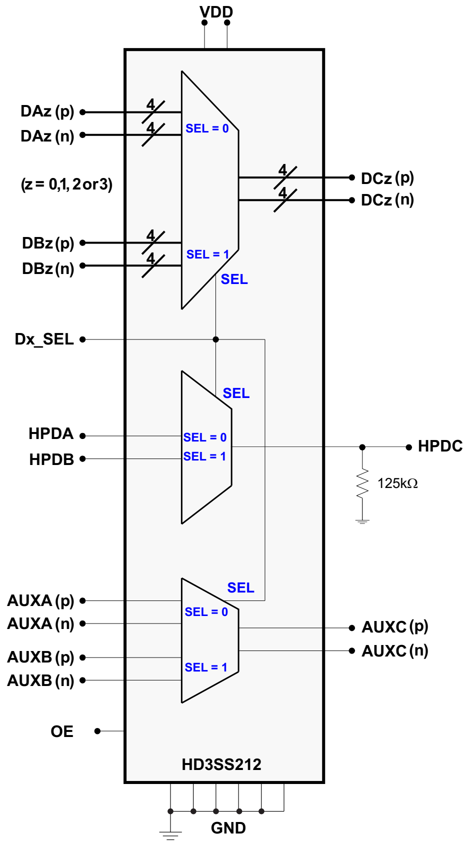
一个典型应用将是包含 2 个图形处理单元 (GPU) 的主板，这些处理单元需要驱动一个 DisplayPort 负输出。GPU 由 Dx_SEL 引脚选择。HD3SS212 采用 48 焊球球状引脚栅格阵列 (BGA) 封装方式并在 -40°C 至 105°C 的完全工业温度范围内由 3.3V 单电源供电运行。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
HD3SS212	BGA MicroStar Junior (48)	5.00mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

功能方框图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (January 2014) to Revision C

	Page
• 已添加 器件信息表，ESD 额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。	1
• 已删除 订购信息表。请参见数据表末尾的 POA。	1

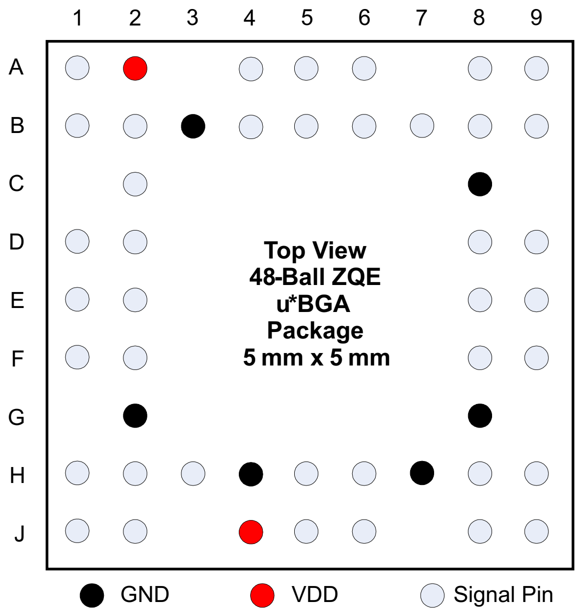
Changes from Revision A (March 2012) to Revision B

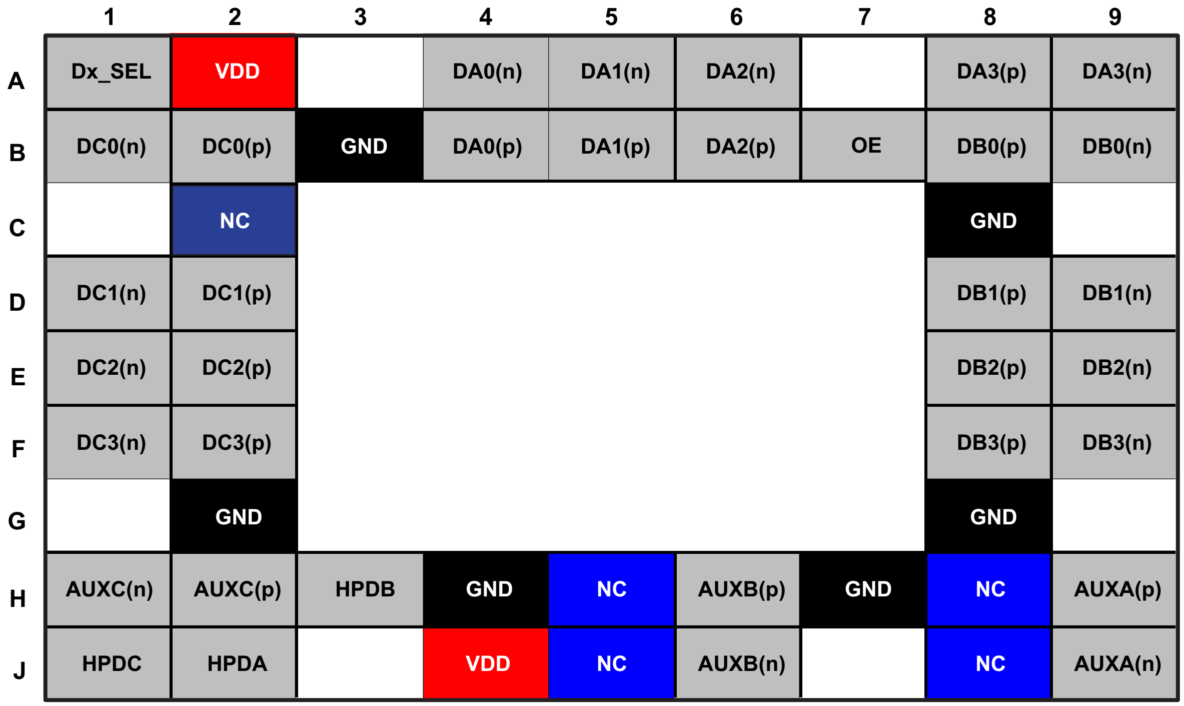
	Page
• 已更改 $\overline{\text{OE}}$ 更改为 OE	1

Changes from Original (December 2011) to Revision A

	Page
• 已更改 说明， 从“–40°C 到 85°C 的整个工业温度范围”更改为“–40°C 到 105°C 的整个工业温度范围”	1
• Added Operating Temperature to the Abs Max Table	5
• Changed the Operating free-air temperature From MAX = 85°C To: 105°C	5
• Changed the values of ψ_{JT} and ψ_{JB} in the Thermal Information table	5
• Changed the MAX value of Leakage current (Dx_SEL), VDD = 0 V From: 8µA To: 10µA	6

5 Pin Configuration and Function





	1	2	3	4	5	6	7	8	9
A	Dx_SEL	VDD		DA0(n)	DA1(n)	DA2(n)		DA3(p)	DA3(n)
B	DC0(n)	DC0(p)	GND	DA0(p)	DA1(p)	DA2(p)	OE	DB0(p)	DB0(n)
C		NC						GND	
D	DC1(n)	DC1(p)						DB1(p)	DB1(n)
E	DC2(n)	DC2(p)						DB2(p)	DB2(n)
F	DC3(n)	DC3(p)						DB3(p)	DB3(n)
G		GND						GND	
H	AUXC(n)	AUXC(p)	HPDB	GND	NC	AUXB(p)	GND	NC	AUXA(p)
J	HPDC	HPDA		VDD	NC	AUXB(n)		NC	AUXA(n)

Pin Functions

PIN	PIN NAME	I/O	DESCRIPTION
A1	Dx_SEL	Control I	High Speed Port Selection Control Pins
B4 A4	DA0(p) DA0(n)	I/O	Port A, Channel 0, High Speed Positive Signal Port A, Channel 0, High Speed Negative Signal
B5 A5	DA1(p) DA1(n)	I/O	Port A, Channel 1, High Speed Positive Signal Port A, Channel 1, High Speed Negative Signal
B6 A6	DA2(p) DA2(n)	I/O	Port A, Channel 2, High Speed Positive Signal Port A, Channel 2, High Speed Negative Signal
A8 A9	DA3(p) DA3(n)	I/O	Port A, Channel 3, High Speed Positive Signal Port A, Channel 3, High Speed Negative Signal
B8 B9	DB0(p) DB0(n)	I/O	Port B, Channel 0, High Speed Positive Signal Port B, Channel 0, High Speed Negative Signal
D8 D9	DB1(p) DB1(n)	I/O	Port B, Channel 1, High Speed Positive Signal Port B, Channel 1, High Speed Negative Signal
E8 E9	DB2(p) DB2(n)	I/O	Port B, Channel 2, High Speed Positive Signal Port B, Channel 2, High Speed Negative Signal
F8 F9	DB3(p) DB3(n)	I/O	Port B, Channel 3, High Speed Positive Signal Port B, Channel 3, High Speed Negative Signal
B2 B1	DC0(p) DC0(n)	I/O	Port C, Channel 0, High Speed Positive Signal Port C, Channel 0, High Speed Negative Signal
D2 D1	DC1(p) DC1(n)	I/O	Port C, Channel 1, High Speed Positive Signal Port C, Channel 1, High Speed Negative Signal
E2 E1	DC2(p) DC2(n)	I/O	Port C, Channel 2, High Speed Positive Signal Port C, Channel 2, High Speed Negative Signal
F2 F1	DC3(p) DC3(n)	I/O	Port C, Channel 3, High Speed Positive Signal Port C, Channel 3, High Speed Negative Signal
H9 J9	AUXA(p) AUXA(n)	I/O	Port A AUX Positive Signal Port A AUX Negative Signal
H6 J6	AUXB(p) AUXB(n)	I/O	Port B AUX Positive Signal Port B AUX Negative Signal
H2 H1	AUXC(p) AUXC(n)	I/O	Port C AUX Positive Signal Port C AUX Negative Signal
J2, H3, J1	HPDA/B/C	I/O	Port A/B/C Hot Plug Detect
B7	OE	I	Output Enable
A2, J4	VDD	Supply	3.3V Positive power supply voltage
B3, C8, G2, G8, H4, H7	GND	Supply	Negative power supply voltage
C2, H5, H8, J5, J8	NC		Electrically not connected

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Supply voltage range (3)	VDD	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control pin	–0.5	VCC +0.5	V
Operating free-air temperature		–40	105	°C
Continuous power dissipation		See *Thermal Information*		
Storage temperature		–55	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±4000	V
		Charged-device model (CDM) (2)	±1000	

(1) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(2) Tested in accordance with JEDEC Standard 22, Test Method A115-A

6.3 Recommended Operating Conditions

Nominal values for all parameters are at V_{CC} = 3.3V and T_A = 25°C, all temperature limits are specified by design

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage	Control Pins, Signal Pins (Dx_SEL, OE) (HPDC, 5V Tolerant)	2.0		VDD	V
V_{IL}	Input low voltage	Control Pins, Signal Pins (Dx_SEL, OE, HPDC)	–0.1		0.8	V
V_{I/O_Diff}	Differential voltage (Dx, AUXx)	Switch I/O diff voltage	0		1.8	Vpp
V_{I/O_CM}	Common voltage (Dx, AUXx)	Switch I/O common mode voltage	0		2.0	V
	Operating free-air temperature		–40		105	°C

6.4 Thermal Information

THERMAL METRIC (1)		HD3SS212	UNIT
		µ*BGA (ZQE)	
		48-Ball	
θ_{JA}	Junction-to-ambient thermal resistance	90.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	41.9	°C/W
θ_{JB}	Junction-to-board thermal resistance	53.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

under recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
I_{IH}	Input high current (Dx_SEL)	VDD = 3.6 V, VIN = VDD		3	10	µA
I_{IL}	Input low current (Dx_SEL)	VDD = 3.6 V, VIN = GND		0.01	1	µA
I_{LK}	Leakage current (Dx_SEL)	VDD = 3.3 V, Vi = 2V, OE = 3.3V		2	5	µA
		VDD = 0 V, Vi = 2 V, OE = 3.3 V		6	10	
	Leakage current (HPDA)	VDD = 3.3 V, Vi = 2 V, OE = 3.3 V; Dx_SEL=3.3 V		0.01	2	
	Leakage current (HPDB)	VDD = 3.3 V, Vi = 2 V, OE = 3.3 V; Dx_SEL=GND		0.01	2	
I_{off}	Device shut down current	VDD = 3.6 V, OE = GND			5	µA
I_{DD}	Supply current	VDD = 3.6 V, Dx_SELx = VCC/GND; Outputs floating		2.5	5	mA
DA, DB, DC HIGH SPEED SIGNAL PATH						
C_{ON}	Outputs ON capacitance	Vi = 0 V, Outputs open, Switch ON		1.5		pF
C_{OFF}	Outputs OFF capacitance	Vi = 0 V, Outputs open, Switch OFF		1		pF
R_{ON}	Output ON resistance	VDD = 3.3 V, VCM = 0.5V - 1.5 V, I_O = –40 mA		6.5	10	Ω
ΔR_{ON}	On resistance match between pairs of the same channel	VDD = 3.3 V; -0.35V ≤ VI ≤ 1.2 V; I_O = –40 mA			1.5	Ω
R_{FLAT_ON}	On resistance flatness ($R_{ON\ (MAX)} - R_{ON\ (MAIN)}$)	VDD = 3.3 V; -0.35 V ≤ VI ≤ 1.2 V		1.3		Ω
AUXx SIGNAL PATH						
C_{ON}	Outputs ON capacitance	Vi = 0 V, Outputs open, Switch ON		9		pF
C_{OFF}	Outputs OFF capacitance	Vi = 0 V, Outputs open, Switch OFF		3		pF
R_{ON}	Output ON resistance	VDD = 3.3 V, VCM = 0.5 V - 1.5 V, I_O = -40 mA		7	12	Ω
DEVICE PARAMETERS (under recommended operating conditions; R_L, R_{sc} = 50 Ω unless otherwise noted						
t_{PD}	Switch propagation delay	R_{sc} and RL = 50 Ω, See Figure 5			200	ps
T_{on}	Dx_SEL -to-Switch Ton (Data and AUX)	R_{sc} and RL = 50 Ω, See Figure 4		175	250	ns
T_{off}	Dx_SEL -to-Switch Toff (Data and AUX)			175	250	
T_{on}	Dx_SEL -to-Switch Ton (HPD)	RL = 50 Ω, See Figure 4		275	350	ns
T_{off}	Dx_SEL -to-Switch Toff (HPD)			275	350	
$T_{SK(O)}$	Inter-pair output skew (CH-CH)	R_{sc} and RL = 1 kΩ, See Figure 5			50	ps
$T_{SK(b-b)}$	Intra-pair output skew (bit-bit)			1	4	
RL	Dx Differential return loss(1)	1.35 GHz, See *Typical Characteristics*		–17		dB
		2.7 GHz, See *Typical Characteristics*		–11		
X_{TALK}	Dx Differential crosstalk(1)	2.7 GHz		–50		
O_{IRR}	Dx Differential off-isolation(1)	2.7 GHz, See *Typical Characteristics*		–22		
I_L	Dx Differential insertion loss(1)	f = 1.35 GHz, See *Typical Characteristics*		–0.7		dB
		f = 2.7 GHz, See *Typical Characteristics*		–1.4		
		f = 5.4 GHz, See *Typical Characteristics*		–1.7		
	AUX Differential insertion loss(1)	f = 360 MHz		–1		dB

(1) For Return Loss, Crosstalk, Off-Isolation, and Insertion Loss values the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

6.6 Typical Characteristics

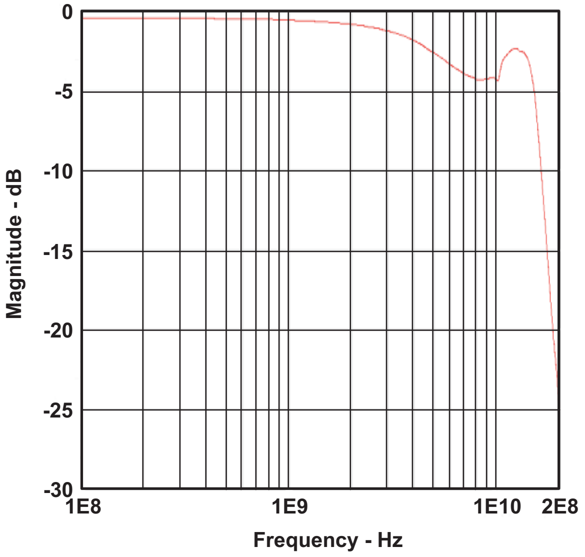


Figure 1. Insertion Loss and -3dB Bandwidth

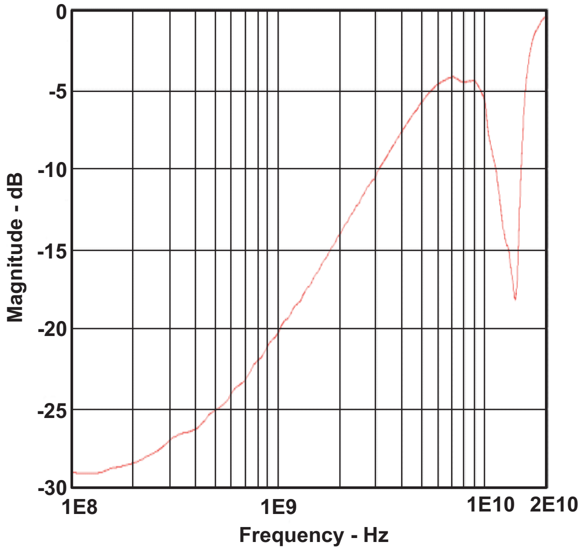


Figure 2. Return Loss

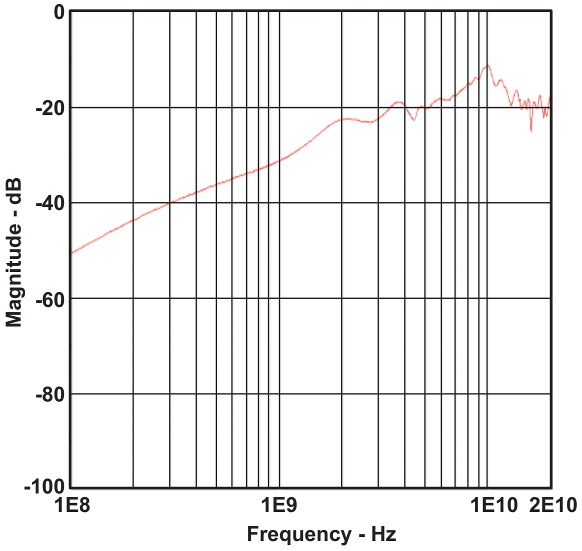


Figure 3. OF Isolation

7 Parameter Measurement Information

7.1 Test Timing Diagrams

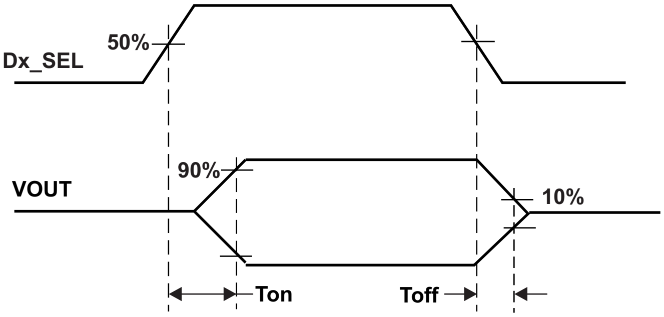
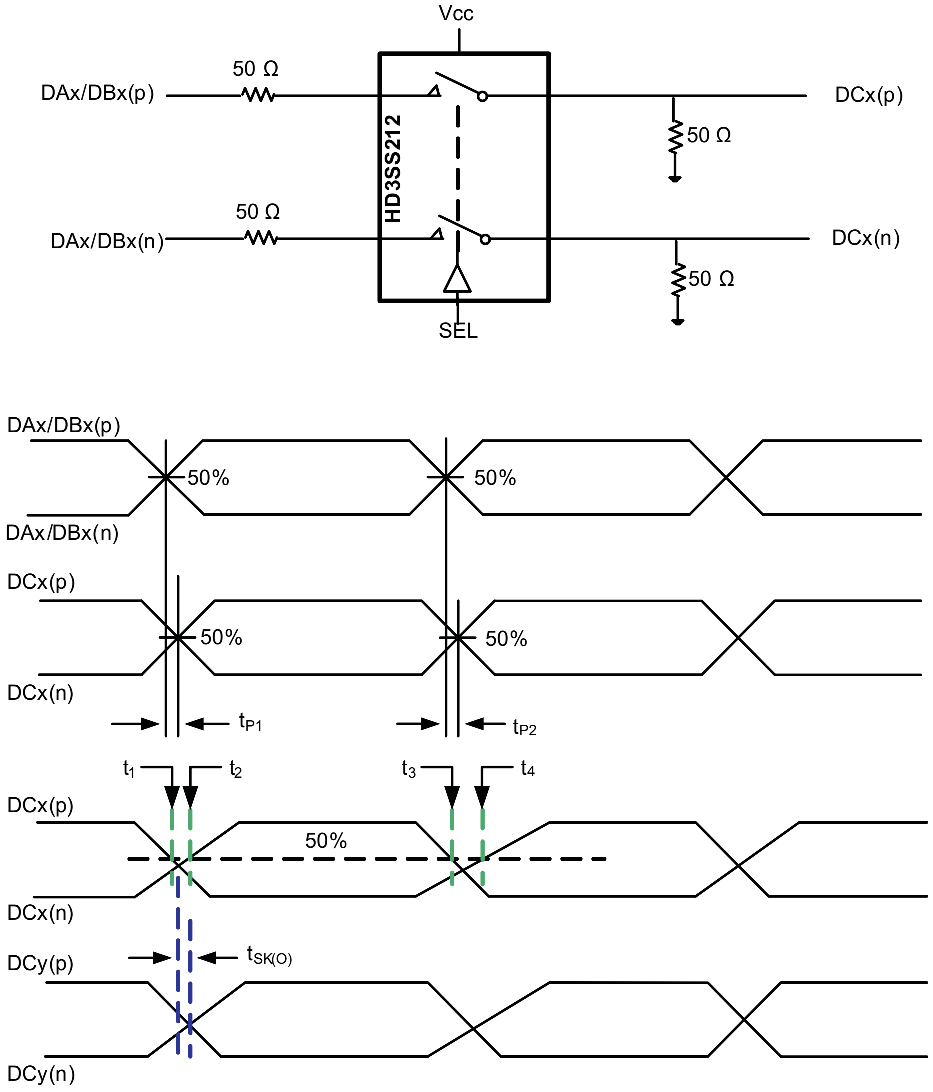


Figure 4. Select to Switch T_{on} and T_{off}

Test Timing Diagrams (continued)



$t_{PD} = \mathrm{Max}(t_{p1}, t_{p2})$

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs

$t_{SK(b\text{-}b)} = 0.5 \times |(t_4 - t_3) + (t_1 - t_2)|$

Figure 5. Propagation Delay and Skew

8 Detailed Description

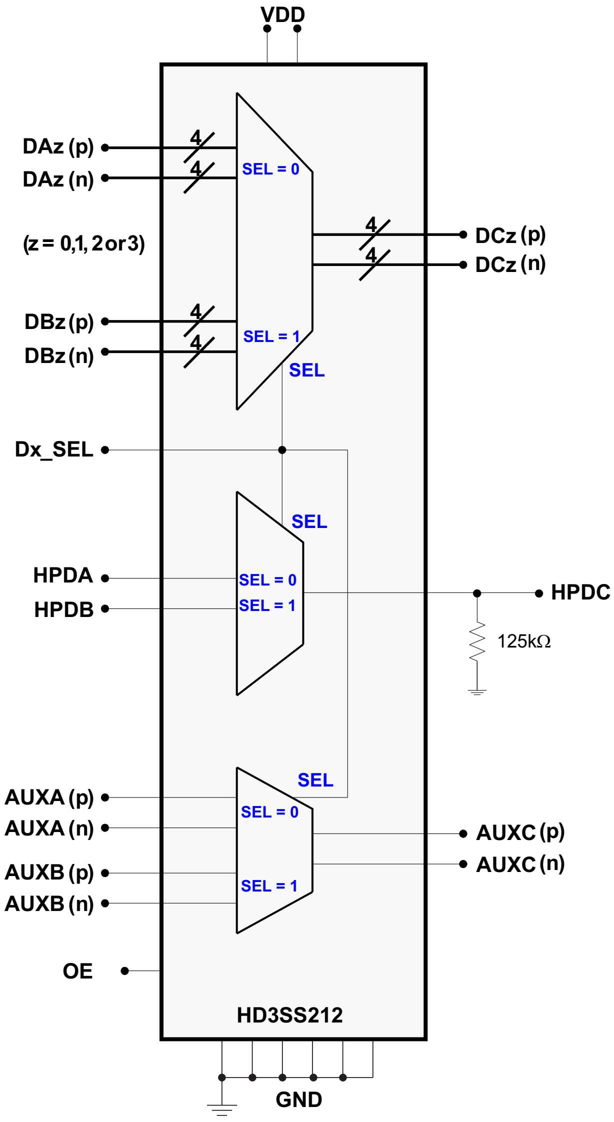
8.1 Overview

The HD3SS212 is a high-speed passive switch offered in an industry standard 48-pin u*BGA package available in a common footprint shared by several other vendors. The device is specified to operate from a single supply voltage of 3.3 V over the industrial temperature range of -40°C to 105°C.

The HD3SS212 is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The HD3SS212 will also support several other high-speed data protocols with a differential amplitude of < 1800 mVpp and a common-mode voltage of < 2.0 V, as with USB 3.0 and DisplayPort 1.2. For Display Port Applications the HD3SS212 also supports switching of both the Auxiliary and Hot Plug Detect signals.

The device’s High Speed Port Selection Control input (Dx_SEL) pin can easily be controlled by an available GPIO pin within a system.

8.2 Functional Block Diagram



8.3 Feature Description

Refer to *Functional Block Diagram*.

The HD3SS212 behaves as a two to one using high bandwidth pass gates. The input port is selected using the Dx_SEL pin according to Table 1.

Table 1. Switch Control Logic

CONTROL LINES	SWITCHED I/O PINS(1)(2)				
Dx_SEL	**DCz(p) PIN z = 0, 1, 2 or 3**	**DCz(n) PIN z = 0, 1, 2 or 3**	**HPDC PIN**	**AUXC(p) PIN**	**AUXC(n) PIN**
L	DAz(p)	DAz(n)	HPDA	AUXA(p)	AUXA(n)
H	DBz(p)	DBz(n)	HPDB	AUXVB(p)	AUXVB(n)

(1) OE pin - For nomal operation, drive OE high. Driving the OE pin low will disable the switch to enable power savings.
(2) The ports which are not selected by the Control Lines will be in High Impedance State.

8.4 Device Functional Modes

The HD3SS212 can be operated in normal operation mode or in shut down mode. In normal operation, the input ports of the HD3SS212 are routed to the output ports according to Table 1. In shut down mode the HD3SS212 is disabled to enable power savings with a typical current consumption of 5 µA. The functional mode is selected through the OE input pin with High for normal operation and LOW for shut down.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 AC Coupling Caps

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs should be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 µF is best and the value should be match for the ± signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board. There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. A few placement options are shown below. In Figure 6, the coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

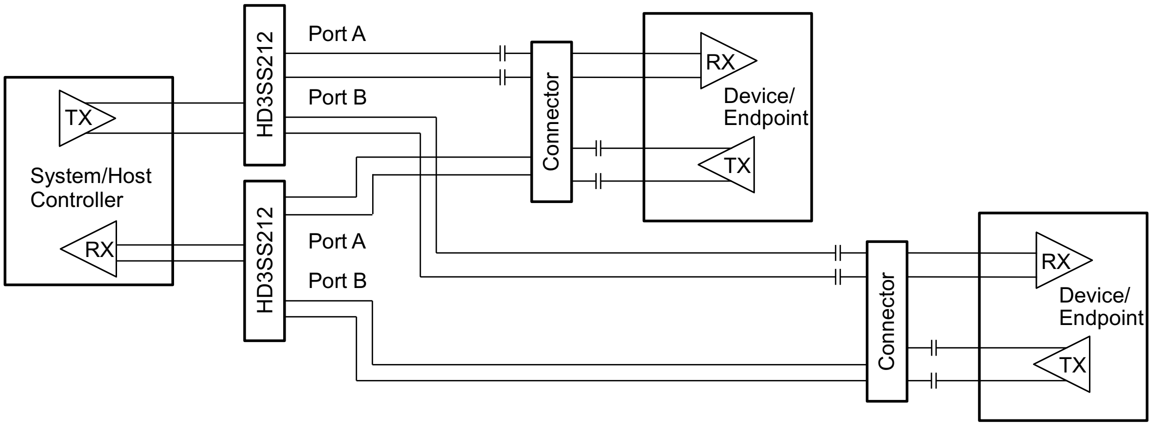


Figure 6. AC Coupling Capacitors Between Switch TX and Endpoint TX

In Figure 7, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on the top is biased by the endpoint and the lower switch is biased by the host controller.

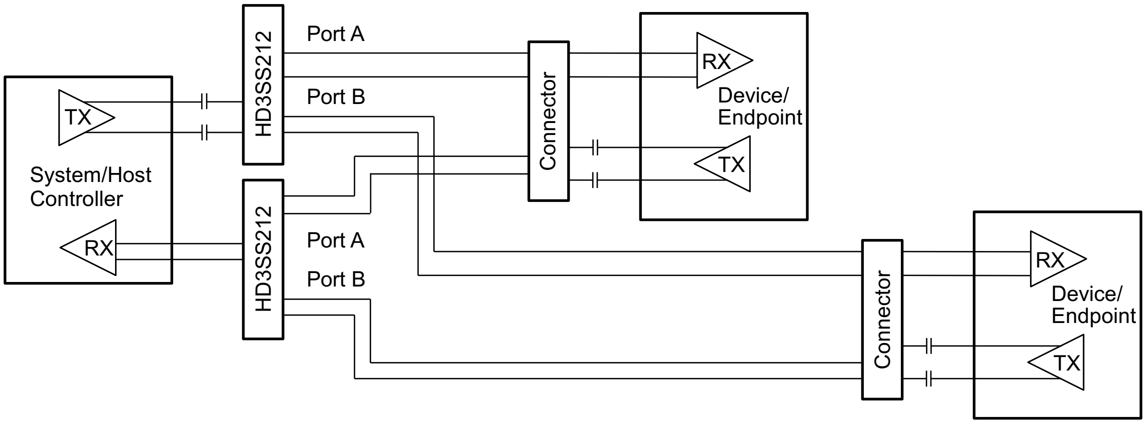


Figure 7. AC Coupling Capacitors on Host TX and Endpoint TX

Application Information (continued)

If the common-mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in Figure 8). A biasing voltage of less than 2 V is required in this case.

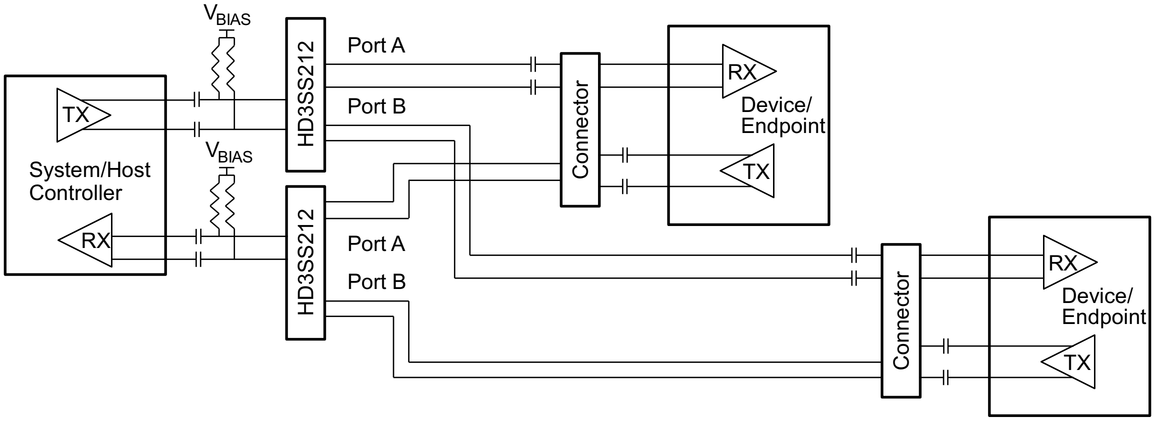


Figure 8. AC Coupling Capacitors on Both Sides of Switch

9.2 Typical Application

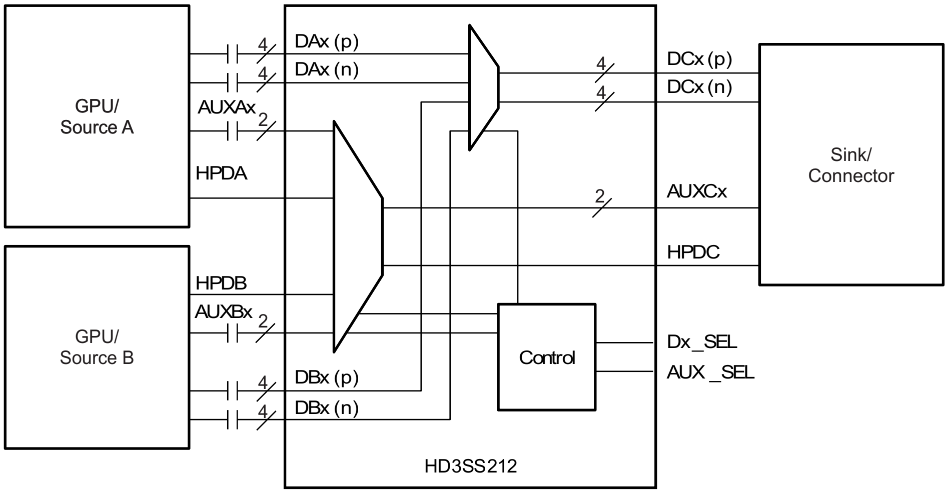


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Figure 9. Dual Source Connection Block Diagram

9.2.1 Design Requirements

Table 2 lists the design parameters.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	3.3 V
Decoupling capacitors	0.1 µF
AC capacitors	75 nF – 200 nF (100 nF shown) USBAA TX p and AC capacitors n lines require AC capacitors. Alternate mode signals may or may not require AC capacitors

9.2.2 Detailed Design Procedure

- Connect VDD and GND pins to the power and ground planes of the printed circuit board, with 0.1-µF bypass capacitor
- Use +3.3-V TTL/CMOS logic level at SEL
- Use controlled-impedance transmission media for all the differential signals
- Ensure the received complimentary signals are with a differential amplitude of < 1800 mVpp and a common-mode voltage of < 2V.

9.2.3 Application Curves

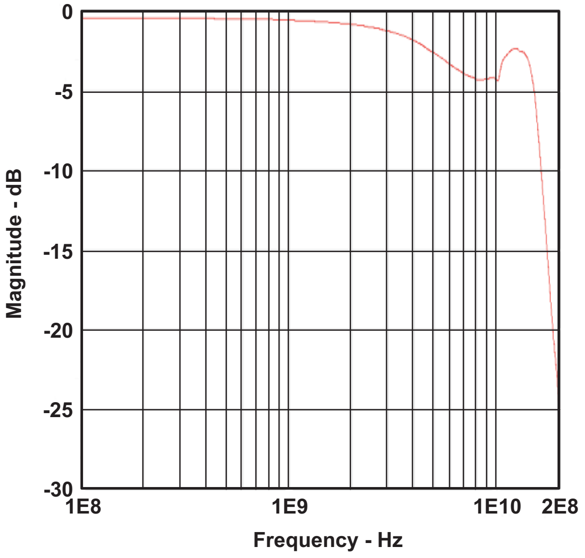

Figure 10. Insertion Loss and -3dB Bandwidth

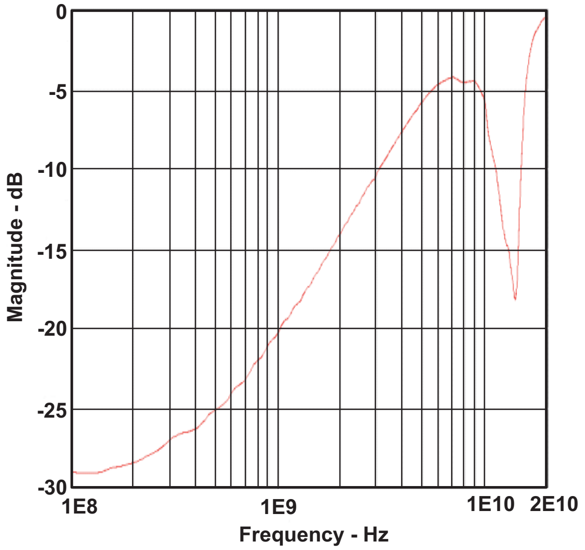

Figure 11. Return Loss

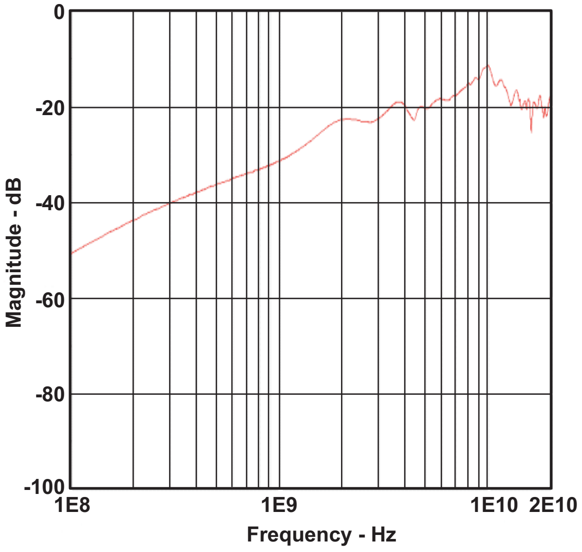

Figure 12. OF Isolation

10 Power Supply Recommendations

The HD3SS212 requires +3.3-V digital power sources. VDD 3.3 supply must have 0.1-µF bypass capacitors to VSS (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01-µF are also recommended on the digital supply terminals.

11 Layout

11.1 Layout Guidelines

- Decoupling caps should be placed next to each power terminal on the HD3SS3412. Take care to minimize the stub length of the race connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling caps
- Place vias as close as possible to the decoupling cop solder pad
- Widen VDD/GND planes to reduce effect if static and dynamic IR drop
- The VBUS traces/planes must be wide enough to carry maximum of 2-A current

11.2 Layout Example

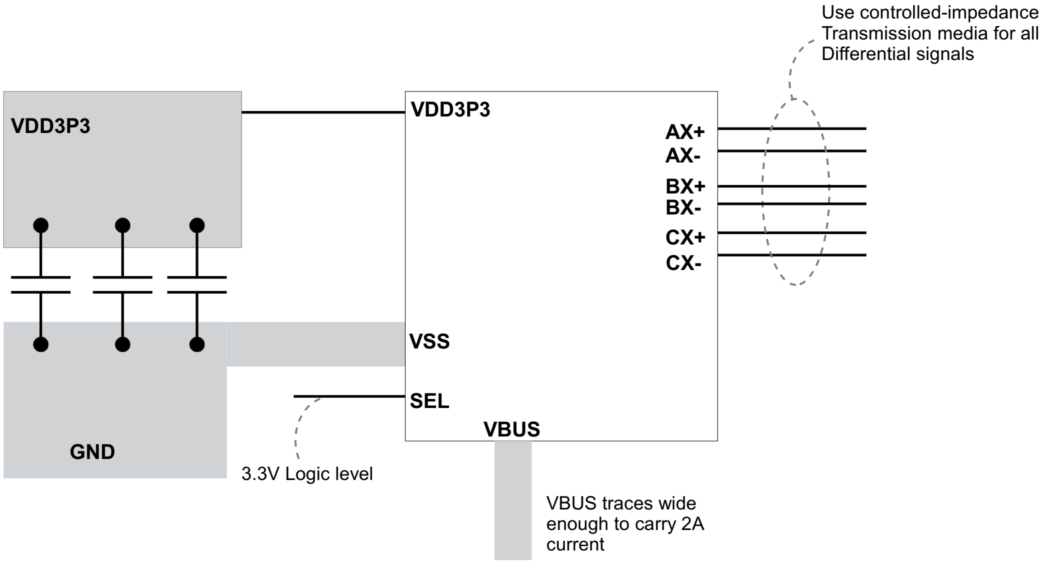

Figure 13. Layout Example

12 器件和文档支持

12.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS212ZXHR	ACTIVE	NFBGA	ZXH	48	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS212	Samples
HD3SS212ZXHT	ACTIVE	NFBGA	ZXH	48	250	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS212	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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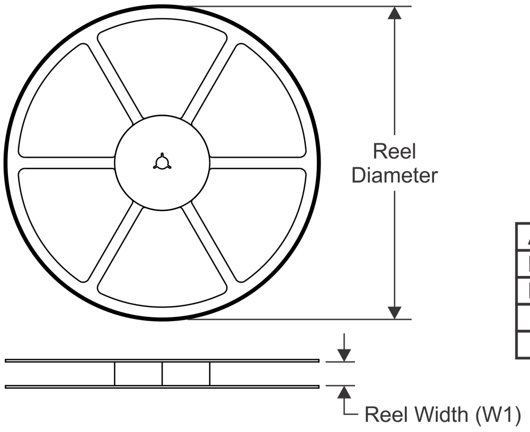
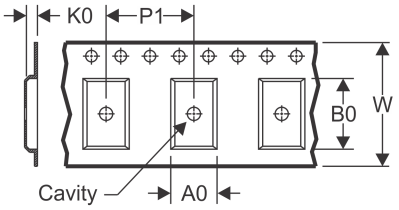
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

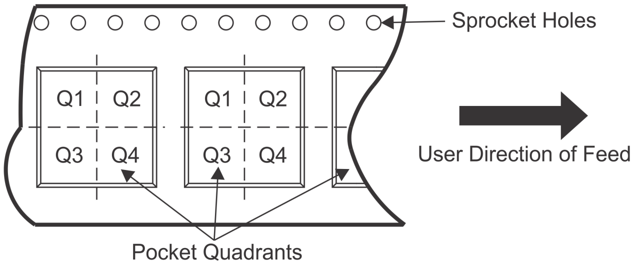


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

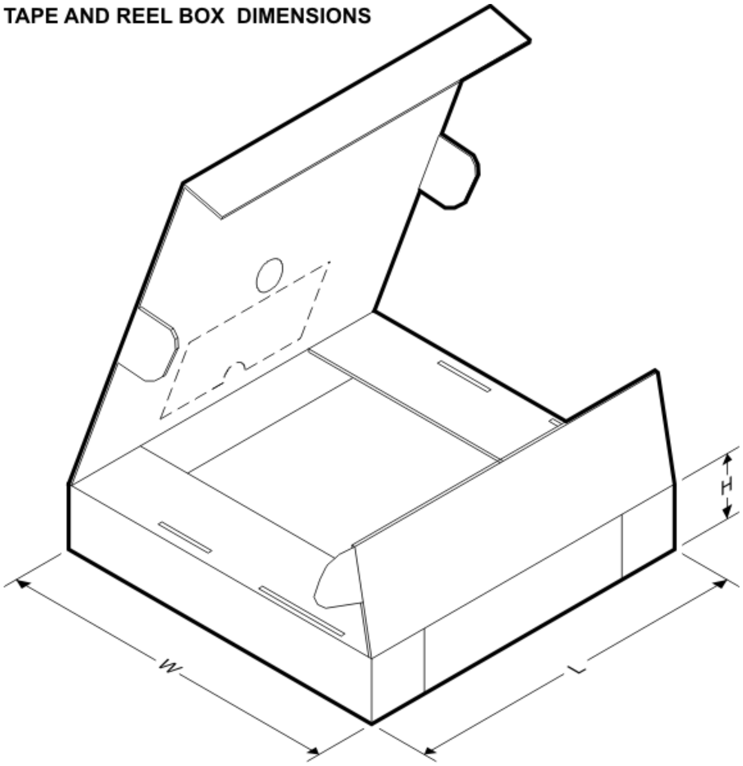
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS212ZXHR	NFBGA	ZXH	48	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
HD3SS212ZXHT	NFBGA	ZXH	48	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



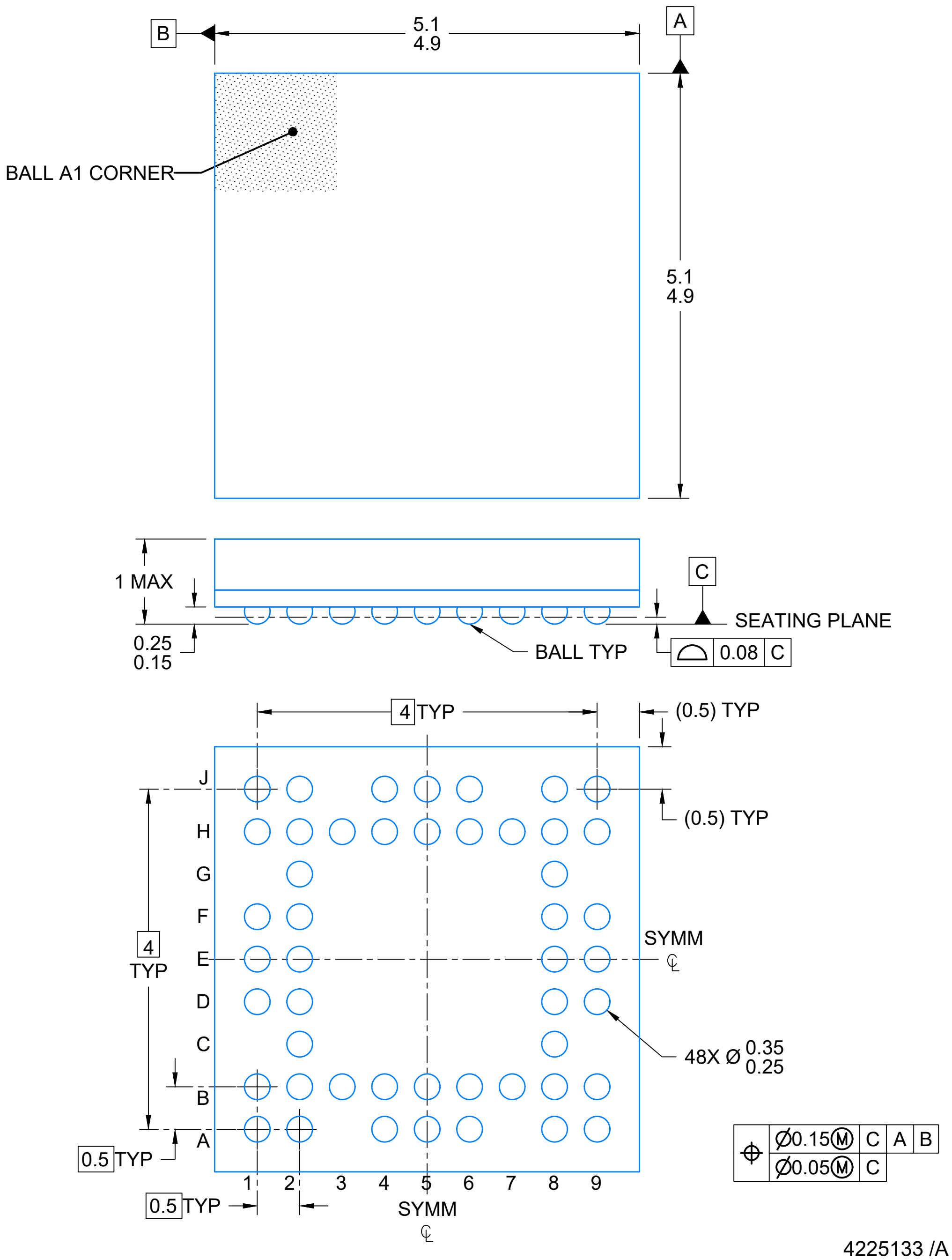
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS212ZXHR	NFBGA	ZXH	48	2500	336.6	336.6	31.8
HD3SS212ZXHT	NFBGA	ZXH	48	250	336.6	336.6	31.8

PACKAGE OUTLINE

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



4225133 /A 08/2019

NOTES:

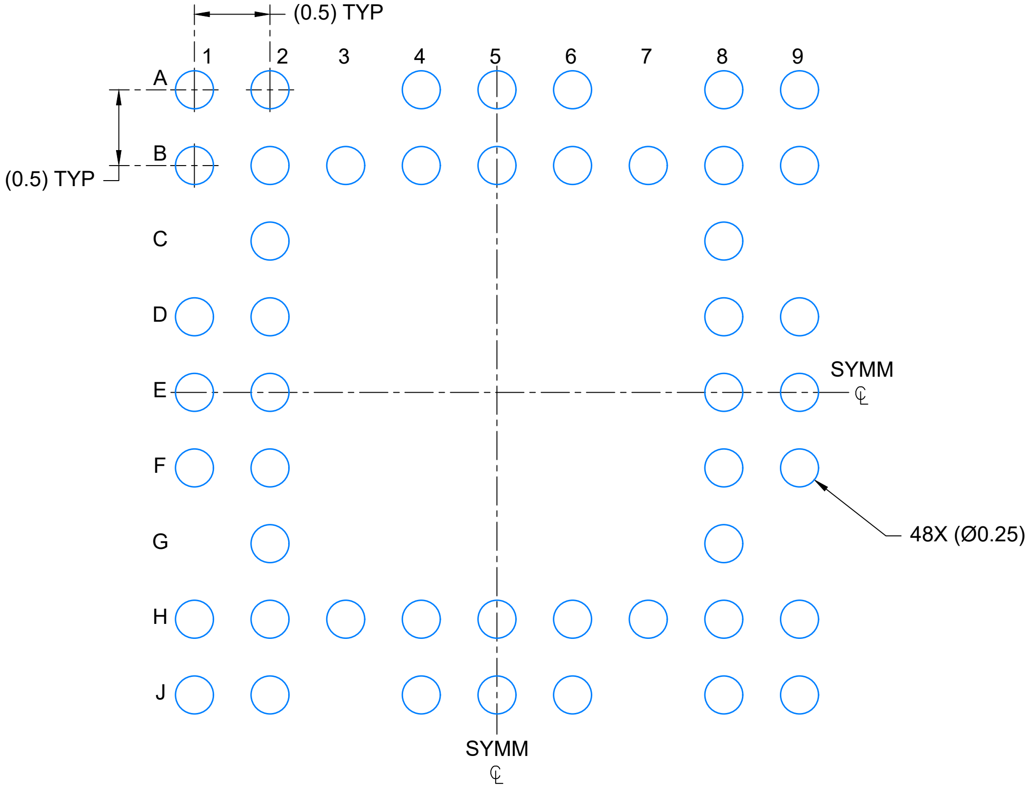
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

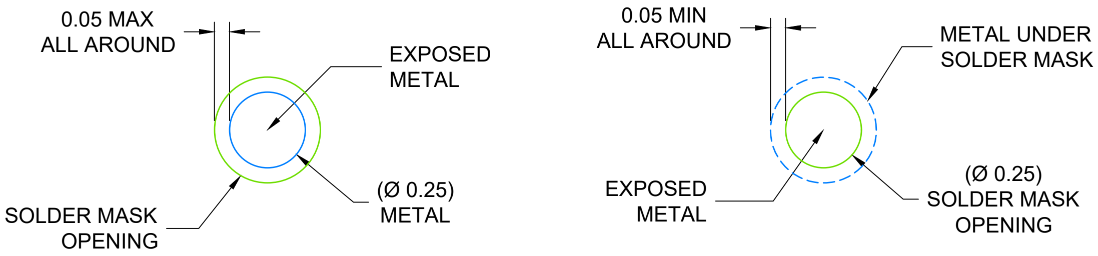
EXAMPLE BOARD LAYOUT

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE: 20X



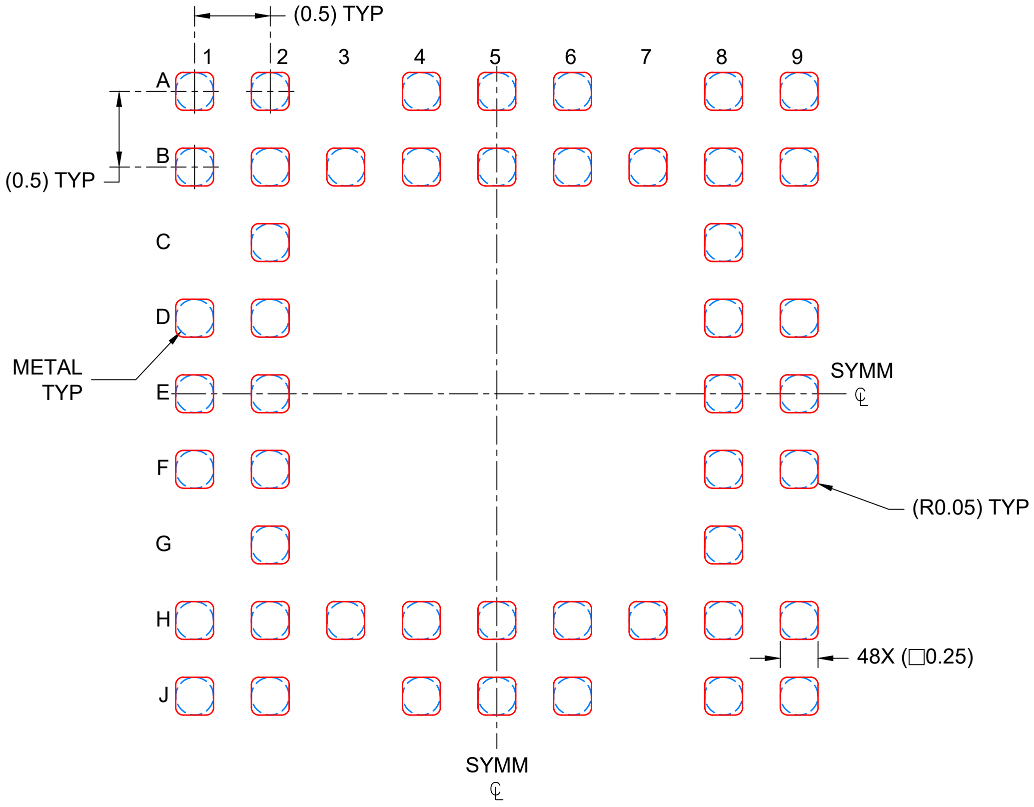
NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 20X

4225133 /A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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