# TPS3899-Q1 具有可编程感应和复位延迟以及按钮监视器的毫微功耗、精密电压监控器

## 1 特性

符合汽车应用标准：

- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 的工作环境温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C7B

专为高性能而设计：

- 毫微静态电流：125nA（典型值）
- 高阈值精度：±0.5%（典型值）
- 内置精密迟滞 ($V_{HYS}$)：5%（典型值）

适用于多种应用：

- 工作电压范围：
  - 0.85V 至 6V（DL 和 PL 输出）
  - 1V 至 6V（PH 输出）
- 可调节阈值电压：0.505V（典型值）
- 精密电压和按钮监视器
- 可编程感应和复位延迟
- 固定电压 ($V_{IT-}$)：0.8 V 至 5.4 V（步长为 0.1 V）

多种输出拓扑/封装类型：

- TPS3899DL-Q1：漏极开路，低电平有效 ($\overline{RESET}$)
- TPS3899PL-Q1：推挽，低电平有效 ($\overline{RESET}$)
- TPS3899PH-Q1：推挽，高电平有效 (RESET)
- 封装：1.5mm × 1.5mm WSON (DSE)

## 2 应用

- 高级驾驶辅助系统 (ADAS)
- 信息娱乐系统音响主机
- 汽车网关
- 摄像头模块
- 雷达 ECU
- 汽车外部放大器

## 3 说明

TPS3899-Q1 是一款毫微级功率、精密电压监控器，具有 ± 0.5% 的阈值精度和可编程感应和复位延时时间，并采用节省空间的 6 引脚 1.5mm × 1.5mm WSON 封装。TPS3899-Q1 是一款功能丰富的电压监控器，可提供同类产品中超小型的总解决方案尺寸。在监控电压轨或按钮信号时，内置迟滞和可编程延迟可防止出现错误的复位信号。

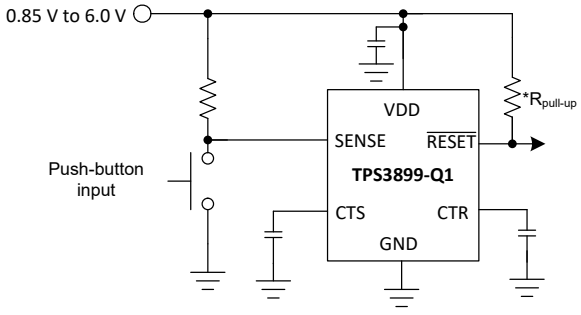
通过单独的 VDD 和 SENSE 引脚，可实现高可靠性系统所需的冗余。SENSE 已从 VDD 去耦，可以监控除 VDD 之外的轨电压。SENSE 引脚的高阻抗输入支持使用可选的外部电阻器。CTS 和 CTR 都提供了对 RESET 信号的上升沿和下降沿进行延迟调整的能力。CTS 忽略受监控电压轨上的电压干扰，从而也可充当去抖动器；作为手动复位工作时，用于强制系统复位。

TPS3899-Q1 以紧凑的外形提供了精密的性能和卓越的功能，成为各种汽车和电池供电/低功耗应用的理想解决方案。该器件的额定工作温度范围为 –40°C 至 +125°C ($T_A$)。

器件信息

| 器件型号 | 封装 (1) | 封装尺寸（标称值） |
|---|---|---|
| TPS3899-Q1 | WSON (6) DSE | 1.5mm x 1.5mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录




*$R_{pull-up}$ is required for open-drain variants only

典型应用电路

# Table of Contents



## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (April 2021) to Revision A (September 2021) | Page |
|---|---|
| • 量产数据发布 | 1 |

## 5 Device Nomenclature

图 5-1 shows the device naming nomenclature of the TPS3899-Q1. For all possible output types and threshold voltage options, see Device Naming Convention for a more detailed explanation. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

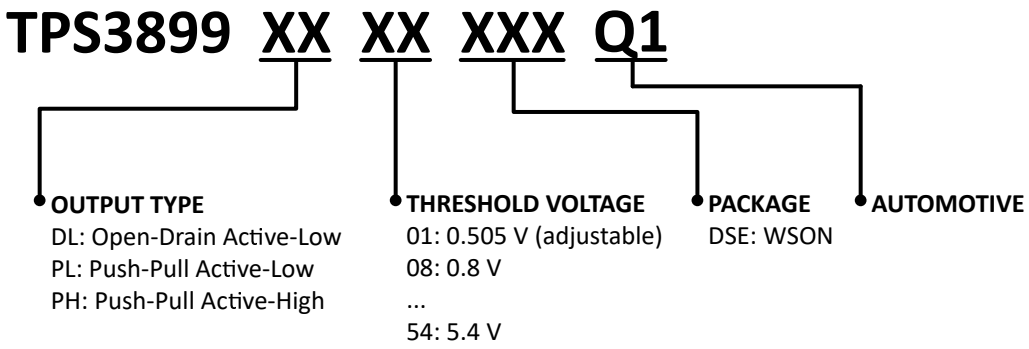



**图 5-1. Device Naming Nomenclature**

# 6 Pin Configuration and Functions

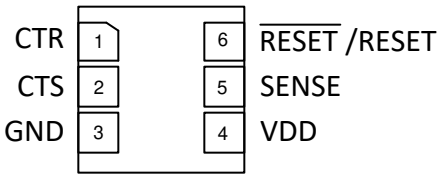



**图 6-1. DSE Package**
**6-Pin WSON**
**TPS3899-Q1 (Top View)**

**表 6-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | CTR | — | Capacitor programmable reset delay: The CTR pin offers a user-adjustable delay time when returning from reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to deassert. |
| 2 | CTS | — | Capacitor programmable sense delay: The CTS pin offers a user-adjustable delay time when asserting reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to assert. |
| 3 | GND | — | Ground |
| 4 | VDD | I | Supply voltage pin: Good analog design practice is to place a 0.1-µF decoupling capacitor close to this pin. |
| 5 | SENSE | I | This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. When the voltage on the SENSE pin transitions below the negative threshold voltage $V_{IT-}$, $\overline{\text{RESET}}$/RESET asserts to active logic after the sense delay set by CTS. When the voltage on the SENSE pin transitions above the positive threshold voltage $V_{IT-} + V_{HYS}$, $\overline{\text{RESET}}$/RESET releases to inactive logic (deasserts) after the reset delay set by CTR. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance. |
| 6 | $\overline{\text{RESET}}$ | O | $\overline{\text{RESET}}$ active-low output that asserts to a logic low state after CTS delay when the monitored voltage on the SENSE pin is lower than the negative threshold voltage $V_{IT-}$. $\overline{\text{RESET}}$ remains logic low (asserted) until the SENSE input rises above $V_{IT-} + V_{HYS}$ and the CTR reset delay expires. |
| 6 | RESET | O | RESET active-high output that asserts to a logic high state after CTS delay when the monitored voltage on the SENSE pin is lower than the negative threshold voltage $V_{IT-}$. RESET remains logic high (asserted) until the SENSE input rises above $V_{IT-} + V_{HYS}$ and the CTR reset delay expires. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | VDD, SENSE, $\overline{\text{RESET}}$ (TPS3899DL) | –0.3 | 6.5 | V |
| | CTR, CTS, $\overline{\text{RESET}}$ (TPS3899PL), RESET (TPS3899PH) | –0.3 | $V_{DD}$+0.3 (3) | V |
| Current | $\overline{\text{RESET}}$ pin and RESET pin | | ±20 | mA |
| Temperature (2) | Operating ambient temperature, $T_A$ | –40 | 125 | °C |
| Temperature (2) | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Rating* (*AMR*) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute maximum rated conditions for long periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 (1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage | VDD, SENSE, $\overline{\text{RESET}}$ (TPS3899DL) | 0 | | 6 | V |
| Voltage | CTR, CTS, $\overline{\text{RESET}}$ (TPS3899PL), RESET (TPS3899PH) | 0 | | VDD | V |
| Current | $\overline{\text{RESET}}$ pin and RESET pin current | 0 | | ±5 | mA |
| $T_A$ | Operating free air temperature | –40 | | 125 | °C |
| $C_{CTR}$ | CTR pin capacitor range | 0 | | 10 | µF |
| $C_{CTS}$ | CTS pin capacitor range | 0 | | 10 | µF |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | TPS3899-Q1 DSE 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 214.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 153.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 112.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 25.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 111.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.5 Electrical Characteristics

CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to $V_{DD}$, output reset load ($C_{LOAD}$) = 10 pF and over the operating free-air temperature range –40℃ to 125℃, unless otherwise noted. $V_{DD}$ ramp rate ≤ 1 V / µs. Typical values are at $T_A$ = 25℃.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **COMMON PARAMETERS** | | | | | | |
| $V_{DD}$ | Input supply voltage (Open Drain Low and Push Pull Low) | | 0.85 | | 6 | V |
| $V_{DD}$ | Input supply voltage (Push Pull High) | | 1 | | 6 | V |
| $V_{IT-}$ (1) | Negative-going input threshold range | for all output configs | 0.8 | | 5.4 | V |
| $V_{ADJ-VIT-}$ | Negative-going input threshold for adjustable sense threshold version | | | 0.505 | | V |
| $V_{IT-}$ accuracy | Negative-going input threshold accuracy | $V_{IT-}$ = 0.505 V (ADJ version) or 0.8 V to 1.7 V (Fixed threshold) | –2.5 | ±0.5 | 2.5 | % |
| | | $V_{IT-}$ = 1.8 V to 5.4 V (Fixed threshold) | –2 | ±0.5 | 2 | |
| $V_{HYS}$ | Hysteresis on $V_{IT-}$ | $V_{IT-}$ = 0.505 V and 0.8 V | 3 | 5 | 8 | % |
| | | $V_{IT-}$ = 0.9 V to 5.4 V | 3 | 5 | 7 | % |
| $I_{SENSE}$ | Current into Sense pin, fixed threshold version | $V_{DD}$ = $V_{SENSE}$ = 6 V | | 0.025 | 0.1 | µA |
| | Current into Sense pin, ADJ version | $V_{DD}$ = $V_{SENSE}$ = 6 V | | 0.025 | 0.05 | µA |
| $I_{DD}$ | Supply current into VDD pin when sense pin is separate | $V_{DD}$ = $V_{SENSE}$ = 6 V<br>$V_{IT-}$ = 0.505 V and 0.8 V to 5.4 V | | 0.125 | 1 | µA |
| $V_{TH\_CTS}$ | Voltage threshold to stop CTS capacitor charge and assert RESET | | | 0.73 * $V_{DD}$ | | V |
| $V_{TH\_CTR}$ | Voltage threshold to stop CTR capacitor charge and deassert RESET | | | 0.73 * $V_{DD}$ | | V |
| $R_{CTS}$ | CTS pin internal pull up resistance | | 410 | 500 | 590 | kΩ |
| $R_{CTR}$ | CTR pin internal pull up resistance | | 410 | 500 | 590 | kΩ |
| **TPS3899DL (Open-drain active-low)** | | | | | | |
| $V_{POR}$ | Power on reset voltage (2) | $V_{OL(max)}$ = 300 mV<br>$I_{\overline{RESET}(Sink)}$ = 15 µA | | | 700 | mV |
| $V_{OL}$ | Low level output voltage | $V_{DD}$ = 0.85 V<br>$I_{\overline{RESET}(Sink)}$ = 15 µA | | | 300 | mV |
| | | $V_{DD}$ = 3.3 V<br>$I_{\overline{RESET}(Sink)}$ = 2 mA | | | 300 | mV |
| $I_{lkg(OD)}$ | Open-Drain output leakage current | $V_{DD}$ = $V_{PULLUP}$ = 6 V, $T_A$ = –40℃ to 85℃ | | 10 | 100 | nA |
| | | $V_{DD}$ = $V_{PULLUP}$ = 6 V | | 10 | 350 | nA |
| **TPS3899PL (Push-pull active-low)** | | | | | | |
| $V_{POR}$ | Power on reset voltage (2) | $V_{OL(max)}$ = 300 mV<br>$I_{\overline{RESET}(Sink)}$ = 15 µA | | | 700 | mV |
| $V_{OL}$ | Low level output voltage | $V_{DD}$ = 0.85 V<br>$I_{\overline{RESET}(Sink)}$ = 15 µA | | | 300 | mV |
| | | $V_{DD}$ = 3.3 V<br>$I_{\overline{RESET}(Sink)}$ = 2 mA | | | 300 | mV |
| $V_{OH}$ | High level output voltage | $V_{DD}$ = 1.8 V<br>$I_{\overline{RESET}(Source)}$ = 500 µA | 0.8$V_{DD}$ | | | V |
| | | $V_{DD}$ = 3.3 V<br>$I_{\overline{RESET}(Source)}$ = 500 µA | 0.8$V_{DD}$ | | | V |
| | | $V_{DD}$ = 6 V<br>$I_{\overline{RESET}(Source)}$ = 2 mA | 0.8$V_{DD}$ | | | V |

## 7.5 Electrical Characteristics (continued)

CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to $V_{DD}$, output reset load ($C_{LOAD}$) = 10 pF and over the operating free-air temperature range –40℃ to 125℃, unless otherwise noted. $V_{DD}$ ramp rate ≤ 1 V / µs. Typical values are at $T_A$ = 25℃.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TPS3899PH (Push-pull active-high)** | | | | | | |
| $V_{POR}$ | Power on reset voltage (2) | $V_{OH(min)}$ = 0.8$V_{DD}$<br>$I_{RESET\ (Source)}$ = 15 uA | | | 900 | mV |
| $V_{OL}$ | Low level output voltage | $V_{DD}$ = 3.3 V<br>$I_{RESET(Sink)}$ = 500 µA | | | 300 | mV |
| | | $V_{DD}$ = 6 V<br>$I_{RESET(Sink)}$ = 2 mA | | | 300 | mV |
| $V_{OH}$ | High level output voltage | $V_{DD}$ = 1V<br>$I_{RESET(Sink)}$ = 15 µA | 0.8$V_{DD}$ | | | V |
| | | $V_{DD}$ = 1.5 V<br>$I_{RESET(Sink)}$ = 500 µA | 0.8$V_{DD}$ | | | V |
| | | $V_{DD}$ = 3.3 V<br>$I_{RESET(Sink)}$ = 2 mA | 0.8$V_{DD}$ | | | V |

(1) $V_{IT-}$ threshold voltage range from 0.8 V to 5.4 V (for DL, PL) and 1 to 5.4 V (for PH) in 100 mV steps, for released versions see Device Voltage Thresholds table.
(2) Minimum $V_{DD}$ voltage level for a controlled output state. Below $V_{POR}$, the output cannot be determined.

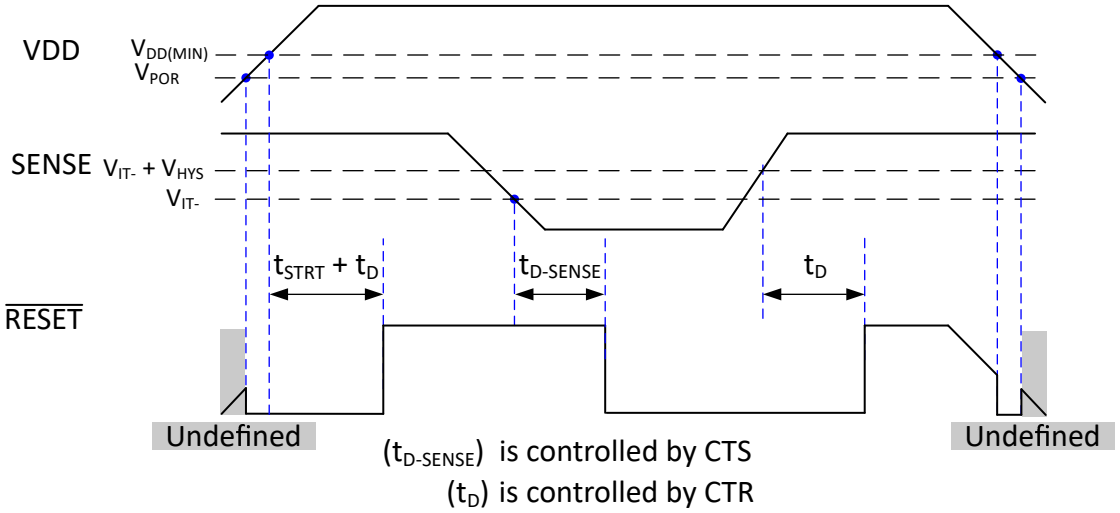
## 7.6 Timing Requirements

At 0.85 V ≤ $V_{DD}$ ≤ 6 V, CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to $V_{DD}$, output reset load ($C_{LOAD}$) = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. $V_{DD}$ ramp rate ≤ 1 V / µs. Typical values are at $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STRT}$ | Startup Delay (1) | CTR pin = Open or NC | | | 300 | µs |
| $t_{D-SENSE}$ | Detect time delay<br>$V_{DD}$ = ($V_{IT+}$ + 10%) to ($V_{IT-}$ – 10%) (2) | CTS pin = Open or NC | | 30 | 50 | µs |
| | | CTS pin = 10 nF | | 6.2 | | ms |
| | | CTS pin = 1 µF | | 619 | | ms |
| $t_D$ | Reset time delay | CTR pin = Open or NC | | 40 | 80 | µs |
| | | CTR pin = 10 nF (3) | | 6.2 | | ms |
| | | CTR pin = 1 µF (3) | | 619 | | ms |
| $t_{GI\_VIT-}$ | Glitch immunity $V_{IT-}$ | 5% $V_{IT-}$ overdrive (4) | | 10 | | µs |

(1) When VDD starts from less than $V_{POR}$ and then exceeds the specified minimum $V_{DD}$, reset is asserted till startup delay ($t_{STRT}$) + $t_D$ delay based on capacitor on CTR pin. After this time, the device controls the RESET pin based on the SENSE pin voltage.
(2) $t_{D\_SENSE}$ measured from threhold trip point ($V_{IT-}$) to $V_{OL}$ for active low variants and $V_{OH}$ for active high variants.
(3) Ideal capacitor
(4) Overdrive % = [($V_{DD}$/ $V_{IT-}$) - 1] × 100%

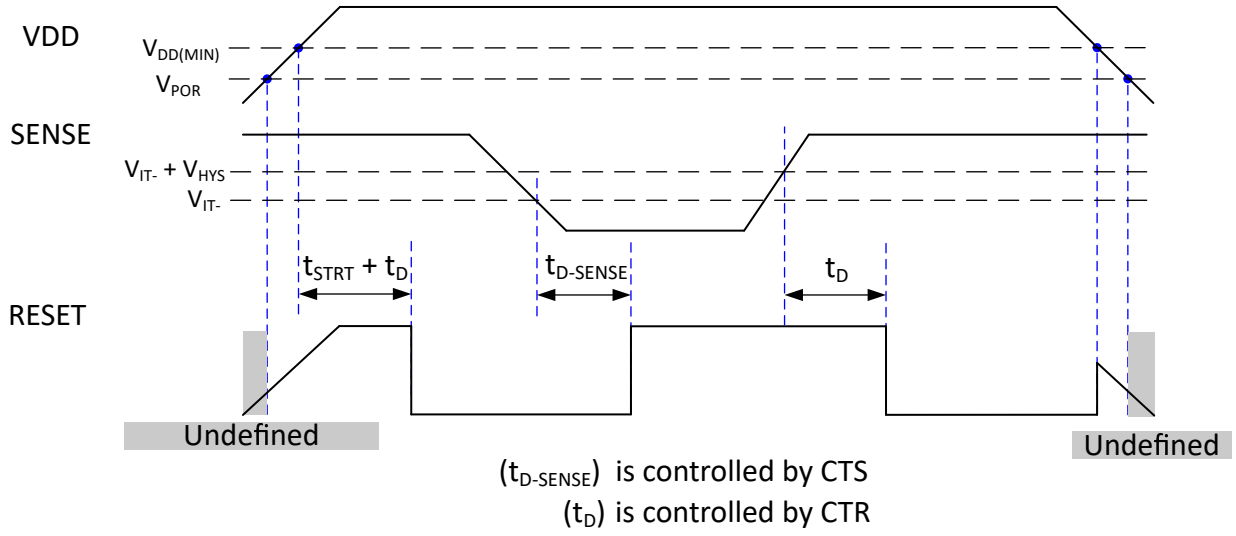
## 7.7 Timing Diagrams




(1) $t_{D\ (no\ cap)}$ is included in $t_{STRT}$ time delay. If $t_D$ delay is programmed by an external capacitor connected to the CTR pin then $t_D$ programmed time will be added to the startup time.

(2) Be advised, in some instances, that the VDD falling slew rate in 图 7-1 can be slow or such that VDD decay time is much larger than the SENSE delay time ($t_{D\text{-}SENSE}$) time allowing the output to assert. If the VDD falling slew rate is much faster than the ($t_{D\text{-}SENSE}$), the output will appear to be not asserted.

**图 7-1. TPS3899DL01-Q1 and TPS3899PL01-Q1 Timing Diagram**




(1) $t_{D\ (no\ cap)}$ is included in $t_{STRT}$ time delay. If $t_D$ delay is programmed by an external capacitor connected to the CTR pin then $t_D$ programmed time will be added to the startup time.

(2) Be advised, in some instances, that the VDD falling slew rate in 图 7-2 can be slow or such that VDD decay time is much larger than the SENSE delay time ($t_{D\text{-}SENSE}$) time allowing the output to assert. If the VDD falling slew rate is much faster than the ($t_{D\text{-}SENSE}$), the output will appear to be not asserted.

**图 7-2. TPS3899PH01-Q1 Timing Diagram**

## 7.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS3899-Q1 device. Test conditions are $T_A$ = 25°C, $V_{DD}$ = 3.3 V, and $R_{pull-up}$ = 100 kΩ, unless otherwise noted.

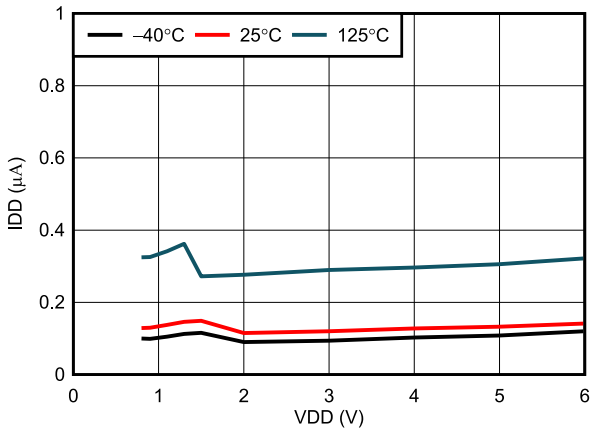



图 7-3. Supply Current vs Supply Voltage

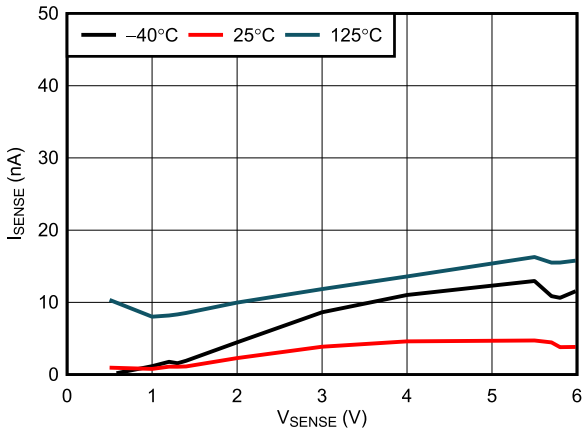



图 7-4. SENSE Current vs $V_{SENSE}$

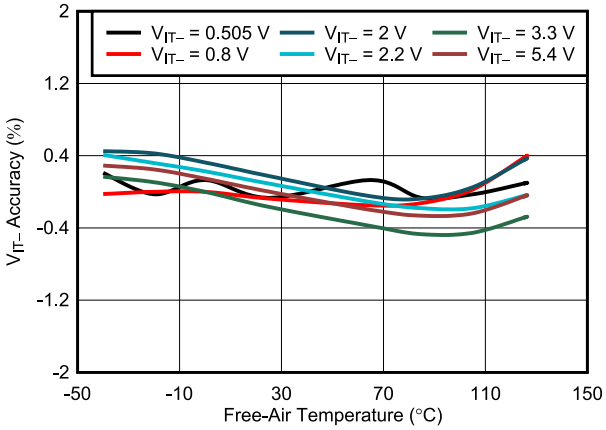



图 7-5. $V_{IT-}$ Accuracy vs Temperature

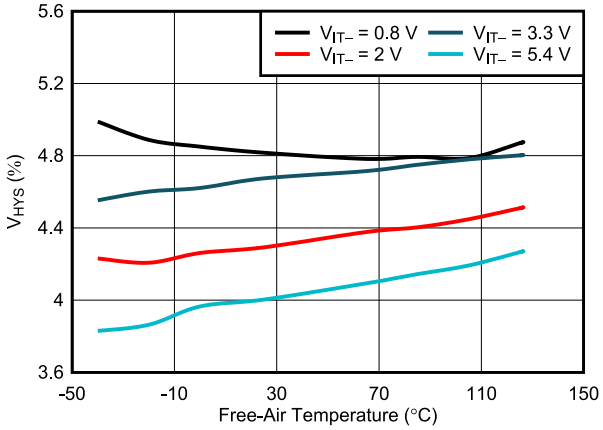



图 7-6. $V_{HYS}$ vs Temperature

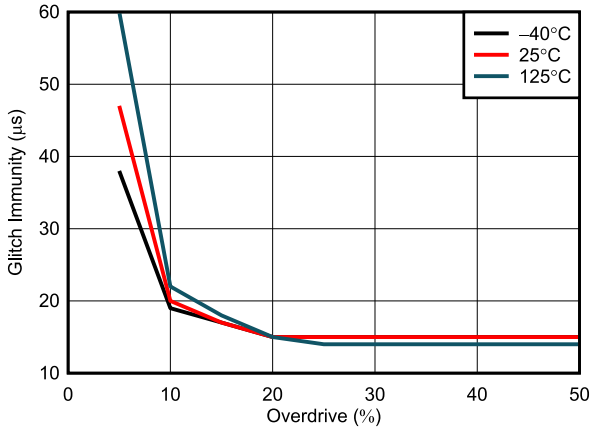



图 7-7. SENSE Glitch Immunity ($V_{IT-}$) vs Overdrive

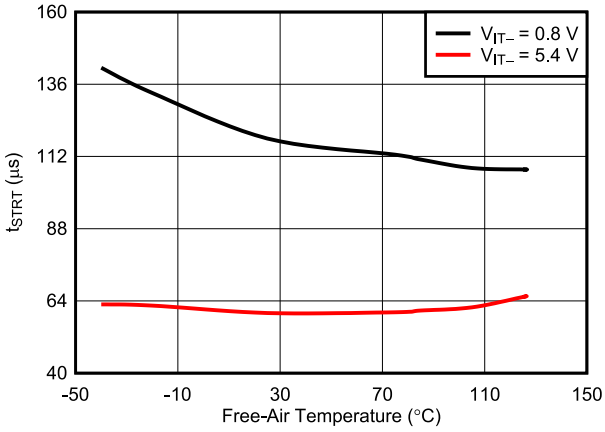



图 7-8. Startup Delay vs Temperature

## 7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3899-Q1 device. Test conditions are $T_A$ = 25°C, $V_{DD}$ = 3.3 V, and $R_{pull-up}$ = 100 kΩ, unless otherwise noted.

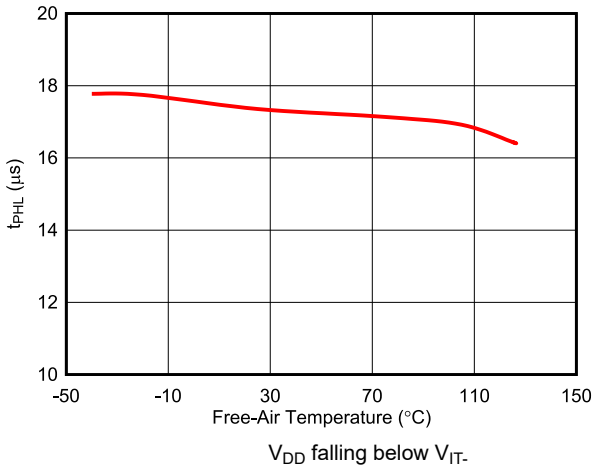



图 7-9. Propagation Delay vs Temperature

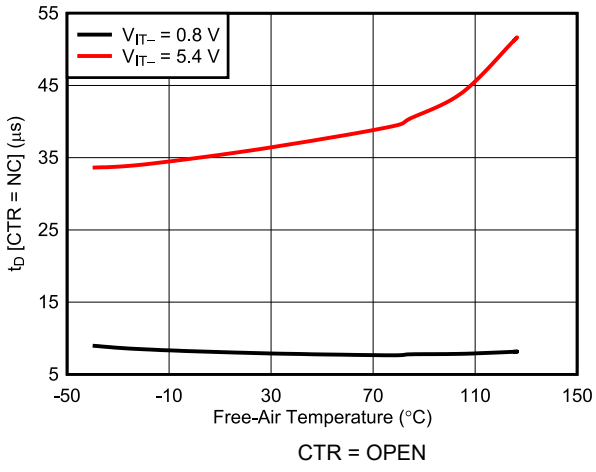



图 7-10. Reset Time Delay vs Temperature

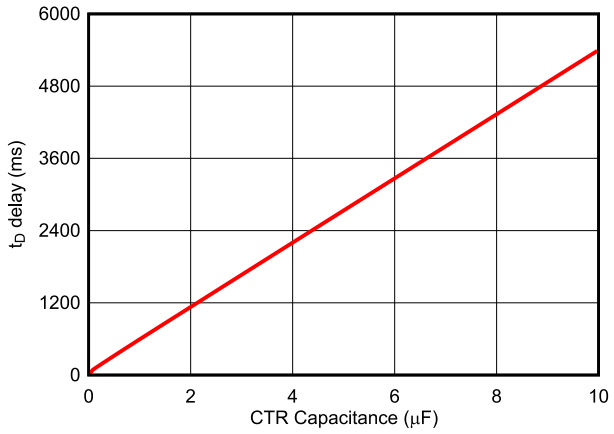



图 7-11. RESET Delay vs CTR Capacitance

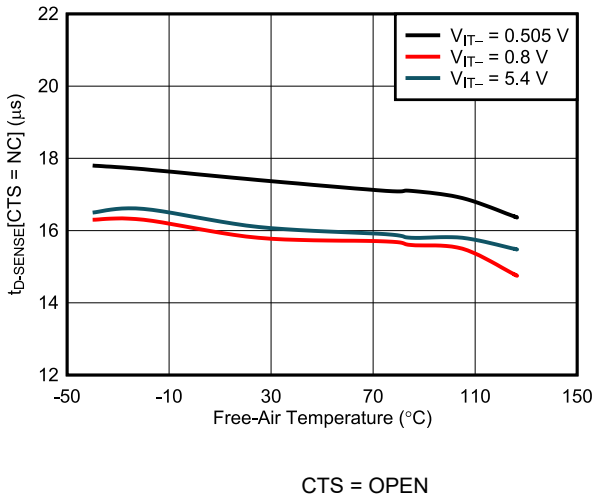



图 7-12. SENSE Delay vs Temperature

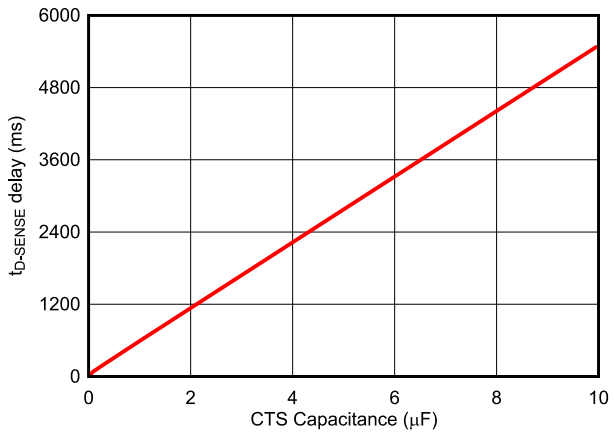



图 7-13. SENSE Delay vs CTS Capacitance

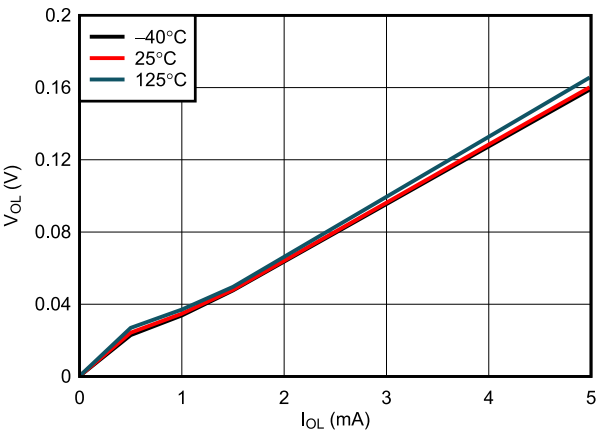



图 7-14. $V_{OL}$ vs $I_{OL}$

## 7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3899-Q1 device. Test conditions are $T_A$ = 25°C, $V_{DD}$ = 3.3 V, and $R_{pull-up}$ = 100 kΩ, unless otherwise noted.

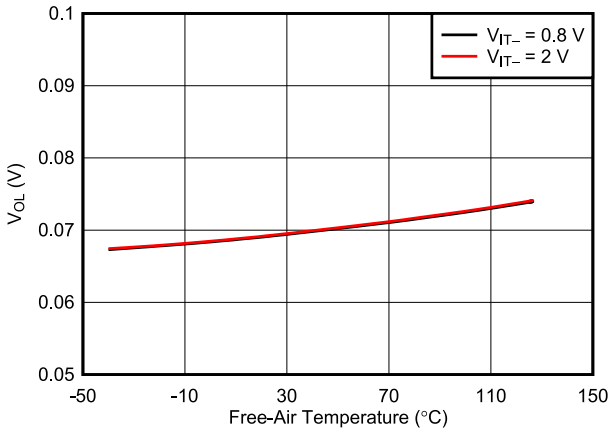



**图 7-15. $V_{OL}$ vs Temperature**

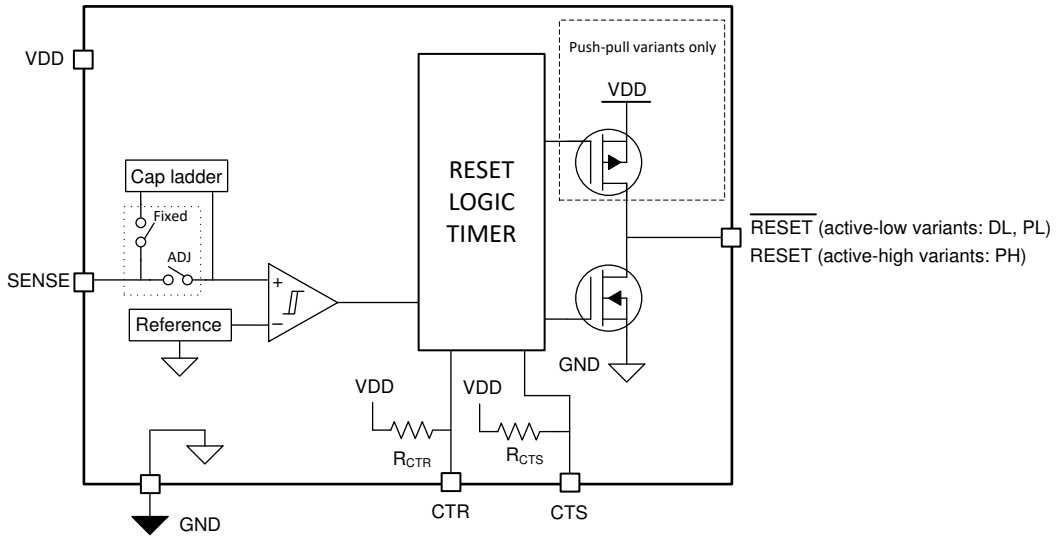
# 8 Detailed Description

## 8.1 Overview

The TPS3899-Q1 voltage supervisor with separate SENSE monitor asserts a $\overline{\text{RESET}}$/RESET signal when the SENSE pin voltage drops below $V_{IT-}$ for the duration of the sense delay set by CTS. If the SENSE pin voltage rises above $V_{IT-}$ + $V_{HYS}$ before the sense delay expires, the $\overline{\text{RESET}}$/RESET pin does not assert. When asserted, the $\overline{\text{RESET}}$/RESET output remains asserted until SENSE voltage returns above $V_{IT-}$ + $V_{HYS}$ for the duration of the reset delay set by CTR. If the SENSE pin voltage falls below $V_{IT-}$ before the reset delay expires while $\overline{\text{RESET}}$ is asserted, $\overline{\text{RESET}}$/RESET will remain asserted.

Like most voltage supervisors, the TPS3899-Q1 includes a reset delay $t_D$ to provide time for the power and clocks to settle before letting the processor out of reset. At power up, the circuits inside the TPS3899-Q1 need additional time to start the reset delay timer after its power supply VDD has reached minimum $V_{DD(MIN)}$ for these circuits to start operating properly. This additional time is specified with the parameter start-up delay $t_{STRT}$. 图 7-1 shows the timing diagram indicating this additional delay. After VDD is stable and above $V_{DD(MIN)}$ subsequent changes of the sense voltage across the threshold voltage will trigger reset after only the reset delay. The reset time delay $t_D$ is set by a capacitor on the CTR pin. The start-up delay has a maximum limit of 300 μs for a ramp rate of $V_{DD} \leqslant 1$ V / μs.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

The combination of user-adjustable sense delay time via CTS and reset delay time via CTR with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages $V_{IT-}$ can be factory set from 0.8 V to 5.4 V in steps of 100 mV [1.1 V to 5.4 V for the -PH (push-pull active high) variants]. CTS and CTR pins allow the sense delay and reset delay to be set to typical values of 30 μs and 40 μs, respectively, by leaving these pins floating. External capacitors can be placed on the CTS and CTR pins to program the sense and reset delays independently.

### 8.3.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below $V_{IT-}$ the output reset is asserted. When the voltage at the VDD pin goes above $V_{IT-}$ plus hysteresis ($V_{HYS}$) the output reset is deasserted after $t_D$ delay.

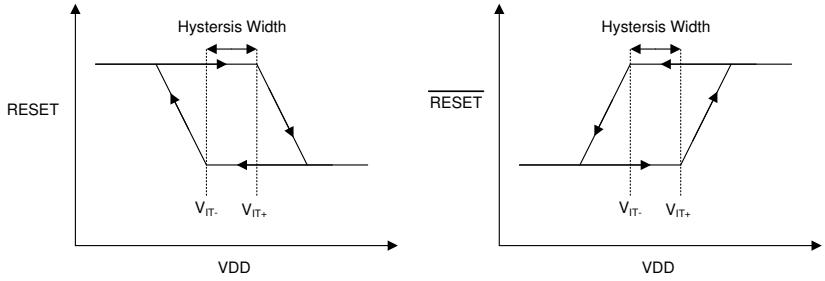



**图 8-1. Hysteresis Diagram**

### 8.3.2 User-Programmable Sense and Reset Time Delay

The sense delay corresponds to the configuration of CTS and the reset delay corresponds to the configuration of CTR. The sense and reset time delay can be set to a minimum value of 50 µs and 80 µs by leaving the CTS and CTR pins floating respectively, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor.

The relationship between external capacitor ($C_{CT\_EXT}$) in Farads at CTS or CTR pins and the time delay in seconds is given by 方程式 1.

$$t_{D\text{-}SENSE\ (typ)} \text{ or } t_{D\ (typ)} = -\ln(0.29) \times R_{CT\ (typ)} \times C_{CT\_EXT} + t_{D\ (CTS \text{ or } CTR = OPEN)} \quad (1)$$

方程式 1 is simplified to 方程式 2 and 方程式 3 by plugging $R_{CT\ (typ)}$ and $t_{D\ (CTS \text{ or } CTR = OPEN)}$ given in 节 7.5 and 节 7.6 section:

$$t_{D\text{-}SENSE} = 618937 \times C_{CTS\_EXT} + 50\ \mu s \quad (2)$$

$$t_D = 618937 \times C_{CTR\_EXT} + 80\ \mu s \quad (3)$$

方程式 4 and 方程式 5 solves for both external capacitor values ($C_{CTS\_EXT}$) and ($C_{CTR\_EXT}$) in units of Farads where $t_{D\text{-}SENSE}$ and $t_D$ are in units of seconds:

$$C_{CTS\_EXT} = (t_{D\text{-}SENSE} - 50\ \mu s) \div 618937 \quad (4)$$

$$C_{CTR\_EXT} = (t_D - 80\ \mu s) \div 618937 \quad (5)$$

The sense or reset delay varies according to three variables: the external capacitor ($C_{CT\_EXT}$), CTS and CTR pin internal resistance ($R_{CT}$) provided in 节 7.5, and a constant. The minimum and maximum variance due to the constant is show in 方程式 6 and 方程式 7:

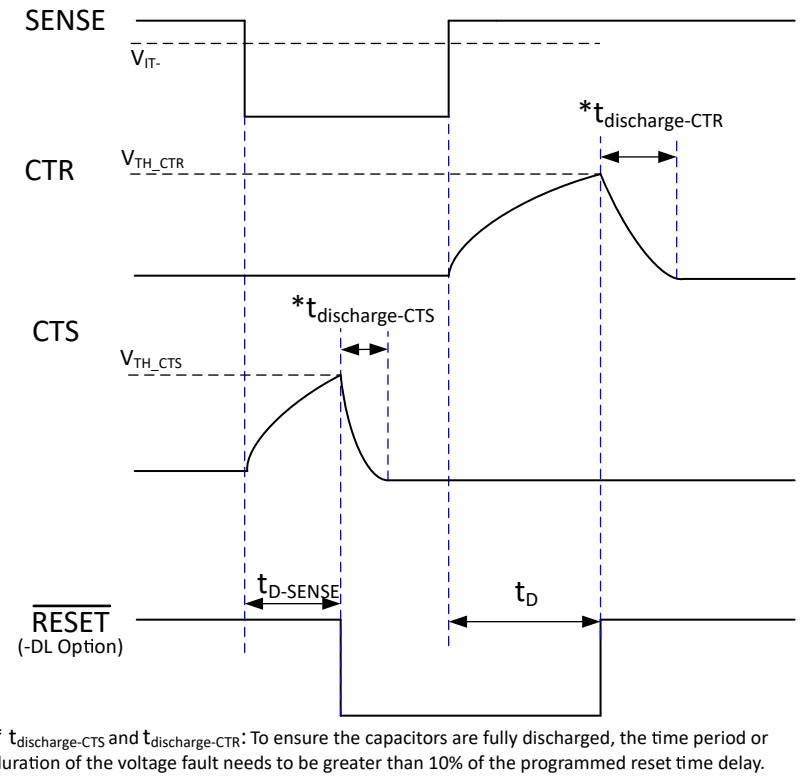
$$t_{D\text{-}SENSE\ (min)} \text{ or } t_{D\ (min)} = -\ln(0.37) \times R_{CT\ (min)} \times C_{CT\_EXT\ (min)} + t_{D\ (no\ cap,\ min)} \quad (6)$$

$$t_{D\text{-}SENSE\ (max)} \text{ or } t_{D\ (max)} = -\ln(0.25) \times R_{CT\ (max)} \times C_{CT\_EXT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (7)$$

The recommended maximum sense and reset delay capacitors for the TPS3899-Q1 is limited to 10 µF as this ensures there is enough time for either capacitors to fully discharge when a voltage fault occurs. When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before either delay capacitors discharges completely, both delays will be shorter than expected. The capacitors will begin charging from a voltage above zero and resulting in shorter than expected time delays. Larger delay capacitors can be used so long as the capacitors have enough time to fully discharge during the

duration of the voltage fault. To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

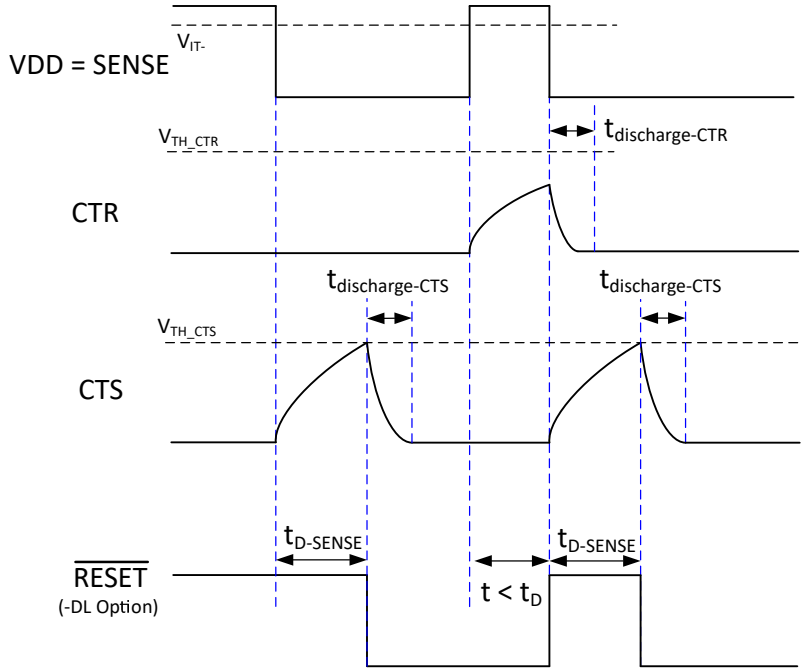
图 8-2 shows the charge and discharge behavior on CTS and CTR that defines the sense and reset delays respectively. When SENSE transitions below $V_{IT-}$, the capacitor connected to CTS begins to charge. Once the CTS capacitor charges to an internal threshold shown as $V_{TH\_CTS}$, $\overline{RESET}$ transitions to active-low logic state and the CTS capacitor then begins to discharge immediately. When SENSE transitions above $V_{IT-} + V_{HYS}$, the capacitor connected to CTR begins to charge. Once the CTR capacitor charges to the internal threshold $V_{TH\_CTR}$, $\overline{RESET}$ releases back to inactive logic high state and the CTR capacitor begins to discharge immediately. Please note that for active-high variants, RESET follows the inverse behavior of $\overline{RESET}$.




* $t_{discharge-CTS}$ and $t_{discharge-CTR}$: To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

**图 8-2. CTS and CTR Charge and Discharge Behavior Relative to SENSE and $\overline{RESET}$**

图 8-3 shows the charge and discharge behavior on CTS and CTR where the monitored voltage is VDD. Similar to 图 8-2, 图 8-3 illustrates a SENSE signal that is transitioning below $V_{IT-}$ before the CTR capacitor reaches to an internal threshold voltage $V_{TH\_CTR}$ and $t < t_D$. The result of the CTR capacitor not reaching the internal threshold voltage $V_{TH\_CTR}$ is $\overline{RESET}$ will become deasserted. Once $\overline{RESET}$ is deasserted, charging beings for the CTS capacitor. When the CTS voltage reaches the internal threshold $V_{TH\_CTS}$, $\overline{RESET}$ will become asserted. This phenomenon is caused by the SENSE falling edge triggering the discharging of the CTR capacitor and producing a deassert signal on the $\overline{RESET}$ output.




* $t_{discharge-CTS}$ and $t_{discharge-CTR}$: To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

**图 8-3. CTS and CTR Charge and Discharge Behavior Relative to VDD, SENSE and $\overline{RESET}$**

### 8.3.3 $\overline{RESET}$/RESET Output

Upon power up, $\overline{RESET}$/RESET begins asserted and remains asserted until the SENSE pin voltage rises above the positive voltage threshold $V_{IT-}$ + $V_{HYS}$ for the duration of the reset delay set by CTR. After the SENSE pin voltage is above $V_{IT-}$ + $V_{HYS}$ for the reset delay, $\overline{RESET}$/RESET deasserts. $\overline{RESET}$/RESET remains deasserted long as the SENSE pin voltage is above the positive threshold. If the SENSE pin voltage falls below the negative threshold ($V_{IT-}$) for the duration of the sense delay set by CTS, then $\overline{RESET}$/RESET is asserted.

An external pull-up resistor is required for the open-drain variants. Connect the external pull-up resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. $\overline{RESET}$/RESET can be pulled up to any voltage up to 6.0 V, independent of the device supply voltage.

### 8.3.4 SENSE Input

The SENSE input can vary from 0 V to 6.0 V, regardless of the device supply voltage used. The SENSE pin is used to monitor a critical voltage rail or push-button input. If the voltage on this pin drops below $V_{IT-}$, then $\overline{RESET}$/RESET is asserted after the sense delay time set by CTS. When the voltage on the SENSE pin rises above the positive threshold voltage $V_{IT-}$ + $V_{HYS}$, $\overline{RESET}$/RESET deasserts after the reset delay time set by CTR. The internal comparator has built-in hysteresis to ensure well-defined $\overline{RESET}$/RESET assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3899-Q1 device is relatively immune to short transients on the SENSE pin. Glitch immunity

($t_{GI\_V_{IT-}SENSE}$), found in 节 7.6, is dependent on threshold overdrive, as illustrated in 图 7-7. Although not required in most cases, for noisy applications, good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

#### 8.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3899-Q1 is immune to short voltage transient spikes on the input pins. To further improve the noise immunity on the SENSE pin, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.

Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much $V_{SENSE}$ exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 方程式 8.

$$\text{Overdrive} = | ((V_{SENSE} / V_{IT-}) - 1) \times 100\% | \quad (8)$$

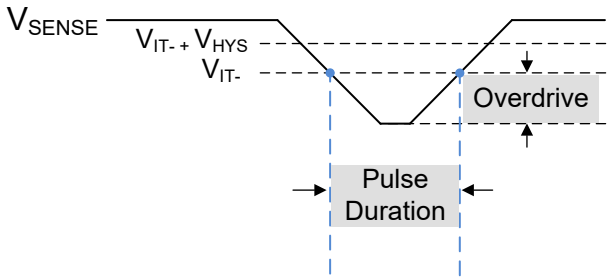



图 8-4. Overdrive vs Pulse Duration

## 8.4 Device Functional Modes

表 8-1 summarizes the various functional modes of the device.

表 8-1. Truth Table

| $V_{DD}$ | SENSE (1) | $\overline{RESET}$ | RESET |
|---|---|---|---|
| $V_{DD} < V_{POR}$ | — | Undefined | Undefined |
| $V_{POR} < V_{DD} < V_{DD(MIN)}$ (2) | — | L | H |
| $V_{DD} \geqslant V_{DD(MIN)}$ | $V_{SENSE} < V_{IT-}$ | L | H |
| $V_{DD} \geqslant V_{DD(MIN)}$ | $V_{SENSE} > V_{IT-} + V_{HYS}$ | H | L |

(1) SENSE pin voltage must be less than $V_{IT-}$ for the sense delay set by CTS or greater than $V_{IT-} + V_{HYS}$ for the reset delay set by CTR before RESET transitions
(2) When $V_{DD}$ falls below $V_{DD(MIN)}$, the internal undervoltage-lockout takes effect and $\overline{RESET}$ is held logic low (RESET is held logic high) until $V_{DD}$ falls below $V_{POR}$ at which the $\overline{RESET}$/RESET output is undefined.

### 8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When $V_{DD}$ is greater than $V_{DD(min)}$, the $\overline{RESET}$/RESET pin is determined by the voltage on the SENSE pin and the sense delay and reset delay set by CTS and CTR respectively.

### 8.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on $V_{DD}$ is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage $V_{POR}$, the $\overline{RESET}$/RESET signal is asserted regardless of the voltage on the SENSE pin.

### 8.4.3 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on $V_{DD}$ is lower than $V_{POR}$, the device does not have enough voltage to assert the output $\overline{RESET}$/RESET to its correct logic state. The output results in being undefined as shown in 图 7-1 or in 图 7-2. If the output $\overline{RESET}$/RESET is an open-drain variant, its voltage may be pulled up to $V_{DD}$ or to the pull-up voltage. Neither output should be relied upon for proper device function.

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

## 9.2 Typical Application

### 9.2.1 Design 1: Dual Rail Monitoring with Power-Up Sequencing

A typical application for the TPS3899-Q1 is voltage rail monitoring and power-up sequencing as shown in 图 9-1. The TPS3899-Q1 can be used to monitor any rail above 0.8 V. In this design application, two TPS3899-Q1 devices monitor two separate voltage rails and sequences the rails upon power-up. The TPS3899DL01-Q1 is used to monitor the 3.3 V main power rail and the TPS3899PL16-Q1 is used to monitor the 1.8 V rail provided by the LDO for other system peripherals. The $\overline{\text{RESET}}$ output of the TPS3899DL01-Q1 is connected to the enable (EN) input of the LDO with an external pull-up resistor $R_{PULL-UP}$ to the 3.3 V power rail. The $\overline{\text{RESET}}$ output of the TPS3899PL16-Q1 is connected to the ($\overline{\text{RESET}}$) input of the microcontroller. A reset event is initiated on either voltage supervisor when the VDD voltage is less than $V_{IT-}$ falling threshold voltage. For a system reset event, a push-button input is placed at the SENSE pin of the TPS3899DL01-Q1.

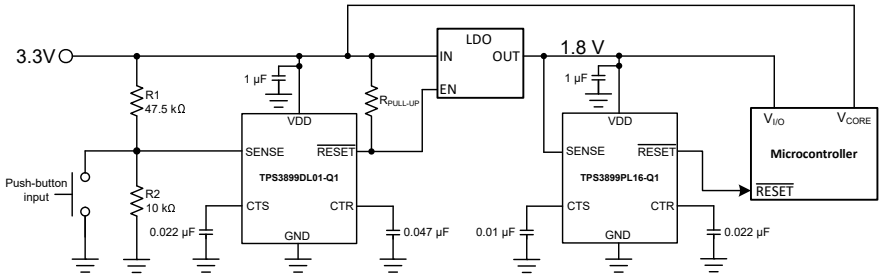



**图 9-1. TPS3899-Q1 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram**

#### *9.2.1.1 Design Requirements*

This design requires voltage supervision on two voltage rails: 3.3 V and 1.8 V. The voltage rails need to sequence upon power up with the 3.3 V coming up at least 25 ms followed by the 1.8 V rail.

| PARAMETER | DESIGN REQUIREMENT | DESIGN RESULT |
|---|---|---|
| Two Rail Voltage Supervision | Monitor 3.3 V and 1.8 V rails | Two TPS3899-Q1 devices provide voltage monitoring with 1% accuracy with either an adjustable threshold device or fixed voltage options available in 0.1 V variations. |
| Voltage Rail Sequencing | Power up the 3.3 V rail first within 25 ms followed by 1.8 V rail | The CTR capacitors on TPS3899DL01-Q1 and TPS3899PL16-Q1 are set to 0.047 µF and 0.022 µF, respectively, for a reset time delays of 29 ms and 13.7 ms typical. |
| Reset Asserting and Timing 1 | Reset needs to assert under the reset condition of a push-button press or VDD < 2.9 V after a period of 10 ms. | Reset will assert under the reset condition of a push-button press or VDD < 2.9 V after a period of 13.7 ms. The $\overline{\text{RESET}}$output will deassert after 29 ms when VDD > 3.05 V. |
| Reset Asserting and Timing 2 | Reset needs to assert under the reset condition of VDD < 1.6 V after a period of 5 ms. | Reset will assert under the reset condition of VDD < 1.6 V after a period of 6.2 ms. The $\overline{\text{RESET}}$ output will deassert after 13.7 ms when VDD > 1.68 V. |

| PARAMETER | DESIGN REQUIREMENT | DESIGN RESULT |
|---|---|---|
| Max device current consumption | 1 µA | Each TPS3899-Q1 requires 125 nA typical. |

### 9.2.1.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS3899-Q1 can monitor any voltage with the adjustable voltage threshold option or fixed voltages between 0.8 V and 5.4 V. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, 图 9-2 shows the output, $\overline{\text{RESET}}$, of the TPS3899DL01-Q1 when the 3.3 V rail falls to 2.9 V after the sense time delay expires. The TPS3899PL16-Q1 triggers a reset when the 1.8 V rail falls to 1.6 V.

The secondary constraint for this application is the sense and reset time delay. If the monitored voltage rail 3.3 V has large voltage ripple noise and it goes below the programmed threshold voltage but returns above the $V_{IT-}$+ $V_{HYS}$ before the sense time delay expires, the output will not assert. Therefore, the sense time delay prevents false sense resets by allowing the monitored voltage rail 3.3 V to not assert the output during the programmed sense time delay period set by the capacitor on the CTS pin. In the application, the CTS capacitors for both the TPS3899DL01-Q1 and TPS3899PL16-Q1 are set to be 0.022 µF and 0.01 µF, respectively, and resulted in sense time delays of 13.7 ms and 6.2 ms. In addition to the sense delay time, the reset time delay for the TPS3899DL01-Q1 must be at least 25 ms to allow the microprocessor, and all other devices using the 3.3 V rail, enough time to startup correctly before the 1.8 V rail is enabled via the LDO. Once the LDO is enabled, the reset time delay for the TPS3899PL16-Q1 must be at least 10 ms to allow the 1.8 V rail to settle. For applications with ambient temperatures ranging from –40°C to +125°C, CTS and CTR can be calculated using $R_{CTS}$ and $R_{CTR}$. Solving for $C_{CTS}$ and $C_{CTR}$ in 方程式 4 and 方程式 5 for 10 ms and 25 ms gives a minimum capacitor value of 0.016 µF and 0.0403 µF which are rounded up to standard values of 0.022 µF and 0.047 µF, respectively, to account for capacitor tolerance.

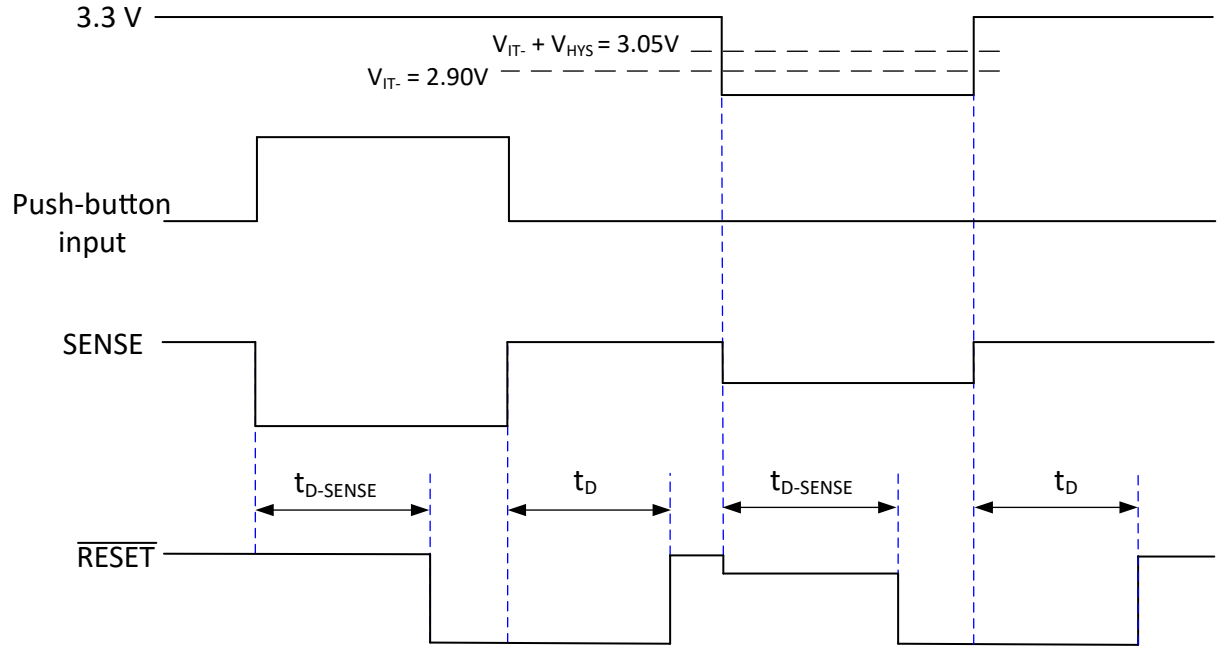



**图 9-2. TPS3899DL01-Q1 3.3 V Voltage Rail Monitor Timing Diagram**

A 1 µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the open-drain device variants and is calculated to ensure that $V_{OL}$ does not exceed max limit given the $I_{\overline{\text{RESET}}(\text{Sink})}$ possible at the expected supply voltage. The open-drain variant is used in this design example and the nominal VDD is 3.3 V but dropping to 2.9 V for $V_{IT-}$, the voltage across the pull-up resistor can be determined. In 节 7.5, max $V_{OL}$ provides 2 mA $I_{\overline{\text{RESET}}(\text{Sink})}$ for 3.3 V VDD. Using 2 mA of $I_{\overline{\text{RESET}}(\text{Sink})}$ and 300

mV max $V_{OL}$, gives us 1.3 kΩ for the pull-up resistor. Any value higher than 1.3 kΩ would ensure that $V_{OL}$ will not exceed 300 mV max specification.

## 9.3 Application Curves

These application curves were taken with the TPS3899EVM which uses the TPS3899DL01DSER. Please see the TPS3899EVM User Guide for more information.

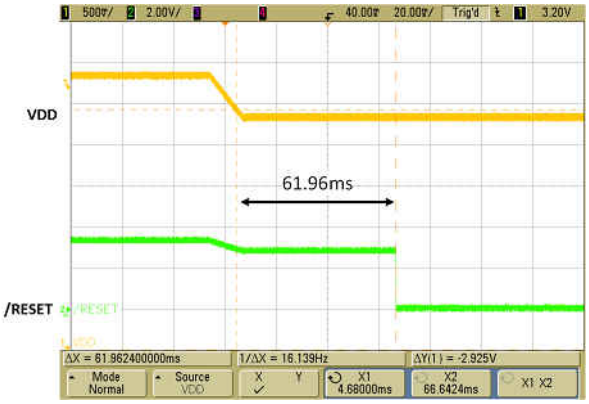



图 9-3. Sense Delay where CTS = 0.1 µF

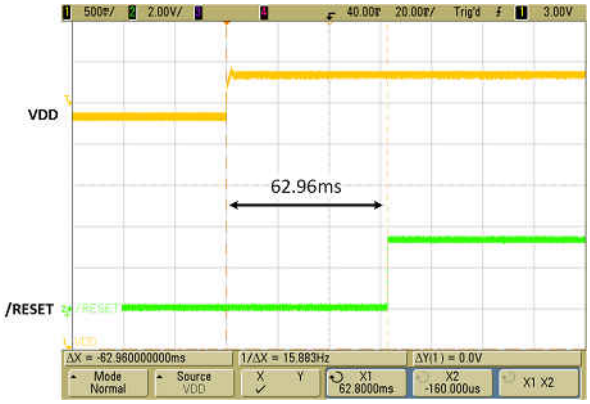



图 9-4. Reset Delay where CTR = 0.1 µF

## 10 Power Supply Recommendations

The TPS3899-Q1 is designed to operate from an input supply with a voltage range between 0.85 V and 6 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1 µF capacitor between the VDD pin and the GND pin. Also, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal. This device has a 6.5 V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6.5 V, additional precautions must be taken.

# 11 Layout

## 11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1 µF ceramic capacitor near the VDD pin. If a capacitor is not connected to the CTS or CTS pins, then minimize parasitic capacitance on this pin so the sense delay or reset delay times are not adversely affected. To improve noise immunity on the SENSE pin, place a capacitor ($C_{SENSE}$) as close as possible to the SENSE pin. Placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.

## 11.2 Layout Example

The layout example in 图 11-1 shows how the TPS3899-Q1 is laid out on a printed circuit board (PCB) with a user-defined sense delay and reset delay.

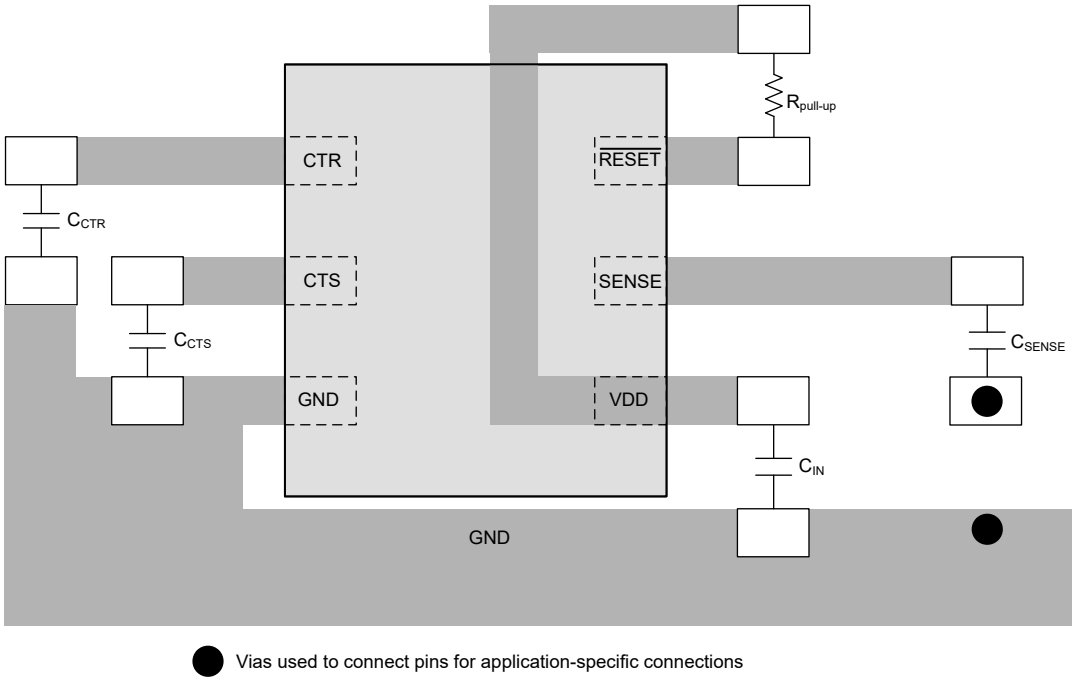



**图 11-1. Recommended Layout**

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Device Nomenclature

图 5-1 in Device Nomenclature and 表 12-1 shows how to decode the function of the device based on its part number shown in 表 12-2.

**表 12-1. Device Naming Convention**

| DESCRIPTION | NOMENCLATURE | VALUE |
|---|---|---|
| Generic Part number | TPS3899-Q1 | TPS3899-Q1 |
| Variant code (Output Toplogy) | DL | Open-Drain, Active-Low |
| | PL | Push-Pull, Active-Low |
| | PH | Push-Pull, Active-High |
| Detect Voltage Option | ## (two characters) | 01: 0.505 V (adjustable) |
| | | Example: 08 stands for 0.8 V threshold<br>0.8 V to 5.4 V (fixed threshold voltage) |
| Package | DSE | WSON |
| Reel | R | Large Reel |
| Automotive Version | Q1 | AEC-Q100 |

表 12-2 shows the possible variants of the TPS3899-Q1. Please refer to the Package Option Addendum (POA), in this datasheet, for which variant is orderable and available; minimum order quantities apply.

**表 12-2. Device Naming Convention**

| ORDERABLE DEVICE NAME | | | THRESHOLD VOLTAGE (V) |
|---|---|---|---|
| -DL (OPEN-DRAIN ACTIVE-LOW) | -PL (PUSH-PULL ACTIVE-LOW) | -PH (PUSH-PULL ACTIVE-HIGH) | |
| TPS3899DL01-Q1 | TPS3899PL01-Q1 | TPS3899PH01-Q1 | 0.505 |
| TPS3899DL08-Q1 | TPS3899PL08-Q1 | N/A | 0.80 |
| TPS3899DL09-Q1 | TPS3899PL09-Q1 | N/A | 0.90 |
| TPS3899DL10-Q1 | TPS3899PL10-Q1 | N/A | 1.00 |
| TPS3899DL11-Q1 | TPS3899PL11-Q1 | TPS3899PH11-Q1 | 1.10 |
| TPS3899DL12-Q1 | TPS3899PL12-Q1 | TPS3899PH12-Q1 | 1.20 |
| TPS3899DL13-Q1 | TPS3899PL13-Q1 | TPS3899PH13-Q1 | 1.30 |
| TPS3899DL14-Q1 | TPS3899PL14-Q1 | TPS3899PH14-Q1 | 1.40 |
| TPS3899DL15-Q1 | TPS3899PL15-Q1 | TPS3899PH15-Q1 | 1.50 |
| TPS3899DL16-Q1 | TPS3899PL16-Q1 | TPS3899PH16-Q1 | 1.60 |
| TPS3899DL17-Q1 | TPS3899PL17-Q1 | TPS3899PH17-Q1 | 1.70 |
| TPS3899DL18-Q1 | TPS3899PL18-Q1 | TPS3899PH18-Q1 | 1.80 |
| TPS3899DL19-Q1 | TPS3899PL19-Q1 | TPS3899PH19-Q1 | 1.90 |
| TPS3899DL20-Q1 | TPS3899PL20-Q1 | TPS3899PH20-Q1 | 2.00 |
| TPS3899DL21-Q1 | TPS3899PL21-Q1 | TPS3899PH21-Q1 | 2.10 |
| TPS3899DL22-Q1 | TPS3899PL22-Q1 | TPS3899PH22-Q1 | 2.20 |
| TPS3899DL23-Q1 | TPS3899PL23-Q1 | TPS3899PH23-Q1 | 2.30 |
| TPS3899DL24-Q1 | TPS3899PL24-Q1 | TPS3899PH24-Q1 | 2.40 |
| TPS3899DL25-Q1 | TPS3899PL25-Q1 | TPS3899PH25-Q1 | 2.50 |
| TPS3899DL26-Q1 | TPS3899PL26-Q1 | TPS3899PH26-Q1 | 2.60 |

表 12-2. Device Naming Convention (continued)

| ORDERABLE DEVICE NAME | | | THRESHOLD VOLTAGE (V) |
|---|---|---|---|
| -DL (OPEN-DRAIN ACTIVE-LOW) | -PL (PUSH-PULL ACTIVE-LOW) | -PH (PUSH-PULL ACTIVE-HIGH) | |
| TPS3899DL27-Q1 | TPS3899PL27-Q1 | TPS3899PH27-Q1 | 2.70 |
| TPS3899DL28-Q1 | TPS3899PL28-Q1 | TPS3899PH28-Q1 | 2.80 |
| TPS3899DL29-Q1 | TPS3899PL29-Q1 | TPS3899PH29-Q1 | 2.90 |
| TPS3899DL30-Q1 | TPS3899PL30-Q1 | TPS3899PH30-Q1 | 3.00 |
| TPS3899DL31-Q1 | TPS3899PL31-Q1 | TPS3899PH31-Q1 | 3.10 |
| TPS3899DL32-Q1 | TPS3899PL32-Q1 | TPS3899PH32-Q1 | 3.20 |
| TPS3899DL33-Q1 | TPS3899PL33-Q1 | TPS3899PH33-Q1 | 3.30 |
| TPS3899DL34-Q1 | TPS3899PL34-Q1 | TPS3899PH34-Q1 | 3.40 |
| TPS3899DL35-Q1 | TPS3899PL35-Q1 | TPS3899PH35-Q1 | 3.50 |
| TPS3899DL36-Q1 | TPS3899PL36-Q1 | TPS3899PH36-Q1 | 3.60 |
| TPS3899DL37-Q1 | TPS3899PL37-Q1 | TPS3899PH37-Q1 | 3.70 |
| TPS3899DL38-Q1 | TPS3899PL38-Q1 | TPS3899PH38-Q1 | 3.80 |
| TPS3899DL39-Q1 | TPS3899PL39-Q1 | TPS3899PH39-Q1 | 3.90 |
| TPS3899DL40-Q1 | TPS3899PL40-Q1 | TPS3899PH40-Q1 | 4.00 |
| TPS3899DL41-Q1 | TPS3899PL41-Q1 | TPS3899PH41-Q1 | 4.10 |
| TPS3899DL42-Q1 | TPS3899PL42-Q1 | TPS3899PH42-Q1 | 4.20 |
| TPS3899DL43-Q1 | TPS3899PL43-Q1 | TPS3899PH43-Q1 | 4.30 |
| TPS3899DL44-Q1 | TPS3899PL44-Q1 | TPS3899PH44-Q1 | 4.40 |
| TPS3899DL45-Q1 | TPS3899PL45-Q1 | TPS3899PH45-Q1 | 4.50 |
| TPS3899DL46-Q1 | TPS3899PL46-Q1 | TPS3899PH46-Q1 | 4.60 |
| TPS3899DL47-Q1 | TPS3899PL47-Q1 | TPS3899PH47-Q1 | 4.70 |
| TPS3899DL48-Q1 | TPS3899PL48-Q1 | TPS3899PH48-Q1 | 4.80 |
| TPS3899DL49-Q1 | TPS3899PL49-Q1 | TPS3899PH49-Q1 | 4.90 |
| TPS3899DL50-Q1 | TPS3899PL50-Q1 | TPS3899PH50-Q1 | 5.00 |
| TPS3899DL51-Q1 | TPS3899PL51-Q1 | TPS3899PH51-Q1 | 5.10 |
| TPS3899DL52-Q1 | TPS3899PL52-Q1 | TPS3899PH52-Q1 | 5.20 |
| TPS3899DL53-Q1 | TPS3899PL53-Q1 | TPS3899PH53-Q1 | 5.30 |
| TPS3899DL54-Q1 | TPS3899PL54-Q1 | TPS3899PH54-Q1 | 5.40 |

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3899DL01DSERQ1 | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | M4 | Samples |
| TPS3899DL30DSERQ1 | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | M5 | Samples |
| TPS3899DL31DSERQ1 | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | M7 | Samples |
| TPS3899PL16DSERQ1 | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LO | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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**OTHER QUALIFIED VERSIONS OF TPS3899-Q1 :**

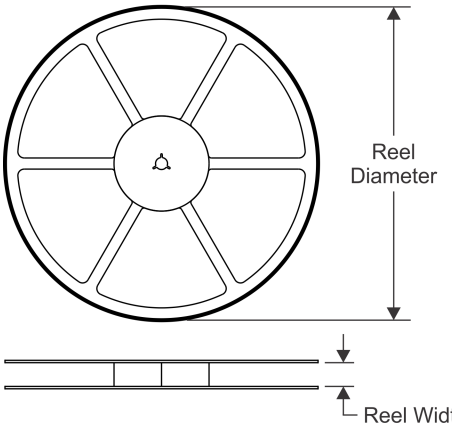
- Catalog : TPS3899

NOTE: Qualified Version Definitions:

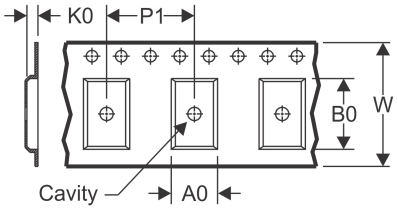
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

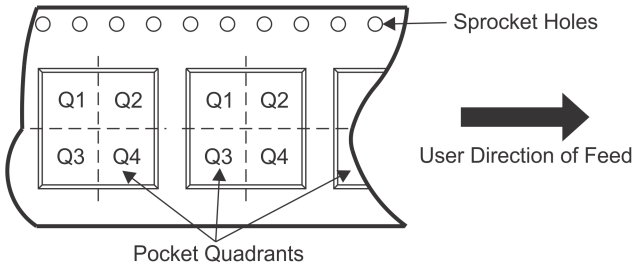



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

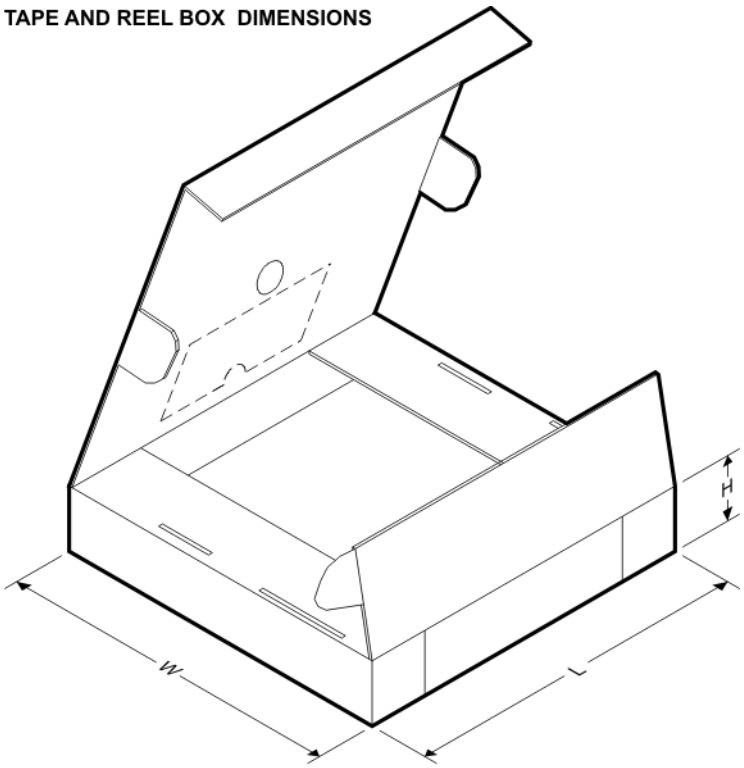
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3899DL01DSERQ1 | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS3899DL30DSERQ1 | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS3899DL31DSERQ1 | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS3899PL16DSERQ1 | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |

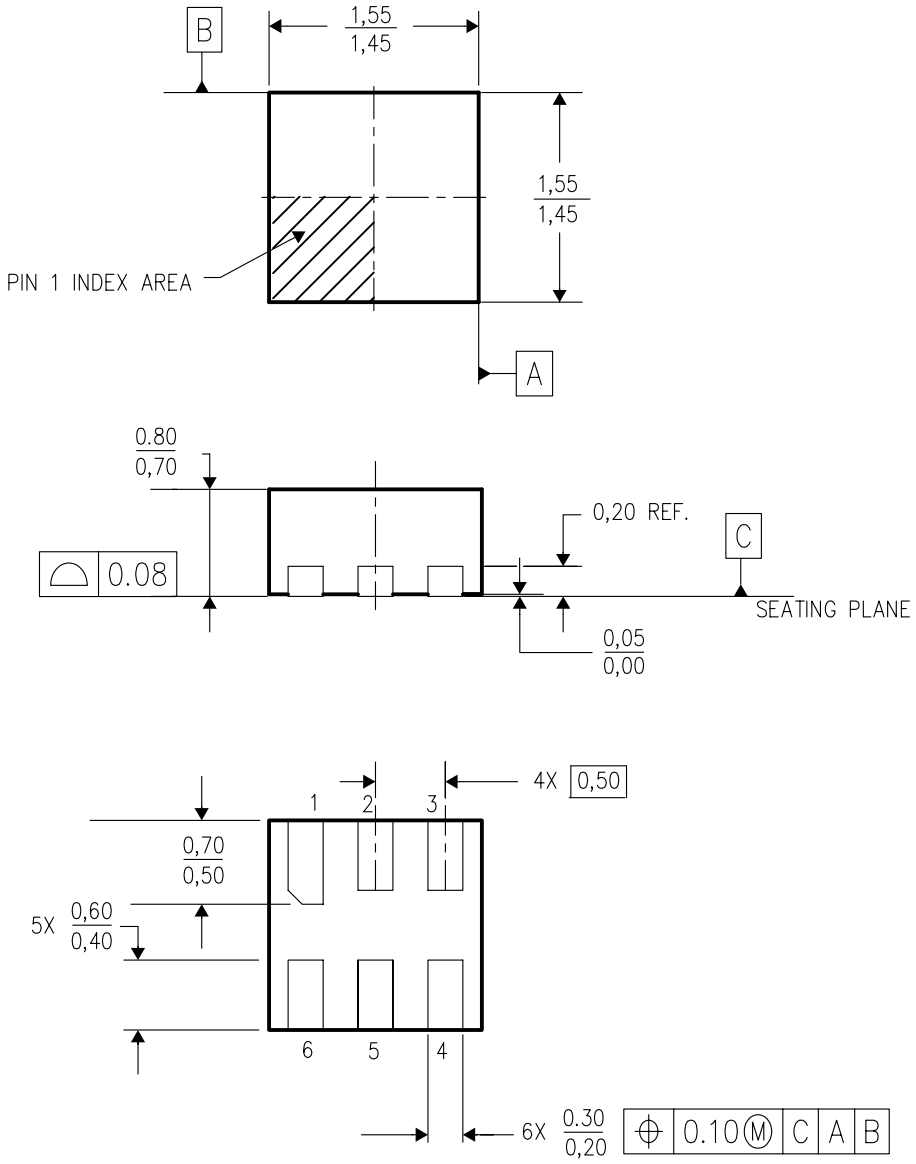
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3899DL01DSERQ1 | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS3899DL30DSERQ1 | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS3899DL31DSERQ1 | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS3899PL16DSERQ1 | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE




4207810/A 03/06

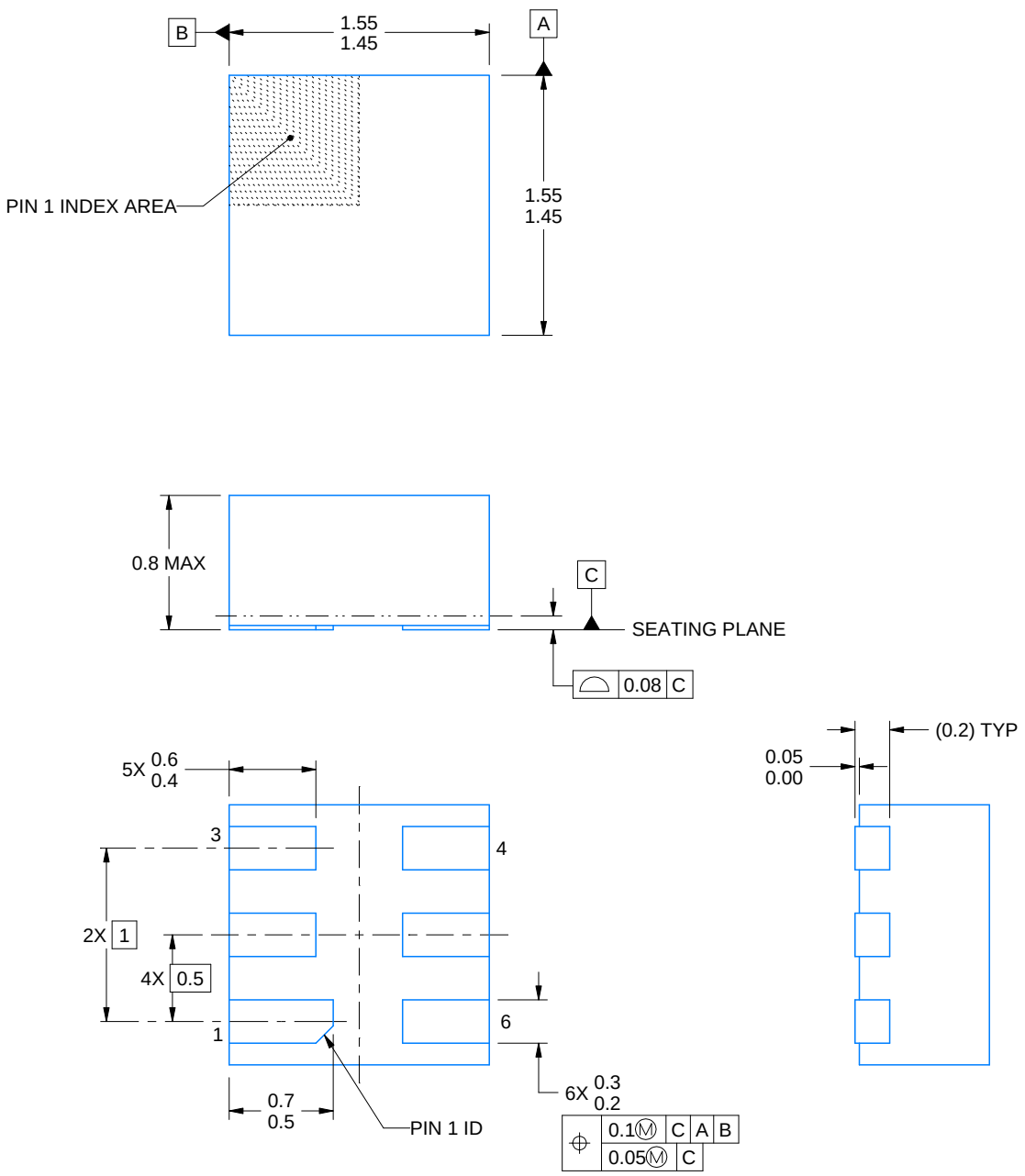
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

# DSE0006A

# PACKAGE OUTLINE

## WSON - 0.8 mm max height

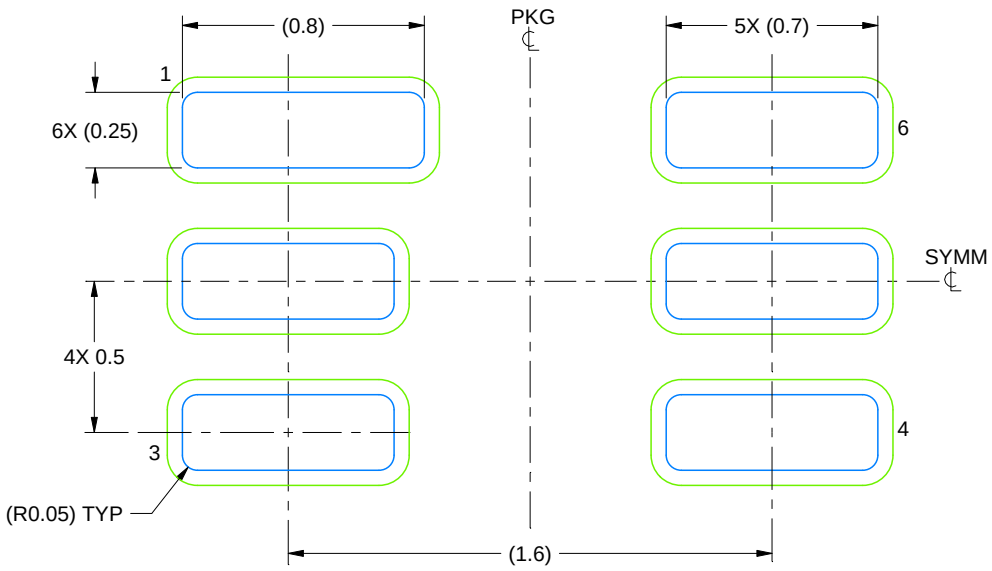
PLASTIC SMALL OUTLINE - NO LEAD



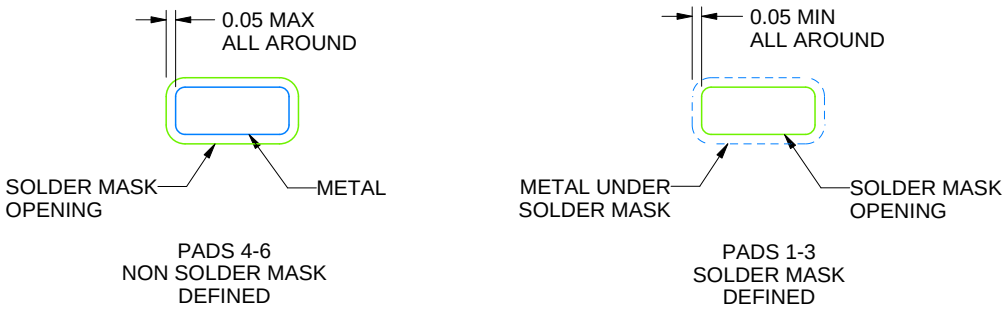

4220552/A 04/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X

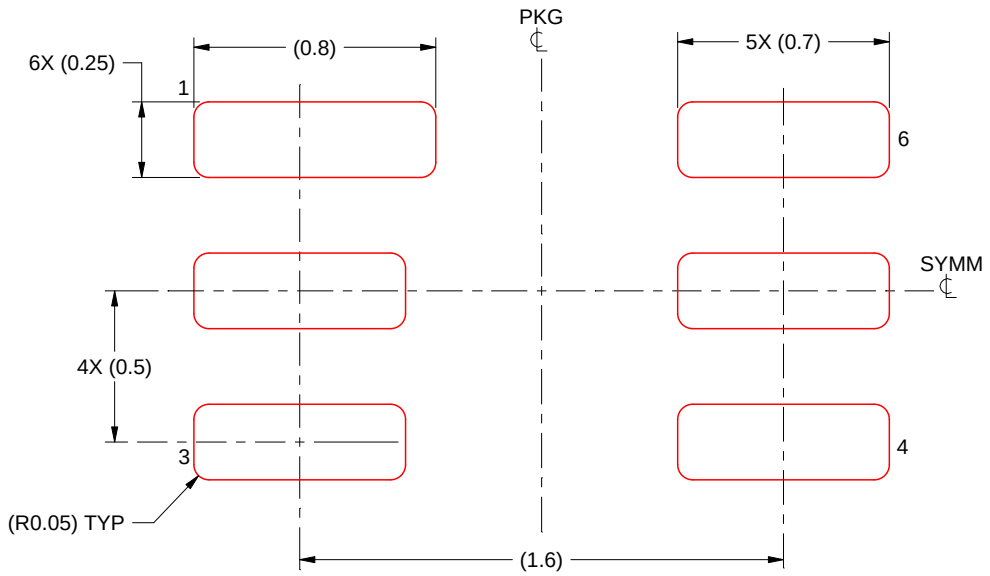



SOLDER MASK DETAILS

4220552/A 04/2021

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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