TPS3899 纳米功率、精密电压监控器，具有可编程感应和复位延迟的按钮监视器

1 特性

- 提供功能安全
  - 可帮助设计功能安全系统的文档
- 精密电压和按钮监视器
- VDD 范围：0.85V 至 6V（DL 和 PL 输出）
- VDD 范围：1V 至 6V（PH 输出）
- 可编程感应和复位延迟
- 纳米静态电流：125nA（典型值）
- 高阈值精度：±0.5%（典型值）
- 精密迟滞：5%（典型值）
- 可调节阈值电压：0.505 V（典型值）
- 固定阈值电压：0.8 V 至 5.4 V
  - 步长为 100mV 的固定阈值电平
- 多路输出拓扑
  - DL：开漏低电平有效
  - PL：推挽低电平有效
  - PH：推挽高电平有效
- 温度范围：–40°C 至 +125°C
- 封装：1.5mm × 1.5mm WSON

2 应用

- 电表
- 楼宇自动化
- 车身控制模块 (BCM)
- 数据中心和企业级计算
- 笔记本电脑、台式机、服务器
- 智能手机、手持产品
- 便携式、电池供电类设备
- 固态硬盘
- STB 和 DVR

3 说明

TPS3899 是一款纳米功率精密电压监控器，具有 ±0.5% 的阈值精度、可编程感应和复位延时时间，并采用空间节省的 6 引脚 1.5mm × 1.5mm WSON 封装。TPS3899 是一款功能丰富的电压监控器，提供了同类产品中最小的总解决方案尺寸。在监控电压轨或按钮信号时，内置迟滞和可编程延迟防止出现错误的复位信号。

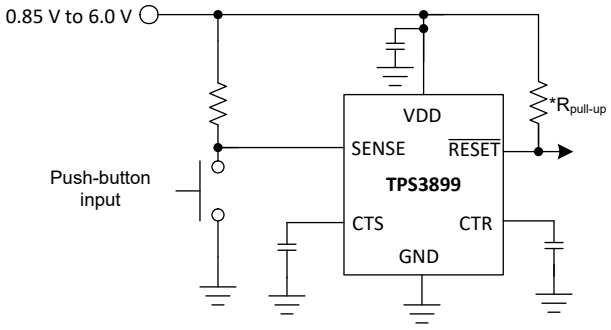
通过单独的 VDD 和 SENSE 引脚，可实现高可靠性系统所需的冗余。SENSE 与 VDD 解耦，可以监控 VDD 以外的轨电压。SENSE 引脚的高阻抗输入支持使用可选的外部电阻器。CTS 和 CTR 都提供了对 RESET 信号的上升沿和下降沿进行延迟调整的能力。CTS 还通过忽略受监控电压轨上的电压电子脉冲干扰而充当去抖动器；并作为“手动复位”，用于强制系统复位。

TPS3899 的精密性能、卓越的功能和紧凑的外形使其成为各种工业和电池供电应用（例如，工厂/楼宇自动化、电机驱动和消费类产品）的理想解决方案。该器件的额定工作温度范围为 –40°C 至 +125°C (T_A)。

器件信息

零件编号	封装 (1)	封装尺寸（标称值）
TPS3899	WSON (6) DSE	1.5mm x 1.5mm

1. 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录



*$R_{pull-up}$ is required for open-drain variants only

典型应用电路

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2020) to Revision B (January 2022)	Page
• 新增了“功能安全型”	1
• Changed IDD from 1.2 µA to 1 µA	5

Changes from Revision * (September 2020) to Revision A (November 2020)	Page
• APL 到 RTM 版本	1

5 Device Comparison

图 5-1 shows the device naming nomenclature of the TPS3899. For all possible output types and threshold voltages options, see Device Naming Convention for a more detailed explanation. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

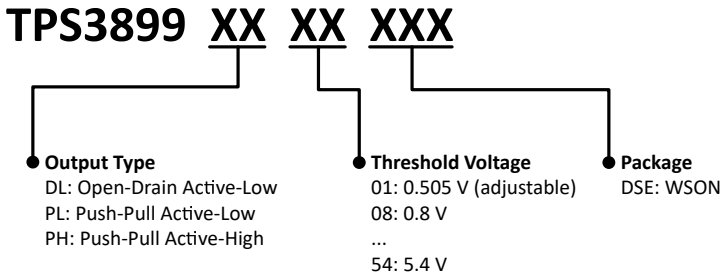


图 5-1. Device Naming Nomenclature

6 Pin Configuration and Functions

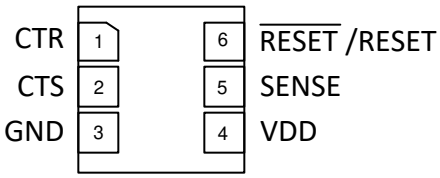


**图 6-1. DSE Package,
6-Pin ,
TPS3899 Top View**

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CTR	—	Capacitor programmable reset delay: The CTR pin offers a user-adjustable delay time when returning from reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to deassert.
2	CTS	—	Capacitor programmable sense delay: The CTS pin offers a user-adjustable delay time when asserting reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to assert.
3	GND	—	Ground
4	VDD	I	Supply voltage pin: Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.
5	SENSE	I	This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. When the voltage on the SENSE pin transistions below the negative threshold voltage V_{IT-}, $\overline{\text{RESET}}$/RESET asserts to active logic after the sense delay set by CTS. When the voltage on the SENSE pin transistions above the positive threshold voltage $V_{IT-} + V_{HYS}$, $\overline{\text{RESET}}$/RESET releases to inactive logic (deasserts) after the reset delay set by CTR. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.
6	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ active-low output that asserts to a logic low state after CTS delay when the monitored voltage on the SENSE pin is lower than the negative threshold voltage V_{IT-}. $\overline{\text{RESET}}$ remains logic low (asserted) until the SENSE input rises above $V_{IT-} + V_{HYS}$ and the CTR reset delay expires.
6	RESET	O	RESET active-high output that asserts to a logic high state after CTS delay when the monitored voltage on the SENSE pin is lower than the negative threshold voltage V_{IT-}. RESET remains logic high (asserted) until the SENSE input rises above $V_{IT-} + V_{HYS}$ and the CTR reset delay expires.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD, SENSE	– 0.3	6.5	V
Voltage	CTR, CTS	– 0.3	V_{DD}+0.3 (3)	V
Voltage	$\overline{\text{RESET}}$ (TPS389DL)	– 0.3	6.5	V
	$\overline{\text{RESET}}$ (TPS3899PL), RESET (TPS3899PH)	-0.3	V_{DD}+0.3 (3)	
Current	$\overline{\text{RESET}}$ pin and RESET pin		±20	mA
Temperature(2)	Operating ambient temperature, T_A	– 40	125	°C
Temperature(2)	Storage, T_{stg}	– 65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD, SENSE	0		6	V
Voltage	CTR, CTS	0		VDD	V
Voltage	$\overline{\text{RESET}}$ (TPS3899DL)	0		6	V
	$\overline{\text{RESET}}$ (TPS3899PL), RESET (TPS3899PH)	0		VDD	
Current	$\overline{\text{RESET}}$ pin and RESET pin current	0		±5	mA
T_A	Operating free air temperature	– 40		125	°C
C_{CTR}	CTR pin capacitor range	0		10	µF
C_{CTS}	CTS pin capacitor range	0		10	µF

7.4 Thermal Information

THERMAL METRIC(1)		TPS3899 DSE 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	112.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	111.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40℃ to 125℃, unless otherwise noted. V_{DD} ramp rate ≤ 1 V/µs. Typical values are at T_A = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage (Open Drain Low and Push Pull Low)		0.85		6	V
V_{DD}	Input supply voltage (Push Pull High)		1		6	V
V_{IT-} (1)	Negative-going input threshold range	for all output configs	0.8		5.4	V
$V_{ADJ-VIT-}$	Negative-going input threshold for adjustable sense threshold version			0.505		V
V_{IT-} accuracy	Negative-going input threshold accuracy	V_{IT-} = 0.505 V (ADJ version) or 0.8 V to 1.7 V (Fixed threshold)	–2.5	±0.5	2.5	%
		V_{IT-} = 1.8 V to 5.4 V (Fixed threshold)	–2	±0.5	2	
V_{HYS}	Hysteresis on V_{IT-}	V_{IT-} = 0.505 V and 0.8 V	3	5	8	%
		V_{IT-} = 0.9 V to 5.4 V	3	5	7	%
I_{SENSE}	Current into Sense pin, fixed threshold version	V_{DD} = V_{SENSE} = 6 V		0.025	0.1	µA
	Current into Sense pin, ADJ version	V_{DD} = V_{SENSE} = 6 V		0.025	0.05	µA
I_{DD}	Supply current into VDD pin when sense pin is separate	V_{DD} = V_{SENSE} = 6 V V_{IT-} = 0.505 V and 0.8 V to 5.4 V		0.125	1	µA
V_{TH_CTS}	Voltage threshold to stop CTS capacitor charge and assert RESET			0.73 * V_{DD}		V
V_{TH_CTR}	Voltage threshold to stop CTR capacitor charge and deassert RESET			0.73 * V_{DD}		V
R_{CTS}	CTS pin internal pull up resistance			500		kΩ
R_{CTR}	CTR pin internal pull up resistance			500		kΩ
TPS3899DL (Open-drain active-low)						
V_{POR}	Power on reset voltage (2)	$V_{OL(max)}$ = 300 mV $I_{\overline{RESET}(Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 0.85 V $I_{\overline{RESET}(Sink)}$ = 15 µA			300	mV
		V_{DD} = 3.3 V $I_{\overline{RESET}(Sink)}$ = 2 mA			300	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	V_{DD} = V_{PULLUP} = 6 V, T_A = –40℃ to 85℃		10	100	nA
		V_{DD} = V_{PULLUP} = 6 V		10	350	nA
TPS3899PL (Push-pull active-low)						
V_{POR}	Power on reset voltage (2)	$V_{OL(max)}$ = 300 mV $I_{\overline{RESET}(Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 0.85 V $I_{\overline{RESET}(Sink)}$ = 15 µA			300	mV
		V_{DD} = 3.3 V $I_{\overline{RESET}(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage	V_{DD} = 1.8 V $I_{\overline{RESET}(Source)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 3.3 V $I_{\overline{RESET}(Source)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 6 V $I_{\overline{RESET}(Source)}$ = 2 mA	0.8V_{DD}			V

7.5 Electrical Characteristics (continued)

CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40℃ to 125℃, unless otherwise noted. V_{DD} ramp rate ≤ 1 V/µs. Typical values are at T_A = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS3899PH (Push-pull active-high)						
V_{POR}	Power on reset voltage(2)	$V_{OH(min)}$ = 0.8V_{DD} $I_{RESET\ (Source)}$ = 15 uA			900	mV
V_{OL}	Low level output voltage	V_{DD} = 3.3 V $I_{RESET(Sink)}$ = 500 µA			300	mV
		V_{DD} = 6 V $I_{RESET(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage	V_{DD} = 1V $I_{RESET(Sink)}$ = 15 µA	0.8V_{DD}			V
		V_{DD} = 1.5 V $I_{RESET(Sink)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 3.3 V $I_{RESET(Sink)}$ = 2 mA	0.8V_{DD}			V

(1) V_{IT-} threshold voltage range from 0.8 V to 5.4 V (for DL, PL) and 1 to 5.4 V (for PH) in 100 mV steps, for released versions see Device Voltage Thresholds table.
(2) Minimum V_{DD} voltage level for a controlled output state. Below V_{POR}, the output cannot be determined.

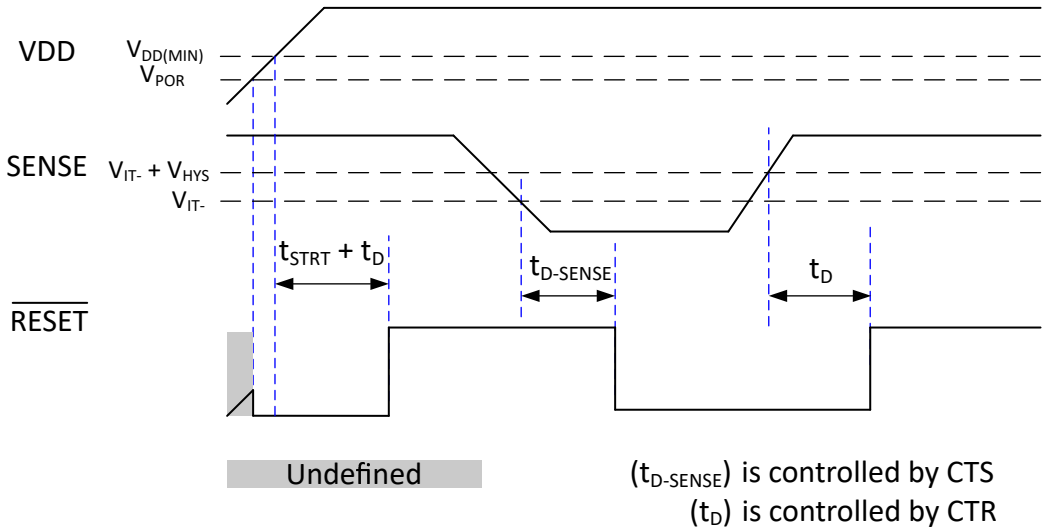
7.6 Timing Requirements

At 0.85 V ≤ V_{DD} ≤ 6 V, CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. V_{DD} ramp rate ≤ 1 V / µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup Delay(1)	CTR pin = Open or NC			300	µs
$t_{D-SENSE}$	Detect time delay V_{DD} = (V_{IT+} + 10%) to (V_{IT-} – 10%)(2)	CTS pin = Open or NC		30	50	µs
		CTS pin = 10 nF		6.2		ms
		CTS pin = 1 µF		619		ms
t_D	Reset time delay	CTR pin = Open or NC		40	80	µs
		CTR pin = 10 nF (3)		6.2		ms
		CTR pin = 1 µF (3)		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(4)		10		µs

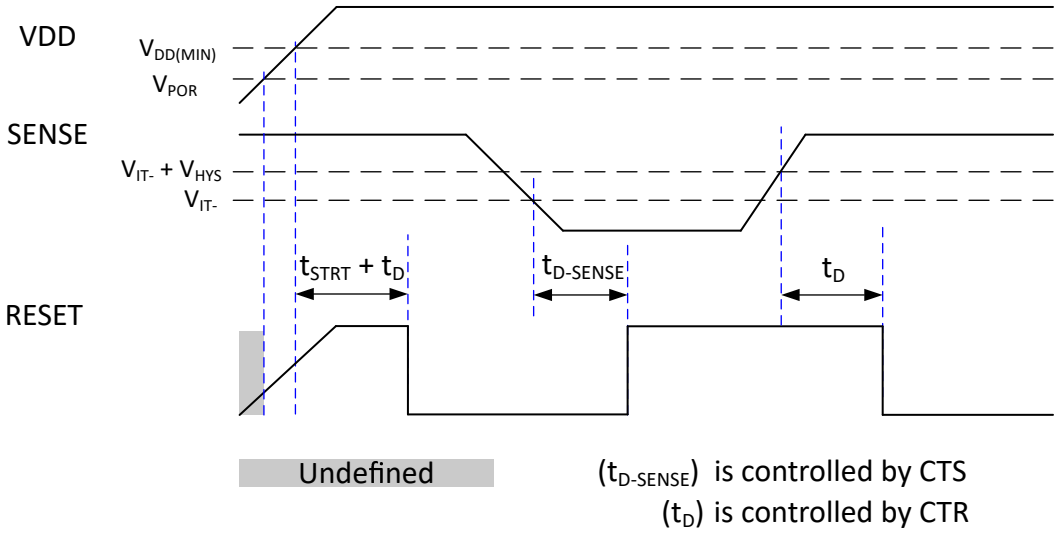
(1) When VDD starts from less than V_{POR} and then exceeds the specified minimum V_{DD}, reset is asserted till startup delay (t_{STRT}) + t_D delay based on capacitor on CTR pin. After this time, the device controls the RESET pin based on the SENSE pin voltage.
(2) t_{D_SENSE} measured from threhold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
(3) Ideal capacitor
(4) Overdrive % = [(V_{DD}/ V_{IT-}) - 1] × 100%

7.7 Timing Diagrams



(1) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to the CTR pin then t_D programmed time will be added to the startup time.

图 7-1. TPS3899DL01 and TPS3899PL01 Timing Diagram



(2) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to the CTR pin then t_D programmed time will be added to the startup time.

图 7-2. TPS3899PH01 Timing Diagram

7.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS3899 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull-up}$ = 100 kΩ, unless otherwise noted.

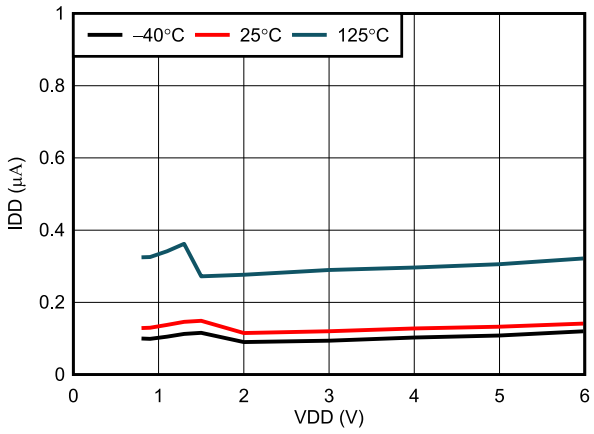


图 7-3. Supply Current vs Supply Voltage

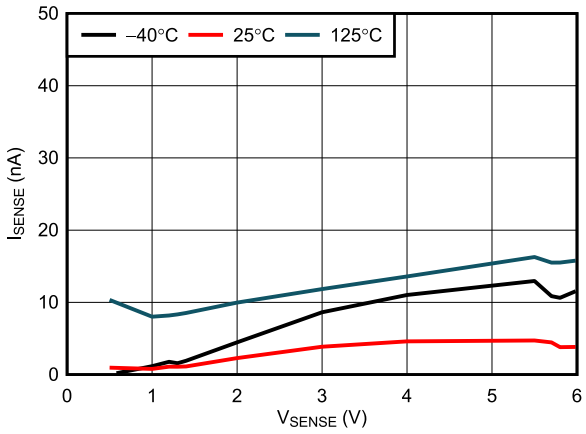


图 7-4. SENSE Current vs V_{SENSE}

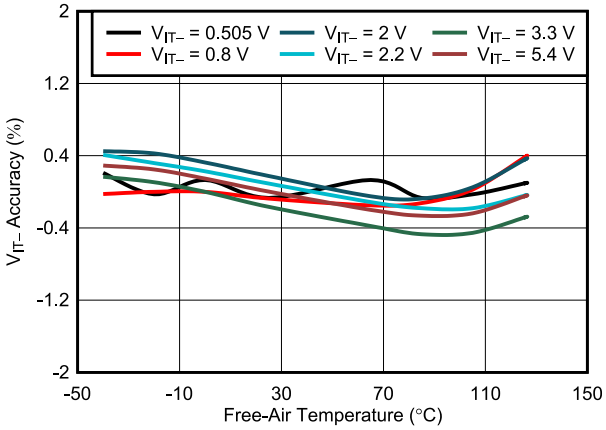


图 7-5. V_{IT-} Accuracy vs Temperature

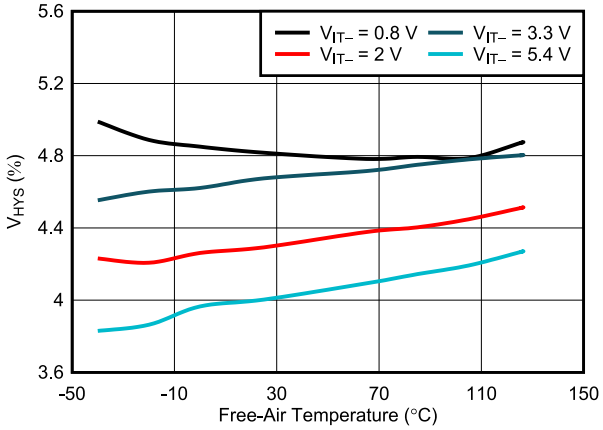


图 7-6. V_{HYS} vs Temperature

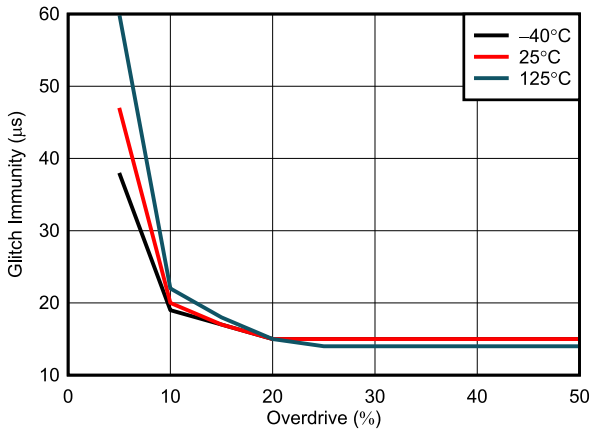


图 7-7. SENSE Glitch Immunity (V_{IT-}) vs Overdrive

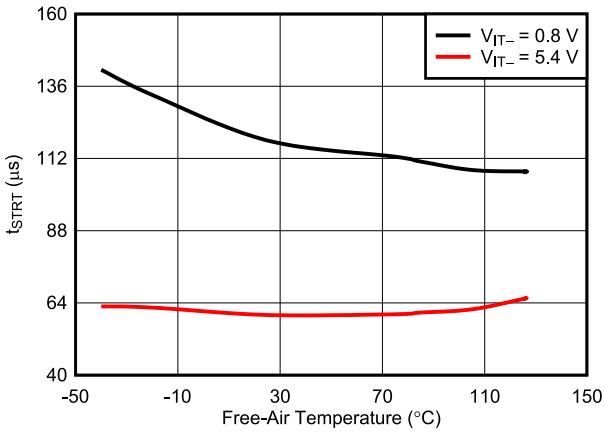
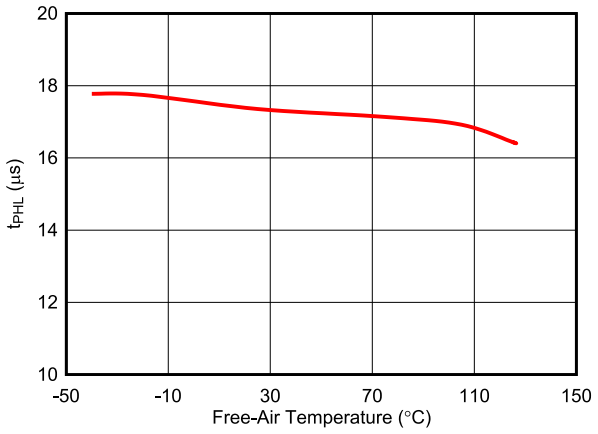


图 7-8. Startup Delay vs Temperature

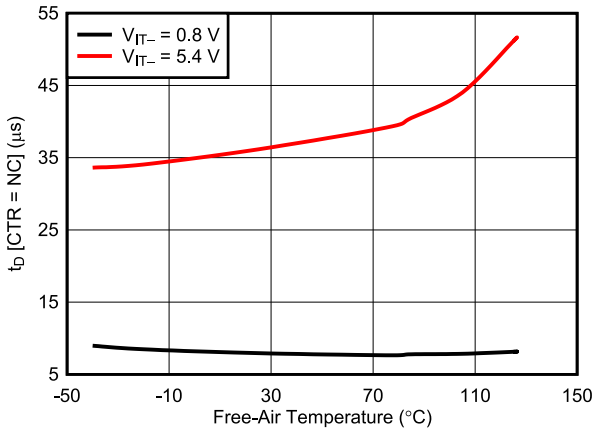
7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3899 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull-up}$ = 100 kΩ, unless otherwise noted.



V_{DD} falling below V_{IT-}

图 7-9. Propagation Delay vs Temperature



CTR = OPEN

图 7-10. Reset Time Delay vs Temperature

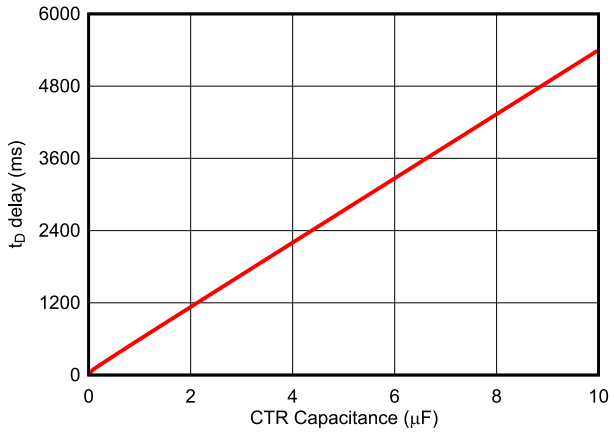
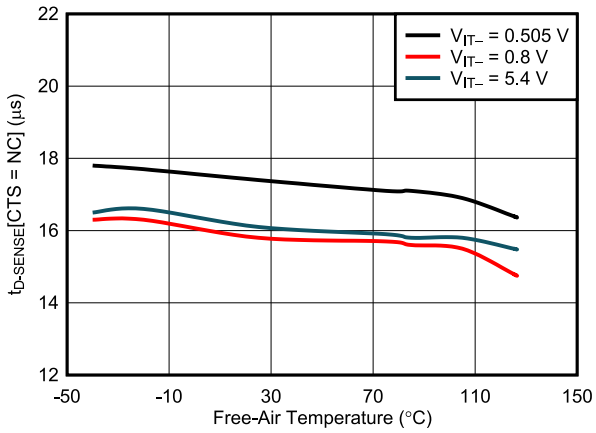


图 7-11. RESET Delay vs CTR Capacitance



CTS = OPEN

图 7-12. SENSE Delay vs Temperature

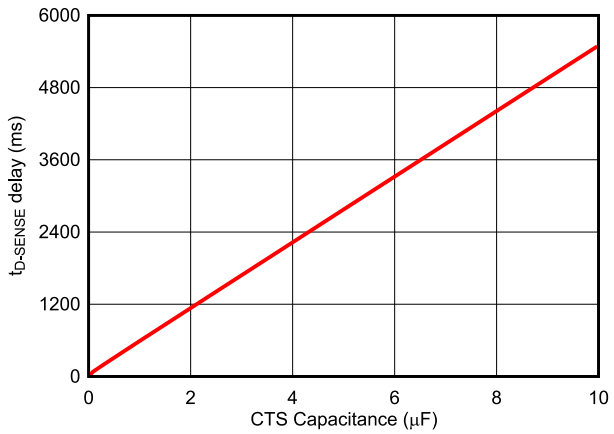


图 7-13. SENSE Delay vs CTS Capacitance

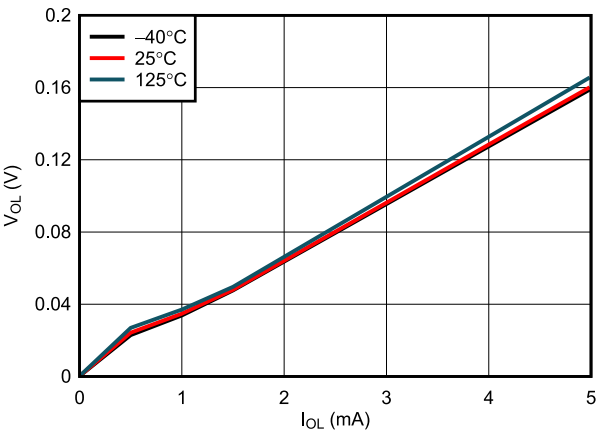


图 7-14. V_{OL} vs I_{OL}

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3899 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull-up}$ = 100 kΩ, unless otherwise noted.

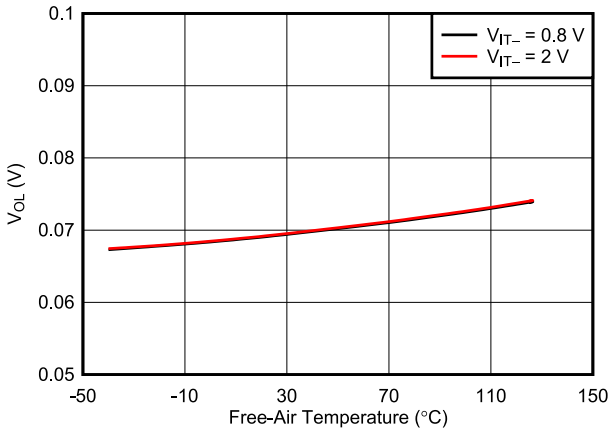


图 7-15. V_{OL} vs Temperature

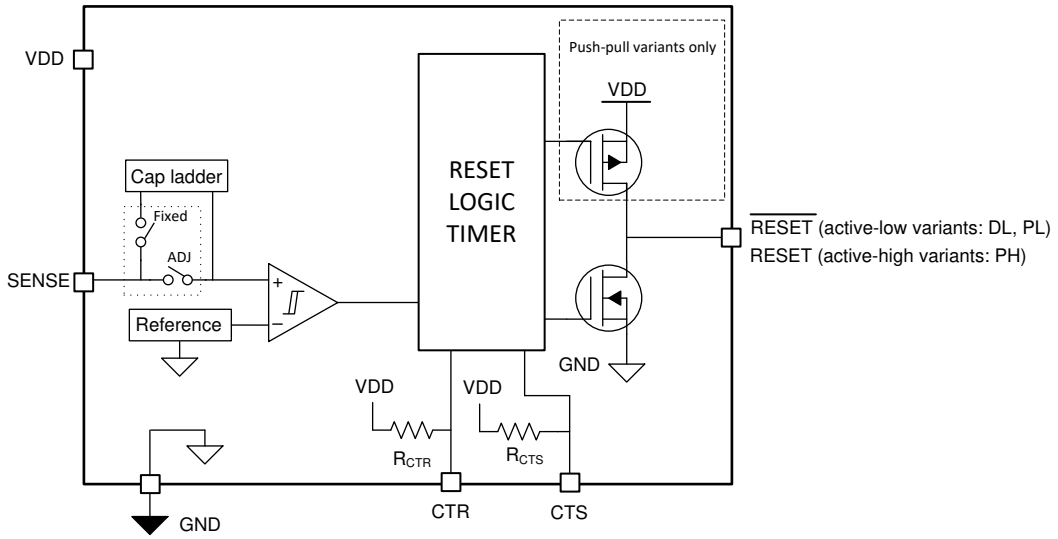
8 Detailed Description

8.1 Overview

The TPS3899 voltage supervisor with push-button monitor asserts a $\overline{\text{RESET}}$/RESET signal when the SENSE pin voltage drops below V_{IT-} for the duration of the sense delay set by CTS. If the SENSE pin voltage rises above V_{IT-} + V_{HYS} before the sense delay expires, the $\overline{\text{RESET}}$/RESET pin does not assert. When asserted, the $\overline{\text{RESET}}$/RESET output remains asserted until SENSE voltage returns above V_{IT-} + V_{HYS} for the duration of the reset delay set by CTR. If the SENSE pin voltage falls below V_{IT-} before the reset delay expires while $\overline{\text{RESET}}$ is asserted, $\overline{\text{RESET}}$/RESET will remain asserted.

Like most voltage supervisors, the TPS3899 includes a reset delay t_D to provide time for the power and clocks to settle before letting the processor out of reset. At power up, the circuits inside the TPS3899 need additional time to start the reset delay timer after its power supply VDD has reached minimum $V_{DD(MIN)}$ for these circuits to start operating properly. This additional time is specified with the parameter start-up delay t_{STRT}. 图 7-1 shows the timing diagram indicating this additional delay. After VDD is stable and above $V_{DD(MIN)}$ subsequent changes of the sense voltage across the threshold voltage will trigger reset after only the reset delay. The reset time delay t_D is set by a capacitor on the CTR pin. The start-up delay has a max spec limit of 300 μs for a ramp rate of $V_{DD} \leq 1$ V / μS.

8.2 Functional Block Diagram



8.3 Feature Description

The combination of user-adjustable sense delay time via CTS and reset delay time via CTR with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages V_{IT-} can be factory set from 0.8 V to 5.4 V in steps of 100 mV [1.1 V to 5.4 V for the -PH (push-pull active high) variants]. CTS and CTR pins allow the sense delay and reset delay to be set to typical values of 30 μs and 40 μs, respectively, by leaving these pins floating. External capacitors can be placed on the CTS and CTR pins to program the sense and reset delays independently.

8.3.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT-} the output reset is asserted. When the voltage at the VDD pin goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

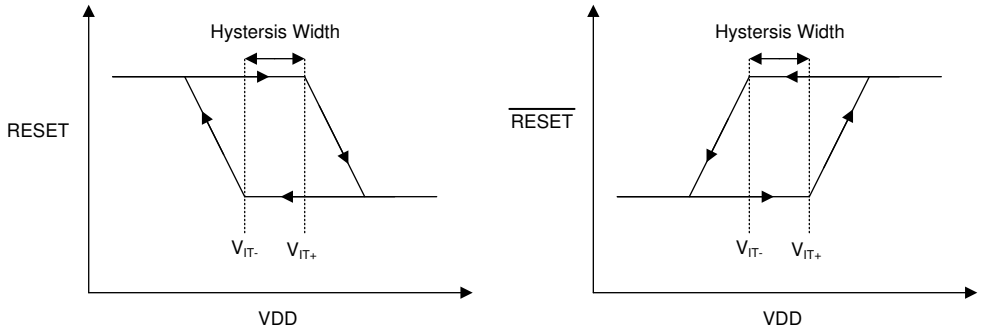


图 8-1. Hysteresis Diagram

8.3.2 User-Programmable Sense and Reset Time Delay

The sense delay corresponds to the configuration of CTS and the reset delay corresponds to the configuration of CTR. The sense and reset time delay can be set to a minimum value of 50 µs and 80 µs by leaving the CTS and CTR pins floating respectively, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor.

The relationship between external capacitor (C_{CT_EXT}) in Farads at CTS or CTR pins and the time delay in seconds is given by 方程式 1.

$$t_D = -\ln(0.29) \times R_{CT} \times C_{CT\_EXT} + t_{D\ (CTS\ or\ CTR\ =\ OPEN)} \quad (1)$$

方程式 1 is simplified to 方程式 2 and 方程式 3 by plugging R_{CT} and $t_{D\ (CTS\ or\ CTR\ =\ OPEN)}$ given in 节 7.5 and 节 7.6 section:

$$t_{D\text{-}SENSE} = 618937 \times C_{CTS\_EXT} + 50\ \mu s \quad (2)$$

$$t_D = 618937 \times C_{CTR\_EXT} + 80\ \mu s \quad (3)$$

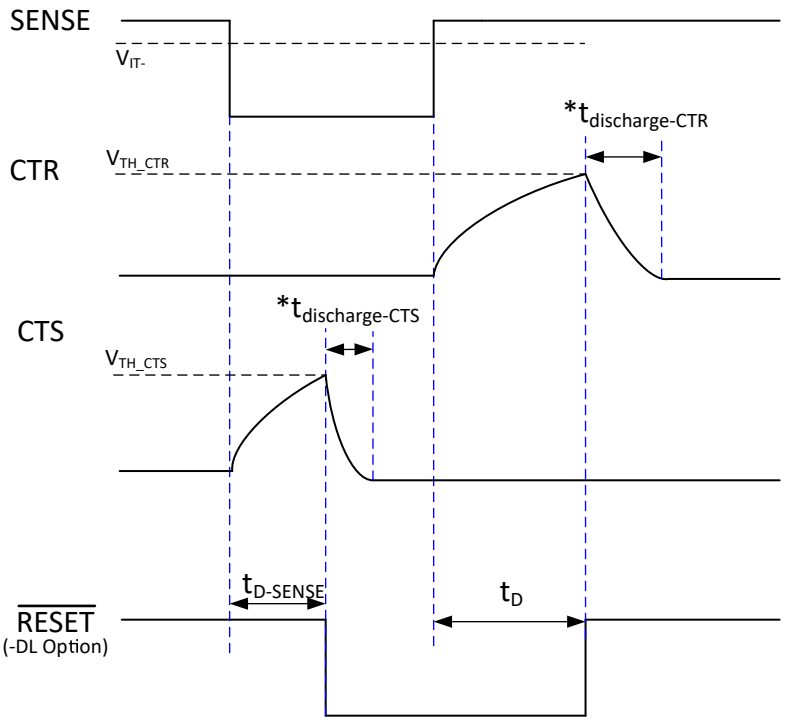
方程式 4 and 方程式 5 solves for both external capacitor values (C_{CTS_EXT}) and (C_{CTR_EXT}) in units of Farads where $t_{D\text{-}SENSE}$ and t_D are in units of seconds

$$C_{CTS\_EXT} = (t_{D\text{-}SENSE} - 50\ \mu s) \div 618937 \quad (4)$$

$$C_{CTR\_EXT} = (t_D - 80\ \mu s) \div 618937 \quad (5)$$

The recommended maximum sense and reset delay capacitors for the TPS3899 is limited to 10 µF as this ensures there is enough time for either capacitors to fully discharge when a voltage fault occurs. When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before either delay capacitors discharges completely, both delays will be shorter than expected. The capacitors will begin charging from a voltage above zero and resulting in shorter than expected time delays. Larger delay capacitors can be used so long as the capacitors have enough time to fully discharge during the duration of the voltage fault. To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

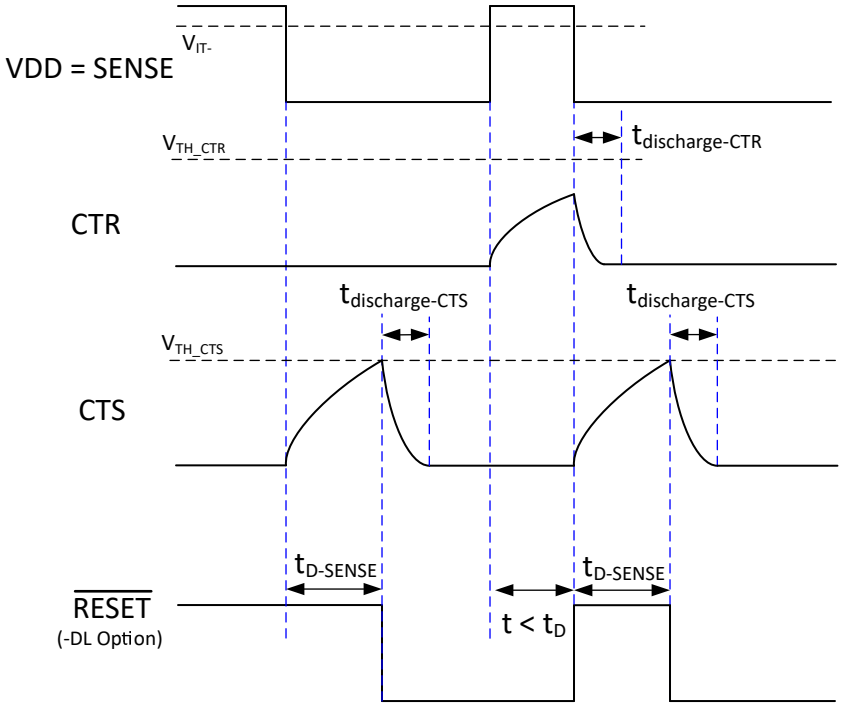
图 8-2 shows the charge and discharge behavior on CTS and CTR that defines the sense and reset delays respectively. When SENSE transitions below V_{IT-}, the capacitor connected to CTS begins to charge. Once the CTS capacitor charges to an internal threshold shown as V_{TH_CTS}, $\overline{RESET}$ transistions to active-low logic state and the CTS capacitor then begins to discharge immediately. When SENSE transistions above $V_{IT-} + V_{HYS}$, the capacitor connected to CTR begins to charge. Once the CTR capacitor charges to the internal threhold V_{TH_CTR}, $\overline{RESET}$ releases back to inactive logic high state and the CTR capacitor beginds to discharge immediately. Please note that for active-high variants, RESET follows the inverse behavior of $\overline{RESET}$.



* $t_{discharge-CTS}$ and $t_{discharge-CTR}$: To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

图 8-2. CTS and CTR Charge and Discharge Behavior Relative to SENSE and $\overline{RESET}$

图 8-3 shows the charge and discharge behavior on CTS and CTR where the monitored voltage is VDD. Similar to 图 8-2, 图 8-3 illustrates a SENSE signal that is transitioning below V_{IT-} before the CTR capacitor reaches to an internal threshold voltage V_{TH_CTR} and t < t_D. The result of the CTR capacitor not reaching the internal threshold voltage V_{TH_CTR} is $\overline{\text{RESET}}$ will become deasserted. Once $\overline{\text{RESET}}$ is deasserted, charging beings for the CTS capacitor. When the CTS voltage reaches the internal threshold V_{TH_CTS}, $\overline{\text{RESET}}$ will become asserted. This phenomenon is caused by the SENSE falling edge triggering the discharging of the CTR capacitor and producing a deassert signal on the $\overline{\text{RESET}}$ output.



* $t_{discharge-CTS}$ and $t_{discharge-CTR}$: To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

图 8-3. CTS and CTR Charge and Discharge Behavior Relative to VDD, SENSE and $\overline{\text{RESET}}$

8.3.3 $\overline{\text{RESET}}$/RESET Output

Upon power up, $\overline{\text{RESET}}$/RESET begins asserted and remains asserted until the SENSE pin voltage rises above the positive voltage threshold V_{IT-} + V_{HYS} for the duration of the reset delay set by CTR. After the SENSE pin voltage is above V_{IT-} + V_{HYS} for the reset delay, $\overline{\text{RESET}}$/RESET deasserts. $\overline{\text{RESET}}$/RESET remains deasserted long as the SENSE pin voltage is above the positive threshold. If the SENSE pin voltage falls below the negative threshold (V_{IT-}) for the duration of the sense delay set by CTS, then $\overline{\text{RESET}}$/RESET is asserted.

An external pull-up resistor is required for the open-drain variants. Connect the external pull-up resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. $\overline{\text{RESET}}$/RESET can be pulled up to any voltage up to 6.0 V, independent of the device supply voltage.

8.3.4 SENSE Input

The SENSE input can vary from 0 V to 6.0 V, regardless of the device supply voltage used. The SENSE pin is used to monitor a critical voltage rail or push-button input. If the voltage on this pin drops below V_{IT-}, then $\overline{\text{RESET}}$/RESET is asserted after the sense delay time set by CTS. When the voltage on the SENSE pin rises above the positive threshold voltage V_{IT-} + V_{HYS}, $\overline{\text{RESET}}$/RESET deasserts after the reset delay time set by CTR. The internal comparator has built-in hysteresis to ensure well-defined $\overline{\text{RESET}}$/RESET assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3899 device is relatively immune to short transients on the SENSE pin. Glitch immunity ($t_{GI\_V_{IT-}SENSE}$), found in 节 7.6, is dependent on threshold overdrive, as illustrated in 图 7-7. Although not required in most

cases, for noisy applications, good analog design practice is to place a 10-nF to 100-nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

8.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3899 is immune to short voltage transient spikes on the input pins. To further improve the noise immunity on the SENSE pin, placing a 10-nF to 100-nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.

Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 方程式 6.

$$\text{Overdrive} = | ((V_{SENSE} / V_{IT-}) - 1) \times 100\% | \quad (6)$$

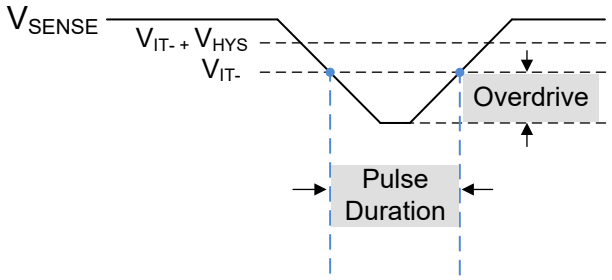


图 8-4. Overdrive vs Pulse Duration

8.4 Device Functional Modes

表 8-1 summarizes the various functional modes of the device.

表 8-1. Truth Table

V_{DD}	SENSE(1)	$\overline{RESET}$	RESET
$V_{DD} < V_{POR}$	—	Undefined	Undefined
$V_{POR} < V_{DD} < V_{DD(MIN)}$ (2)	—	L	H
$V_{DD} \geqslant V_{DD(MIN)}$	$V_{SENSE} < V_{IT-}$	L	H
$V_{DD} \geqslant V_{DD(MIN)}$	$V_{SENSE} > V_{IT-} + V_{HYS}$	H	L

(1) SENSE pin voltage must be less than V_{IT-} for the sense delay set by CTS or greater than $V_{IT-} + V_{HYS}$ for the reset delay set by CTR before RESET transistions

(2) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and $\overline{RESET}$ is held logic low (RESET is held logic high) until V_{DD} falls below V_{POR} at which the $\overline{RESET}$/RESET output is undefined.

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$/RESET pin is determined by the voltage on the SENSE pin and the sense delay and reset delay set by CTS and CTR respecively.

8.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage V_{POR}, the $\overline{RESET}$/RESET signal is asserted regardless of the voltage on the SENSE pin.

8.4.3 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than V_{POR}, the device does not have enough voltage to internally pull the asserted $\overline{RESET}$ output low and $\overline{RESET}$ is undefined. RESET is also undefined and may pull up to V_{DD} or to the pull-up voltage. Neither output should be relied upon for proper device function.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

Design 1: Adjustable Voltage Supervisor with Push-Button Functionality

A typical application for the TPS3899 is voltage rail monitoring with push-button functionality and specific timing requirements.

In this design application, the TPS3899DL01 is being used to monitor a 3.3 V power rail and will trigger a reset when the voltage drops below 2.9 V or when the push-button is pressed. The reset output connects to an MCU for system resetting or servicing the push-button.

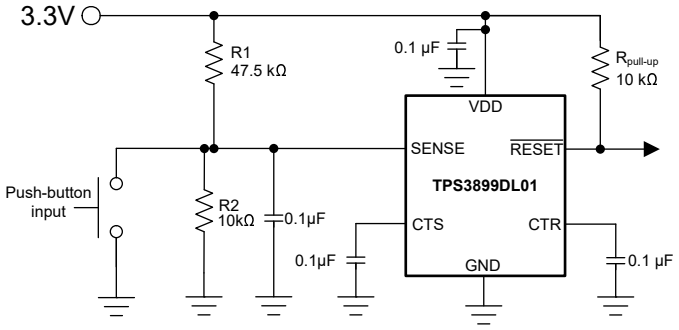


图 9-1. Design 1 - Adjustable Voltage Supervisor with Push-Button Functionality Circuit

9.2.1 Design Requirements

The design requirements, described in 表 9-1, for this design has a defined reset threshold voltage of 2.9 V, a sense delay of 60 ms, a reset delay of 60 ms, and an output current no larger than 500 µA.

表 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENTS	DESIGN RESULTS
Reset Asserting	Reset needs to assert when under the reset condition of a button press or VDD ⩽ 2.9 V.	Reset asserts when under the reset condition of a button press or VDD ⩽ 2.93 V.
Reset Asserting Timing	Reset output needs to assert when the reset conditions are met for 60 ms, and needs to de-assert after 60 ms of no reset conditions.	Reset output asserts when the reset conditions are met for 62 ms and will deassert after 62 ms of no reset conditions.
Output Current	The output current must not exceed 500 µA.	The output current is 300 µA under the reset condition.

9.2.2 Detailed Design Procedure

The TPS3899DL01 can monitor any voltage above 0.505 V using an external voltage divider. This device has a negative going input threshold voltage of 0.505 V; however, the design needs to assert a reset when VDD drops below 2.9 V. By using a resistor divider (R1 = 47.5 kΩ, R2 = 10 kΩ) the negative going threshold voltage becomes 2.93 V. The device's positive going voltage threshold is V_{IT-} + V_{HYS}. The typical V_{HYS} is 25.5 mV. This in combination with the resistor divider makes the design's positive going threshold voltage equal to 3.08 V. If VDD falls below 2.93 V for the duration of sense delay ($t_{D-SENSE}$), the reset will assert. If VDD rises above 3.08 V for the duration of reset delay (t_D), the reset will deassert. See 图 9-2 for a timing diagram detailing the voltage levels and reset assertion/deassertion conditions.

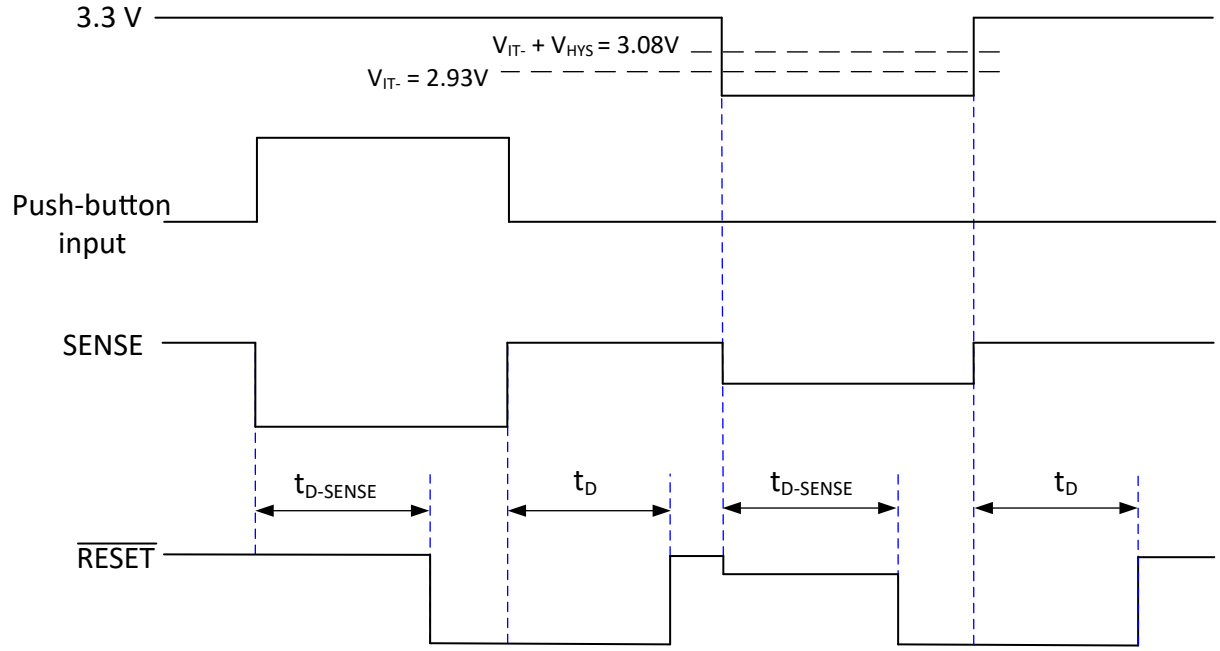


图 9-2. Design 1 Timing Diagram

This design will also enter a reset condition when the push-button (PB) is asserted. The push-button is tied to ground and when pressed will drop the SENSE voltage to 0 V, making the device assert a reset. As a good analog practice, a 0.1 µF capacitor was also placed on VDD.

The desired reset timing conditions are sense delay time of 60 ms (how long it takes to trigger a reset) and a reset delay time of 60 ms (how long it takes to recover from a reset). Using 方程式 4 and 方程式 5, respectively, to solve for CTS and CTR capacitor values, CTS = 0.1 µF and CTR = 0.1 µF. These capacitor values give a nominal sense delay time of 62 ms and nominal reset delay time of 62 ms. 图 9-3 and 图 9-4 are the results of the described application where the measured sense and reset delay time are shown respectively.

For the requirement of a maximum output current, an external pull-up resistor needs to be selected so that the current through the external pull-up resistor exceeds no more than 500 µA. When the reset output is low, the voltage drop across the external pull-up resistor is equal to VDD. Ohm’s law is used to calculate the minimum resistor value. The resistor needs to be greater than 6 kΩ in order to pull less than 500 µA in the reset asserted low condition. A resistor value of 10 kΩ was selected to accomplish this.

Note that this design does not account for tolerances.

9.2.3 Application Curves

图 9-3. Sense Delay

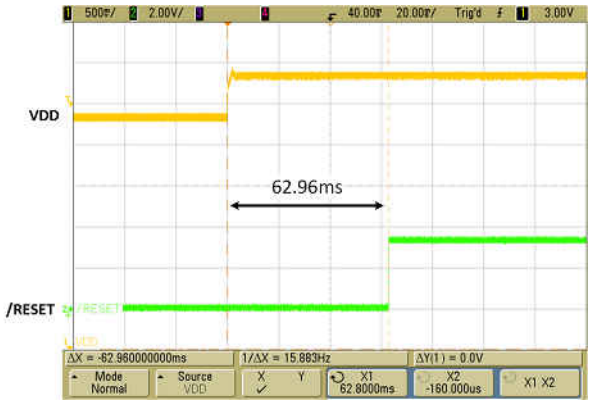


图 9-4. Reset Delay

10 Power Supply Recommendations

The TPS3899 is designed to operate from an input supply with a voltage range between 0.85 V and 6 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin. Also, placing a 10-nF to 100-nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal. This device has a 6.5 V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6.5 V, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor near the VDD pin. If a capacitor is not connected to the CTS or CTS pins, then minimize parasitic capacitance on this pin so the sense delay or reset delay times are not adversely affected. For fixed voltage threshold devices, good analog design practice is to place a 0.1-µF ceramic capacitor near the SENSE pin.

11.2 Layout Example

The layout example in 图 11-1 shows how the TPS3899 is laid out on a printed circuit board (PCB) with a user-defined sense delay and reset delay.

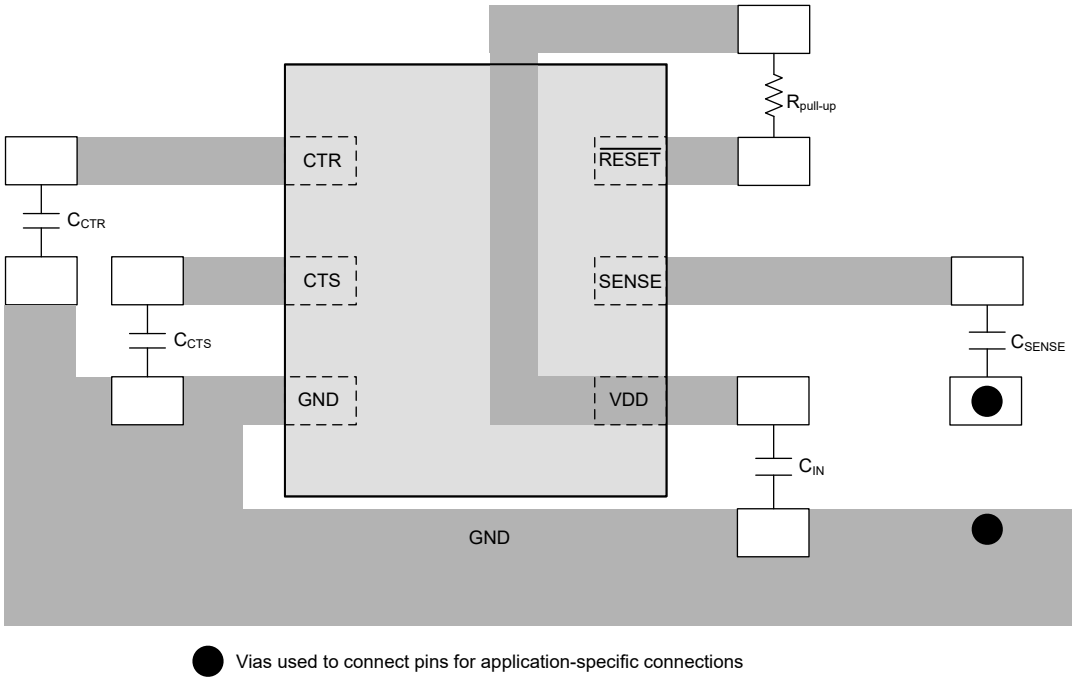


图 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

图 5-1 in Device Comparison shows how to decode the function of the device based on its part number shown in 表 12-1.

表 12-1. Device Naming Convention

ORDERABLE DEVICE NAME			THRESHOLD VOLTAGE (V)
-DL (OPEN-DRAIN ACTIVE-LOW)	-PL (PUSH-PULL ACTIVE-LOW)	-PH (PUSH-PULL ACTIVE-HIGH)	
TPS3899DL01DSE	TPS3899PL01DSE	TPS3899PH01DSE	0.505
TPS3899DL08DSE	TPS3899PL08DSE	N/A	0.80
TPS3899DL09DSE	TPS3899PL09DSE	N/A	0.90
TPS3899DL10DSE	TPS3899PL10DSE	N/A	1.00
TPS3899DL11DSE	TPS3899PL11DSE	TPS3899PH11DSE	1.10
TPS3899DL12DSE	TPS3899PL12DSE	TPS3899PH12DSE	1.20
TPS3899DL13DSE	TPS3899PL13DSE	TPS3899PH13DSE	1.30
TPS3899DL14DSE	TPS3899PL14DSE	TPS3899PH14DSE	1.40
TPS3899DL15DSE	TPS3899PL15DSE	TPS3899PH15DSE	1.50
TPS3899DL16DSE	TPS3899PL16DSE	TPS3899PH16DSE	1.60
TPS3899DL17DSE	TPS3899PL17DSE	TPS3899PH17DSE	1.70
TPS3899DL18DSE	TPS3899PL18DSE	TPS3899PH18DSE	1.80
TPS3899DL19DSE	TPS3899PL19DSE	TPS3899PH19DSE	1.90
TPS3899DL20DSE	TPS3899PL20DSE	TPS3899PH20DSE	2.00
TPS3899DL21DSE	TPS3899PL21DSE	TPS3899PH21DSE	2.10
TPS3899DL22DSE	TPS3899PL22DSE	TPS3899PH22DSE	2.20
TPS3899DL23DSE	TPS3899PL23DSE	TPS3899PH23DSE	2.30
TPS3899DL24DSE	TPS3899PL24DSE	TPS3899PH24DSE	2.40
TPS3899DL25DSE	TPS3899PL25DSE	TPS3899PH25DSE	2.50
TPS3899DL26DSE	TPS3899PL26DSE	TPS3899PH26DSE	2.60
TPS3899DL27DSE	TPS3899PL27DSE	TPS3899PH27DSE	2.70
TPS3899DL28DSE	TPS3899PL28DSE	TPS3899PH28DSE	2.80
TPS3899DL29DSE	TPS3899PL29DSE	TPS3899PH29DSE	2.90
TPS3899DL30DSE	TPS3899PL30DSE	TPS3899PH30DSE	3.00
TPS3899DL31DSE	TPS3899PL31DSE	TPS3899PH31DSE	3.10
TPS3899DL32DSE	TPS3899PL32DSE	TPS3899PH32DSE	3.20
TPS3899DL33DSE	TPS3899PL33DSE	TPS3899PH33DSE	3.30
TPS3899DL34DSE	TPS3899PL34DSE	TPS3899PH34DSE	3.40
TPS3899DL35DSE	TPS3899PL35DSE	TPS3899PH35DSE	3.50
TPS3899DL36DSE	TPS3899PL36DSE	TPS3899PH36DSE	3.60
TPS3899DL37DSE	TPS3899PL37DSE	TPS3899PH37DSE	3.70
TPS3899DL38DSE	TPS3899PL38DSE	TPS3899PH38DSE	3.80

表 12-1. Device Naming Convention (continued)

ORDERABLE DEVICE NAME			THRESHOLD VOLTAGE (V)
-DL (OPEN-DRAIN ACTIVE-LOW)	-PL (PUSH-PULL ACTIVE-LOW)	-PH (PUSH-PULL ACTIVE-HIGH)	
TPS3899DL39DSE	TPS3899PL39DSE	TPS3899PH39DSE	3.90
TPS3899DL40DSE	TPS3899PL40DSE	TPS3899PH40DSE	4.00
TPS3899DL41DSE	TPS3899PL41DSE	TPS3899PH41DSE	4.10
TPS3899DL42DSE	TPS3899PL42DSE	TPS3899PH42DSE	4.20
TPS3899DL43DSE	TPS3899PL43DSE	TPS3899PH43DSE	4.30
TPS3899DL44DSE	TPS3899PL44DSE	TPS3899PH44DSE	4.40
TPS3899DL45DSE	TPS3899PL45DSE	TPS3899PH45DSE	4.50
TPS3899DL46DSE	TPS3899PL46DSE	TPS3899PH46DSE	4.60
TPS3899DL47DSE	TPS3899PL47DSE	TPS3899PH47DSE	4.70
TPS3899DL48DSE	TPS3899PL48DSE	TPS3899PH48DSE	4.80
TPS3899DL49DSE	TPS3899PL49DSE	TPS3899PH49DSE	4.90
TPS3899DL50DSE	TPS3899PL50DSE	TPS3899PH50DSE	5.00
TPS3899DL51DSE	TPS3899PL51DSE	TPS3899PH51DSE	5.10
TPS3899DL52DSE	TPS3899PL52DSE	TPS3899PH52DSE	5.20
TPS3899DL53DSE	TPS3899PL53DSE	TPS3899PH53DSE	5.30
TPS3899DL54DSE	TPS3899PL54DSE	TPS3899PH54DSE	5.40

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3899DL01DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KH	Samples
TPS3899DL08DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LJ	Samples
TPS3899DL09DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M3	Samples
TPS3899DL10DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LS	Samples
TPS3899DL11DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LZ	Samples
TPS3899DL13DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LX	Samples
TPS3899DL14DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LN	Samples
TPS3899DL15DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LL	Samples
TPS3899DL20DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M1	Samples
TPS3899DL22DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP	Samples
TPS3899DL26DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV	Samples
TPS3899DL28DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LI	Samples
TPS3899DL29DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LK	Samples
TPS3899DL30DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM	Samples
TPS3899DL31DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M6	Samples
TPS3899DL35DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LT	Samples
TPS3899DL41DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LU	Samples
TPS3899DL43DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M2	Samples
TPS3899PL31DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LH	Samples
TPS3899PL42DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3899 :

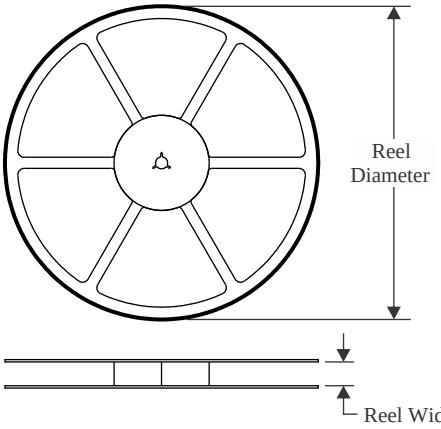
- Automotive : TPS3899-Q1

NOTE: Qualified Version Definitions:

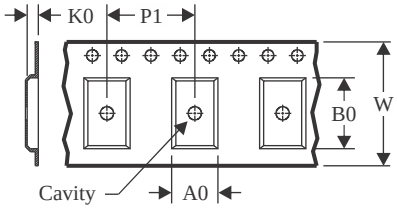
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

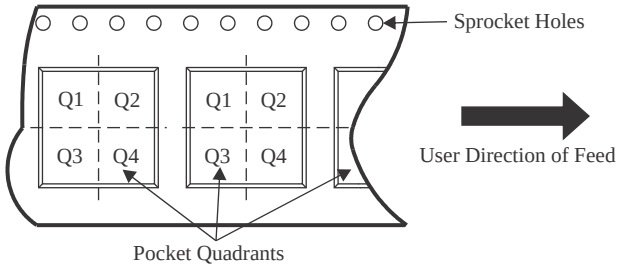


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

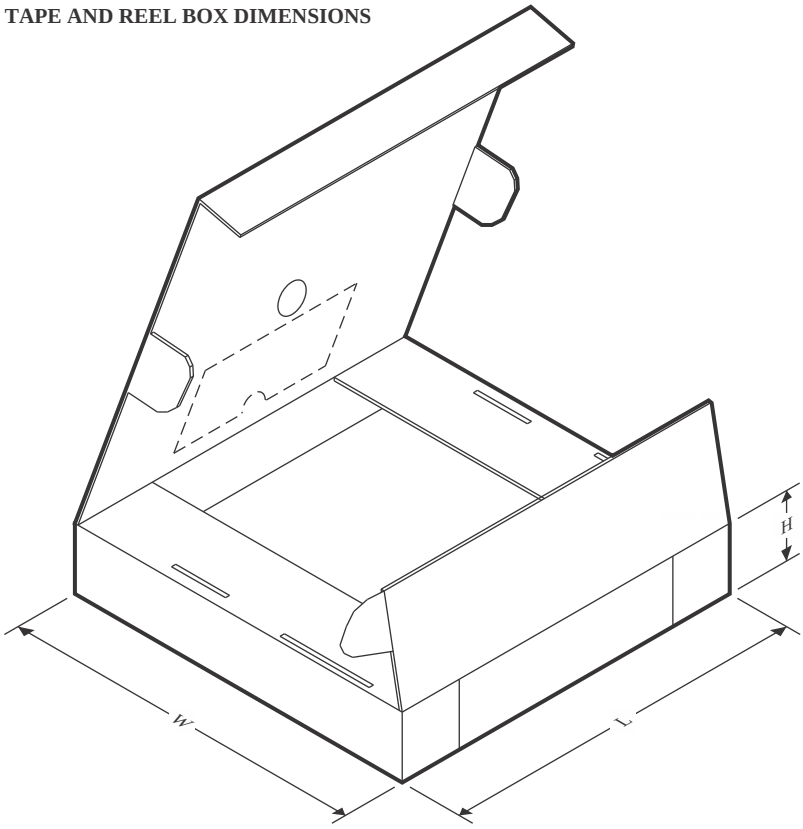


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3899DL01DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3899DL01DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL08DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL09DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL10DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL11DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL13DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL14DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL15DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL20DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL22DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL26DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL28DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL29DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL30DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL31DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3899DL35DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL41DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL43DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899PL31DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899PL42DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

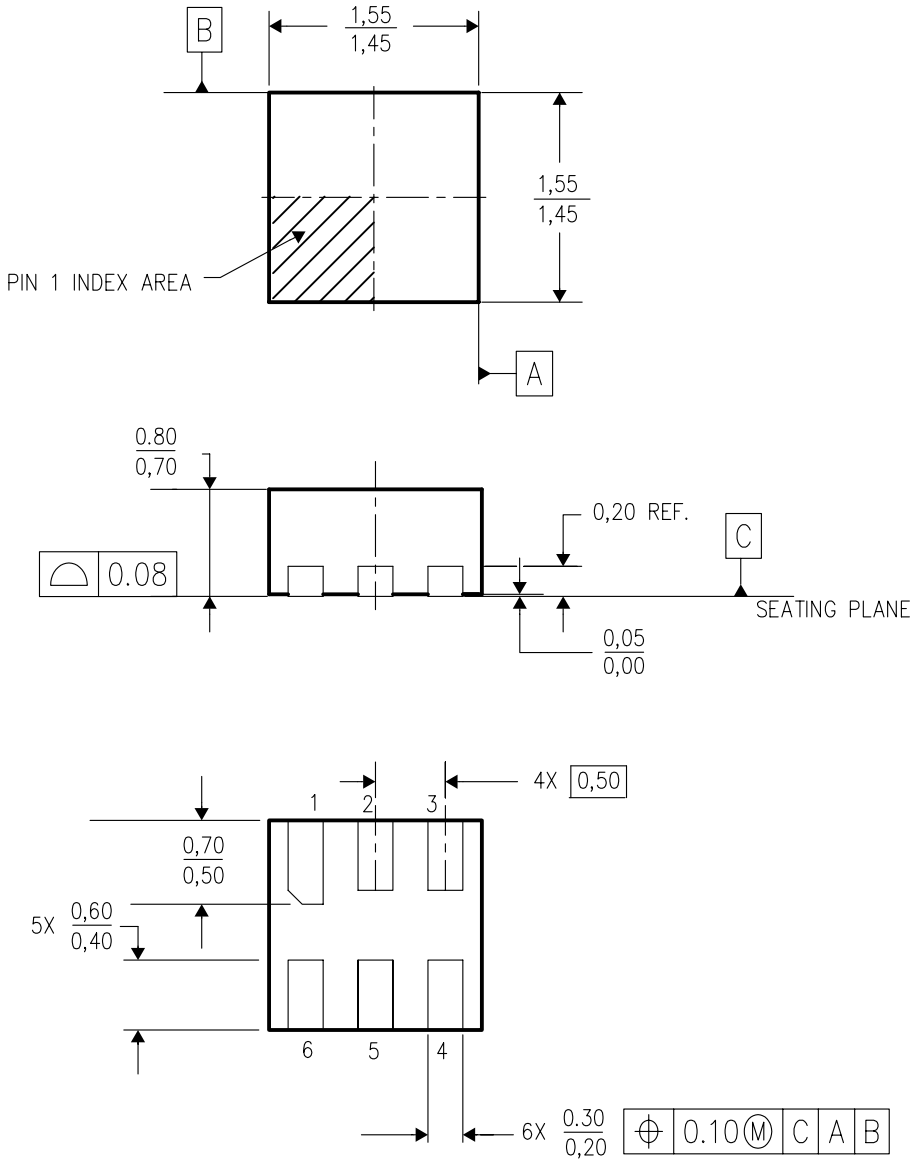


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3899DL01DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3899DL01DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL08DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL09DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL10DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL11DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL13DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL14DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL15DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL20DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL22DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL26DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL28DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL29DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL30DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL31DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL35DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL41DSER	WSON	DSE	6	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3899DL43DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899PL31DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899PL42DSER	WSON	DSE	6	3000	210.0	185.0	35.0

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

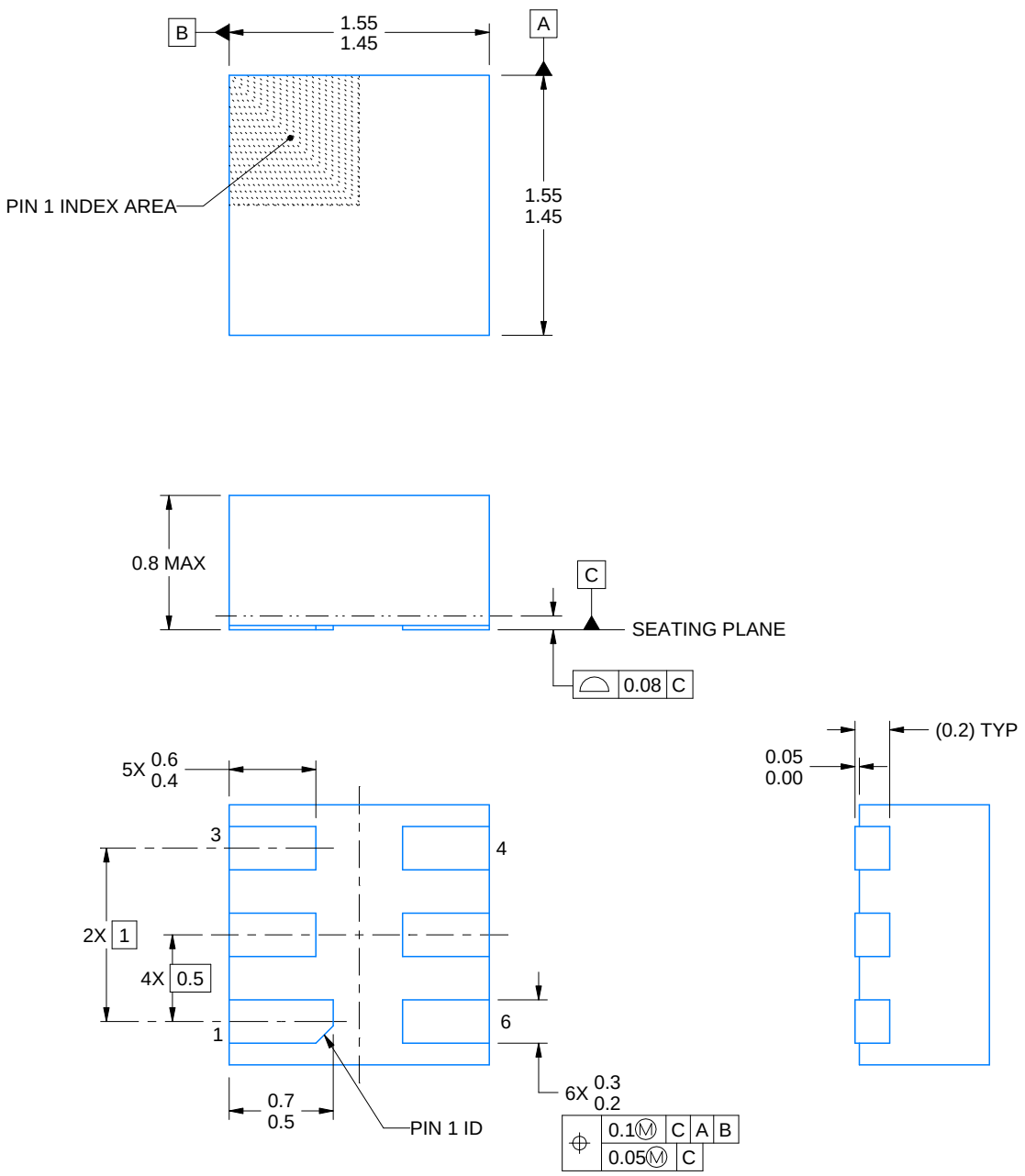
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

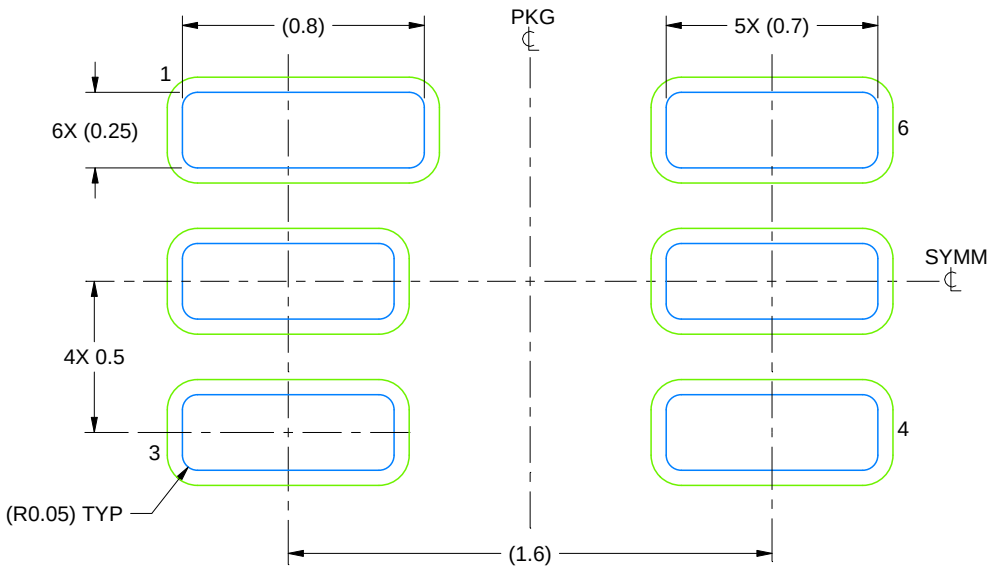
PLASTIC SMALL OUTLINE - NO LEAD



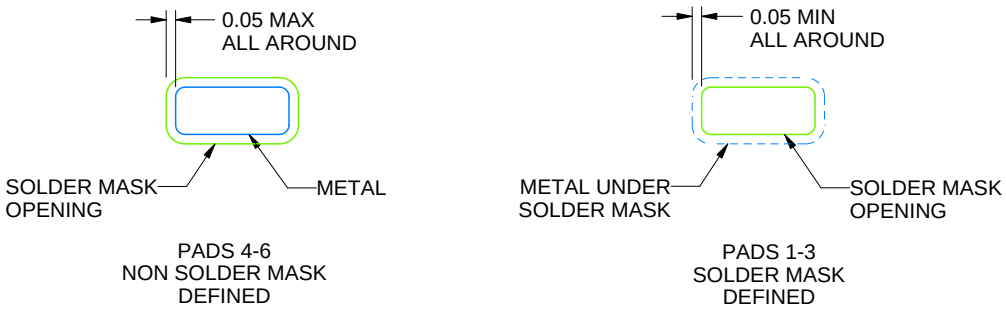
4220552/A 04/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

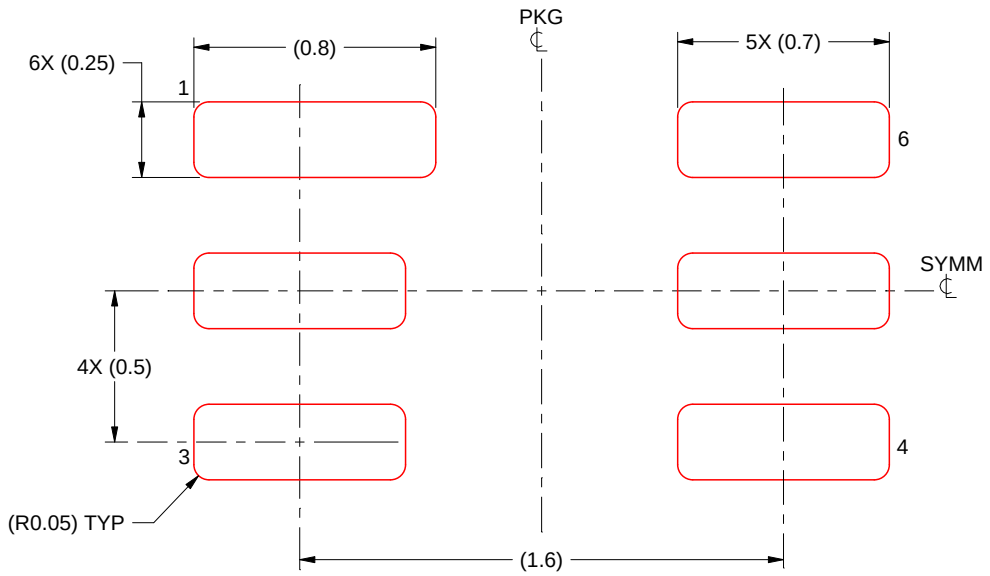


SOLDER MASK DETAILS

4220552/A 04/2021

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265