

## OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Check for Samples: [SN54AHCT541](#), [SN74AHCT541](#)

### FEATURES

- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

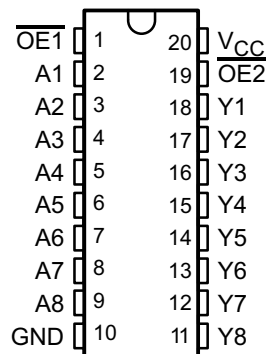
### DESCRIPTION

The 'AHCT541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

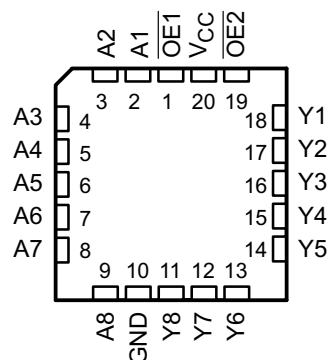
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHCT541 . . . J or W PACKAGE  
SN74AHCT541 . . . DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT541 . . . FK PACKAGE  
(TOP VIEW)



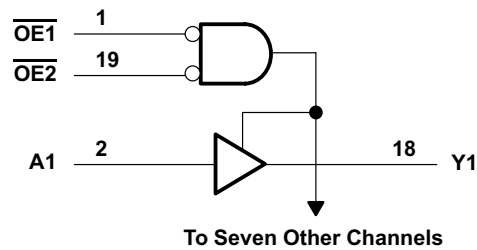
**FUNCTION TABLE  
(EACH FLIP-FLOP)**

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)**



**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	VALUE	UNIT
Supply voltage range, $V_{CC}$	-0.5 to 7	V
Input voltage range, $V_I$ <sup>(2)</sup>	-0.5 to 7	V
Output voltage range, $V_O$ <sup>(2)</sup>	-0.5 to $V_{CC} + 0.5$	V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 20$	mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$	mA
Continuous current through $V_{CC}$ or GND	$\pm 75$	mA
Package thermal impedance, $\theta_{JA}$ <sup>(3)</sup>	DB package	70
	DGV package	92
	DW package	58
	N package	69
	NS package	60
	PW package	83
Storage temperature range, $T_{stg}$	-65 to 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		SN54AHCT541		SN74AHCT541		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level Input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8		-8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
Δt/Δv	Input Transition rise or fall rate		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

**ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
			MIN	TYP	MAX	SN54AHCT541		SN74AHCT541		SN74AHCT541		
						MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4		4.4	V	
	I <sub>OH</sub> = -8 mA		3.94			3.8		3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1			0.1		0.1	V	
	I <sub>OH</sub> = 8 mA				0.36		0.44		0.44			0.44
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 <sup>(1)</sup>		±1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		20		40	μA
ΔI <sub>CC</sub> <sup>(2)</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			2				10			pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5V			4							

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
						Recommended						
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$	4.1 <sup>(1)</sup>	6.0 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	ns
$t_{PHL}$				4.1 <sup>(1)</sup>	6.0 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5.0 <sup>(1)</sup>	7.0 <sup>(1)</sup>	1 <sup>(1)</sup>	8.0 <sup>(1)</sup>	1	8.0	1	8.0	ns
$t_{PZL}$				5.0 <sup>(1)</sup>	7.0 <sup>(1)</sup>	1 <sup>(1)</sup>	8.0 <sup>(1)</sup>	1	8.0	1	8.0	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	4.5 <sup>(1)</sup>	7.0 <sup>(1)</sup>	1 <sup>(1)</sup>	8.0 <sup>(1)</sup>	1	8.0	1	8.0	ns
$t_{PLZ}$				4.5 <sup>(1)</sup>	7.0 <sup>(1)</sup>	1 <sup>(1)</sup>	8.0 <sup>(1)</sup>	1	8.0	1	8.0	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	6.2	8.5	1	9.5	1	9.5	1	9.5	ns
$t_{PHL}$				6.2	8.5	1	9.5	1	9.5	1	9.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	7.5	10.0	1	12	1	12	1	12	ns
$t_{PZL}$				7.5	10.0	1	12	1	12	1	12	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	7.0	10.0	1	12	1	12	1	12	ns
$t_{PLZ}$				7.0	10.0	1	12	1	12	1	12	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1 <sup>(2)</sup>				1	1		

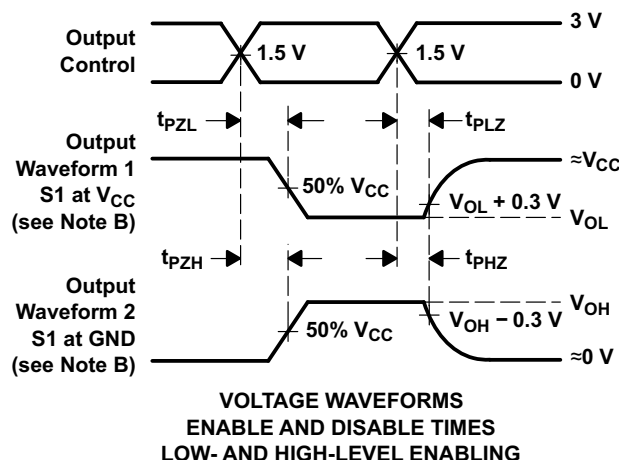
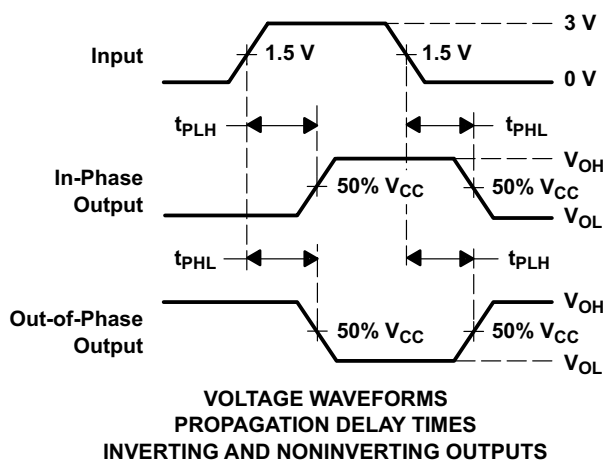
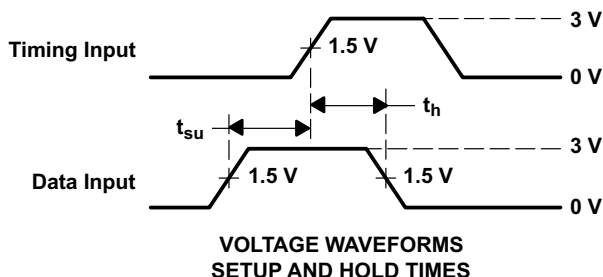
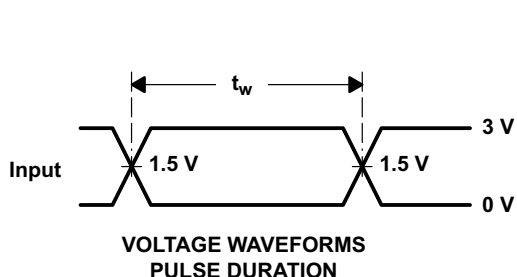
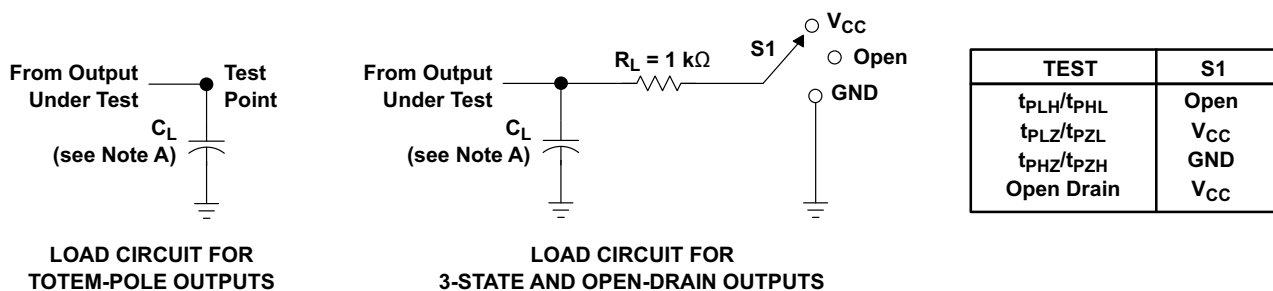
- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.  
 (2) On products compliant to MIL-PRF-38535, this parameter does not apply

## OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF

PARAMETER MEASUREMENT INFORMATION



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## REVISION HISTORY

Changes from Revision O (July 2003) to Revision P	Page
• Changed document format from Quicksilver to DocZone. ....	1
• Extended operating temperature range to 125°C .....	3

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685801Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801Q2A SNJ54AHCT 541FK	<a href="#">Samples</a>
5962-9685801QRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801QR A SNJ54AHCT541J	<a href="#">Samples</a>
5962-9685801QSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801QS A SNJ54AHCT541W	<a href="#">Samples</a>
SN74AHCT541DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	<a href="#">Samples</a>
SN74AHCT541DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	<a href="#">Samples</a>
SN74AHCT541N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT541N	<a href="#">Samples</a>
SN74AHCT541NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	<a href="#">Samples</a>
SN74AHCT541PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541PWE4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541PWRG3	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SNJ54AHCT541FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801Q2A SNJ54AHCT 541FK	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHCT541J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801QR A SNJ54AHCT541J	<a href="#">Samples</a>
SNJ54AHCT541W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801QS A SNJ54AHCT541W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AHCT541, SN74AHCT541 :**

- Catalog : [SN74AHCT541](#)
- Enhanced Product : [SN74AHCT541-EP](#), [SN74AHCT541-EP](#)
- Military : [SN54AHCT541](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

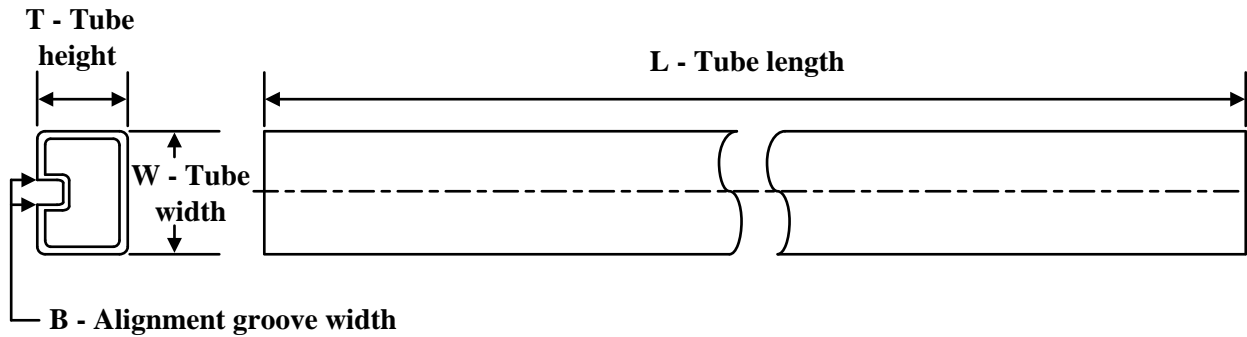

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT541DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT541NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHCT541PWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHCT541PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

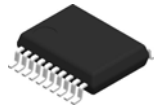
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT541DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHCT541DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT541NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHCT541PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHCT541PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74AHCT541PWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74AHCT541PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9685801Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9685801QSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74AHCT541DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AHCT541N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHCT541PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74AHCT541PWE4	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74AHCT541PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54AHCT541FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54AHCT541W	W	CFP	20	1	506.98	26.16	6220	NA

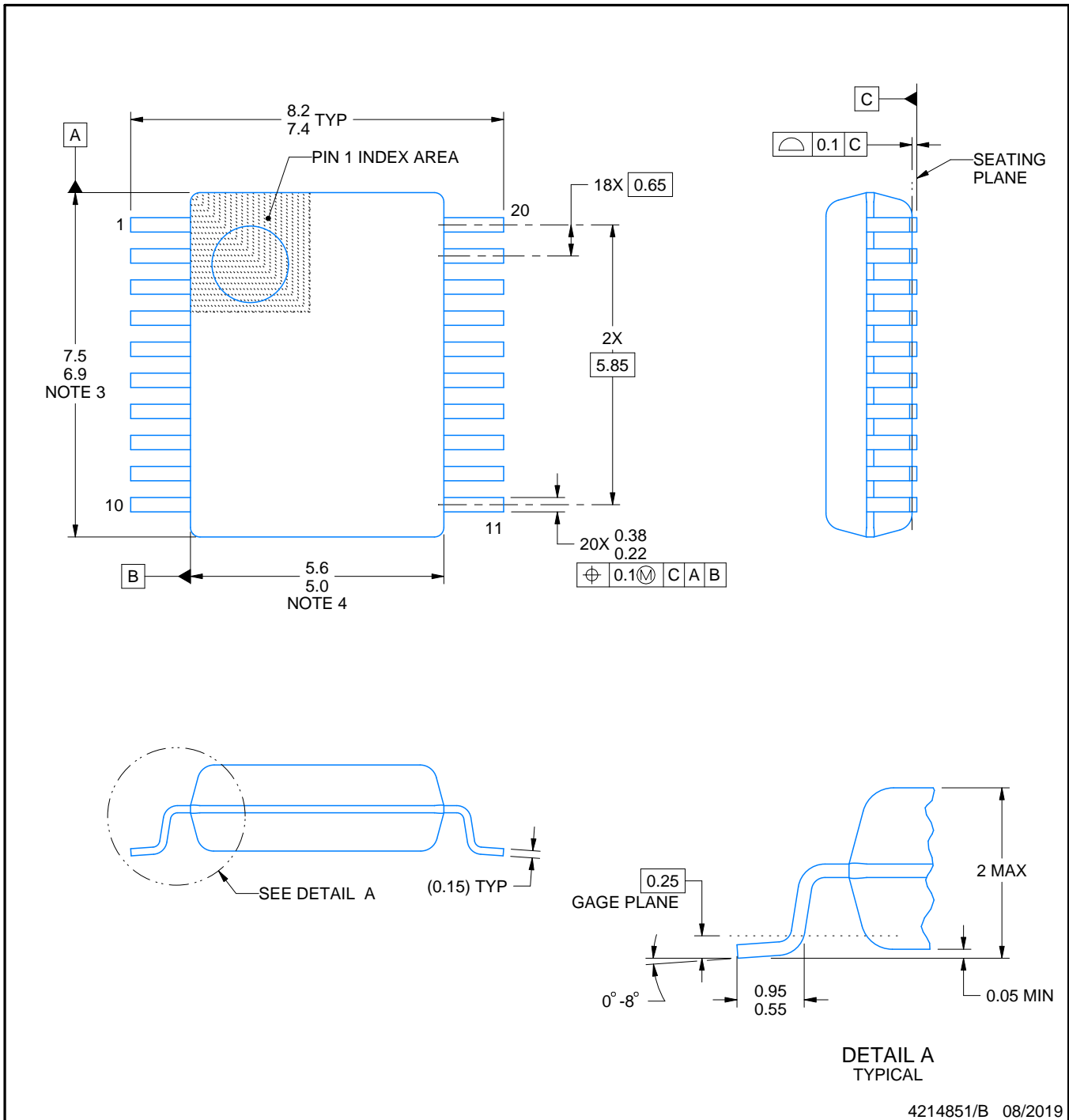
# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



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### NOTES:

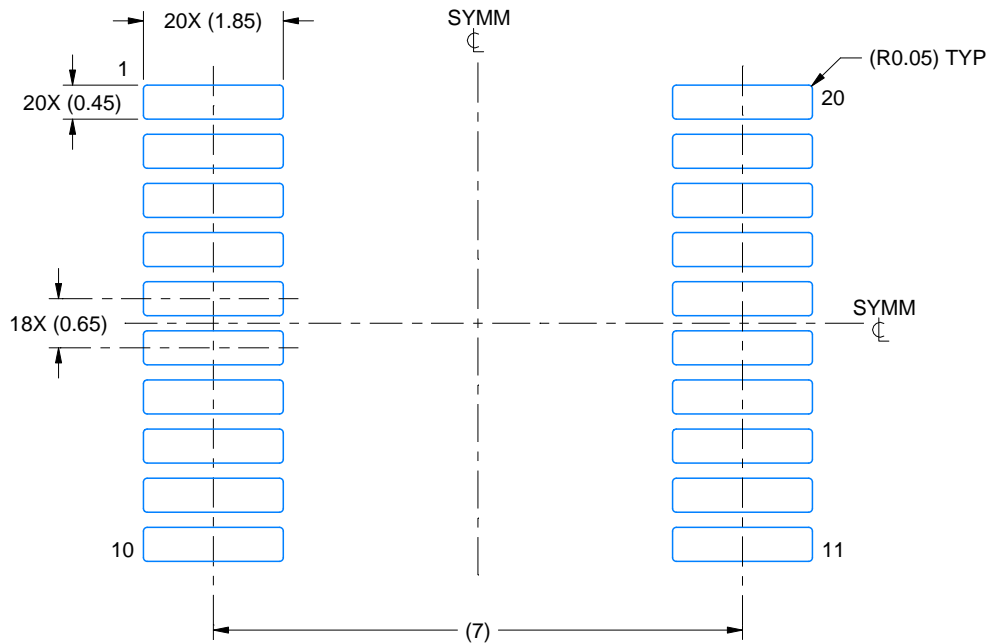
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

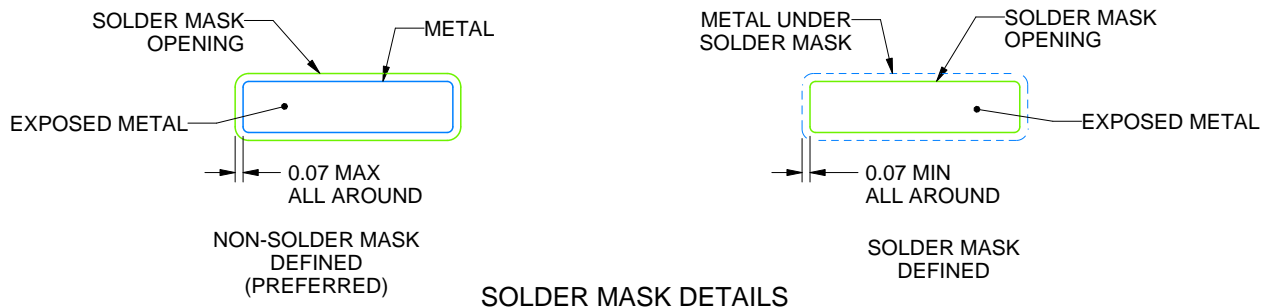
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

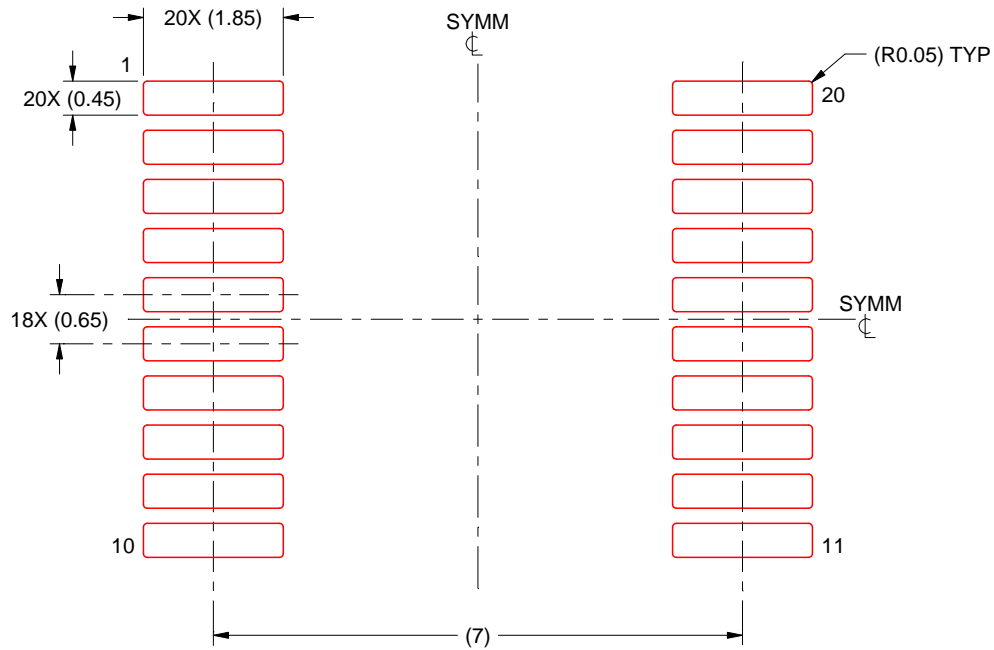
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



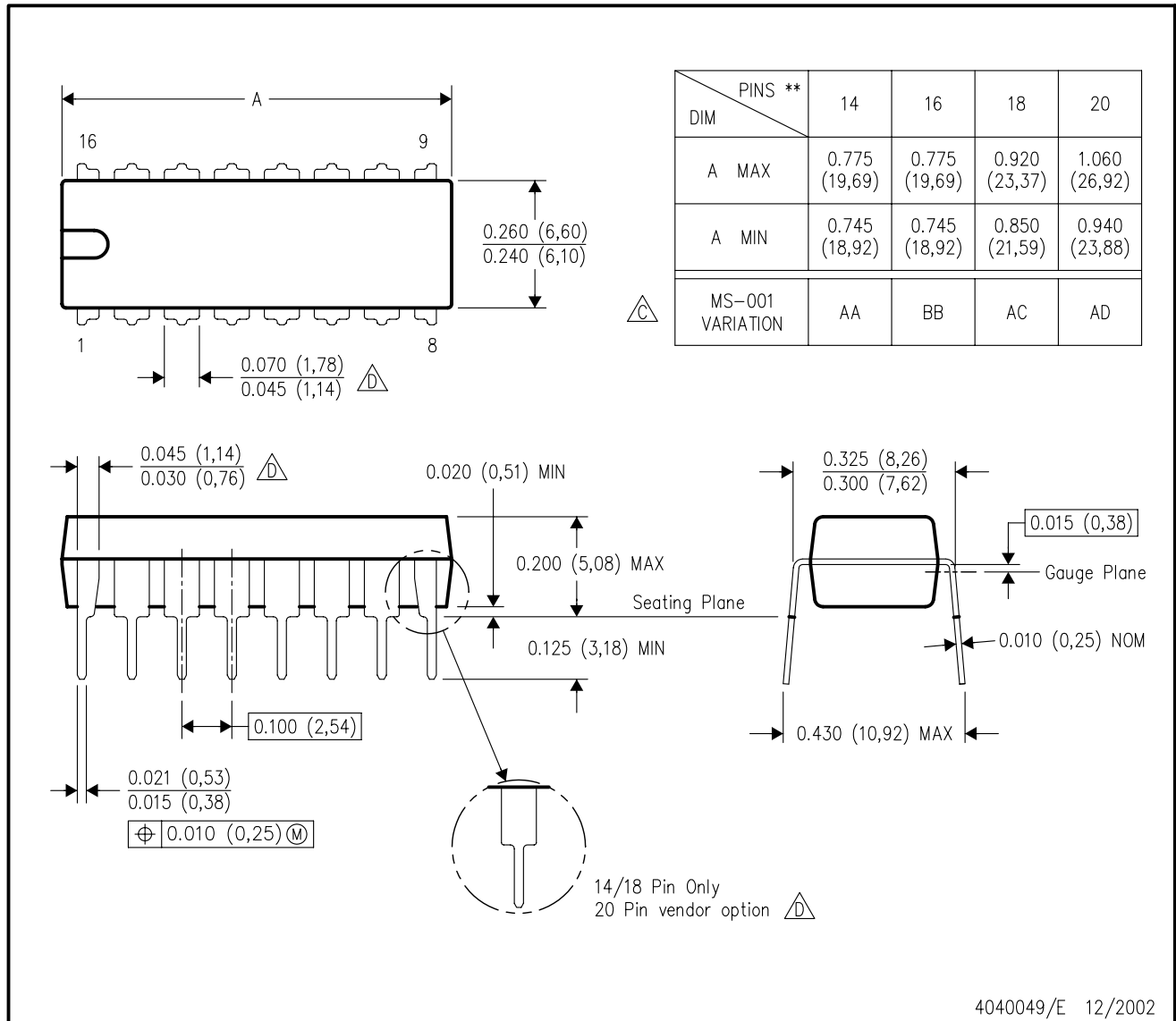
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

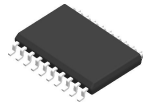
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

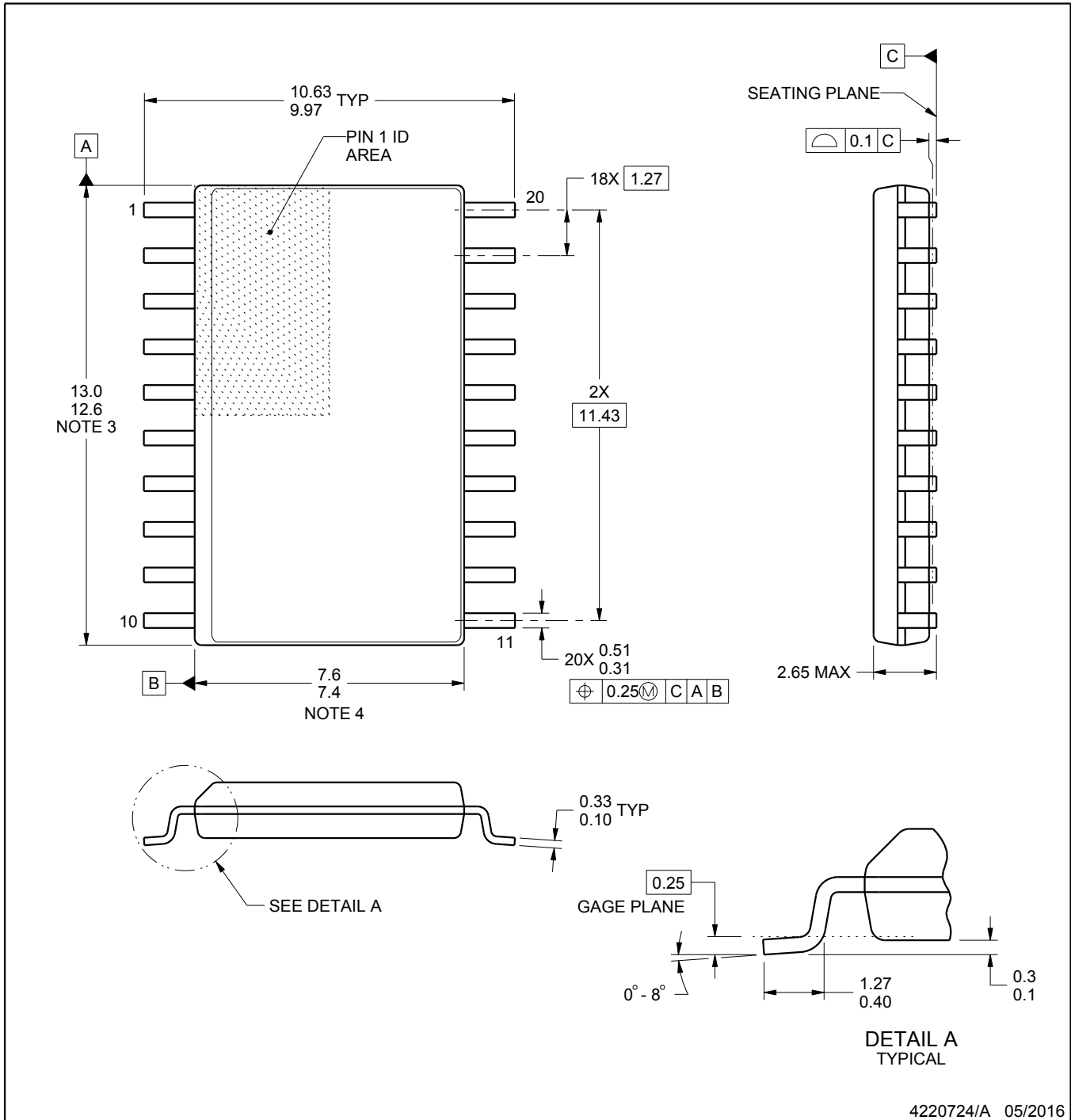
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

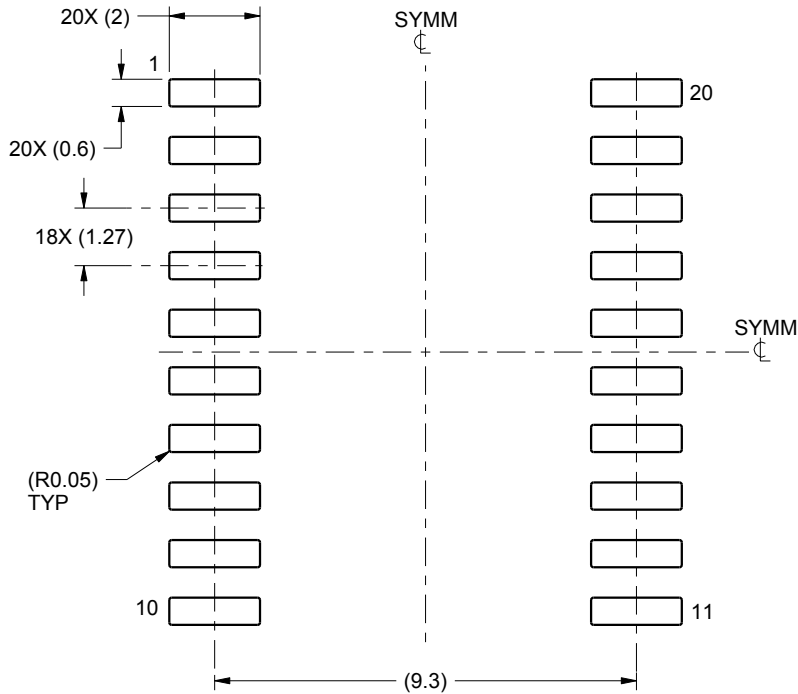
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

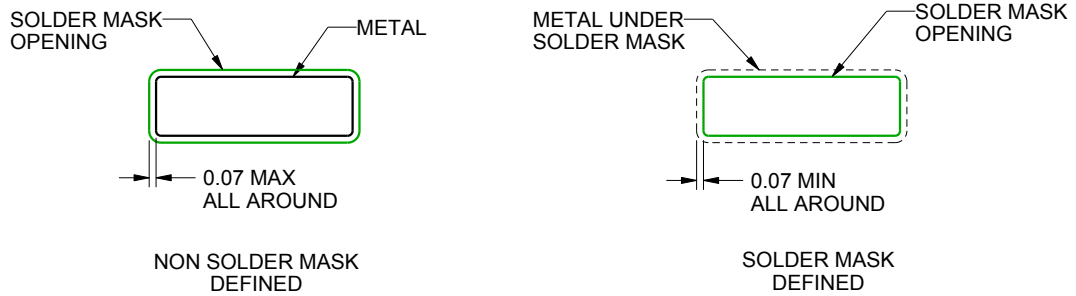
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

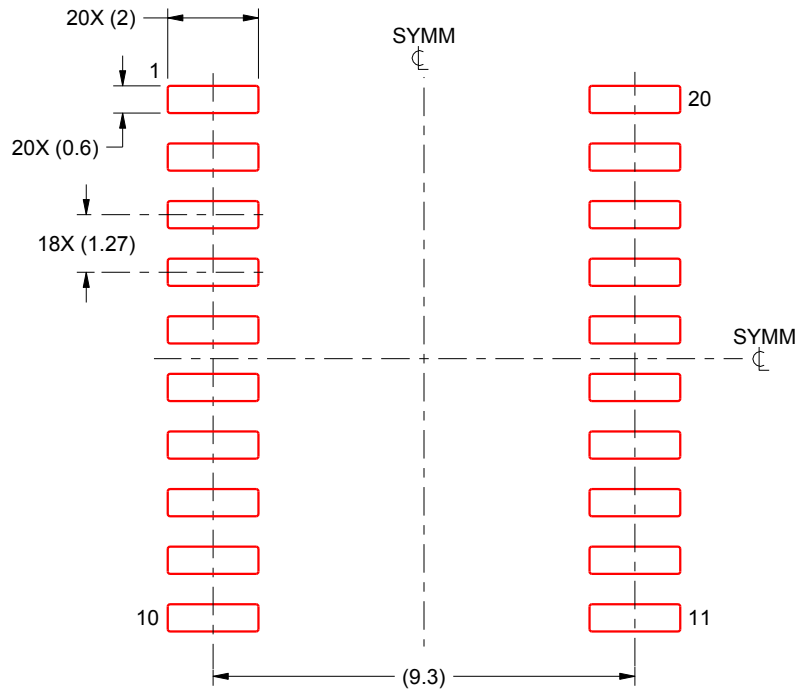
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

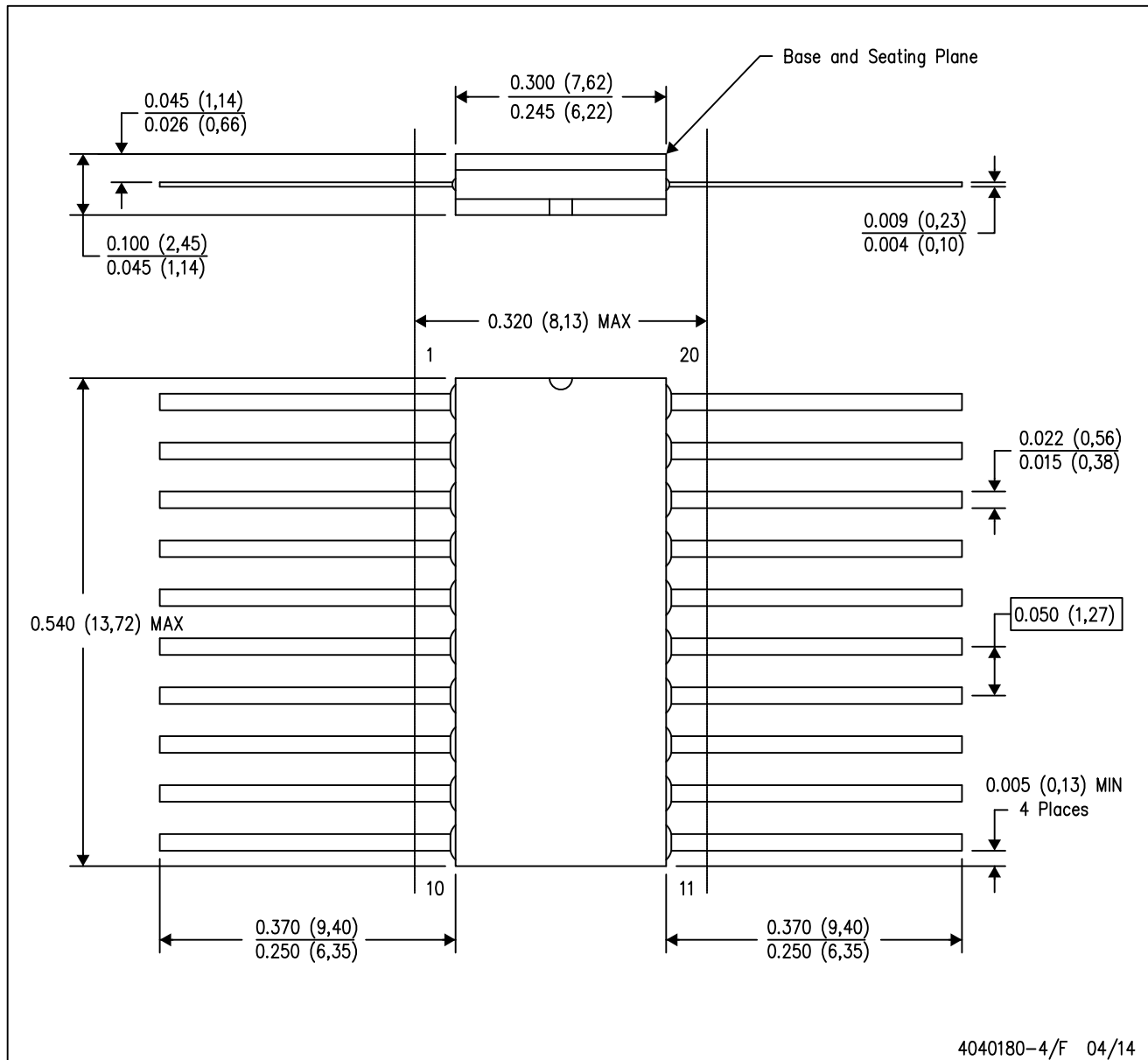
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

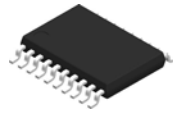
CERAMIC DUAL FLATPACK



4040180-4/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

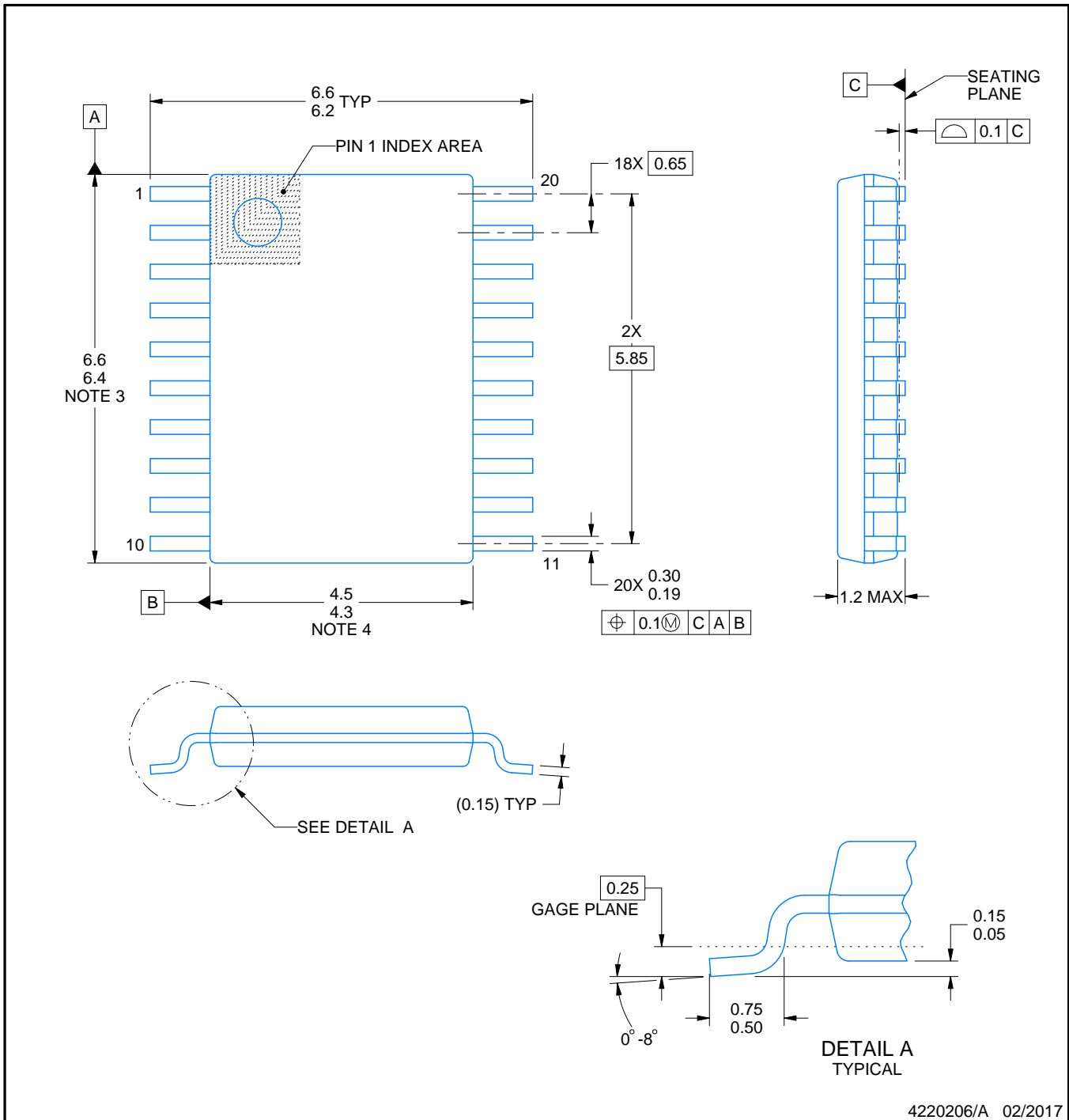
PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

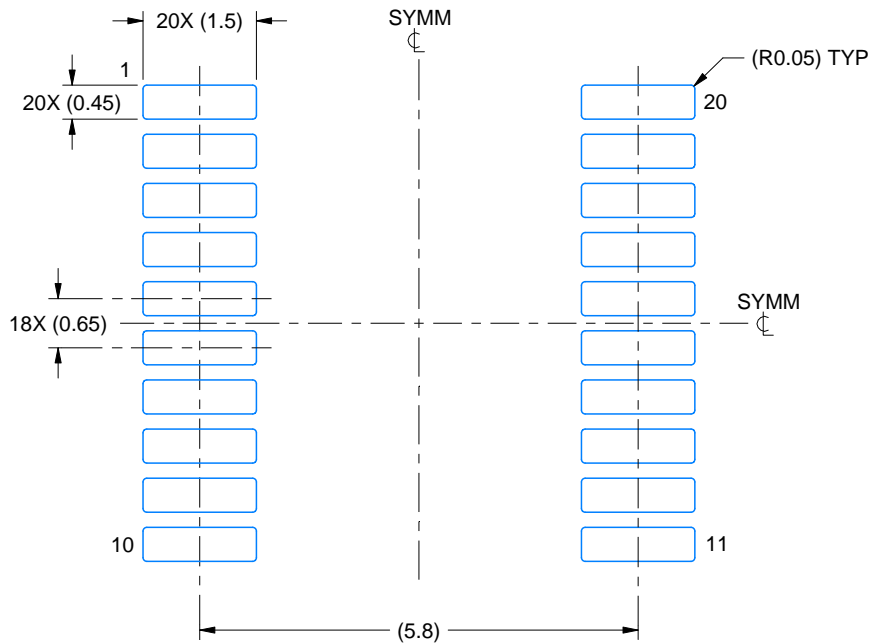
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

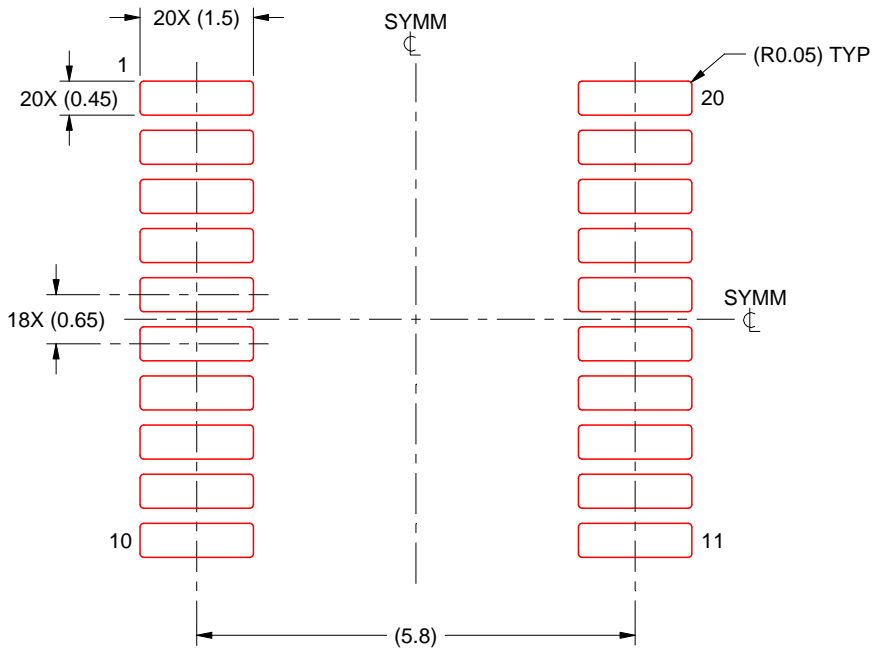


# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

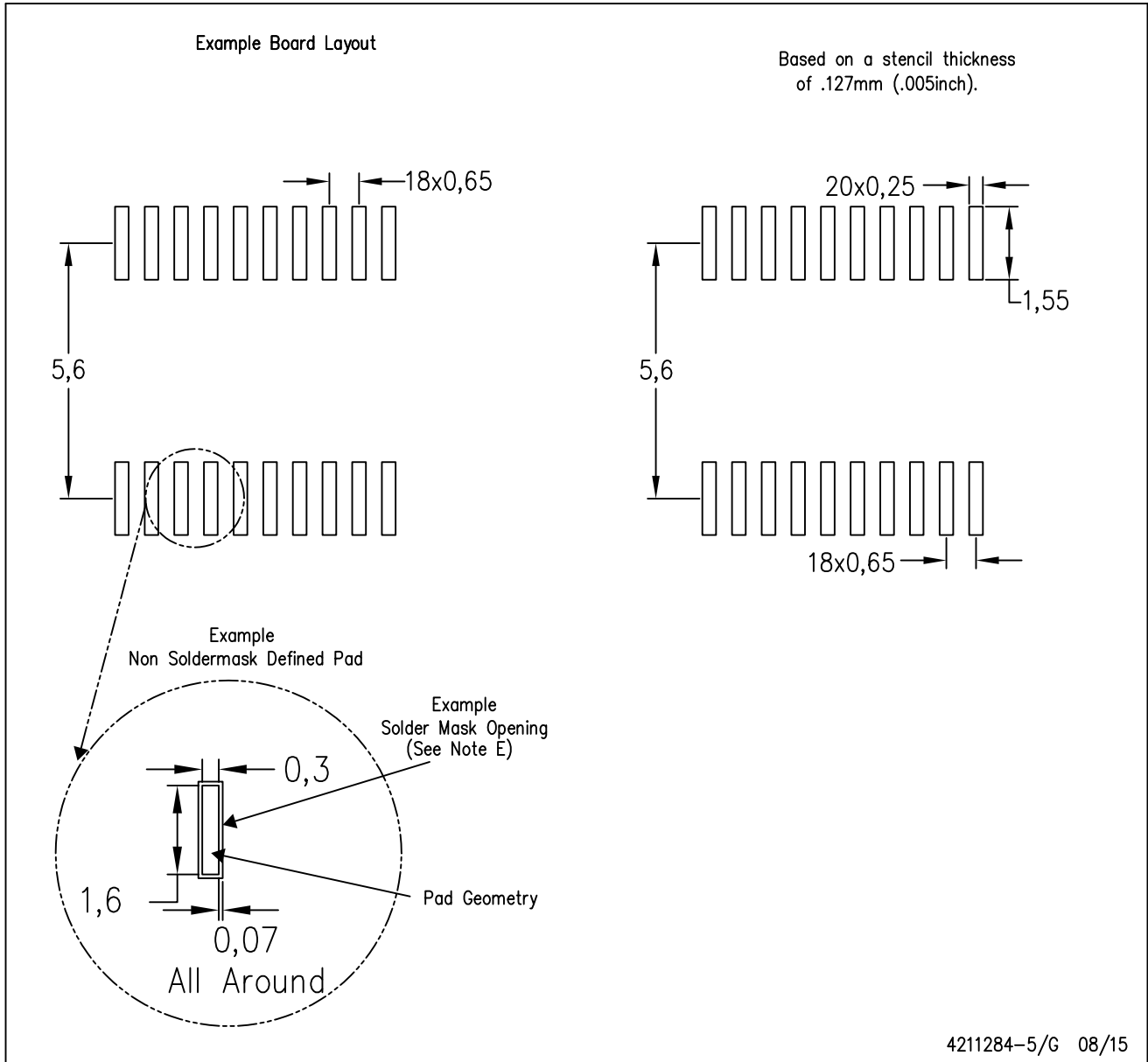
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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