

# SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS245A – DECEMBER 1982 – REVISED JANUARY 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Low-Power Versions of 'ALS245 Series
- 'ALS1245 Series Is Identical to 'ALS1645 Series
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

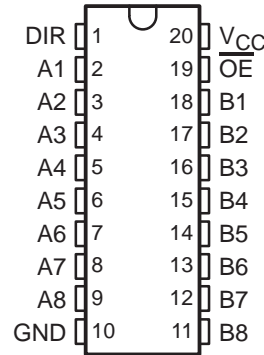
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

The SN54ALS1245A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS1245A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

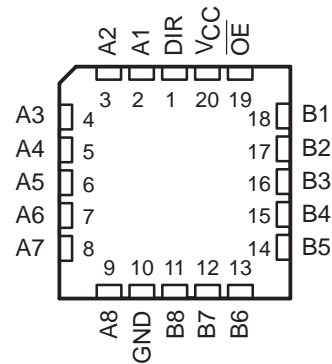
FUNCTION TABLE

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |

SN54ALS1245A . . . J PACKAGE  
SN74ALS1245A . . . DW OR N PACKAGE  
(TOP VIEW)



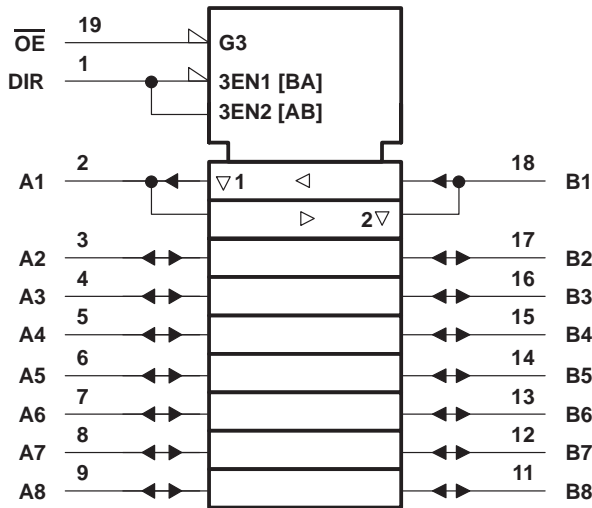
SN54ALS1245A . . . FK PACKAGE  
(TOP VIEW)



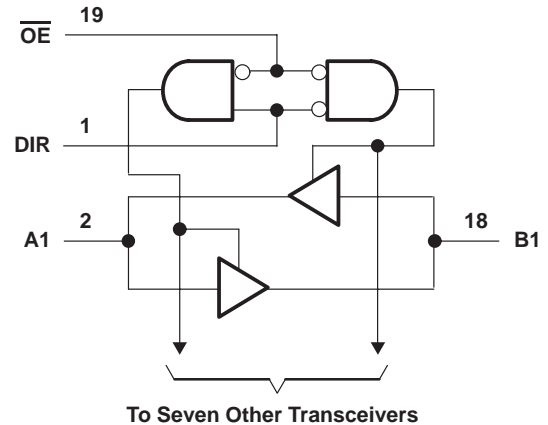
# SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS245A – DECEMBER 1982 – REVISED JANUARY 1995

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|  |                |
|--|----------------|
| Supply voltage, $V_{CC}$                                   | 7 V            |
| Input voltage, $V_I$ : All inputs                          | 7 V            |
| I/O ports  | 5.5 V          |
| Operating free-air temperature range, $T_A$ : SN54ALS1245A | -55°C to 125°C |
| SN74ALS1245A   | 0°C to 70°C    |
| Storage temperature range                                  | -65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

|                                      | SN54ALS1245A |     |     | SN74ALS1245A |     |     | UNIT |
|--------------------------------------|--------------|-----|-----|--------------|-----|-----|------|
|                                      | MIN          | NOM | MAX | MIN          | NOM | MAX |      |
| $V_{CC}$ Supply voltage              | 4.5          | 5   | 5.5 | 4.5          | 5   | 5.5 | V    |
| $V_{IH}$ High-level input voltage    | 2            |     |     | 2            |     |     | V    |
| $V_{IL}$ Low-level input voltage     |              |     | 0.7 |              |     | 0.8 | V    |
| $I_{OH}$ High-level output current   |              |     | -12 |              |     | -15 | mA   |
| $I_{OL}$ Low-level output current    |              |     | 8   |              |     | 16  | mA   |
| $T_A$ Operating free-air temperature | -55          |     | 125 | 0            |     | 70  | °C   |

# SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS245A – DECEMBER 1982 – REVISED JANUARY 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS   | SN54ALS1245A                                   |      | SN74ALS1245A         |      | UNIT |               |
|-----------|---|--|------|----------------------|------|------|---------------|
|           |   | MIN  | TYP† | MAX                  | MIN  |      | TYP†          |
| $V_{IK}$  | $V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$                     |  |      | -1.5                 |      |      | V             |
| $V_{OH}$  | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$                                   |      | $V_{CC} - 2$         |      | V    |               |
|           | $V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$                   | 2.4  | 3.2  | 2.4                  | 3.2  |      |               |
|           | $V_{CC} = 4.5\text{ V}$ , $I_{OH} = -12\text{ mA}$                  | 2  |      |                      |      |      |               |
| $V_{OL}$  | $V_{CC} = 4.5\text{ V}$   |  |      | 0.25                 | 0.4  | 0.25 | 0.4           |
|           |   |  |      |                      |      | 0.35 | 0.5           |
|           |   |  |      |                      |      |      |               |
| $I_I$     | Control inputs  | $V_{CC} = 5.5\text{ V}$                        |      | $V_I = 7\text{ V}$   |      | 0.1  | 0.1           |
|           | A or B ports  | $V_{CC} = 5.5\text{ V}$                        |      | $V_I = 5.5\text{ V}$ |      | 0.1  | 0.1           |
| $I_{IH}$  | Control inputs  | $V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$ |      | 20                   |      | 20   | $\mu\text{A}$ |
|           | A or B ports‡   | $V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$ |      | 20                   |      | 20   |               |
| $I_{IL}$  | Control inputs  | $V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$ |      | -0.1                 |      | -0.1 | mA            |
|           | A or B ports‡   | $V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$ |      | -0.1                 |      | -0.1 |               |
| $I_{O\S}$ | $V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$                     | -20  | -112 | -30                  | -112 | mA   |               |
| $I_{CC}$  | $V_{CC} = 5.5\text{ V}$   | Outputs high                                   |      | 21                   | 33   | 21   | 30            |
|           |   | Outputs low                                    |      | 23                   | 36   | 23   | 33            |
|           |   | Outputs disabled                               |      | 25                   | 40   | 25   | 36            |

† All typical values are  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

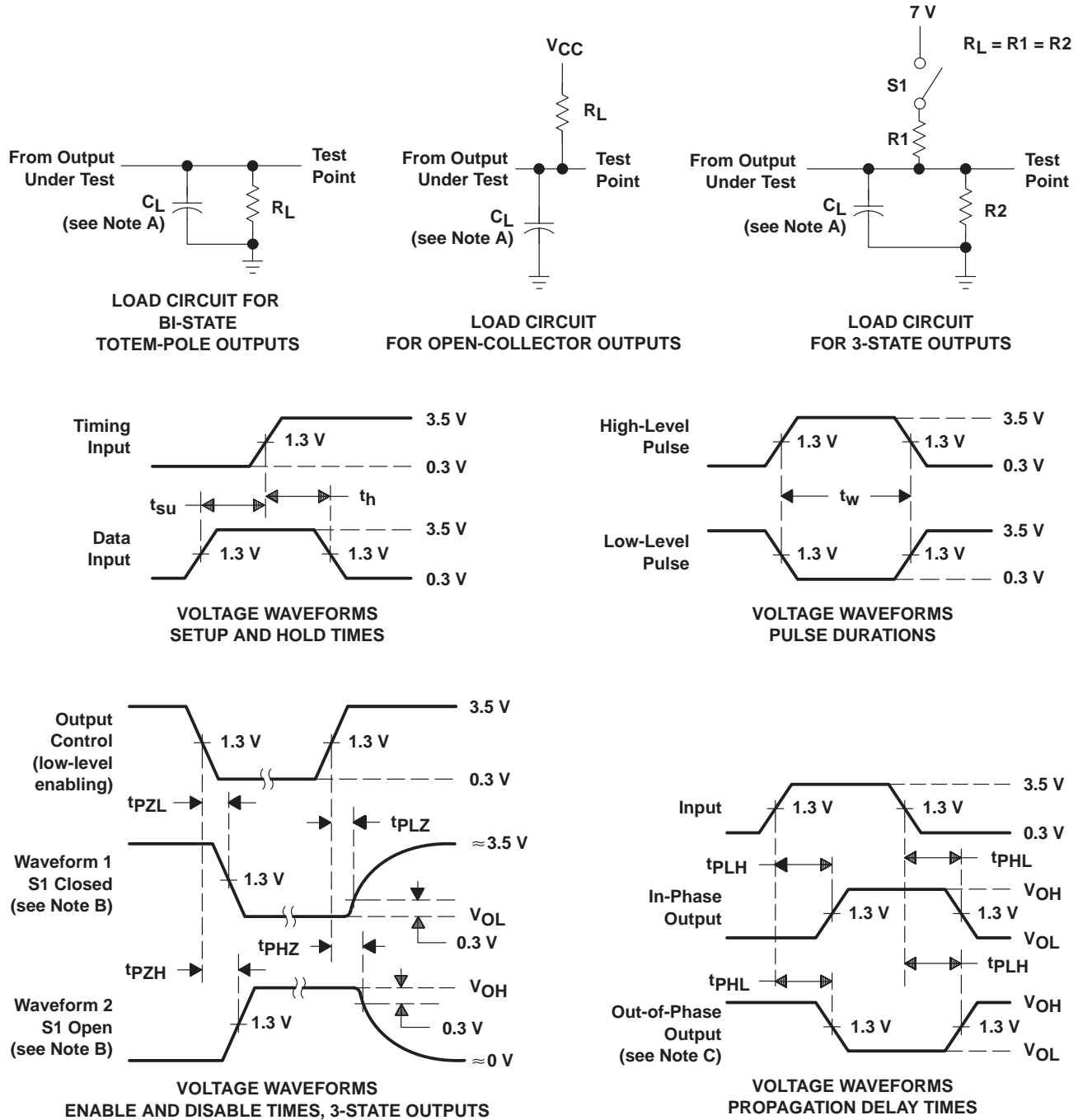
| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,<br>$C_L = 50\text{ pF}$ ,<br>$R_1 = 500\ \Omega$ ,<br>$R_2 = 500\ \Omega$ ,<br>$T_A = \text{MIN to MAX}\parallel$ |     |              |     | UNIT |
|-----------|-----------------|-------------|---|-----|--------------|-----|------|
|           |                 |             | SN54ALS1245A  |     | SN74ALS1245A |     |      |
|           |                 |             | MIN   | MAX | MIN          | MAX |      |
| $t_{PLH}$ | A or B          | B or A      | 2   | 19  | 2            | 13  | ns   |
| $t_{PHL}$ |                 |             | 2   | 15  | 2            | 13  |      |
| $t_{PZH}$ | $\overline{OE}$ | A or B      | 8   | 30  | 8            | 25  | ns   |
| $t_{PZL}$ |                 |             | 8   | 29  | 8            | 25  |      |
| $t_{PHZ}$ | $\overline{OE}$ | A or B      | 2   | 14  | 2            | 12  | ns   |
| $t_{PLZ}$ |                 |             | 3   | 30  | 3            | 18  |      |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS245A – DECEMBER 1982 – REVISED JANUARY 1995

## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                   | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|---|-------------------------|
| 5962-88737012A   | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>88737012A<br>SNJ54ALS<br>1245AFK | <a href="#">Samples</a> |
| 5962-8873701RA   | ACTIVE        | CDIP         | J               | 20   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8873701RA<br>SNJ54ALS1245AJ          | <a href="#">Samples</a> |
| SN74ALS1245AN    | ACTIVE        | PDIP         | N               | 20   | 20          | RoHS &<br>Non-Green | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74ALS1245AN                             | <a href="#">Samples</a> |
| SNJ54ALS1245AFK  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>88737012A<br>SNJ54ALS<br>1245AFK | <a href="#">Samples</a> |
| SNJ54ALS1245AJ   | ACTIVE        | CDIP         | J               | 20   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8873701RA<br>SNJ54ALS1245AJ          | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

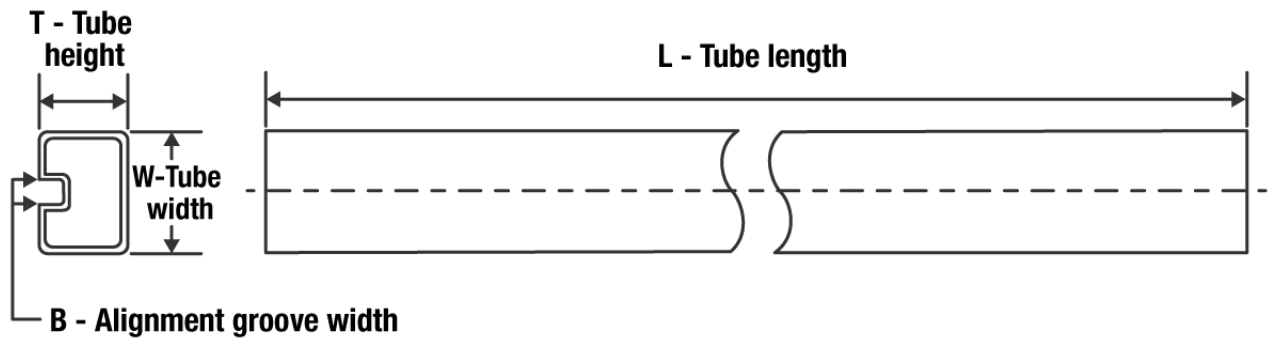
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ALS1245A, SN74ALS1245A :**

- Catalog : [SN74ALS1245A](#)
- Military : [SN54ALS1245A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TUBE**


\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-88737012A  | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| SN74ALS1245AN   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54ALS1245AFK | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated