具有 15mA 低空闲电流和 AM 抑制功能的 TPA3126D2 50W 立体声、模拟输入 D 类音频放大器

1 特性

- 电池使用时间更长：
  - 超低空闲电流：12V 时为 15mA
- 21V 电压、10% THD+N、4Ω 负载条件下的功率为 2 × 50W
- 宽电压范围：4.5V 至 26V
- 高效 D 类运行模式
  - 混合调制方案可动态降低功率损耗
  - 低至 90mΩ 的 $R_{ds(on)}$ 可确保效率 > 90%
- 噗声和嘀哒声噪声抑制
- 支持立体声、单声道 BTL 和单声道 PBTL
- 多种开关频率：
  - AM 抑制
  - 主从同步
  - 300kHz 至 1.2MHz 开关频率
- 可选增益：20dB、26dB、32dB、36dB
- 可编程功率限制
- 支持单电源和双电源
- 带错误报告的综合保护功能：
  - 过压、欠压、过热、直流检测和短路
- 热增强型封装
  - DAD（32 引脚 HTSSOP PowerPAD™封装，焊盘朝上）
- 性能在 TPA3116D2 基础上升级
  - 空闲电流降低 70%；引脚对引脚兼容

2 应用

- 扬声器底座
- Bluetooth®和 Wi-Fi 扬声器
- 声控扬声器或智能扬声器
- 条形音箱
- 书架立体声系统

3 说明

TPA3126D2 是一款采用热增强型封装的 50W 立体声低空闲电流 D 类放大器。TPA3126D2 采用了 TI 专有的混合调制方案，可在低功率水平下动态降低空闲电流，从而延长便携式音频系统（如蓝牙扬声器）的电池寿命。

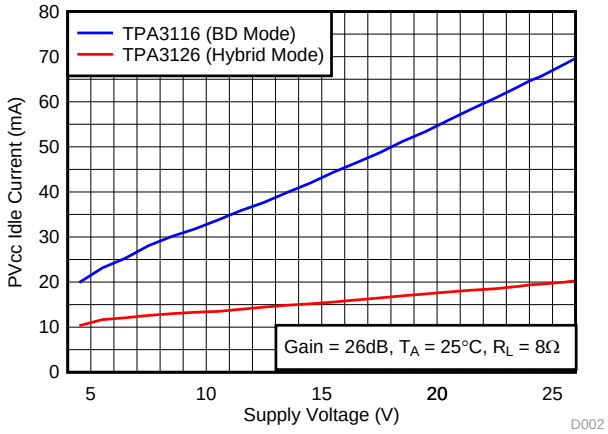
为了进一步简化设计，该 D 类放大器集成了全面的保护 特性 ，包括短路、热关断、过压、欠压和直流扬声器保护。在过载情况下，器件会将故障情况报告给处理器，从而避免自身遭到损坏。

器件信息(1)

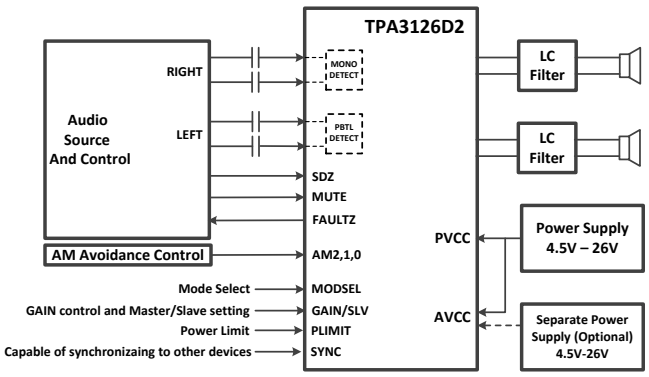
器件型号	封装	封装尺寸（标称值）
TPA3126D2	HTSSOP (32)	11.00mm x 6.20mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

TPA3126 和 TPA3116 空闲电流



简化应用电路



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4 修订历史记录

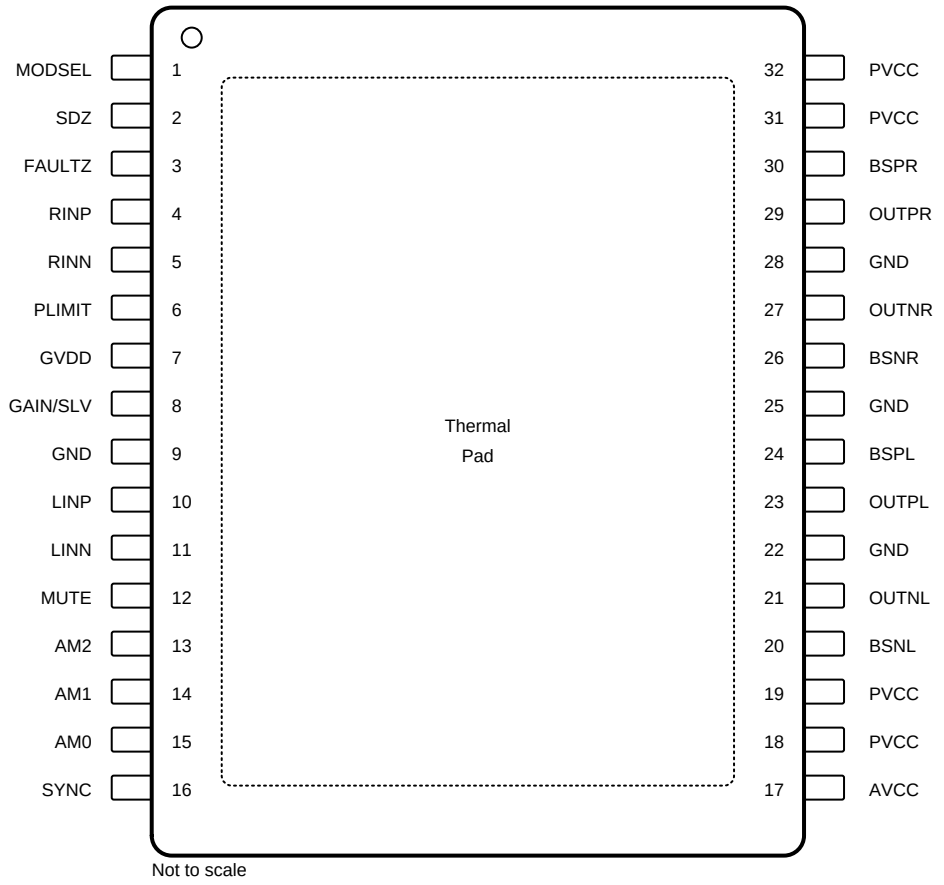
日期	修订版本	说明
2018 年 4 月	*	最初发布版本。

5 Device Comparison Table

PRODUCT	DESCRIPTION	MODULATION SCHEME	THERMAL PAD LOCATION	TPA3126 PIN-COMPATIBLE
TPA3116D2	50-W Stereo, Analog-Input Class D Amplifier	BD, 1SPW	Top	Y
TPA3118D2	30-W Stereo, Analog-Input Class D Amplifier	BD, 1SPW	Bottom	Y
TPA3128D2	30-W Stereo, Analog-Input Class D Amplifier with Low Idle Power Dissipation	BD, 1SPW, Hybrid	Bottom	Y
TPA3156D2	70-W Stereo, Analog-Input Class D Amplifier with Low Idle Power Dissipation	BD, 1SPW, Hybrid	Top	Y

6 Pin Configuration and Functions

DAD Package
32-Pin HTSSOP With PowerPAD™ Up
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	MODSEL	I	Mode selection logic input (LOW = Hybrid Mode, HIGH = BD Mode). TTL logic levels with compliance to AVCC. Refer to: Device Modulation Scheme
2	SDZ	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC. Refer to: Startup and Shutdown Operation
3	FAULTZ	DO	General fault reporting including Over-temp, DC Detect. Open drain. Refer to: Device Protection System FAULTZ = High, normal operation FAULTZ = Low (an external 100 kΩ pull-up resistor required), fault condition
4	RINP	I	Positive audio input for right channel. Connect to GND for MONO mode.
5	RINN	I	Negative audio input for right channel. Connect to GND for MONO mode.
6	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit. Refer to: PLIMIT Operation
7	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the PLIMIT and GAIN/SLV resistor dividers. Refer to: GVDD Supply
8	GAIN/SLV	I	Selects Gain and selects between Master and Slave mode depending on pin voltage divider. Refer to: Gain Setting and Master and Slave
9	GND	G	Ground

(1) DO = Digital Output, I = Analog Input, G = General Ground, PO = Power Output, BST = Boot Strap.

Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
10	LINP	I	Positive audio input for left channel. Connect to GND for PBTL mode.
11	LINN	I	Negative audio input for left channel. Connect to GND for PBTL mode.
12	MUTE	I	Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
13	AM2	I	AM Avoidance Frequency Selection
14	AM1	I	AM Avoidance Frequency Selection
15	AM0	I	AM Avoidance Frequency Selection
16	SYNC	DIO	Clock input/output for synchronizing multiple Class-D devices. Direction determined by GAIN/SLV terminal. Refer to: Gain Setting and Master and Slave
17	AVCC	P	Analog Supply
18	PVCC	P	Power supply
19	PVCC	P	Power supply
20	BSNL	BST	Boot strap for negative left channel output, connect to 220 nF X5R, or better ceramic cap to OUTPL
21	OUTNL	PO	Negative left channel output
22	GND	G	Ground
23	OUTPL	PO	Positive left channel output
24	BSPL	BST	Boot strap for positive left channel output, connect to 220 nF X5R, or better ceramic cap to OUTNL Refer to: BSPx and BSNx Capacitors
25	GND	G	Ground
26	BSNR	BST	Boot strap for negative right channel output, connect to 220 nF X5R, or better ceramic cap to OUTNR. Refer to: BSPx and BSNx Capacitors
27	OUTNR	PO	Negative right channel output
28	GND	G	Ground
29	OUTPR	PO	Positive right channel output
30	BSPR	BST	Boot strap for positive right channel output, connect to 220 nF X5R or better ceramic cap to OUTPR. Refer to: BSPx and BSNx Capacitors
31	PVCC	P	Power supply
32	PVCC	P	Power supply
	PowerPAD™	G	Connect to GND for best system performance. If not connected to GND, leave floating.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	–0.3	30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	–0.3	6.3	V
	PLIMIT, GAIN/SLV, SYNC	–0.3	GVDD+0.3	V
	AM0, AM1, AM2, MUTE, SDZ, MODSEL	–0.3	PVCC+0.3	V
Slew rate, maximum(2)	AM0, AM1, AM2, MUTE, SDZ, MODSEL		10	V/ms
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature , T_J		–40	150	°C
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under absolute maximum ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) 100-kΩ series resistor is required if maximum slew rate is exceeded.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}	4.5		26	V
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL	2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 kΩ, PV_{CC} = 26 V			0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, SDZ, MODSEL (V_I = 2 V, V_{CC} = 18 V)			50	μA
R_L(BTL)	Minimum load Impedance	Output filter: L = 10 μH, C = 680 nF	3.2	4		Ω
R_L(PBTL)		Output filter: L = 10 μH, C = 1 μF	1.6	2		
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition	1			μH

7.4 Thermal Information

THERMAL METRIC(1)		TPA3126D2 DAD(2) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	N/A	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) For the PCB layout, see the TPA3126D2EVM user guide.

7.5 DC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω, f_s = 400 kHz, hybrid mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V		1.5	5	mV
I_{CC}	Quiescent supply current	SDZ = 2 V, With load and filter, PV_{CC} = 12 V		15		mA
		SDZ = 2 V, With load and filter, PV_{CC} = 24 V		23		
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ = 0.8 V, With load and filter, PV_{CC} = 12 V		20		µA
		SDZ = 0.8 V, With load and filter, PV_{CC} = 24 V		30		
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PV_{CC} = 21 V, I_{out} = 500 mA, T_J = 25°C		90		mΩ
G	Gain (BTL)	R1 = 5.6 kΩ, R2 = Open	19	20	21	dB
		R1 = 20 kΩ, R2 = 100 kΩ	25	26	27	
		R1 = 39 kΩ, R2 = 100 kΩ	31	32	33	dB
		R1 = 47 kΩ, R2 = 75 kΩ	35	36	37	
G	Gain (SLV)	R1 = 51 kΩ, R2 = 51 kΩ	19	20	21	dB
		R1 = 75 kΩ, R2 = 47 kΩ	25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	dB
		R1 = 100 kΩ, R2 = 16 kΩ	35	36	37	
t_{on}	Turn-on time	SDZ = 2 V		40		ms
t_{OFF}	Turn-off time	SDZ = 0.8 V		2		µs
GVDD	Gate drive supply	I_{GVDD} < 200 µA	5.1	5.6	6.3	V
V_O	Output voltage maximum under PLIMIT control	$V_{(PLIMIT)}$ = 2 V; V_I = 1 V_{rms}	6.75	8.2	8.75	V

7.6 AC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 26 dB, Inputs AC-coupled to GND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, PV_{CC} = 14.4 V		25		W
		THD+N = 10%, f = 1 kHz, PV_{CC} = 21 V		50		
THD+N	Total harmonic distortion + noise	V_{CC} = 21 V, f = 1 kHz, P_O = 15 W (half-power)		0.1%		
Vn	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		μV
				–80		dBV
	Crosstalk	V_O = 1 V_{rms}, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency	AM2=0, AM1=0, AM0=0	376	400	424	kHz
		AM2=0, AM1=0, AM0=1	470	500	530	
		AM2=0, AM1=1, AM0=0	564	600	636	
		AM2=0, AM1=1, AM0=1	940	1000	1060	
		AM2=1, AM1=0, AM0=0	1128	1200	1278	
		AM2=1, AM1=0, AM0=1	282	300	318	
		AM2=1, AM1=1, AM0=0 Modulation scheme Fixed in 1SPW Mode	282	300	318	
		AM2=1, AM1=1, AM0=1, Reserved				
	Thermal trip point			≥150		°C
	Thermal hysteresis			15		°C
	Over current trip point			7.5		A

7.7 Typical Characteristics

f_s = 400 kHz, Hybrid Mode, TPA3126D2EVM Tested With AP2722. (unless otherwise noted)

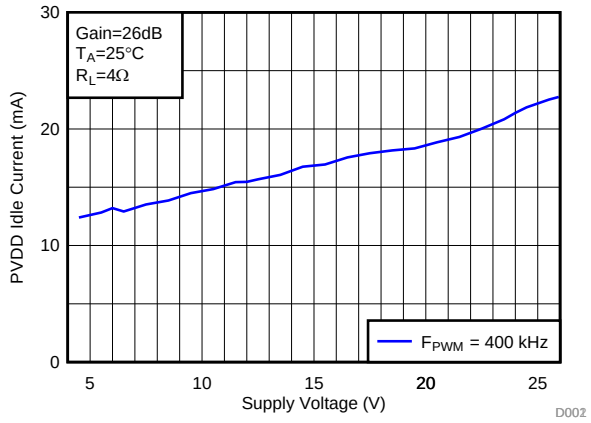


图 1. Idle Current vs PVCC

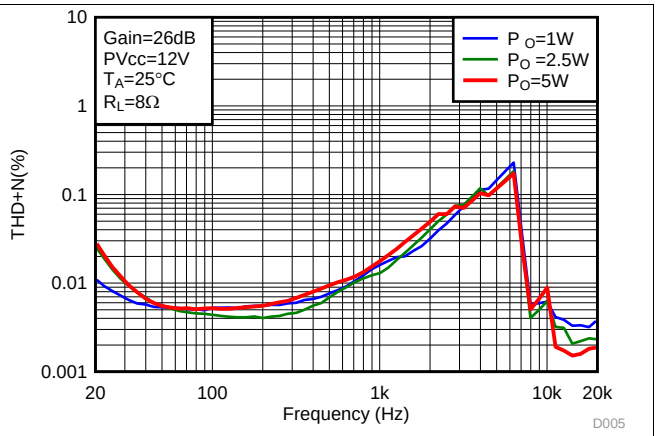


图 2. Total Harmonic Distortion + Noise (BTL) vs Frequency

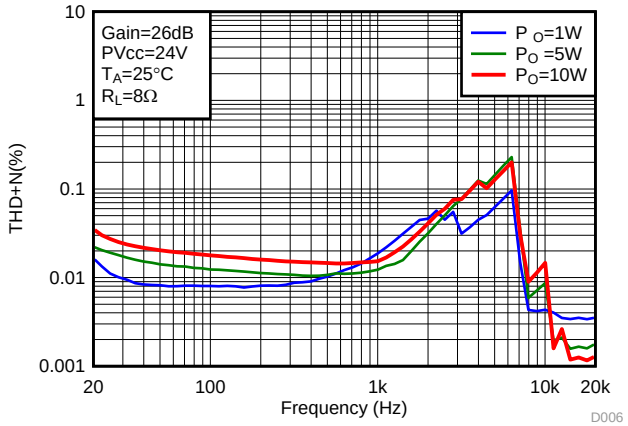


图 3. Total Harmonic Distortion + Noise (BTL) vs Frequency

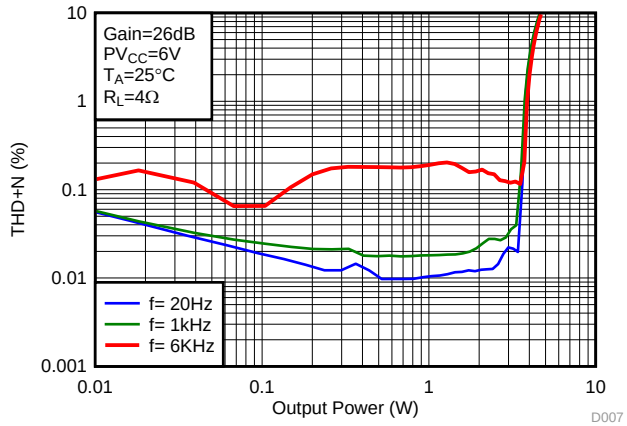


图 4. Total Harmonic Distortion + Noise (BTL) vs Output Power

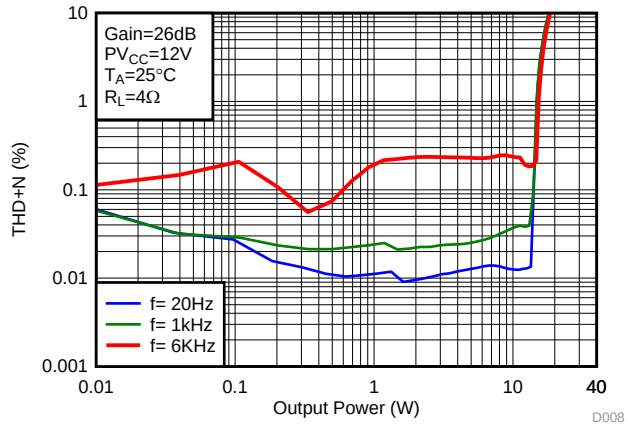


图 5. Total Harmonic Distortion + Noise (BTL) vs Output Power

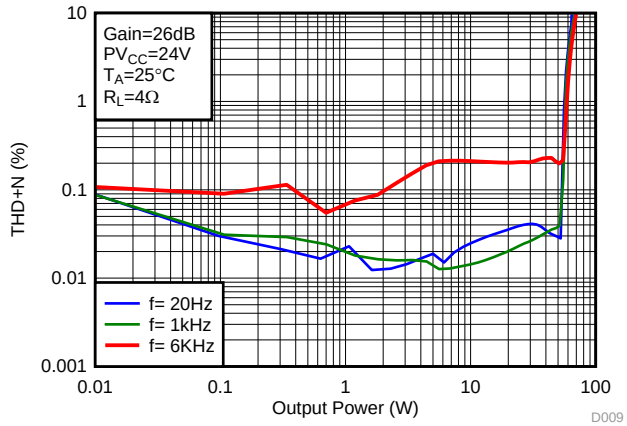


图 6. Total Harmonic Distortion + Noise (BTL) vs Output Power

Typical Characteristics (接下页)

f_s = 400 kHz, Hybrid Mode, TPA3126D2EVM Tested With AP2722. (unless otherwise noted)

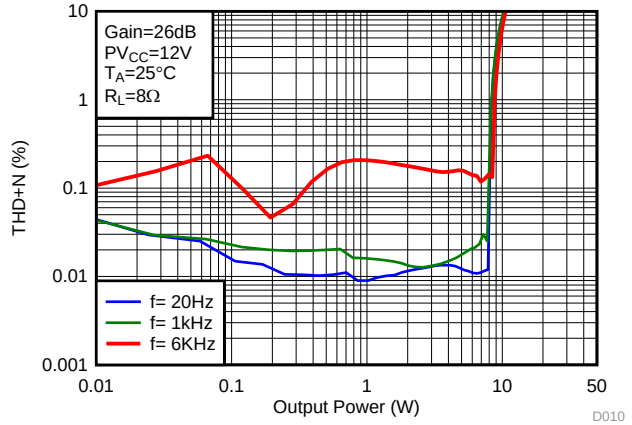


图 7. Total Harmonic Distortion + Noise (BTL) vs Output Power

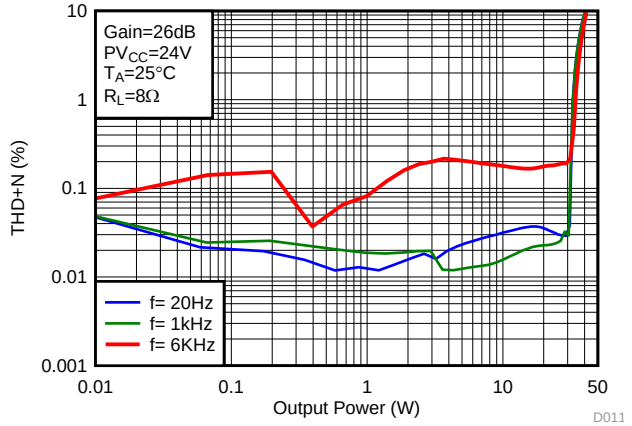


图 8. Total Harmonic Distortion + Noise (BTL) vs Output Power

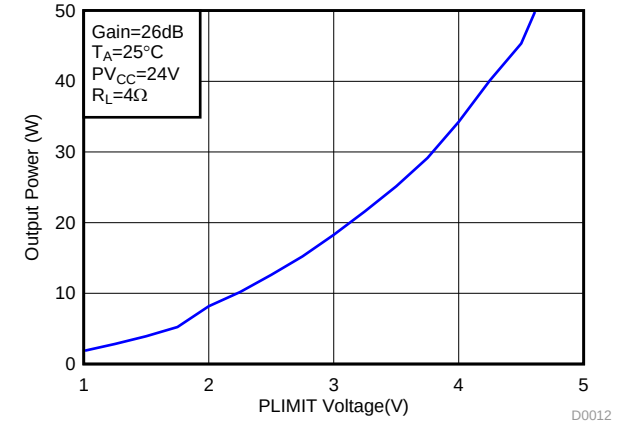


图 9. Output Power (BTL) vs PLIMIT Voltage

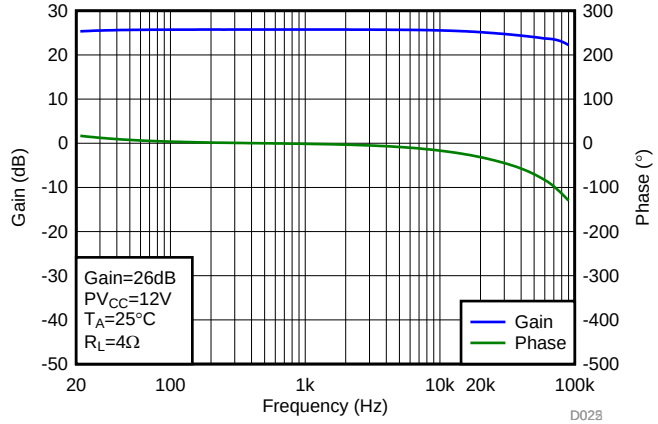


图 10. Gain/Phase (BTL) vs Frequency

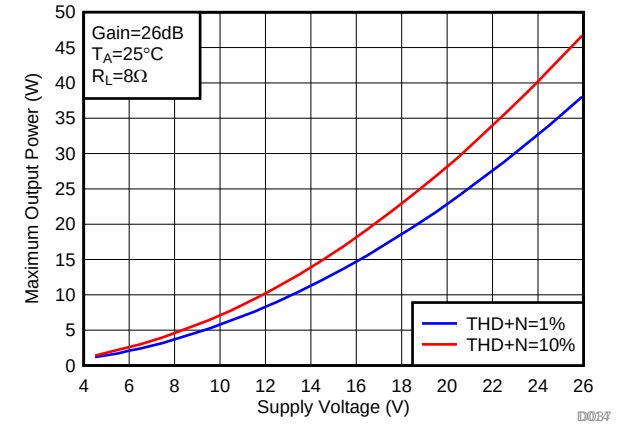


图 11. Maximum Output Power (BTL) vs Supply Voltage

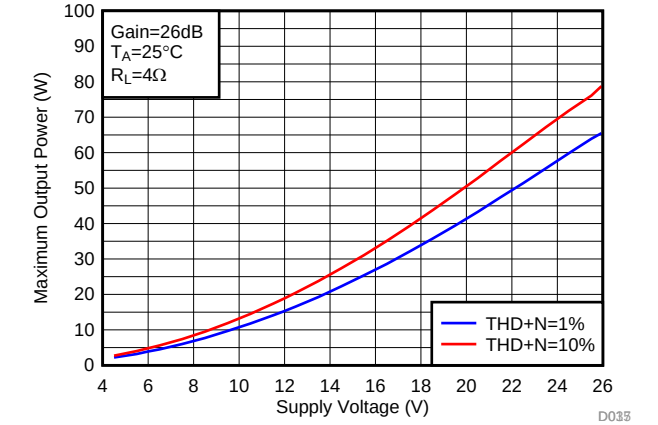


图 12. Maximum Output Power (BTL) vs Supply Voltage

Typical Characteristics (接下页)

f_s = 400 kHz, Hybrid Mode, TPA3126D2EVM Tested With AP2722. (unless otherwise noted)

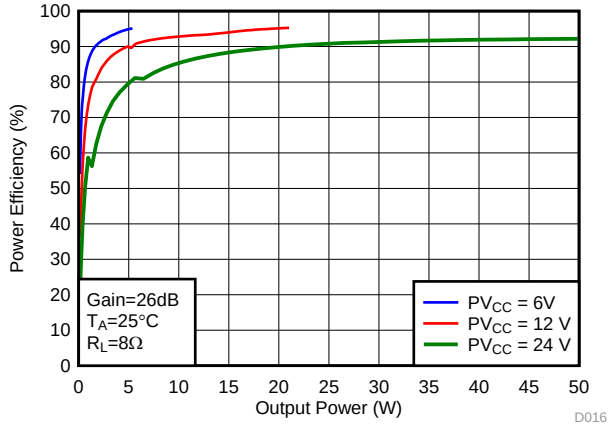


图 13. Power Efficiency (BTL) vs Output Power

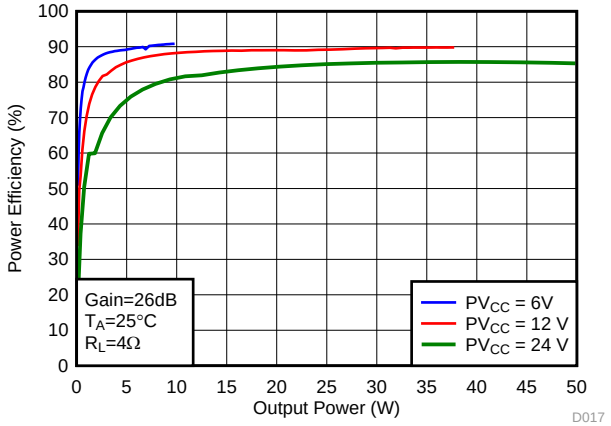


图 14. Power Efficiency (BTL) vs Output Power

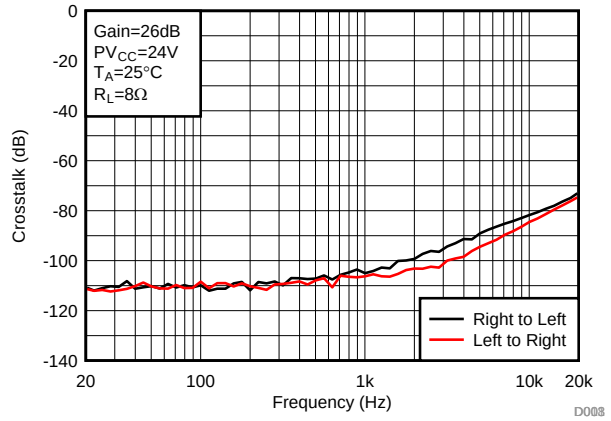


图 15. Crosstalk vs Frequency

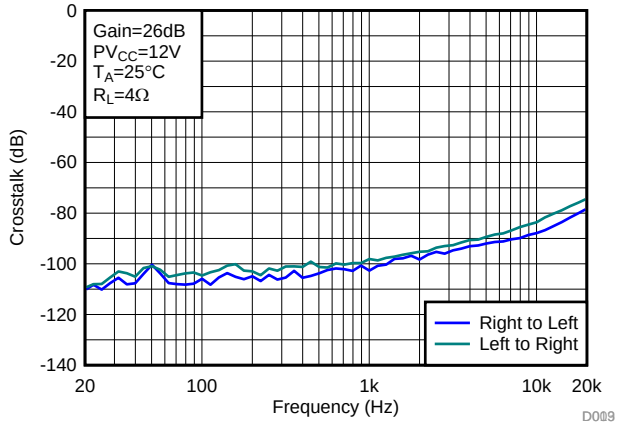


图 16. Crosstalk vs Frequency

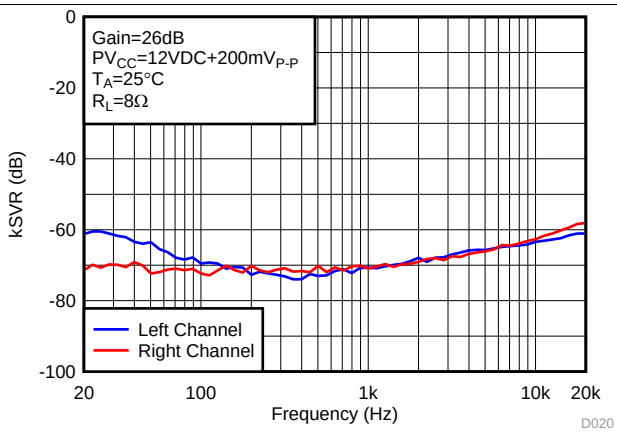


图 17. Supply Ripple Rejection Ratio (BTL) vs Frequency

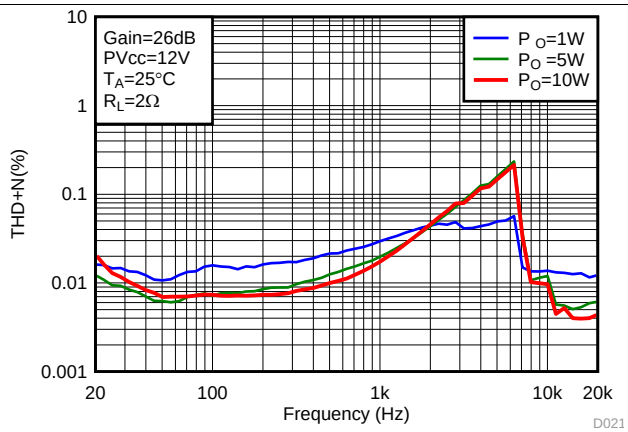


图 18. Total Harmonic Distortion + Noise (PBTL) vs Frequency

Typical Characteristics (接下页)

f_s = 400 kHz, Hybrid Mode, TPA3126D2EVM Tested With AP2722. (unless otherwise noted)

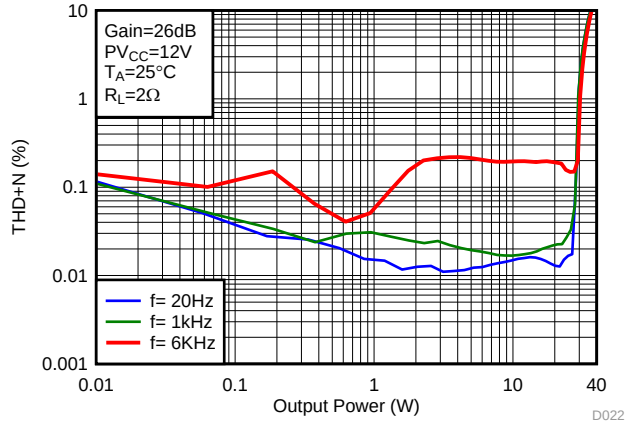


图 19. Total Harmonic Distortion + Noise (PBTL) vs Output Power

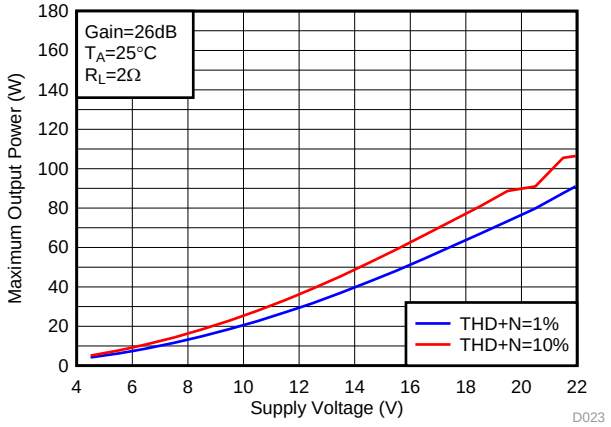


图 20. Maximum Output Power (PBTL) vs Supply Voltage

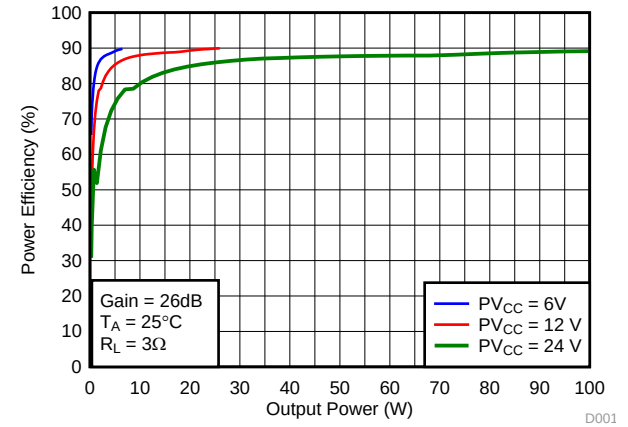


图 21. Power Efficiency (PBTL) vs Output Power

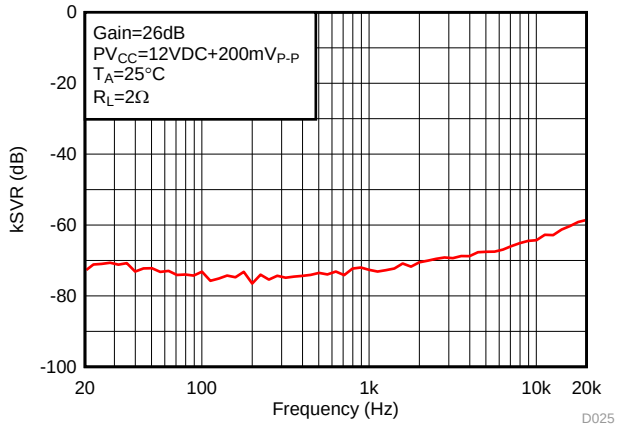


图 22. Supply Ripple Rejection Ratio (PBTL) vs Frequency

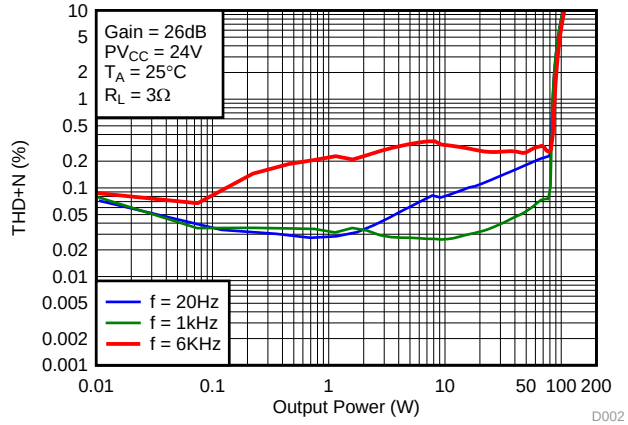


图 23. Total Harmonic Distortion + Noise (PBTL) vs Output Power

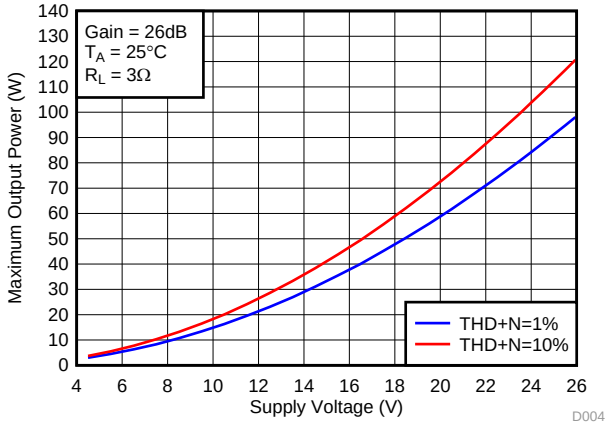


图 24. Maximum Output Power (PBTL) vs Supply Voltage

8 Detailed Description

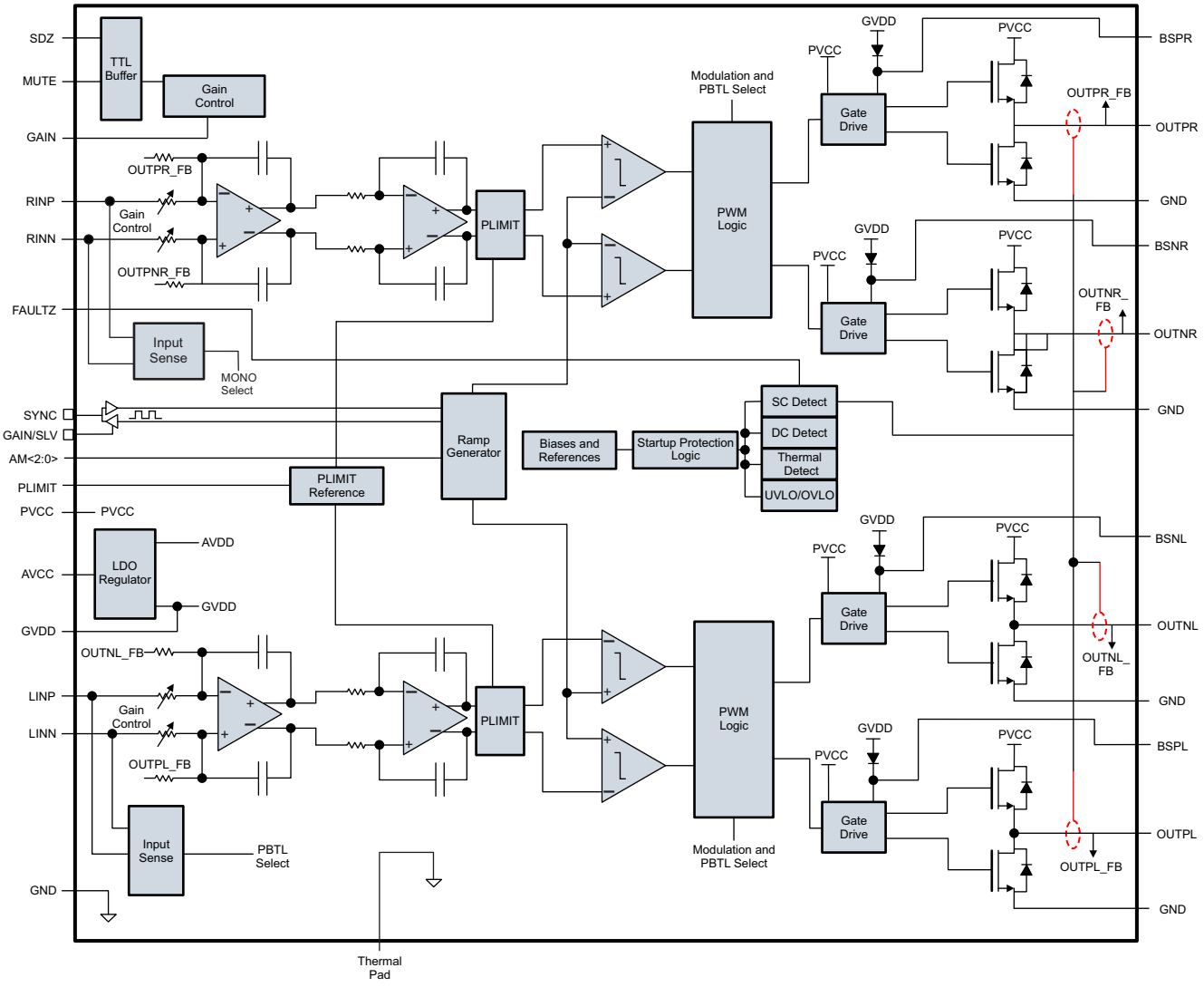
8.1 Overview

The analog-input Class-D amplifier TPA3126D2 is a performance upgrade to the prior generation TPA3116D2. It features a more efficient, 90-mΩ MOSFET, and has an extremely-low idle current of < 23 mA (24 V) in the standard LC filter configuration. The device can operate from the ultra-low-idle-loss modulation scheme, which enables low power dissipation in both idle condition and while playing music, optimized for battery-powered audio systems.

The TPA3126D2 supports both stereo and mono BTL modes, as well as mono PBTL mode. Comparing to the conventional Class-D amplifiers, in the mono BTL mode, the idle channel of the TPA3126D2 is not in the switching mode; therefore, it saves nearly half of the power loss, enabling low-power operation in single channel applications.

The device may be configured for either master or slave operation by using the SYNC pin. This configuration helps prevent the audible beats noise.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Gain Setting and Master and Slave

The gain of the TPA3126D2 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four states set the GAIN in Master mode with gains of 20, 26, 32, and 36 dB respectively, while the next four states set the GAIN in Slave mode with gains of 20, 26, 32, and 36 dB respectively. The gain setting is latched during power-up and cannot be changed while the device is powered on. 表 1 lists the recommended resistor values for different state settings.

表 1. Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

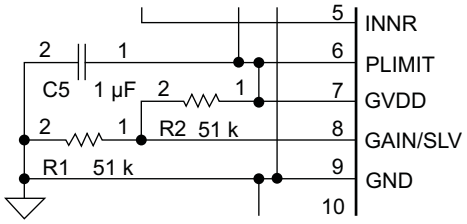


图 25. Gain, Master/Slave

In Master mode, the SYNC terminal is an output, while in Slave mode, the SYNC terminal is an input for a clock. TTL logic levels with compliance to GVDD.

8.3.2 Input Impedance

The TPA3126D2 input stage is a fully differential input stage and the input impedance changes with the gain setting from 7.3 kΩ at 36 dB gain to 50 kΩ at 20 dB gain. 表 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so that the minimum value will be higher than 5.9 kΩ. The inputs must be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input AC-coupling capacitor along with the input impedance forms a high-pass filter with the following cut-off frequency:

$$f = \frac{1}{2\pi Z_i C_i} \quad (1)$$

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. 表 2 lists the recommended AC-coupling capacitors for each gain setting. If a –3-dB frequency response is accepted at 20 Hz, 10 times lower capacitors (for example, a 1-µF capacitor) can be used.

表 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	50 kΩ	1.5 µF	2.1 Hz
26 dB	25 kΩ	3.3 µF	1.9 Hz
32 dB	12.5 kΩ	5.6 µF	2.3 Hz
36 dB	7.3 kΩ	10 µF	2.2 Hz

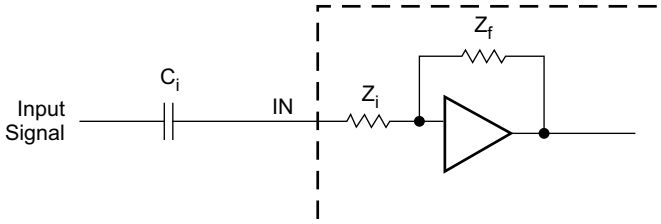


图 26. Input Impedance

The input capacitors should be a type of low leakage, such as quality electrolytic, tantalum, or ceramic capacitors. If a polarized type is used the positive connection should face the input pins which are biased to 3 Vdc.

8.3.3 Startup and Shutdown Operation

The TPA3126D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of non-use for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low puts the outputs to mute and the amplifier to enter a low-current state. Do not leave SDZ unconnected, because the amplifier operation is unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle, and cannot be changed until the next power-up.

8.3.4 PLIMIT Operation

The TPA3126D2 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail. The amplifier operates as if it was powered by a lower supply voltage, and thereby, limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1-µF capacitor from pin PLIMIT to ground to ensure stability.

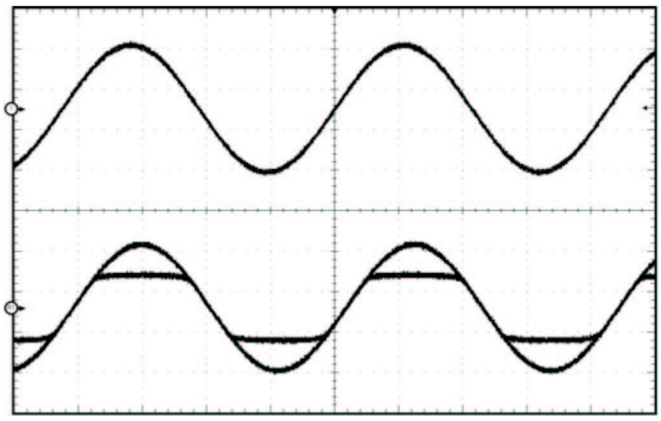


图 27. Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. This is done by limiting the duty cycle to a fixed maximum value. The limit can be considered as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is approximately four times the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

where

- P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)
- R_L is the load resistance.
- R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
- V_P is the peak amplitude, which is limited by the "virtual" voltage rail. (2)

表 3. Power Limit Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Open	Short	17.9
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9
12 V	GVDD	Open	Short	10.33
12 V	2.25	24 kΩ	51 kΩ	9
12 V	1.5	18 kΩ	68 kΩ	6.3

(1) PLIMIT measurements taken with EVM gain set to 26 dB and input voltage set to 1 V_{rms}.

8.3.5 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. The GVDD supply can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. Decouple GVDD with a X5R ceramic 1-µF capacitor to GND. The GVDD supply is not intended to be used for external supply. The current consumption should be limited by using resistor voltage dividers for GAIN/SLV and PLIMIT of 100 kΩ or more.

8.3.6 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input. (See the application circuit diagram in 图 34.) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

8.3.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3126D2 with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input. To use the TPA3126D2 with a single-ended source, AC ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be AC grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible to allow the input DC blocking capacitors to become completely charged during the 40-ms power-up time. If the input capacitors are not allowed to completely charged, there will be some additional sensitivity to the component matching which can result in pop if the input components are not well matched.

8.3.8 Device Protection System

The TPA3126D2 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin signals if an error is detected according to 表 4:

表 4. Fault Reporting

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	LATCHED/SELF-CLEARING
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	T_j > 150°C	Low	Output high impedance	Latched
Too High DC Offset	DC output voltage	Low	Output high impedance	Latched
Under Voltage on PVCC	PVCC < 4.5V	–	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 27V	–	Output high impedance	Self-clearing

8.3.9 DC Detect Protection

The TPA3126D2 has circuitry which protects the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault is reported on the FAULT pin as a low state. The DC Detect fault causes the amplifier to shutdown by changing the state of the outputs to Hi-Z.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. Connecting the FAULTZ and SDZ pins allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the DC Detect protection latch.

A DC Detect Fault is issued when the output differential voltage of either channel exceeds DC protection threshold level for more than 640 ms at the same polarity. 表 5 shows some examples of the typical DC Detect Protection threshold for several values of the supply voltage. The Detect Protection Threshold feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

表 5 lists the minimum output offset voltages required to trigger the DC detect. The outputs must remain at or above the voltage listed in the table for more than 640 ms to trigger the DC detect.

表 5. DC Detect Threshold

PV_{CC} (V)	V_{OS} - OUTPUT OFFSET VOLTAGE (V)
4.5	1.35
6	1.8
12	3.6
18	5.4

8.3.10 Short-Circuit Protection and Automatic Recovery Feature

The TPA3126D2 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. Connecting the FAULTZ and SDZ pins allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

8.3.11 Thermal Protection

Thermal protection on the TPA3126D2 prevents damage to the device when the internal die temperature exceeds 150°C. This trip point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state.

If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

8.3.12 Device Modulation Scheme

The TPA3126D2 has the option of running in either BD modulation or ultra-low idle current Hybrid Mode.

8.3.12.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amplifier is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

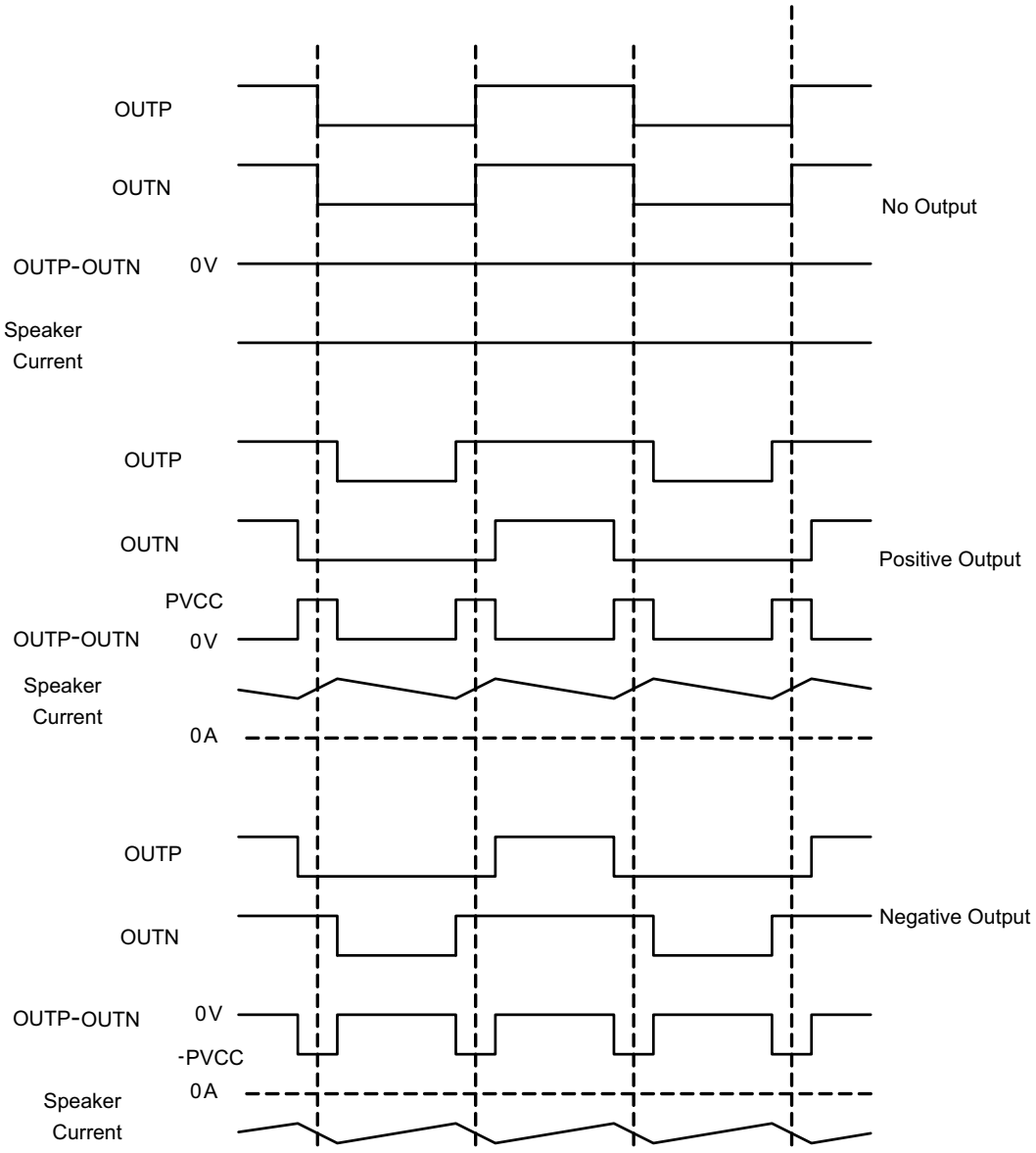


图 28. BD Mode Modulation

8.3.13 Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

Many traditional Class-D amplifiers are based on the AD modulation. Due to the out-of-phase nature of a BTL or PBTL amplifier operating in the AD modulation, if no LC filter was present, the load sees the full PWM signal across its terminals. This causes a high-frequency ripple current to pass through the load, which leads to high power dissipation, poor efficiency, and potential speaker damage. The ripple current is large in the AD modulation scheme, because it is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × VCC, and the time at each voltage is half the period for the AD modulation scheme. An ideal LC filter is required to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The modulation schemes implemented in the TPA3126D2 have little loss in the load even without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases and the pulses widen, the ripple current can go up. In this case, the ripple current can be filtered with an LC filter for increased efficiency. However, in most applications the filter is not required.

With an LC filter, specifically as the cut-off frequency of the LC filter is smaller than the PWM switching frequency of the amplifier, the ripple current is reduced such that only a small residual ripple voltage is present after the LC filter. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, hence increasing efficiency.

8.3.14 Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3126D2, a high efficiency Class-D audio amplifier can be designed while minimizing interference to the surrounding circuits. Designing the amplifier can also be accomplished with only a low-cost ferrite bead filter. In this case the user must carefully select the ferrite bead used in the filter. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, therefore the user must select a material that is effective in the 10-MHz to 100-MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30-MHz. The ferrite bead filter should be used to block radiation in the 30-MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000-pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead or capacitor filter should be less than 10-MHz.

Also, the ferrite bead must be large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, the device can also estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3136D2 can be seen in the TPA3136D2EVM user guide SLOU444.

A high quality ceramic capacitor is also required for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the Class-D outputs to ground. Suggested values for a simple RC series snubber network would be 18-Ω in series with a 330-pF capacitor, although design of the snubber network is specific to different applications and must be designed with the consideration of the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, verify the layout of the snubber network is tight and returns directly to the GND pins on the IC.

图 29 and 图 30 are TPA3126D2 EN55022 Radiated Emissions results uses TPA3126D2EVM with 8-Ω speakers.

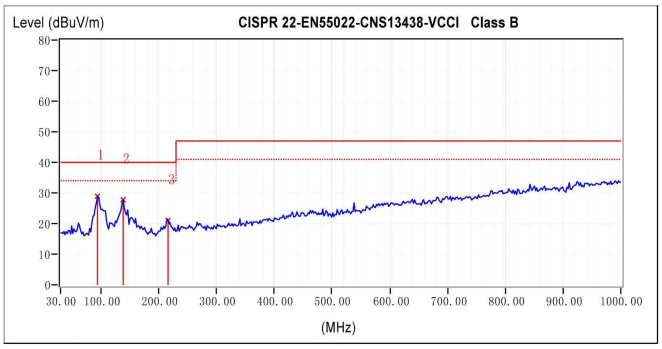


图 29. TPA3126D2 Radiated Emissions-Horizontal (PVCC=19V, P_O=1W)

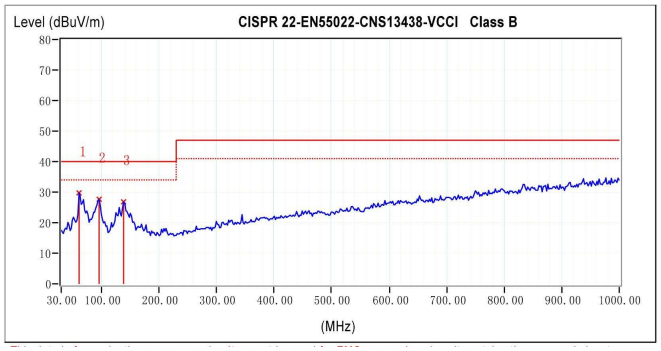


图 30. TPA3126D2 Radiated Emissions-Vertical (PVCC=19V, P_O=1W)

8.3.15 When to Use an Output Filter for EMI Suppression

A complete LC reconstruction filter should be added in some circuit instances. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in 图 31 can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest-cost methods to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective in preventing line conducted interference.

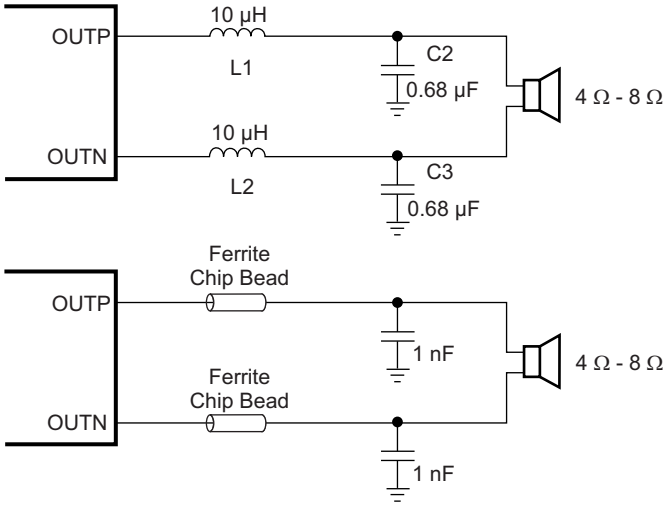


图 31. Output Filters

8.3.16 AM Avoidance EMI Reduction

表 6. AM Frequencies

US	EUROPEAN	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
AM FREQUENCY (kHz)	AM FREQUENCY (kHz)				
540-917	540-914	500	0	0	1
917-1125	914-1122	600 (or 400)	0	1	0
			0	0	0
1125-1375	1122-1373	500	0	0	1
1375-1547	1373-1548	600 (or 400)	0	1	0
			0	0	0
1547-1700	1548-1701	600 (or 500)	0	1	0
			0	0	1

8.4 Device Functional Modes

TPA3126D2 can be configured in either a stereo BTL (Bridge Tied Load) mode, mono BTL mode (only one output BTL channel active), or in a mono PBTL (Parallel Bridge Tied Load) mode.

8.4.1 Mono PBTL Mode

In mono PBTL mode, the device can deliver up to 100-W output power. Configuration steps for mono PBTL mode are as follows:

- Connect LINP and LINN directly to Ground (without capacitors), so the device is set in a mono PBTL mode during power up.
- Connect OUTPR and OUTNR together for the positive speaker terminal, and OUTNL and OUTPL together for the negative speaker terminal.
- Analog input signal is applied to RINP and RINN.

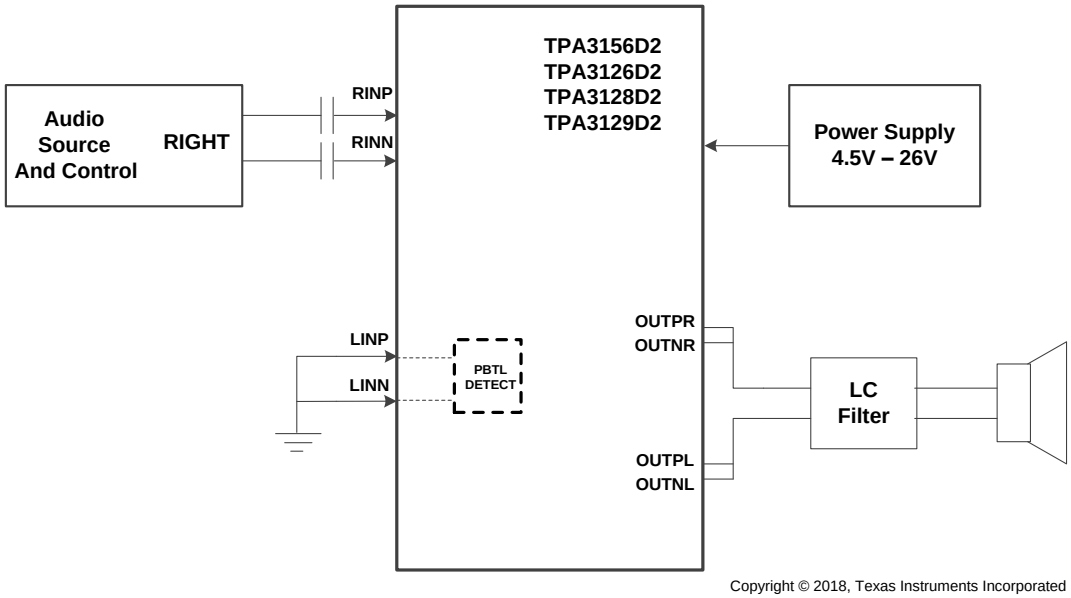


图 32. Mono PBTL Mode

Device Functional Modes (接下页)

8.4.2 Mono BTL Mode (Single Channel Mode)

The TPA3126D2 can be connected in mono BTL mode while cutting the idle power-loss nearly by half.

- Connect RINP and RINN directly to Ground (without capacitors), so the device is set in mono BTL mode during power up.
- Connect OUTPL to the positive speaker terminal, and OUTNL to the negative speaker terminal.
- Analog input signal is applied to LINP and LINN.

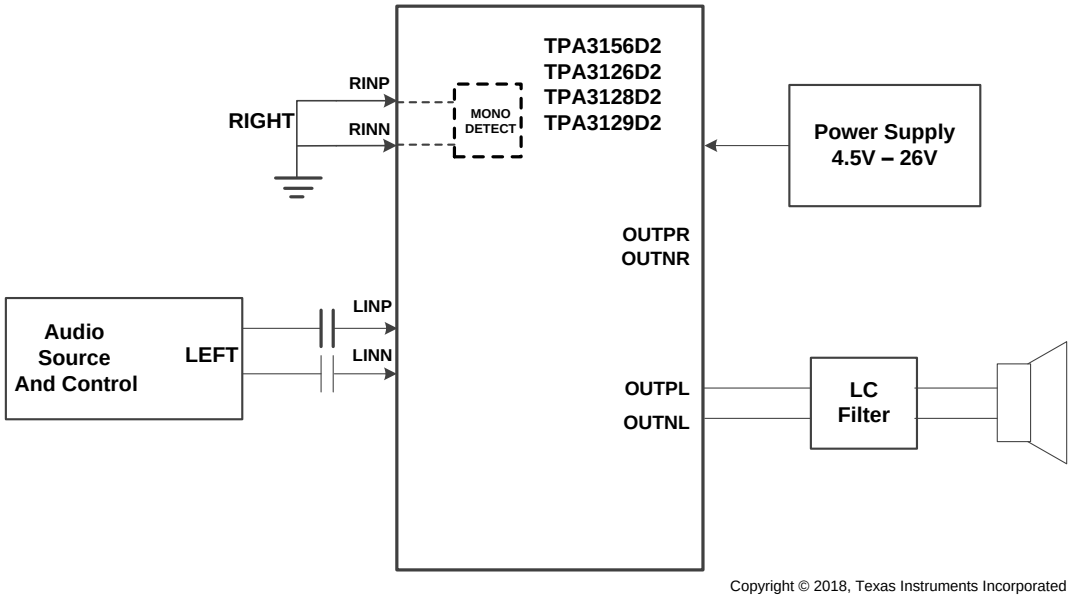


图 33. Mono BTL Mode

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Typical Application

This section describes a 2.1 Master and Slave application. The Master (U1 TPA3126D2) is configured as stereo BTL outputs with 400-kHz switching frequency and no power limit implemented, and the Slave (U2) is configured as a mono PBTL output. Both U1 and U2 are setup with a gain of 26-dB. Inputs are connected for differential inputs.

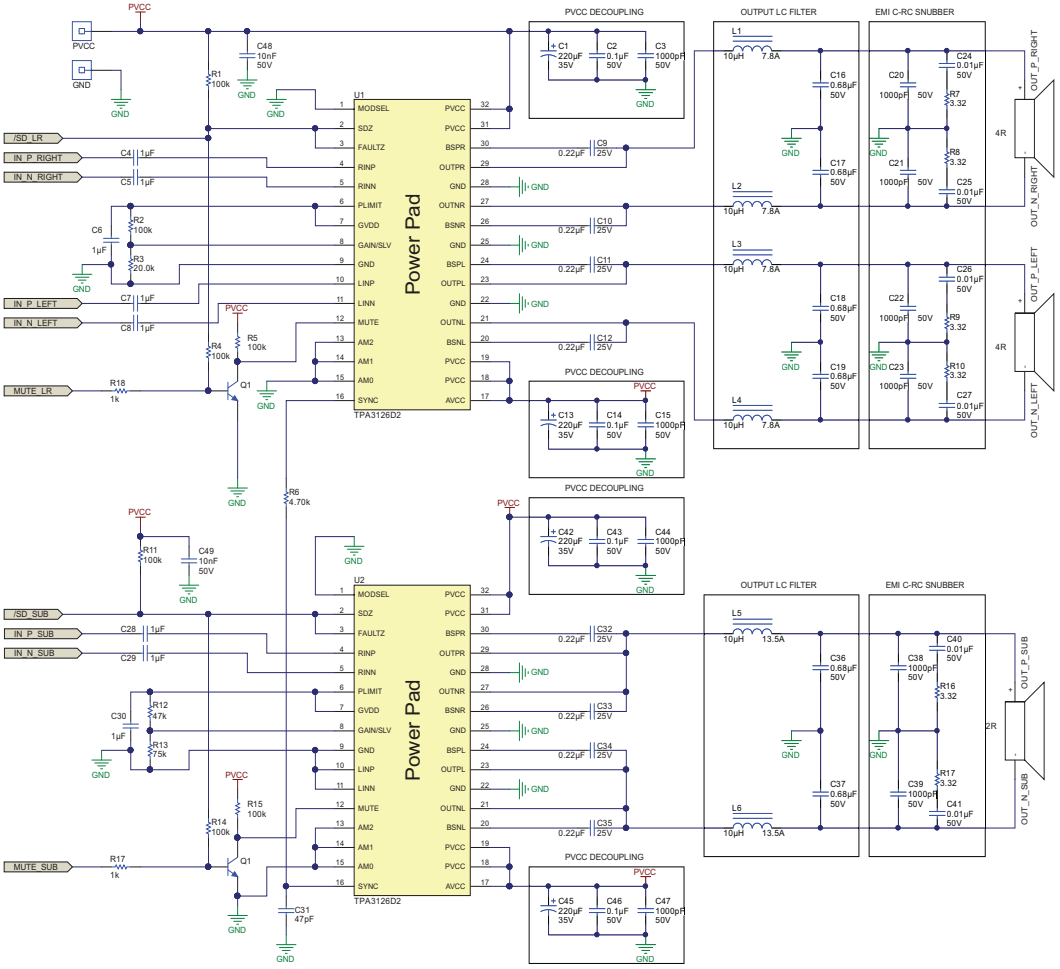


图 34. TPA3126D2 in a 2.1 Mode Application

Application Information (接下页)

9.1.1.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range PVCC	4.5 V to 26 V
PWM output frequencies	300kHz, 400 kHz, 500 kHz, 600 kHz, 1 MHz or 1.2 MHz
Maximum output power	2 × 50 W

9.1.1.2 Detailed Design Procedure

The TPA3126D2 devices are very flexible and easy-to-use Class D amplifiers; therefore, the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

- PVCC rail planned for the design
- Speaker or load impedance
- Maximum output power requirement
- Desired PWM frequency

9.1.1.2.1 Select the PWM Frequency

Set the PWM frequency by using AM0, AM1 and AM2 pins.

9.1.1.2.2 Select the Amplifier Gain and Master/Slave Mode

To select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once these parameters have been determined, calculate the required output voltage swing which delivers the maximum output power.

Choose the lowest analog gain setting that corresponds to produce an output voltage swing greater than the required output swing for maximum power. The analog gain and master/slave mode can be set by selecting the voltage divider resistors (R1 and R2) on the Gain/SLV pin.

9.1.1.2.3 Select Input Capacitance

Select the bulk capacitors at the PVCC inputs for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed power supply, two 100-μF, 50-V capacitors should be sufficient. One capacitor should be placed near the PVCC inputs at each side of the device. PVCC capacitors should be a low ESR type because they are being used in a fast-switching application.

9.1.1.2.4 Select Decoupling Capacitors

Good quality decoupling capacitors must be added at each of the PVCC inputs to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances.

9.1.1.2.5 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.22-μF, 25-V capacitors of X5R quality or better.

9.1.1.3 Application Curves

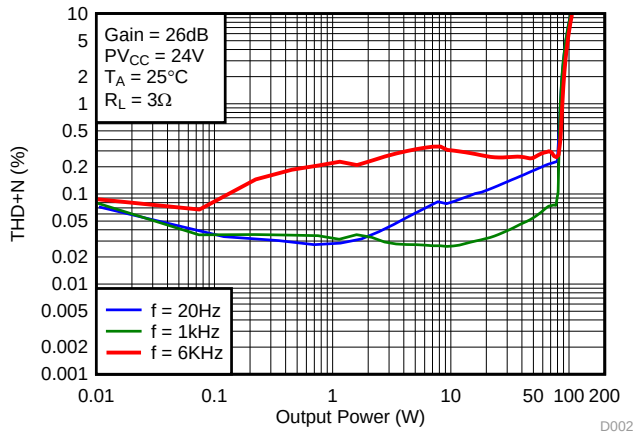


图 35. Total Harmonic Distortion + Noise (PBTL) vs Output Power

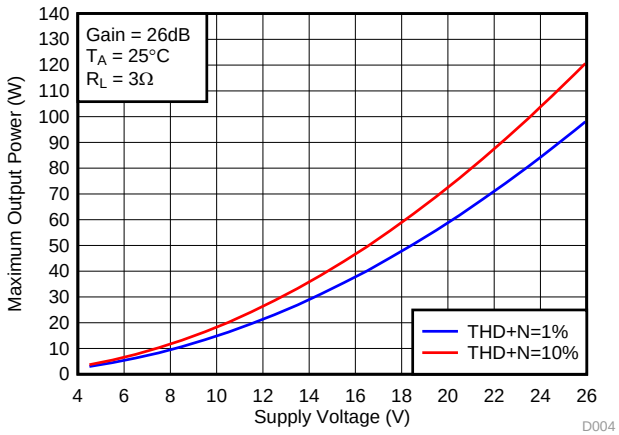


图 36. Maximum Output Power (PBTL) vs Supply Voltage

10 Power Supply Recommendations

The TPA3126D2 device requires an external power supply, between 4.5 V and 26 V, for the analog circuitry (AVCC) and the power stage (PVCC) of the amplifier. Several on-chip regulators are included on the TPA3126D2 to generate the voltages necessary for the internal circuitry of the audio path. The voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The AVCC supply feeds internal LDO including GVDD. This LDO output are connected to external pins for filtering purposes, but should not be connected to external circuits. GVDD LDO output have been sized to provide current necessary for internal functions but not for external loading.

10.1 Power Supply Mode

The TPA3126D2 supports both single and dual power supply modes. For dual power supply mode application, when AVCC is supplied with 4.5-V power, PVCC is recommended to be lower than 20 V. When PVCC is supplied with power greater than 20 V, AVCC is recommended to be higher than 6 V.

11 Layout

11.1 Layout Guidelines

The TPA3126D2 can be used with a small, inexpensive ferrite bead output filter in most applications. However, because the Class-D switching edges are fast, the layout of the printed circuit board must be planned carefully. The following suggestions helps to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (100-μF or greater) bulk power supply decoupling capacitors should be placed near the TPA3126D2 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220-pF and 1-nF, and a larger mid-frequency cap of value between 100-nF and 1-μF also of good quality to the PVCC connections at each end of the chip.
- Minimize the current loop from each of the outputs through the ferrite bead filter and back to GND. The size of this current loop determines its effectiveness as an antenna.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the TPA3126D2.
- Output filter — The ferrite EMI filter (see 图 31) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

For an example layout, see the TPA3126D2 Evaluation Module (TPA3126D2EVM) User Guide (SLOU506). Both the EVM user manual and the thermal pad application reports, SLMA002 and SLMA004, are available on the TI Web site at http://www.ti.com.

11.2 Layout Example

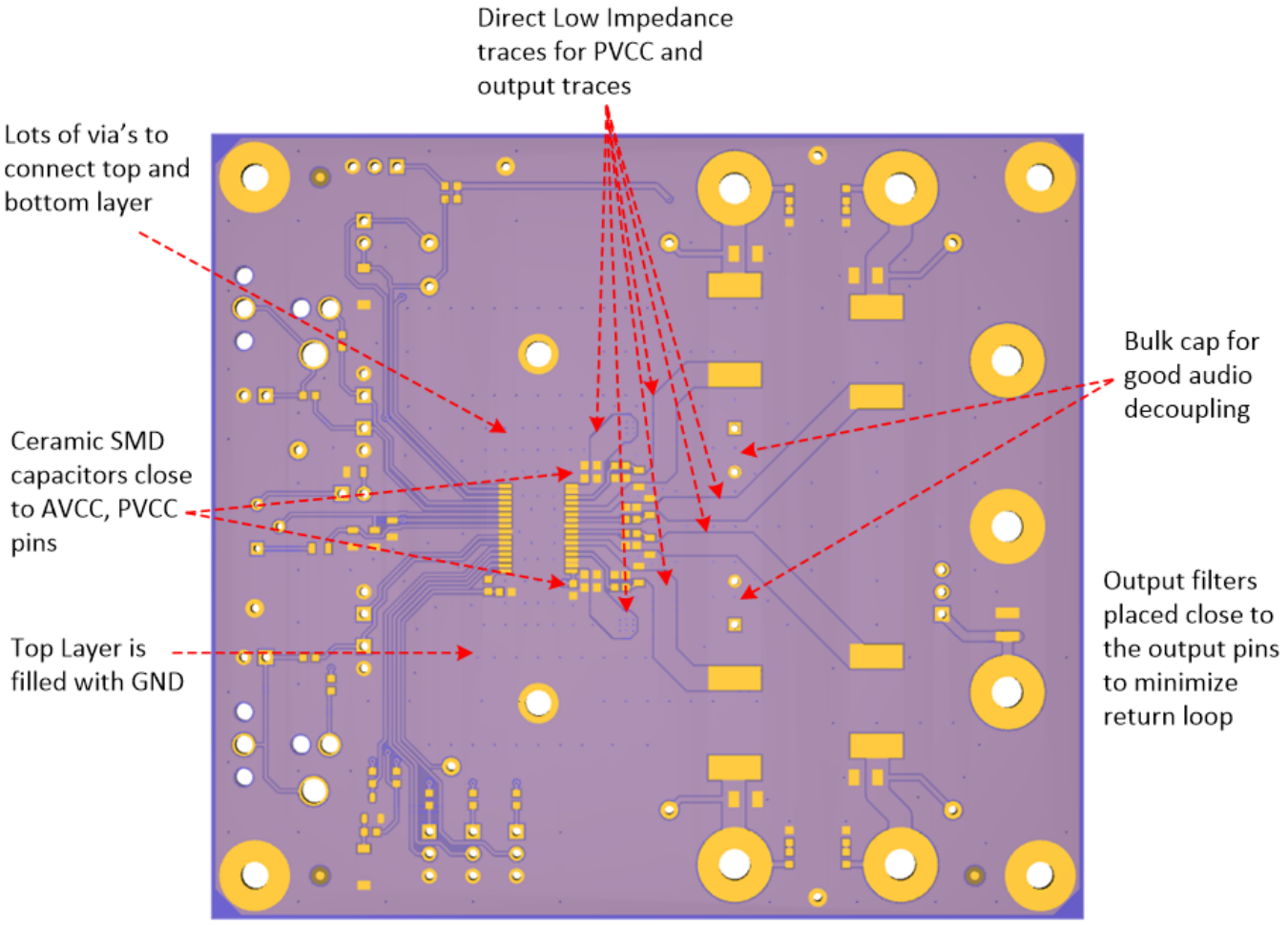


图 37. Layout Example Top

Layout Example (接下页)

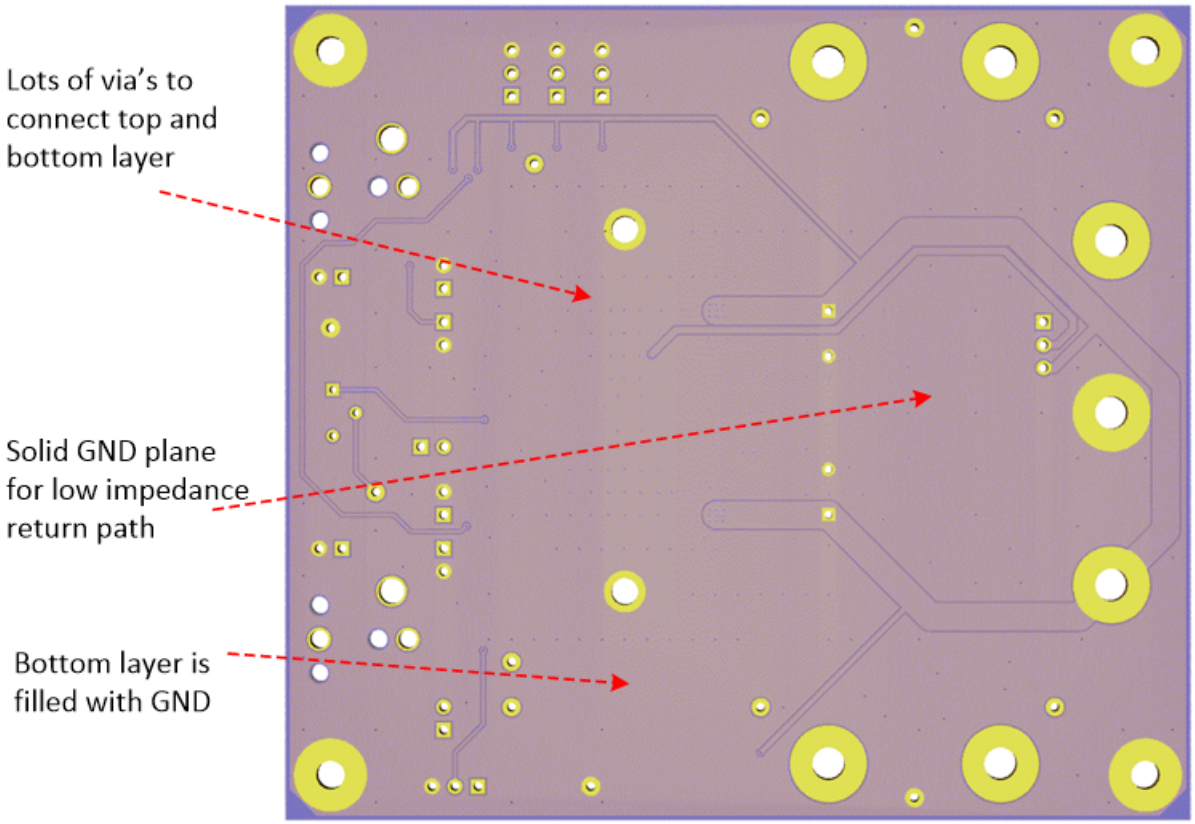


图 38. Layout Example Bottom

11.3 Heat Sink Used on the EVM

The heat sink (part number ATS-TI 10 OP-521-C1-R1) used on the EVM is an 14x25x50 mm extruded aluminum heat sink with three fins (see drawing below). For additional information on the heat sink, go to www.qats.com.

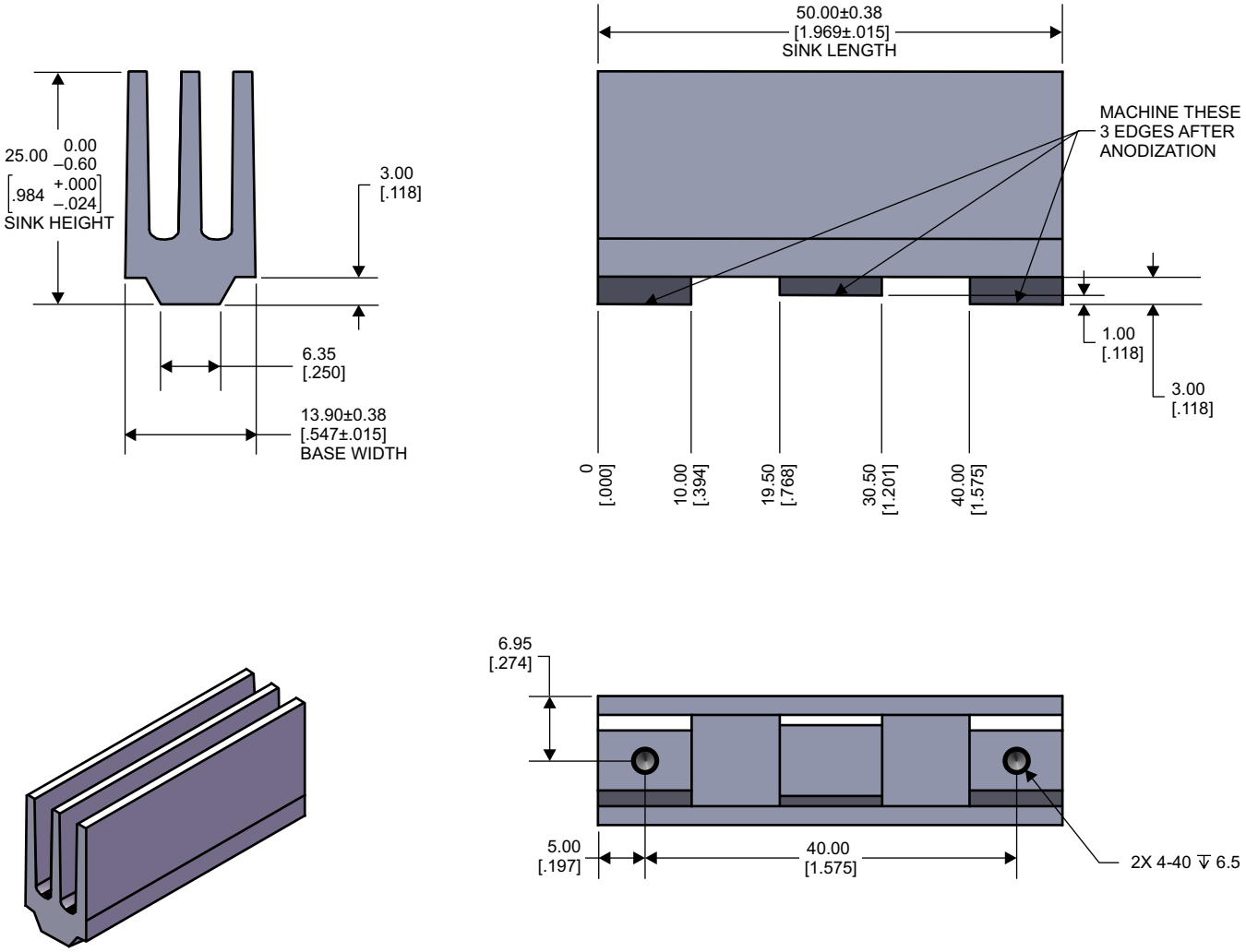


图 39. EVM Heat Sink

This size heat sink has shown to be sufficient for continuous output power. The crest factor of music and having airflow will lower the requirement for the heat sink size and smaller types can be used.

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

《TPA3126D2 评估模块用户指南》

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 相关文档

如需相关文档，请参阅：

- *《D 类音频放大器系统级保护概述》*
- *《借助 TPA3128D2 实现超低空闲电流》*

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3126D2DAD	ACTIVE	HTSSOP	DAD	32	46	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA 3126 D2	Samples
TPA3126D2DADR	ACTIVE	HTSSOP	DAD	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA 3126 D2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

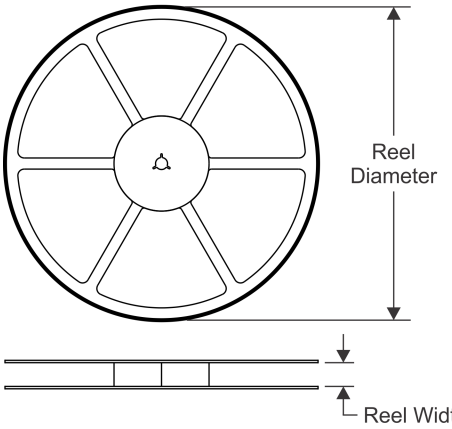
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

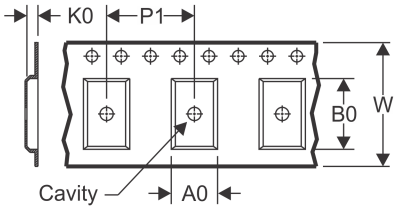
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

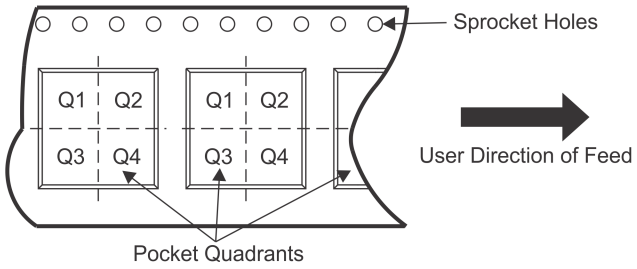


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

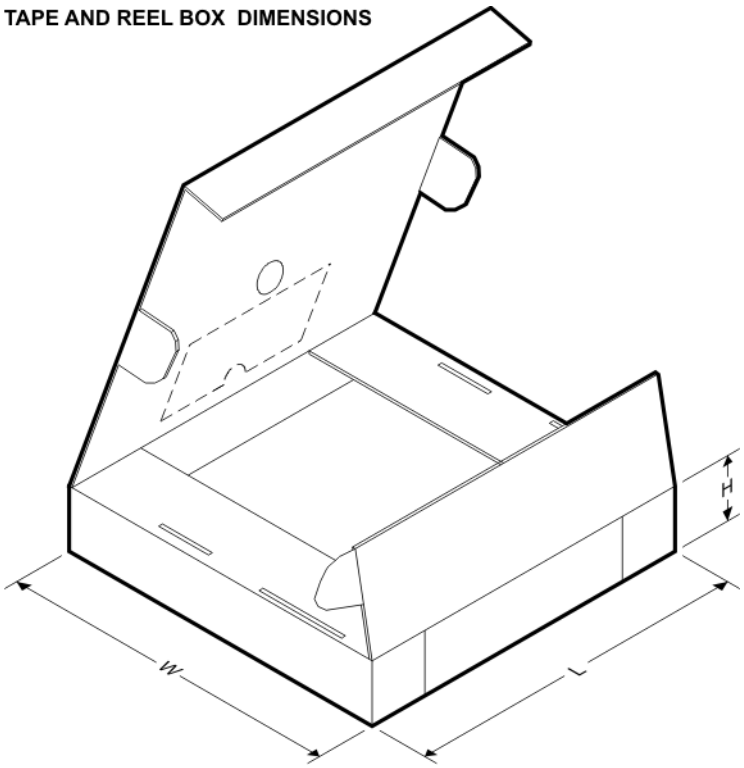
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3126D2DADR	HTSSOP	DAD	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

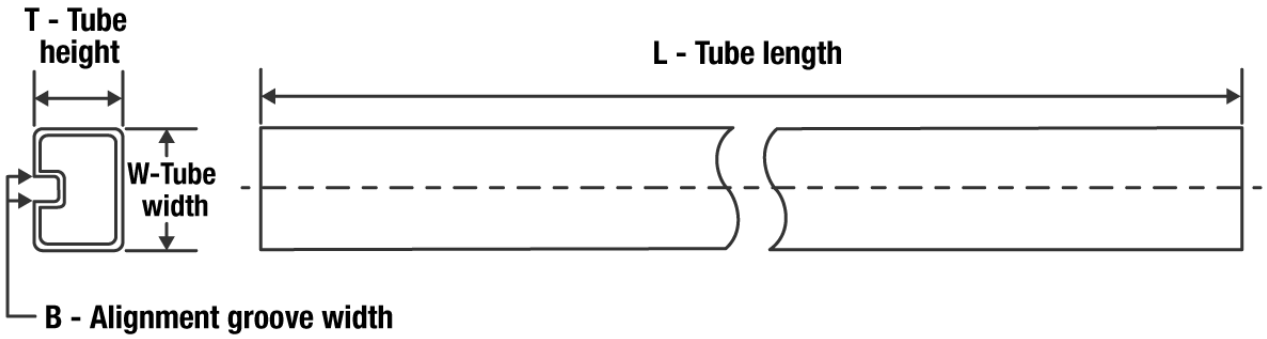
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3126D2DADR	HTSSOP	DAD	32	2000	350.0	350.0	43.0

TUBE

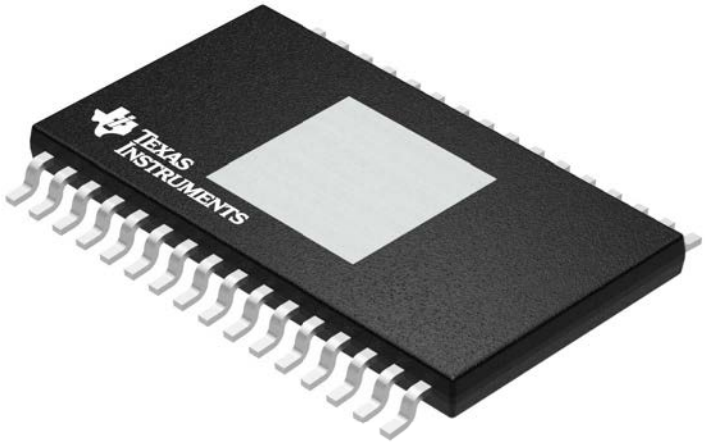


*All dimensions are nominal

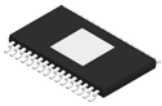
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3126D2DAD	DAD	HTSSOP	32	46	530	11.89	3600	4.9

DAD 32 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

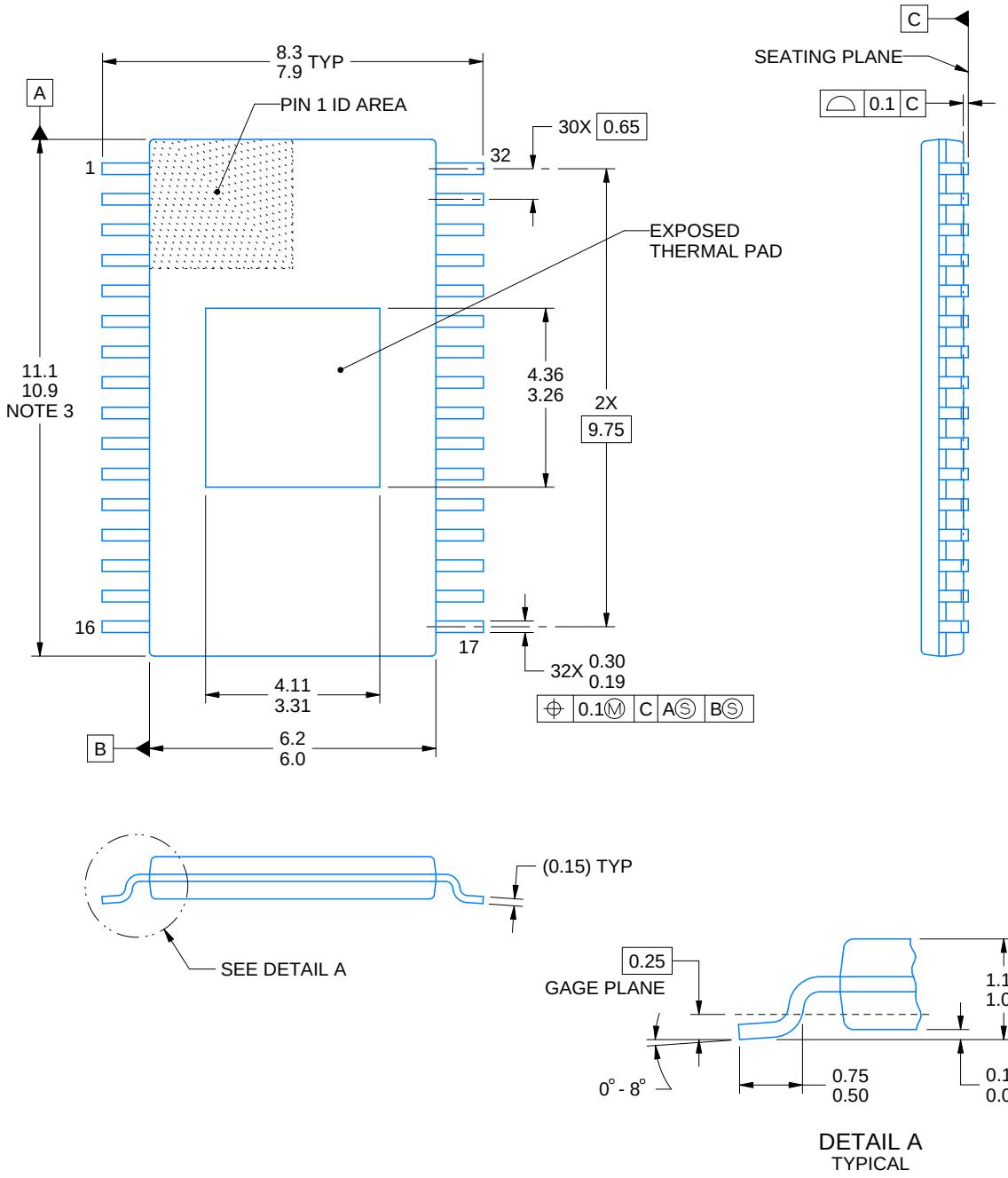


PACKAGE OUTLINE

DAD0032A

PowerPAD ™TSSOP - 1.15 mm max height

PLASTIC SMALL OUTLINE

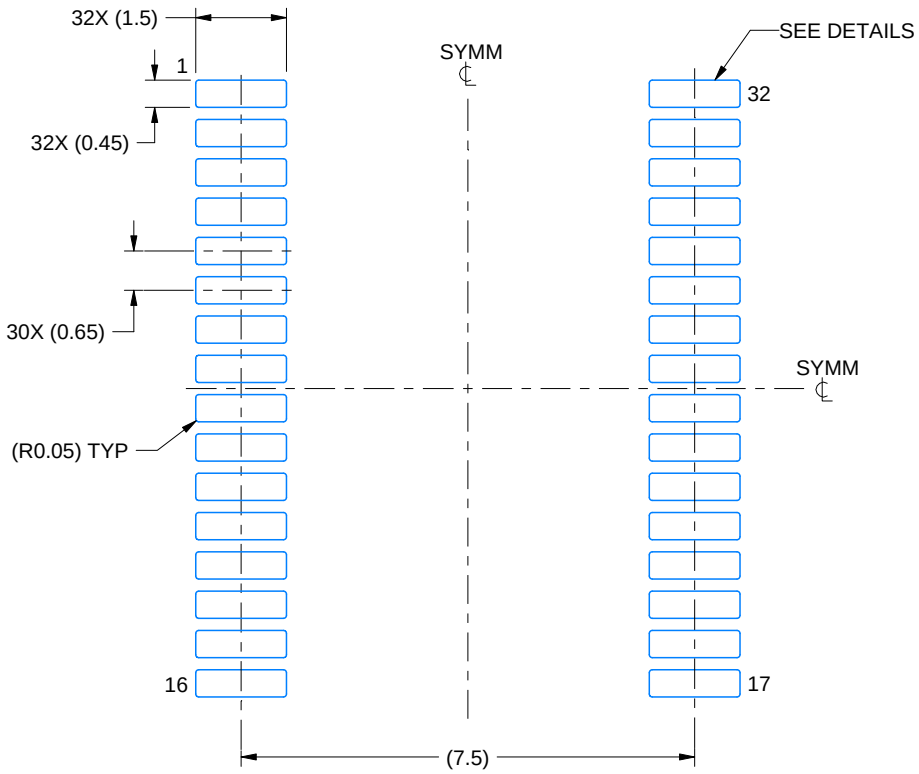


4222646/B 02/2020

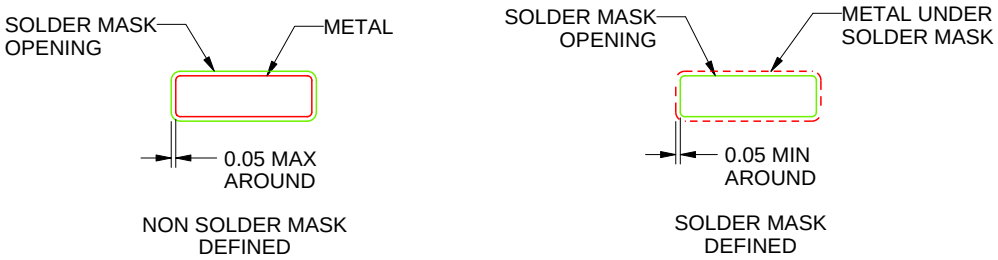
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:8X

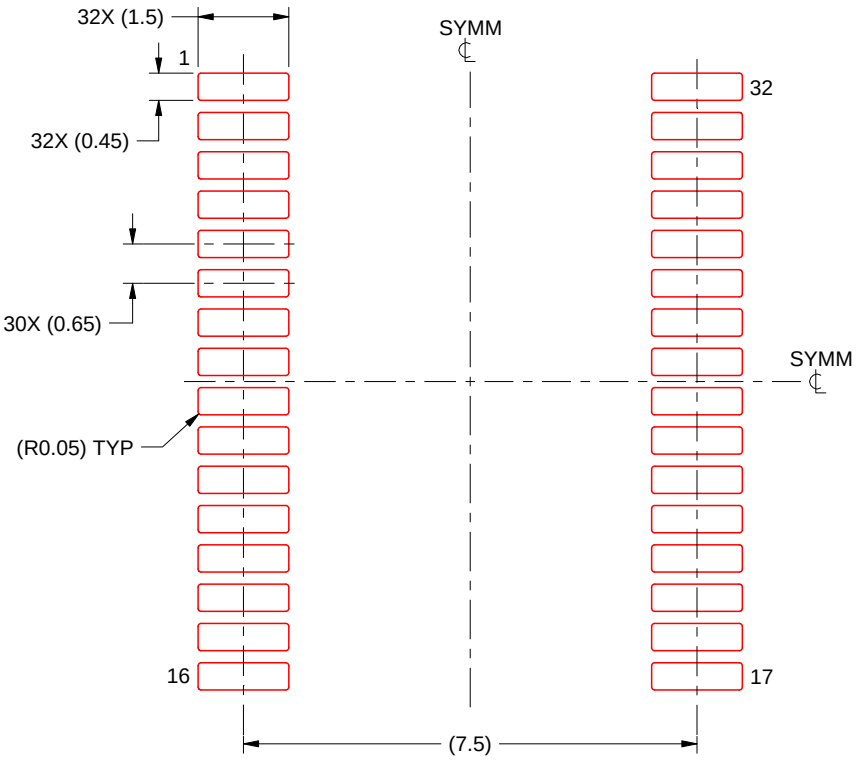


SOLDER MASK DETAILS
NOT TO SCALE

4222646/B 02/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4222646/B 02/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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