# LM3102 同步 1MHz 2.5A 降压稳压器

## 1 特性

- 低组件数量和小型解决方案尺寸
- 与陶瓷电容和其他低等效串联电阻 (ESR) 电容一起工作时可保持稳定
- 无需环路补偿
- 可通过断续导通模式 (DCM) 操作在轻负载条件下实现高效率
- 预偏置启动
- 超快速瞬态响应
- 可编程软启动
- 可编程开关频率高达 1MHz
- 谷值电流限值
- 输出过压保护
- 精密内部基准实现可调节输出电压低至 0.8V
- 热关断
- 主要技术规格
  - 输入电压范围为 4.5V 至 42V
  - 2.5A 输出电流
  - 0.8V，±1.5% 基准
  - 集成双 N 沟道主 MOSFET 和同步 MOSFET
  - 耐热增强型带散热片薄型小外形尺寸封装 (HTSSOP)-20 封装

## 2 应用

- 5VDC、12VDC、24VDC、12VAC 和 24VAC 系统
- 嵌入式系统和工业控制
- 汽车远程信息处理和车身电子装置
- 负载点稳压器
- 存储系统
- 宽带基础设施
- 直接对 2 节、3 节 和 4 节锂电池系统进行降压转换

## 3 说明

LM3102 同步整流降压转换器 采用 实现低成本高效率的降压稳压器所需的全部功能。该器件可为负载提供 2.5A 电流以及低至 0.8V 的输出电压。双 N 沟道同步 MOSFET 开关可减少组件数量，从而降低电路复杂度并最大限度地减小电路板尺寸。

LM3102 不同于大多数其他 COT 稳压器，因为它不依赖输出电容器 ESR 来获得稳定性，专为与陶瓷及其他 ESR 极低的输出电容器完美配合工作而设计。该器件无需环路补偿，可提供快速负载瞬态响应并实现简单电路。由于输入电压和导通时间之间呈反比关系，因此在线路发生变化时，器件的工作频率几乎保持恒定。通过外部编程，工作频率可高达 1MHz。

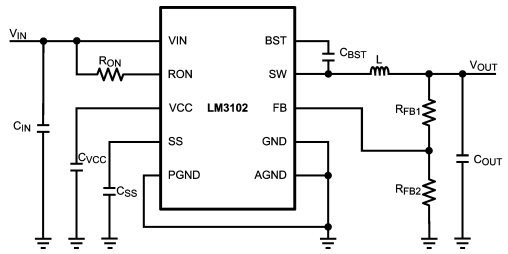
保护 特性 包括 $V_{CC}$ 欠压锁定 (UVLO)、输出过压保护、热关断和栅极驱动欠压锁定。LM3102 采用热增强型 HTSSOP-20 封装，而且 LM3102 还可以采用输出电流降低的 DSBGA 低厚度芯片级封装。

器件信息(1)

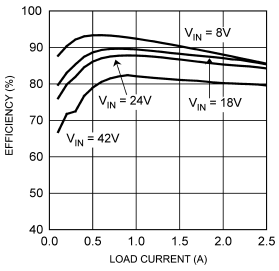
| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| LM3102 | DSBGA (28) | 3.645mm x 2.45mm |
| LM3102 | HTSSOP (20) | 6.50mm x 4.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用原理图




效率与负载电流间的关系 ($V_{OUT}$ = 3.3V)



# 目录



## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision H (June 2015) to Revision I** **Page**

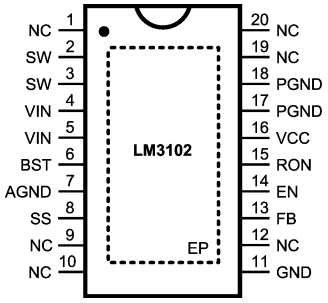
- 已更改 LM3102 和 LM3102-Q1 改为单独的数据表 ... 1

**Changes from Revision G (January 2012) to Revision H** **Page**

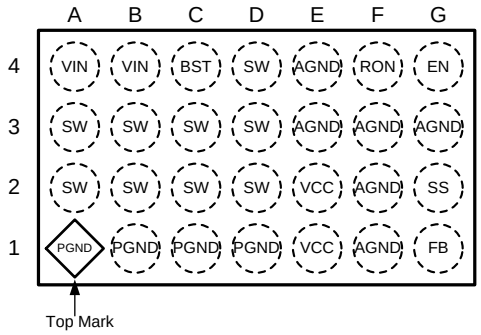
- 已将 LM3102Q 的部件号更新为 LM3102-Q1 ... 1
- 已添加 添加了*引脚配置和功能* 部分、*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施*部分、*电源建议* 部分、*布局*部分、*器件和文档支持*部分，以及*机械、封装和可订购信息*部分 ... 1

# 5 Pin Configuration and Functions

**PWP Package**
**20-Pin HTSSOP**
**Top View**




**YPA Package**
**28–Ball DSBGA**
**Top View**




**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | PIN NO. | BALL NO. | | |
| N/C | 1 | — | — | No Connection |
| | 9 | | | |
| | 10 | | | |
| | 12 | | | |
| | 19 | | | |
| | 20 | | | |
| SW | 2 | A2 | Power | Switching Node |
| | | A3 | | |
| | | B2 | | |
| | | B3 | | |
| | | C2 | | |
| | 3 | C3 | | |
| | | D2 | | |
| | | D3 | | |
| | | D4 | | |
| VIN | 4 | A4 | Power | Input supply voltage |
| | 5 | B4 | | |
| BST | 6 | C4 | Power | Connection for bootstrap capacitor |
| AGND | 7 | E3 | Ground | Analog Ground |
| | | E4 | | |
| | | F1 | | |
| | | F2 | | |
| | | F3 | | |
| | | G3 | | |
| SS | 8 | G2 | Analog | Soft-Start |
| GND | 11 | — | Ground | Ground |
| FB | 13 | G1 | Analog | Feedback |
| EN | 14 | G4 | Analog | Enable |
| RON | 15 | F4 | Analog | ON-time Control |
| VCC | 16 | E1 | Power | Start-up regulator Output |
| | | E2 | | |

**Pin Functions (continued)**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | PIN NO. | BALL NO. | | |
| PGND | 17 | A1 | Ground | Power Ground |
| | | B1 | | |
| | 18 | C1 | | |
| | | D1 | | |
| EP | EP | — | Ground | Exposed Pad |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| VIN, RON to AGND | –0.3 | 43.5 | V |
| SW to AGND | –0.3 | 43.5 | V |
| SW to AGND (Transient) | | –2 (< 100 ns) | V |
| VIN to SW | –0.3 | 43.5 | V |
| BST to SW | –0.3 | 7 | V |
| All Other Inputs to AGND | –0.3 | 7 | V |
| Junction Temperature, $T_J$ | | 150 | °C |
| Storage Temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage Range (VIN) | 4.5 | 42 | V |
| Junction Temperature Range ($T_J$) | −40 | 125 | °C |

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Ratings* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LM3102 PWP (HTSSOP) 20 PINS | LM3102 YPA (DSBGA) 28 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 30 | 50 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 6.5 | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

Specifications with standard type are for $T_J$ = 25°C unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN}$ = 18 V, $V_{OUT}$ = 3.3 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **START-UP REGULATOR, $V_{CC}$** | | | | | | | |
| $V_{CC}$ | $V_{CC}$ output voltage | $C_{CC}$ = 680 nF, no load | | | 6 | | V |
| | | | over the full Operating Junction Temperature ($T_J$) range | 5 | | 7.2 | |
| $V_{IN} – V_{CC}$ | $V_{IN} – V_{CC}$ dropout voltage | $I_{CC}$ = 2 mA | | | 50 | | mV |
| | | | over the full Operating Junction Temperature ($T_J$) range | | | 200 | |
| | | $I_{CC}$ = 20 mA | | | 350 | | |
| | | | over the full Operating Junction Temperature ($T_J$) range | | | 570 | |
| $I_{VCCL}$ | $V_{CC}$ current limit(1) | $V_{CC}$ = 0 V | | | 65 | | mA |
| | | | over the full Operating Junction Temperature ($T_J$) range | 40 | | | |
| $V_{CC-UVLO}$ | $V_{CC}$ undervoltage lockout threshold (UVLO) | $V_{IN}$ increasing | | | 3.75 | | V |
| | | | over the full Operating Junction Temperature ($T_J$) range | 3.6 | | 3.9 | |
| $V_{CC-UVLO-HYS}$ | $V_{CC}$ UVLO hysteresis | $V_{IN}$ decreasing – HTSSOP package | | | 130 | | mV |
| $V_{CC-UVLO-HYS}$ | $V_{CC}$ UVLO hysteresis | $V_{IN}$ decreasing – DSBGA package | | | 150 | | mV |
| $t_{VCC-UVLO-D}$ | $V_{CC}$ UVLO filter delay | | | | 3 | | µs |
| $I_{IN}$ | $I_{IN}$ operating current | No switching, $V_{FB}$ = 1 V | | | 0.7 | | mA |
| | | | over the full Operating Junction Temperature ($T_J$) range | | | 1 | |
| $I_{IN-SD}$ | $I_{IN}$ operating current, Device shutdown | $V_{EN}$ = 0 V | | | 25 | | µA |
| | | | over the full Operating Junction Temperature ($T_J$) range | | | 40 | |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $R_{DS-UP-ON}$ | Main MOSFET $R_{DS(on)}$ | | | | 0.18 | | Ω |
| | | over the full Operating Junction Temperature ($T_J$) range | | | | 0.375 | |
| $R_{DS-DN-ON}$ | Syn. MOSFET $R_{DS(on)}$ | | | | 0.11 | | Ω |
| | | over the full Operating Junction Temperature ($T_J$) range | | | | 0.225 | |
| $V_{G-UVLO}$ | Gate drive voltage UVLO | $V_{BST}$ - $V_{SW}$ increasing | | | 3.3 | | V |
| | | | over the full Operating Junction Temperature ($T_J$) range | | | 4 | |
| **SOFT-START** | | | | | | | |
| $I_{SS}$ | SS pin source current | $V_{SS}$ = 0.5 V | | | 8 | | µA |
| | | | over the full Operating Junction Temperature ($T_J$) range | 6 | | 10 | |

(1) $V_{CC}$ provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

## Electrical Characteristics (continued)

Specifications with standard type are for $T_J$ = 25°C unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN}$ = 18 V, $V_{OUT}$ = 3.3 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **CURRENT LIMIT** | | | | | | | |
| $I_{CL}$ | Syn. MOSFET current limit threshold | LM3102 | | | 2.7 | | A |
| $I_{CL}$ | Syn. MOSFET current limit threshold | LM3102TLX–1 | | | 1.5 | | A |
| **ON/OFF TIMER** | | | | | | | |
| $t_{on}$ | ON timer pulse width | $V_{IN}$ = 10 V, $R_{ON}$ = 100 kΩ | | | 1.38 | | µs |
| | | $V_{IN}$ = 30 V, $R_{ON}$ = 100 kΩ | | | 0.47 | | |
| $t_{on-MIN}$ | ON timer minimum pulse width | | | | 150 | | ns |
| $t_{off}$ | OFF timer pulse width | | | | 260 | | ns |
| **ENABLE INPUT** | | | | | | | |
| $V_{EN}$ | EN Pin input threshold | $V_{EN}$ rising | | | 1.18 | | V |
| | | | over the full Operating Junction Temperature ($T_J$) range | 1.13 | | 1.23 | |
| $V_{EN-HYS}$ | Enable threshold hysteresis | $V_{EN}$ falling | | | 90 | | mV |
| **REGULATION AND OVERVOLTAGE COMPARATOR** | | | | | | | |
| $V_{FB}$ | In-regulation feedback voltage | $V_{SS}$ ≥ 0.8 V<br>$T_J$ = −40°C to +125°C | | | 0.8 | | V |
| | | | over the full Operating Junction Temperature ($T_J$) range | 0.784 | | 0.816 | |
| | | $V_{SS}$ ≥ 0.8 V<br>$T_J$ = 0°C to +125°C | over the full Operating Junction Temperature ($T_J$) range | 0.788 | | 0.812 | |
| $V_{FB-OV}$ | Feedback overvoltage threshold | | | | 0.92 | | V |
| | | over the full Operating Junction Temperature ($T_J$) range | | 0.888 | | 0.945 | |
| $I_{FB}$ | | | | | 5 | | nA |
| **THERMAL SHUTDOWN** | | | | | | | |
| $T_{SD}$ | Thermal shutdown temperature | $T_J$ rising | | | 165 | | °C |
| $T_{SD-HYS}$ | Thermal shutdown temperature hysteresis | $T_J$ falling | | | 20 | | °C |

## 6.6 Typical Characteristics

All curves are taken at $V_{IN}$ = 18 V with the configuration in the typical application circuit for $V_{OUT}$ = 3.3 V shown in this data sheet. $T_A$ = 25°C, unless otherwise specified.

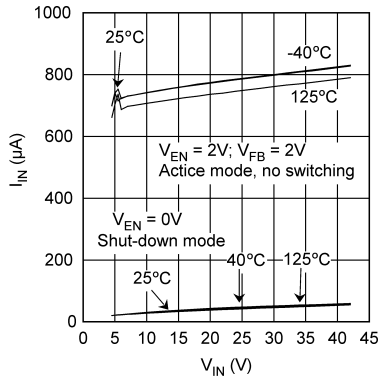



**Figure 1. Quiescent Current, $I_{IN}$ vs $V_{IN}$**

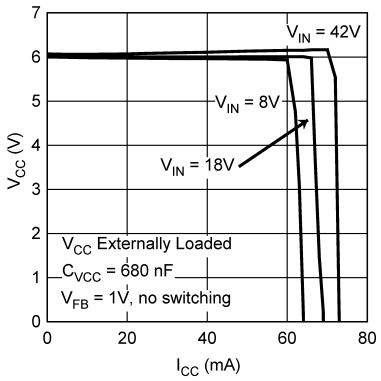



**Figure 2. $V_{CC}$ vs $I_{CC}$**

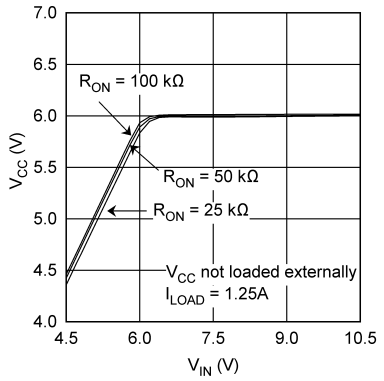



**Figure 3. $V_{CC}$ vs $V_{IN}$**

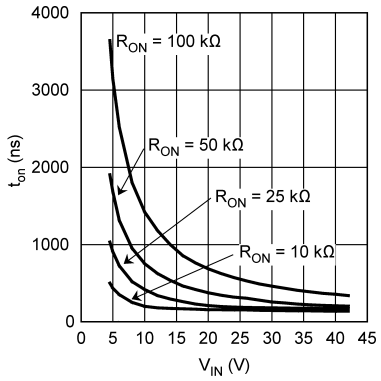



**Figure 4. $t_{on}$ vs $V_{IN}$**

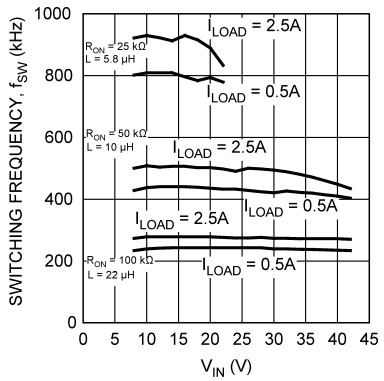



**Figure 5. Switching Frequency, $f_{SW}$ vs $V_{IN}$**

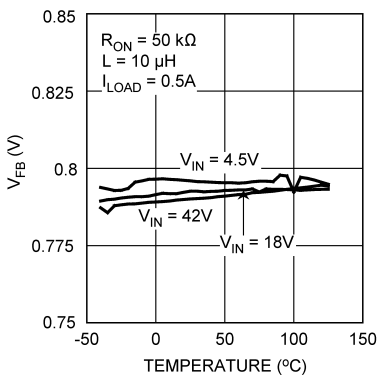



**Figure 6. $V_{FB}$ vs Temperature**

## Typical Characteristics (continued)

All curves are taken at $V_{IN}$ = 18 V with the configuration in the typical application circuit for $V_{OUT}$ = 3.3 V shown in this data sheet. $T_A$ = 25°C, unless otherwise specified.

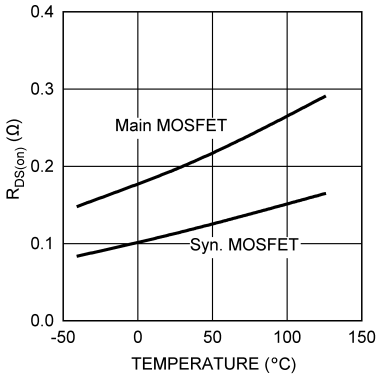



**Figure 7. $R_{DS(on)}$ vs Temperature**

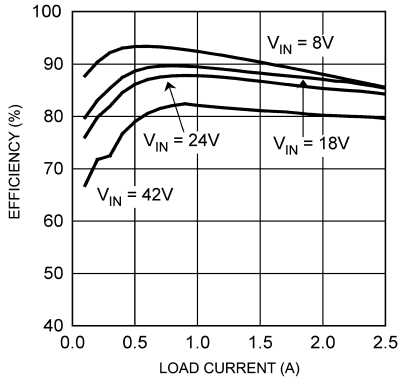



**Figure 8. Efficiency vs Load Current ($V_{OUT}$ = 3.3 V)**

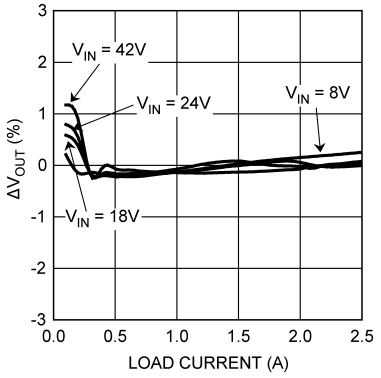



**Figure 9. $V_{OUT}$ Regulation vs Load Current ($V_{OUT}$ = 3.3 V)**

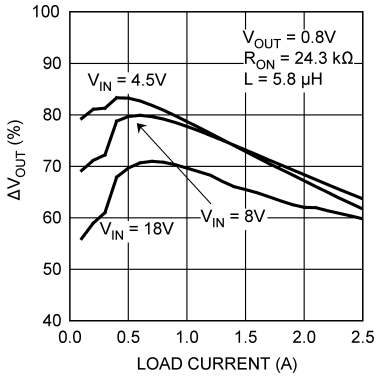



**Figure 10. Efficiency vs Load Current ($V_{OUT}$ = 0.8 V)**

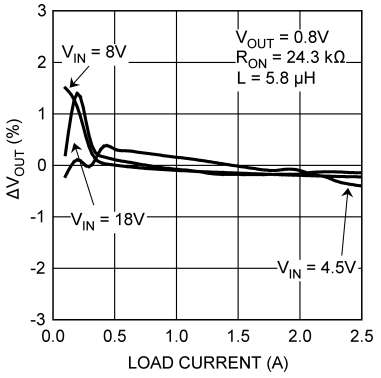



**Figure 11. $V_{OUT}$ Regulation vs Load Current ($V_{OUT}$ = 0.8 V)**

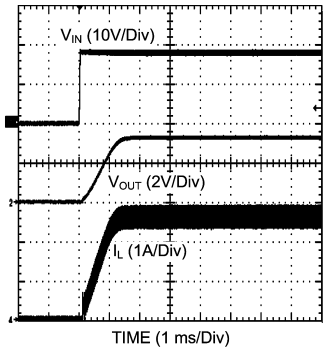



**Figure 12. Power Up ($V_{OUT}$ = 3.3 V, 2.5 A Loaded)**

## Typical Characteristics (continued)

All curves are taken at $V_{IN}$ = 18 V with the configuration in the typical application circuit for $V_{OUT}$ = 3.3 V shown in this data sheet. $T_A$ = 25°C, unless otherwise specified.

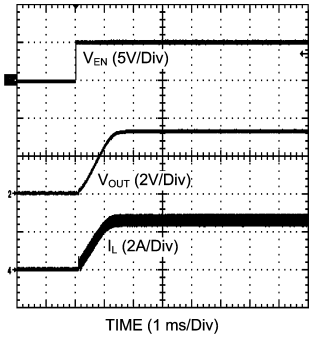



**Figure 13. Enable Transient ($V_{OUT}$ = 3.3 V, 2.5 A Loaded)**

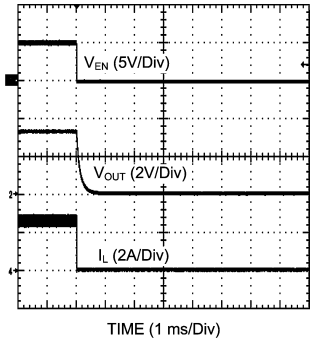



**Figure 14. Shutdown Transient ($V_{OUT}$ = 3.3 V, 2.5 A Loaded)**

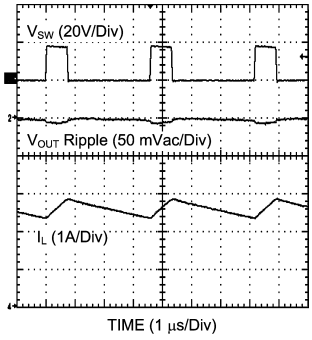



**Figure 15. Continuous Mode Operation ($V_{OUT}$ = 3.3 V, 2.5 A Loaded)**

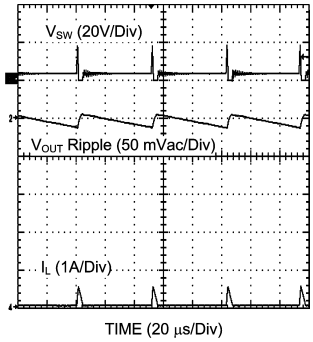



**Figure 16. Discontinuous Mode Operation ($V_{OUT}$ = 3.3 V, 0.025 A Loaded)**

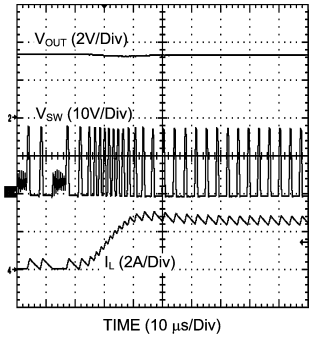



**Figure 17. DCM to CCM Transition ($V_{OUT}$ = 3.3 V, 0.15-A - 2.5-A Load)**

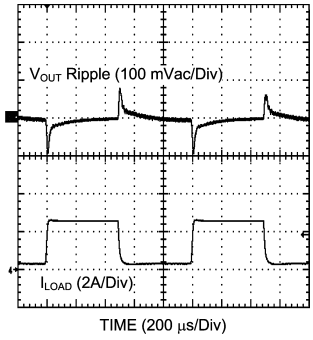



**Figure 18. Load Transient ($V_{OUT}$ = 3.3 V, 0.25-A - 2.5-A Load, Current Slew Rate: 2.5 A/µs)**

## Typical Characteristics (continued)

All curves are taken at $V_{IN}$ = 18 V with the configuration in the typical application circuit for $V_{OUT}$ = 3.3 V shown in this data sheet. $T_A$ = 25°C, unless otherwise specified.

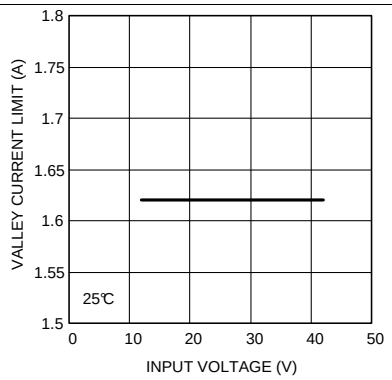



**Figure 19. DSBGA Valley Current Limit $V_{OUT}$ = 5 V at 25°C**

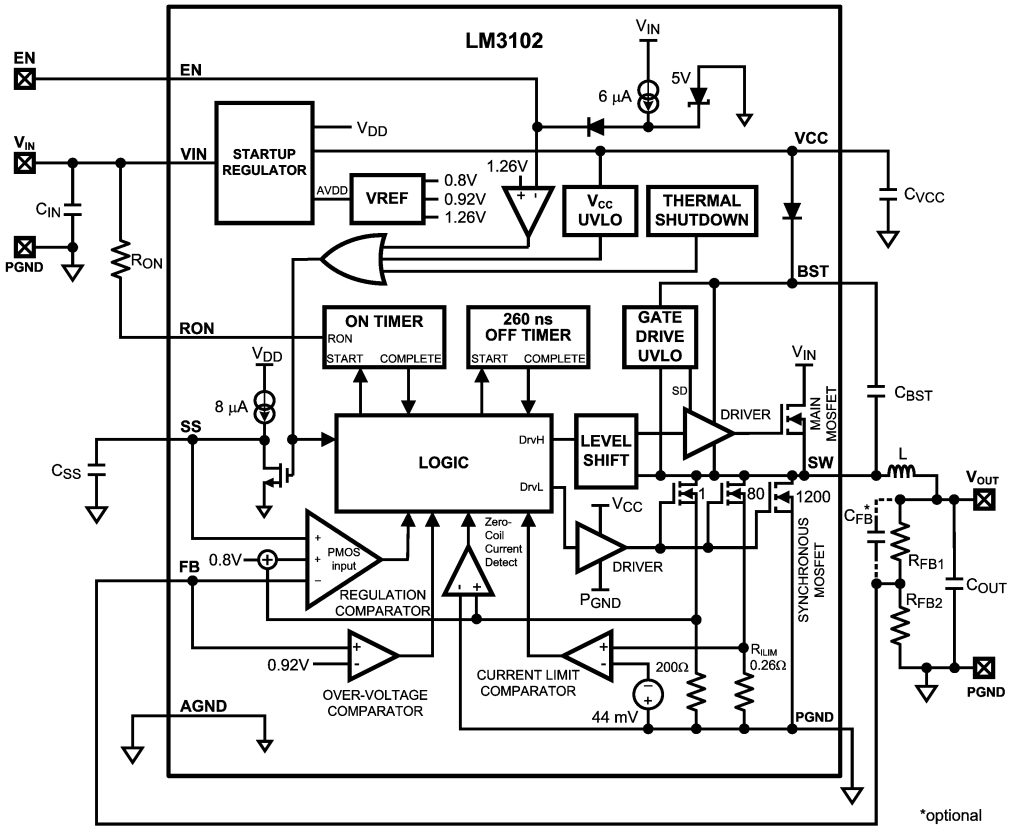
# 7 Detailed Description

## 7.1 Overview

The LM3102 Step-Down Switching Regulator features all required functions to implement a cost-effective, efficient buck power converter capable of supplying 2.5 A to a load. It contains Dual N-channel main and synchronous MOSFETs. The Constant ON-Time (COT) regulation scheme requires no loop compensation, results in fast load transient response and simple circuit implementation. The regulator can function properly even with an all ceramic output capacitor network, and does not rely on the ESR of the output capacitor for stability. The operating frequency remains constant with line variations due to the inverse relationship between the input voltage and the ON-time. The valley current limit detection circuit, with the limit set internally at 2.7 A, inhibits the main MOSFET until the inductor current level subsides.

The LM3102 can be applied in numerous applications and can operate efficiently for inputs as high as 42 V. Protection features include output overvoltage protection, thermal shutdown, $V_{CC}$ UVLO, gate drive UVLO. The LM3102 is available in the thermally enhanced HTSSOP-20 package.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 COT Control Circuit Overview

COT control is based on a comparator and a one-shot ON-timer, with the output voltage feedback (feeding to the FB pin) compared with an internal reference of 0.8 V. If the voltage of the FB pin is below the reference, the main MOSFET is turned on for a fixed ON-time determined by a programming resistor $R_{ON}$ and the input voltage $V_{IN}$, upon which the ON-time varies inversely. Following the ON-time, the main MOSFET remains off for a minimum of 260 ns. Then, if the voltage of the FB pin is below the reference, the main MOSFET is turned on again for another ON-time period. The switching will continue to achieve regulation.

## Feature Description (continued)

The regulator will operate in the discontinuous conduction mode (DCM) at a light load, and the continuous conduction mode (CCM) with a heavy load. In the DCM, the current through the inductor starts at zero and ramps up to a peak during the ON-time, and then ramps back to zero before the end of the OFF-time. It remains zero and the load current is supplied entirely by the output capacitor. The next ON-time period starts when the voltage at the FB pin falls below the internal reference. The operating frequency in the DCM is lower and varies larger with the load current as compared with the CCM. Conversion efficiency is maintained because conduction loss and switching loss are reduced with the reduction in the load and the switching frequency, respectively. The operating frequency in the DCM can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT} (V_{IN} - 1) \times L \times 1.18 \times 10^{20} \times I_{OUT}}{(V_{IN} - V_{OUT}) \times R_{ON}^2} \quad (1)$$

In the continuous conduction mode (CCM), the current flows through the inductor in the entire switching cycle, and never reaches zero during the OFF-time. The operating frequency remains relatively constant with load and line variations. The CCM operating frequency can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT}}{1.3 \times 10^{-10} \times R_{ON}} \quad (2)$$

The output voltage is set by two external resistors $R_{FB1}$ and $R_{FB2}$. The regulated output voltage is

$$V_{OUT} = 0.8V \times (R_{FB1} + R_{FB2})/R_{FB2} \quad (3)$$

### 7.3.2 Start-Up Regulator ($V_{CC}$)

A startup regulator is integrated within the LM3102. The input pin VIN can be connected directly to a line voltage up to 42 V. The $V_{CC}$ output regulates at 6 V, and is current limited to 65 mA. Upon power up, the regulator sources current into an external capacitor $C_{VCC}$, which is connected to the VCC pin. For stability, $C_{VCC}$ must be at least 680 nF. When the voltage on the VCC pin is higher than the UVLO threshold of 3.75 V, the main MOSFET is enabled and the SS pin is released to allow the soft-start capacitor $C_{SS}$ to charge.

The minimum input voltage is determined by the dropout voltage of the regulator and the $V_{CC}$ UVLO falling threshold (≅3.7 V). If $V_{IN}$ is less than ≅4.0 V, the regulator shuts off and $V_{CC}$ goes to zero.

### 7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to a 0.8-V internal reference. In normal operation (the output voltage is regulated), an ON-time period is initiated when the voltage at the FB pin falls below 0.8 V. The main MOSFET stays on for the ON-time, causing the output voltage and consequently the voltage of the FB pin to rise above 0.8 V. After the ON-time period, the main MOSFET stays off until the voltage of the FB pin falls below 0.8 V again. Bias current at the FB pin is nominally 5 nA.

### 7.3.4 Zero Coil Current Detect

The current of the synchronous MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operation, which improves the efficiency at a light load.

### 7.3.5 Overvoltage Comparator

The voltage at the FB pin is compared to a 0.92-V internal reference. If the voltage rises above 0.92 V, the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage or the output load changes suddenly. Once the OVP is activated, the main MOSFET remains off until the voltage at the FB pin falls below 0.92 V. The synchronous MOSFET will stay on to discharge the inductor until the inductor current reduces to zero, and then switch off.

## Feature Description (continued)

### 7.3.6 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the re-circulating current through the synchronous MOSFET. Referring to the *Functional Block Diagram*, when the main MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 2.7 A, the current limit comparator toggles, and as a result disabling the start of the next ON-time period. The next switching cycle starts when the re-circulating current falls back below 2.7 A (and the voltage at the FB pin is below 0.8V). The inductor current is monitored during the ON-time of the synchronous MOSFET. As long as the inductor current exceeds 2.7 A, the main MOSFET will remain inhibited to achieve current limit. The operating frequency is lower during current limit due to a longer OFF-time.

Figure 20 illustrates an inductor current waveform. On average, the output current $I_{OUT}$ is the same as the inductor current $I_L$, which is the average of the rippled inductor current. In case of current limit (the current limit portion of Figure 20), the next ON-time will not initiate until that the current drops below 2.7 A (assume the voltage at the FB pin is lower than 0.8 V). During each ON-time the current ramps up an amount equal to:

$$I_{LR} = \frac{(V_{IN} - V_{OUT}) \times t_{on}}{L} \quad (4)$$

During current limit, the LM3102 operates in a constant current mode with an average output current $I_{OUT(CL)}$ equal to 2.7 A + $I_{LR}$ / 2.

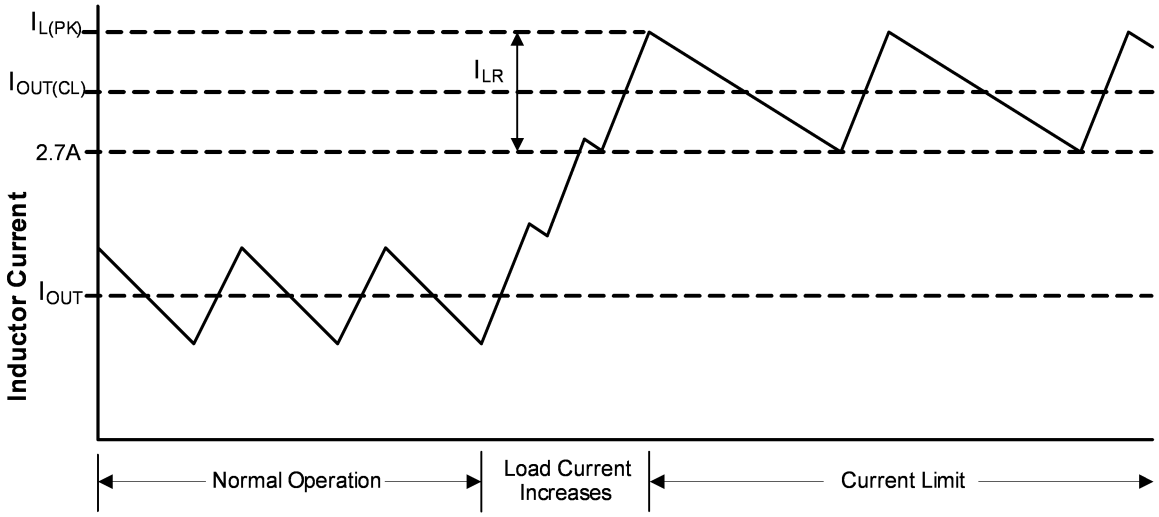



**Figure 20. Inductor Current - Current Limit Operation**

### 7.3.7 N-Channel MOSFET and Driver

The LM3102 integrates an N-channel main MOSFET and an associated floating high voltage main MOSFET gate driver. The gate drive circuit works in conjunction with an external bootstrap capacitor $C_{BST}$ and an internal high voltage diode. $C_{BST}$ connecting between the BST and SW pins powers the main MOSFET gate driver during the main MOSFET ON-time. During each OFF-time, the voltage of the SW pin falls to approximately –1 V, and $C_{BST}$ charges from $V_{CC}$ through the internal diode. The minimum OFF-time of 260 ns provides enough time for charging $C_{BST}$ in each cycle.

### 7.3.8 Soft-Start

The soft-start feature allows the converter to gradually reach a steady-state operating point, thereby reducing startup stresses and current surges. Upon turnon, after $V_{CC}$ reaches the undervoltage threshold, an 8-µA internal current source charges up an external capacitor $C_{SS}$ connecting to the SS pin. The ramping voltage at the SS pin (and the non-inverting input of the regulation comparator as well) ramps up the output voltage $V_{OUT}$ in a controlled manner.

## Feature Description (continued)

An internal switch grounds the SS pin if any of the following three cases happens: (i) $V_{CC}$ is below the UVLO threshold; (ii) a thermal shutdown occurs; or (iii) the EN pin is grounded. Alternatively, the output voltage can be shut off by connecting the SS pin to ground using an external switch. Releasing the switch allows the SS pin to ramp up and the output voltage to return to normal. The shutdown configuration is shown in Figure 21.

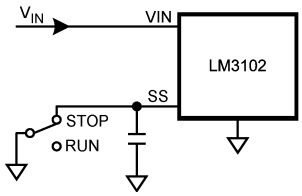



**Figure 21. Alternate Shutdown Implementation**

### 7.3.9 Thermal Protection

The junction temperature of the LM3102 should not exceed the maximum limit. Thermal protection is implemented by an internal Thermal Shutdown circuit, which activates (typically) at 165°C to make the controller enter a low power reset state by disabling the main MOSFET, disabling the ON-timer, and grounding the SS pin. Thermal protection helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20°C), the SS pin is released and normal operation resumes.

### 7.3.10 Thermal Derating

The LM3102 can supply 2.5 A below an ambient temperature of 100°C. Under worst-case operation, with either input voltage up to 42 V, operating frequency up to 1 MHz, or voltage of the RON pin below the absolute maximum of 7 V, the LM3102 can deliver a minimum of 1.9-A output current without thermal shutdown with a PCB ground plane copper area of 40 $cm^2$, 2 oz/Cu. Figure 22 shows a thermal derating curve for the minimum output current without thermal shutdown against ambient temperature up to 125°C. Obtaining 2.5-A output current is possible by increasing the PCB ground plane area, or reducing the input voltage or operating frequency.

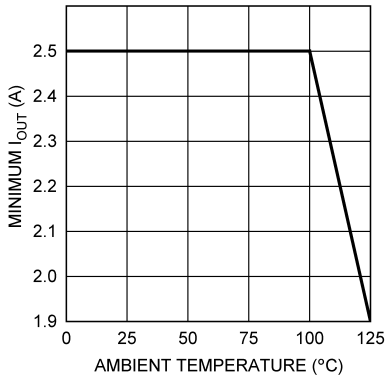



**Figure 22. Thermal Derating Curve**

## 7.4 Device Functional Modes

### 7.4.1 ON-Time Timer, Shutdown

The ON-time of the LM3102 main MOSFET is determined by the resistor $R_{ON}$ and the input voltage $V_{IN}$. It is calculated as follows:

$$t_{on} = \frac{1.3 \times 10^{-10} \times R_{ON}}{V_{IN}} \quad (5)$$

## Device Functional Modes (continued)

The inverse relationship of $t_{on}$ and $V_{IN}$ gives a nearly constant frequency as $V_{IN}$ is varied. $R_{ON}$ should be selected such that the ON-time at maximum $V_{IN}$ is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for $t_{on}$. This limits the maximum operating frequency, which is governed by Equation 6:

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \times 150\ ns} \quad (6)$$

The LM3102 can be remotely shutdown by pulling the voltage of the EN pin below 1 V. In this shutdown mode, the SS pin is internally grounded, the ON-timer is disabled, and bias currents are reduced. Releasing the EN pin allows normal operation to resume because the EN pin is internally pulled up.

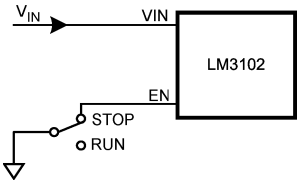



**Figure 23. Shutdown Implementation**

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LM3102 is a step-down DC-to-DC controller. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2.5 A. The following design procedure can be used to select components for the LM3102. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH® software uses iterative design procedure and accesses comprehensive databases of components. For more details, go to www.ti.com.

## 8.2 Typical Application

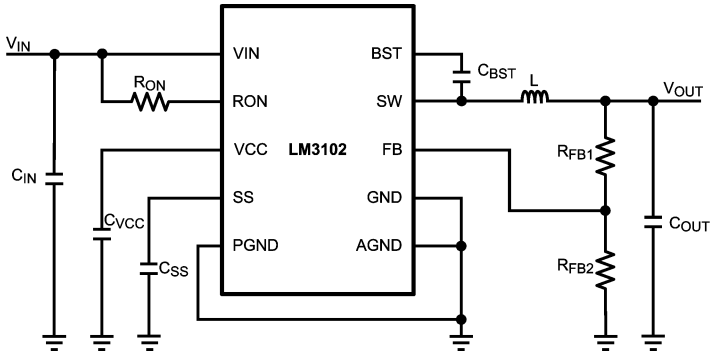



**Figure 24. Typical Application Schematic**

### 8.2.1 Design Requirements

For this example the following application parameters exist.

- $V_{IN}$ Range = 8 V to 42 V
- $V_{OUT}$ = 3.3 V
- $I_{OUT}$ = 2.5 A

Refer to *Detailed Design Procedure* for more information on operational guidelines and limits.

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Design Steps for the LM3102 Application*

The LM3102 is fully supported by WEBENCH which offers the following: component selection, electrical simulation, thermal simulation, as well as the build-it prototype board for a reduction in design time. The following list of steps can be used to manually design the LM3102 application.

1. Program $V_O$ with divider resistor selection.
2. Program turnon time with soft-start capacitor selection.
3. Select $C_O$.
4. Select $C_{IN}$.
5. Set operating frequency with $R_{ON}$.
6. Determine thermal dissipation.
7. Lay out PCB for required thermal performance.

## Typical Application (continued)

### 8.2.2.2 External Components

The following guidelines can be used to select external components.

**$R_{FB1}$ and $R_{FB2}$**: These resistors should be chosen from standard values in the range of 1.0 kΩ to 10 kΩ, satisfying the following ratio:

$$R_{FB1}/R_{FB2} = (V_{OUT}/0.8\ V) - 1 \quad (7)$$

For $V_{OUT}$ = 0.8 V, the FB pin can be connected to the output directly with a pre-load resistor drawing more than 20 µA. It is because the converter operation needs a minimum inductor current ripple to maintain good regulation when no load is connected.

**$R_{ON}$:** Equation 2 can be used to select $R_{ON}$ if a desired operating frequency is selected. But the minimum value of $R_{ON}$ is determined by the minimum ON-time. It can be calculated as follows:

$$R_{ON} \geq \frac{V_{IN(MAX)} \times 150\ ns}{1.3 \times 10^{-10}} \quad (8)$$

If $R_{ON}$ calculated from Equation 2 is smaller than the minimum value determined in Equation 8, a lower frequency should be selected to recalculate $R_{ON}$ by Equation 2. Alternatively, $V_{IN(MAX)}$ can also be limited to keep the frequency unchanged. The relationship of $V_{IN(MAX)}$ and $R_{ON}$ is shown in Figure 25.

On the other hand, the minimum OFF-time of 260 ns can limit the maximum duty ratio. Larger $R_{ON}$ should be selected in any application requiring large duty ratio.

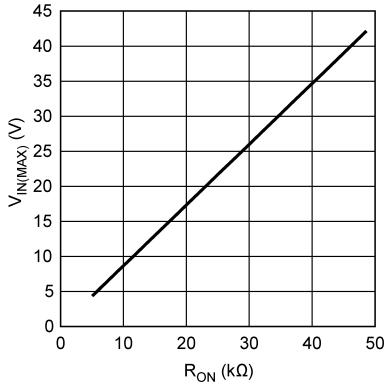



**Figure 25. Maximum $V_{IN}$ for Selected $R_{ON}$**

**L:** The main parameter affected by the inductor is the amplitude of inductor current ripple ($I_{LR}$). Once $I_{LR}$ is selected, L can be determined by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{LR} \times f_{SW} \times V_{IN}}$$

where

- $V_{IN}$ is the maximum input voltage
- $f_{SW}$ is determined from Equation 2

(9)

If the output current $I_{OUT}$ is determined, by assuming that $I_{OUT} = I_L$, the higher and lower peak of $I_{LR}$ can be determined. Beware that the higher peak of $I_{LR}$ should not be larger than the saturation current of the inductor and current limits of the main and synchronous MOSFETs. Also, the lower peak of $I_{LR}$ must be positive if CCM operation is required.

Figure 26 and Figure 27 show curves on inductor selection for various $V_{OUT}$ and $R_{ON}$. For small $R_{ON}$, according to (8), $V_{IN}$ is limited. Some curves are therefore limited as shown in the figures.

## Typical Application (continued)

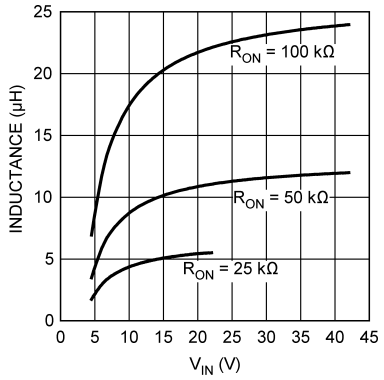



**Figure 26. Inductor Selection for $V_{OUT}$ = 3.3 V**

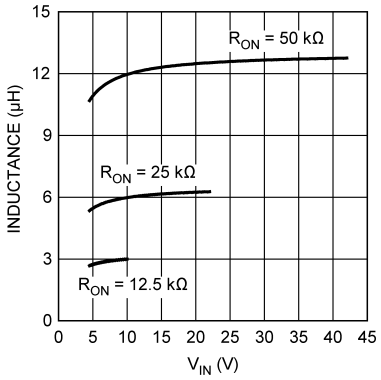



**Figure 27. Inductor Selection for $V_{OUT}$ = 0.8 V**

**$C_{VCC}$:** The capacitor on the $V_{CC}$ output provides not only noise filtering and stability, but also prevents false triggering of the $V_{CC}$ UVLO at the main MOSFET on/off transitions. $C_{VCC}$ should be no smaller than 680 nF for stability, and should be a good quality, low-ESR, ceramic capacitor.

**$C_{OUT}$ and $C_{OUT3}$:** $C_{OUT}$ should generally be no smaller than 10 µF. Experimentation is usually necessary to determine the minimum value for $C_{OUT}$, as the nature of the load may require a larger value. A load which creates significant transients requires a larger $C_{OUT}$ than a fixed load.

$C_{OUT3}$ is a small value ceramic capacitor located close to the LM3102 to further suppress high frequency noise at $V_{OUT}$. A 100-nF capacitor is recommended.

**$C_{IN}$ and $C_{IN3}$:** The function of $C_{IN}$ is to supply most of the main MOSFET current during the ON-time, and limit the voltage ripple at the VIN pin, assuming that the voltage source connecting to the VIN pin has finite output impedance. If the voltage source's dynamic impedance is high (effectively a current source), $C_{IN}$ supplies the average input current, but not the ripple current.

At the maximum load current, when the main MOSFET turns on, the current to the VIN pin suddenly increases from zero to the lower peak of the inductor's ripple current and ramps up to the higher peak value. It then drops to zero at turnoff. The average current during the ON-time is the load current. For a worst case calculation, $C_{IN}$ must be capable of supplying this average load current during the maximum ON-time. $C_{IN}$ is calculated from:

$$C_{IN} = \frac{I_{OUT} \times t_{on}}{\Delta V_{IN}}$$

where

- $I_{OUT}$ is the load current
- $t_{on}$ is the maximum ON-time
- $\Delta V_{IN}$ is the allowable ripple voltage at $V_{IN}$ (10)

The purpose of $C_{IN3}$ is to help avoid transients and ringing due to long lead inductance at the VIN pin. A low ESR 0.1-µF ceramic chip capacitor located close to the LM3102 is recommended.

**$C_{BST}$:** A 33-nF, high-quality ceramic capacitor with low ESR is recommended for $C_{BST}$ because it supplies a surge current to charge the main MOSFET gate driver at turnon. Low ESR also helps ensure a complete recharge during each OFF-time.

**$C_{SS}$:** The capacitor at the SS pin determines the soft-start time, that is, the time for the reference voltage at the regulation comparator and the output voltage to reach their final value. The time is determined from the following equation:

$$t_{SS} = \frac{C_{SS} \times 0.8V}{8\ \mu A} \quad (11)$$

**$C_{FB}$:** If the output voltage is higher than 1.6 V, $C_{FB}$ is needed in the Discontinuous Conduction Mode to reduce the output ripple. The recommended value for $C_{FB}$ is 10 nF.

## Typical Application (continued)

### 8.2.3 Application Curve

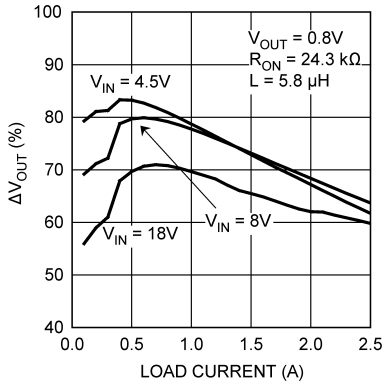



**Figure 28. Efficiency vs Load Current ($V_{OUT}$ = 0.8 V)**

## 8.3 System Examples

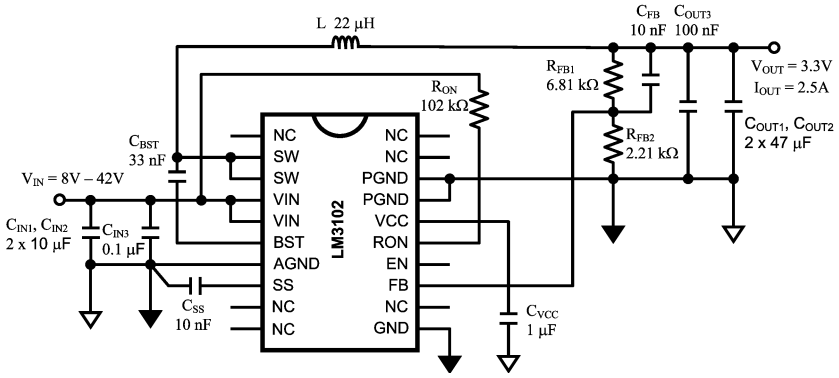



**Figure 29. Typical Application Schematic for $V_{OUT}$ = 3.3 V**

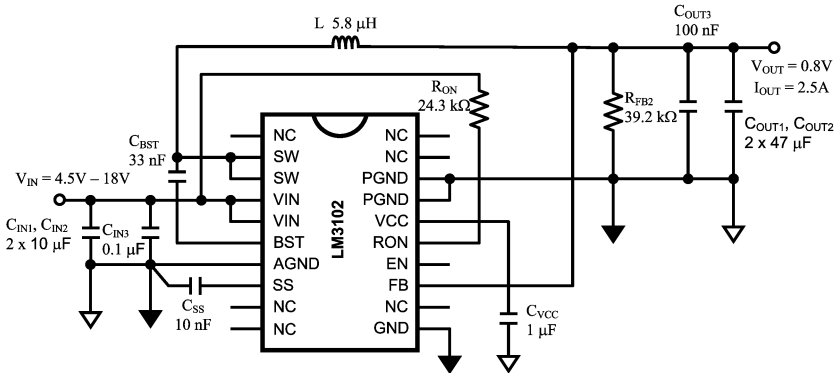



**Figure 30. Typical Application Schematic for $V_{OUT}$ = 0.8 V**

# 9 Power Supply Recommendations

The LM3102 device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LM3102 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LM3102, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

# 10 Layout

## 10.1 Layout Guidelines

The LM3102 regulation, overvoltage, and current limit comparators are very fast so they will respond to short duration noise pulses. Layout is therefore critical for optimum performance. It must be as neat and compact as possible, and all external components must be as close to their associated pins of the LM3102 as possible.

Refer to *Layout Example*, the loop formed by $C_{IN}$, the main and synchronous MOSFET internal to the LM3102, and the PGND pin should be as small as possible. The connection from the PGND pin to $C_{IN}$ should be as short and direct as possible. Vias should be added to connect the ground of $C_{IN}$ to a ground plane, located as close to the capacitor as possible. The bootstrap capacitor $C_{BST}$ should be connected as close to the SW and BST pins as possible, and the connecting traces should be thick. The feedback resistors and capacitor $R_{FB1}$, $R_{FB2}$, and $C_{FB}$ should be close to the FB pin.

A long trace running from $V_{OUT}$ to $R_{FB1}$ is generally acceptable because this is a low-impedance node. Ground $R_{FB2}$ directly to the AGND pin (pin 7). The output capacitor $C_{OUT}$ should be connected close to the load and tied directly to the ground plane. The inductor L should be connected close to the SW pin with as short a trace as possible to reduce the potential for EMI (electromagnetic interference) generation.

If it is expected that the internal dissipation of the LM3102 will produce excessive junction temperature during normal operation, making good use of the PCB ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the LM3102 IC package can be soldered to the ground plane, which should extend out from beneath the LM3102 to help dissipate heat.

The exposed pad is internally connected to the LM3102 IC substrate. Additionally the use of thick traces, where possible, can help conduct heat away from the LM3102. Using numerous vias to connect the die attached pad to the ground plane is a good practice. Judicious positioning of the PCB within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

## 10.2 Layout Example

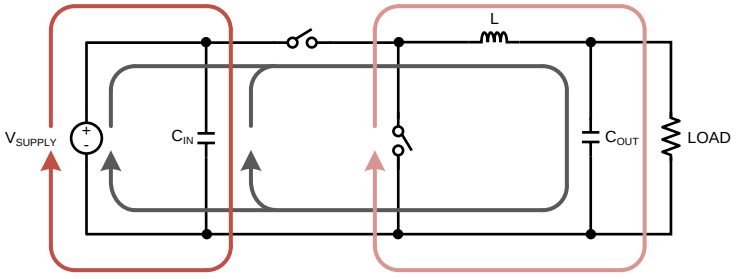



**Figure 31. Minimize Area of Current Loops in Buck Regulators**

## Layout Example (continued)

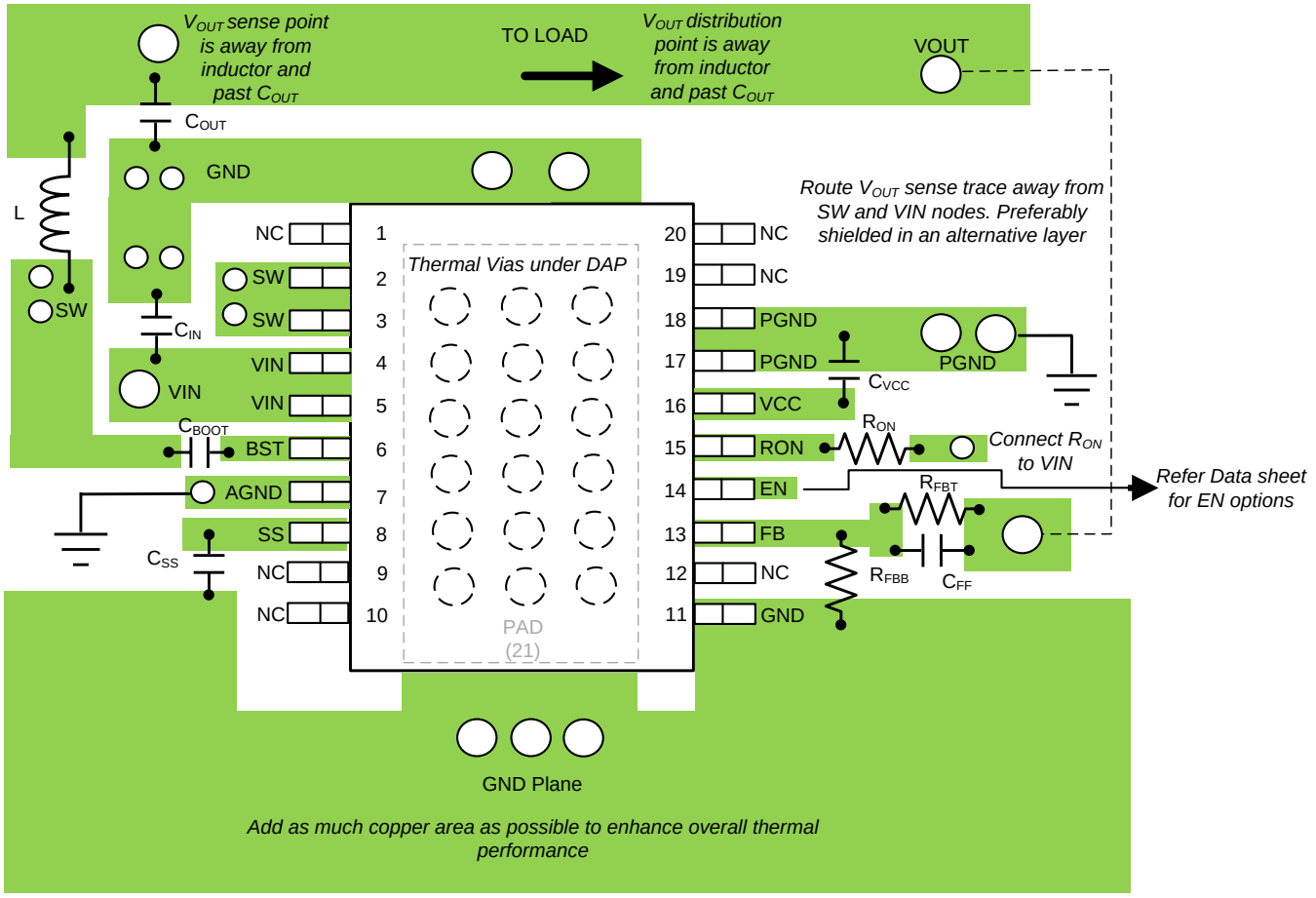



**Figure 32. PCB Layout Example - Top View**

# 11 器件和文档支持

## 11.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

**TI E2E™ 在线社区** ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

## 11.2 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

# 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3102MH/NOPB | ACTIVE | HTSSOP | PWP | 20 | 73 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LM3102 MH | Samples |
| LM3102MHX/NOPB | ACTIVE | HTSSOP | PWP | 20 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LM3102 MH | Samples |
| LM3102TL-1/NOPB | ACTIVE | DSBGA | YPA | 28 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | | 3102 | Samples |
| LM3102TLX-1/NOPB | ACTIVE | DSBGA | YPA | 28 | 1000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | | 3102 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

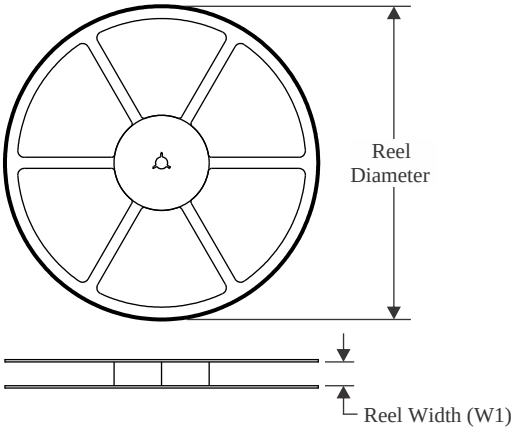
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

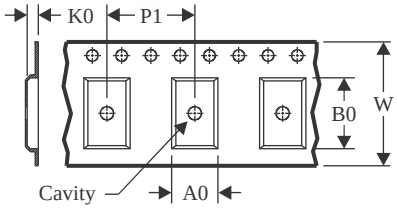
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

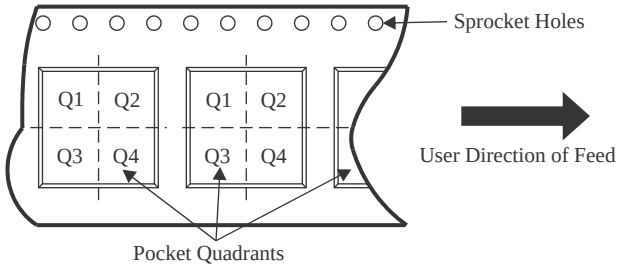



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

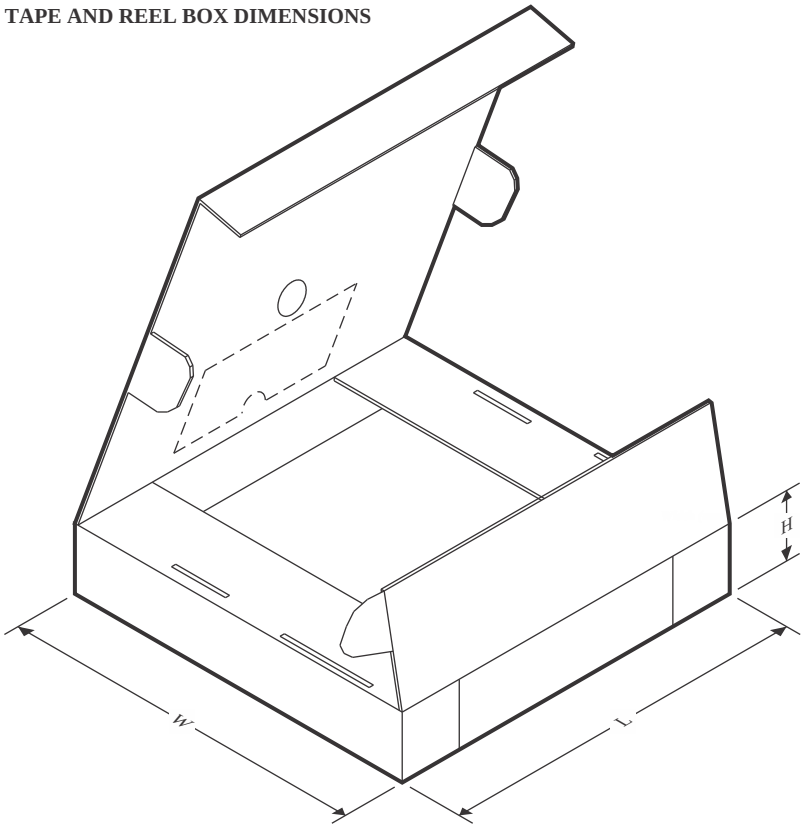
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3102MHX/NOPB | HTSSOP | PWP | 20 | 2500 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| LM3102TL-1/NOPB | DSBGA | YPA | 28 | 250 | 178.0 | 12.4 | 2.64 | 3.84 | 0.76 | 8.0 | 12.0 | Q1 |
| LM3102TLX-1/NOPB | DSBGA | YPA | 28 | 1000 | 178.0 | 12.4 | 2.64 | 3.84 | 0.76 | 8.0 | 12.0 | Q1 |

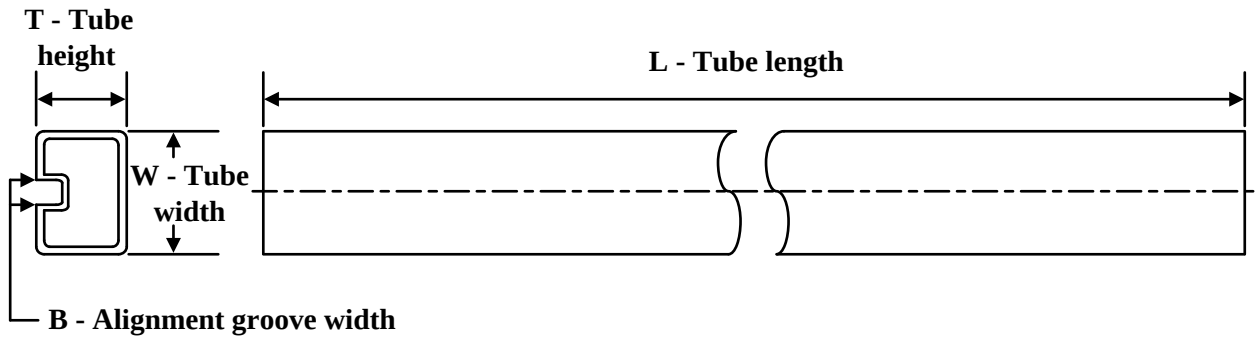
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM3102MHX/NOPB | HTSSOP | PWP | 20 | 2500 | 367.0 | 367.0 | 35.0 |
| LM3102TL-1/NOPB | DSBGA | YPA | 28 | 250 | 208.0 | 191.0 | 35.0 |
| LM3102TLX-1/NOPB | DSBGA | YPA | 28 | 1000 | 208.0 | 191.0 | 35.0 |

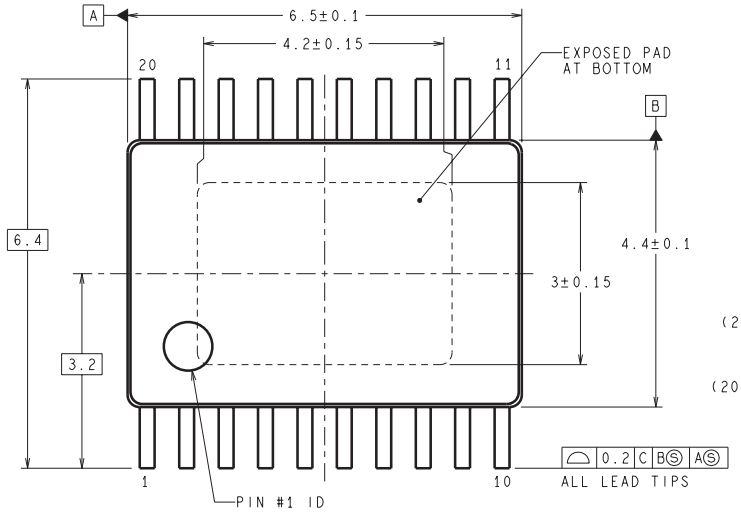
## TUBE

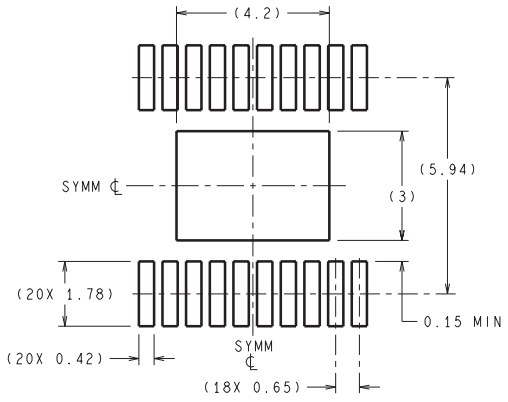



*All dimensions are nominal

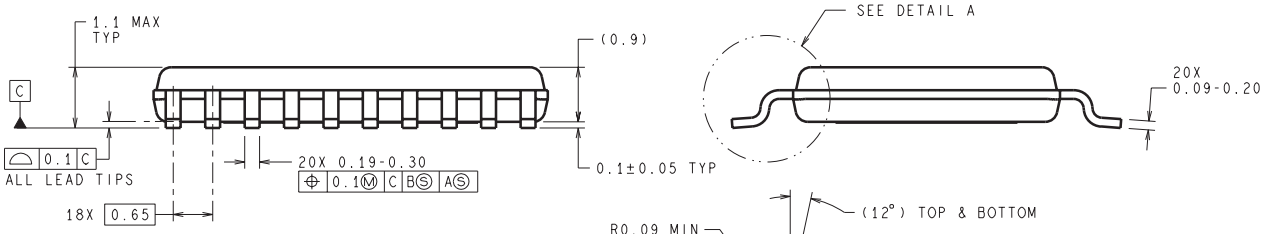
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM3102MH/NOPB | PWP | HTSSOP | 20 | 73 | 495 | 8 | 2514.6 | 4.06 |

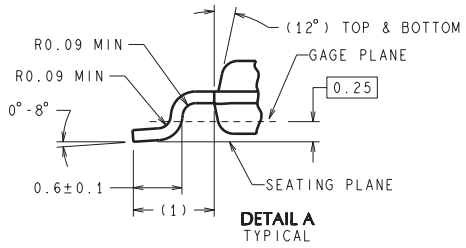
# PWP0020A




RECOMMENDED LAND PATTERN



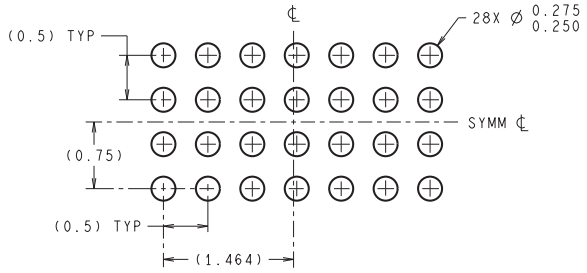




DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

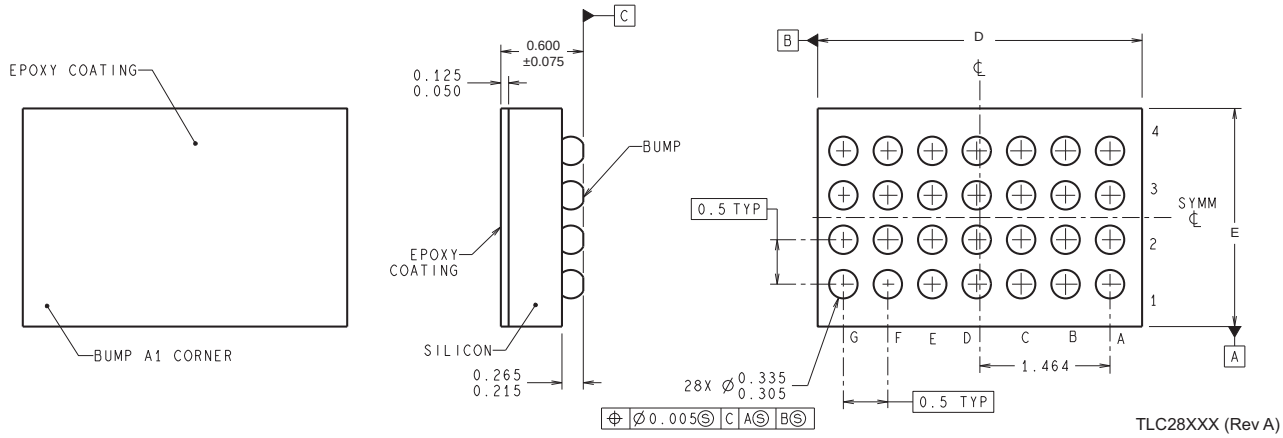
MXA20A (Rev C)

# YPA0028




LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY




TLC28XXX (Rev A)

D: Max = 3.676 mm, Min =3.615 mm

E: Max = 2.48 mm, Min = 2.419 mm

4215064/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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