

与 USB 完全兼容的完全集成双输入开关模式单节锂离子充电器和 USB-OTG 支持

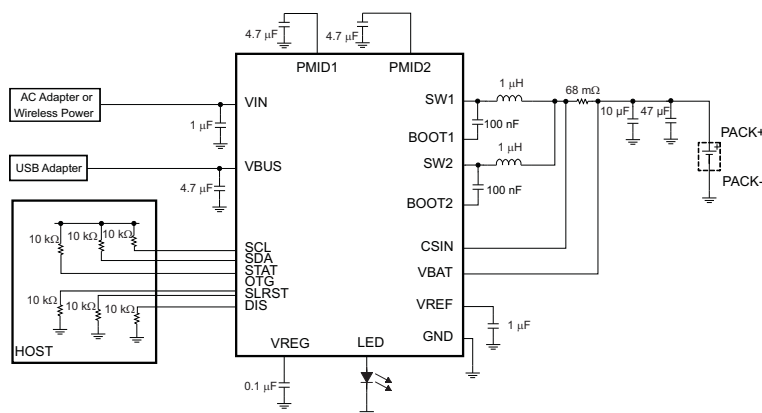
 查询样品: [bq24140](#)

特性

- 用于单节锂离子和锂聚合物电池组的高有效性迷你 **USB/AC** 电池充电器
- 在为电池充电的同时提供 **USB-OTG** 支持
- 高准确度电压和电流调节
 - 输入电流调节准确度: **±5% (100mA, 500mA)**
 - 充电电压调节准确度: **±0.5% (25°C), ±1% (0-125°C)**
 - 充电电流调节准确度: **±5%**
- 用于 **USB OTG** 的升压模式操作:
 - 输入电压范围 (电池供电): **2.3V to 4.5V**
 - **VBUS** 输出: **5.05V/500 mA**
- 基于动态电源管理的输入电压提供电流限制适配器的保护
- 故障适配器检测和抑制
- 通过限制最大充电电压和最大充电电流安全限制寄存器提供附加的安全
- **20-V** 绝对最大输入电压等级
- **9.0-V** 最大工作输入电压
- 比线性充电器更快的充电
- 内置输入电流感应和限制
- 集成了功率 **FET**, 充电率高达 **1.5A**
- 经 **I²C** 接口 (高达 **3.4 Mbps**) 设定的可编程充电参数:
 - 输入电流
 - 快速充电/终止电流
 - 充电电压 (**3.5-4.44V**)
 - 具有重置控制的安全定时器
 - 具有重置控制的安全定时器
 - 终止使能
- 同步固定频率 **PWM** 控制器工作在 **3 MHz**, 占空比 **0% 至 99.5%**
- 用于低功耗的自动高阻抗模式
- 强健的保护
 - 反向漏电保护防止电池漏电
 - 热调整及保护
 - 输入/输出过压保护
- 充电和故障的状态输出
- **USB** 友好型启动序列
- **2.35 × 2.65 mm 30-引脚 WCSP** 封装

应用

- 手机与智能电话
- **MP3** 播放器
- 手持式设备



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



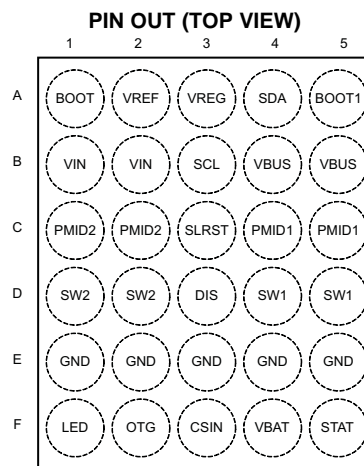
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

说明

bq24140 是一款紧凑、灵活、高效、USB 友好的开关模式充电管理设备，此设备适用于广泛便携式应用中使用的单节锂离子和锂聚合物电池。可通过 I²C 接口对充电参数进行编程。此 IC 集成了两个将同步 PWM 控制器、功率 MOSFET、输入电流感应、高精度电流和电压调节以及充电终止功能集成到一个小型 WCSP 封装中。

电池充电发生于以下三个阶段：调节、恒定电流和恒定电压。输入电流值由主机自动限制。当达到用户可选最低电流水平时，充电被终止。具有重置控制的安全定时器为 I²C 接口提供安全备份。在正常操作下，如果电池电压降低到低于内部阈值的时候，IC 自动重启充电周期，当输入供电被移除时，IC 自动进入睡眠模式或者高阻抗模式。可使用 I²C 接口将充电状态报告给主机。在充电过程中，IC 监视它的结点温度 (T_J) 并且一旦 T_J 增加到 125°C 典型值，IC 将降低充电电流。为了支持 USB OTG 设备，IC 能通过对电池电压升压来提供 VBUS (典型值 5.05V)。此 IC 采用 30-引脚 WCSP 封装。

DEVICE INFORMATION



PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|-------|---------|-----|---|
| NAME | NO. | | |
| BOOT | A1 | O | Boot-strapped capacitor for the high-side MOSFET gate driver. Connect a 100nF ceramic capacitor (voltage rating above 10V) from BOOT pin to SW2 pin. |
| VREF | A2 | O | Internal bias regulator voltage. Connect a 1μF ceramic capacitor from this output to PGND. |
| VREG | A3 | O | Voltage regulator. 2.5V with 10mA current capability. Connect a 0.1μF ceramic capacitor to ground |
| SDA | A4 | I/O | I ² C interface data. Connect a 10-kΩ pull-up resistor to 1.8V rail. |
| BOOT1 | A5 | O | Boot-strapped capacitor for the high-side MOSFET gate driver. Connect a 100nF ceramic capacitor (voltage rating above 10V) from BOOT1 pin to SW1 pin. |
| VIN | B1 – B2 | I | Charger input voltage. Bypass it with a 1μF ceramic capacitor from VIN to GND. |
| SCL | B3 | I | I ² C interface clock. Connect a 10-kΩ pull-up resistor to 1.8V rail. |
| VBUS | B4 – B5 | I/O | Charger input voltage. Bypass it with a 4.7μF ceramic capacitor from VBUS to GND. This pin also provides the output of the boost converter when in Boost Mode. |
| PMID2 | C1 – C2 | O | Connection point between reverse blocking FET and high-side switching FET. Bypass it with a minimum of 3.3μF capacitor from PMID2 to GND. |
| SLRST | C3 | I | Safety limit register control. When SLRST = 0, all the safety limit values are reset to default values, regardless of the write actions to the safety limits registers. When SLRST = 1, the host can program the safety limits register until any write action to other registers locks the programmed safety limits. |

PIN FUNCTIONS (continued)

| PIN | | I/O | DESCRIPTION |
|-------|---------|-----|---|
| NAME | NO. | | |
| PMID1 | C4 – C5 | O | Connection point between reverse blocking FET and high-side switching FET. Bypass it with a minimum of 3.3µF capacitor from PMID1 to GND. |
| SW2 | D1 – D2 | O | Internal switch to output inductor connection. |
| DIS | D3 | I | Charge disable control pin. DIS=0, charge is enabled. DIS=1, charge is disabled. VIN and VBUS pins are high impedance to PGND. In 15min mode, DIS=1 will reset the 15min timer; while in 32s mode, DIS=1 will NOT reset the 32-second timer. |
| SW1 | D4 – D5 | O | Internal switch to output inductor connection. |
| GND | E1 – E5 | | Ground pins. |
| LED | F1 | O | High side LED driver. Current, on and off times can be programmed through I2C to select different modes. |
| OTG | F2 | I | Boost mode enable control and VBUS input current limiting selection pin. When OTG is in active status per the control register, VBUS converter will be forced to operate in boost mode. It has higher priority over I ² C control and can be disabled through control register. The polarity of OTG active status can also be controlled. At POR, the OTG control register is ignored and the OTG pin is used as the input current limiting selection pin for VBUS converter. When OTG=High, IIN_LIMIT=500mA and when OTG=Low, IIN_LIMIT=100mA. |
| CSIN | F3 | I | Charge current-sense input. Battery current is sensed via the voltage drop across an external sense resistor. A 0.1µF ceramic capacitor to GND is required. |
| VBAT | F4 | I | Battery voltage and current sense input. Bypass it with a ceramic capacitor (minimum 0.1µF) to GND if there are long inductive leads to battery. |
| STAT | F5 | O | Charge status pin. Pull low when charge in progress. Open drain for other conditions. During faults, a 128µS pulse is sent out. STAT pin can be disabled by the EN_STAT bit in control register. STAT can be used to drive a LED or communicate with a host processor. |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | | UNIT |
|---|--|-------|--------------------|------|
| | | MIN | MAX | |
| Supply voltage range (with respect to GND) | VBUS, VIN | -2 | 20 | V |
| Input voltage range (with respect to and GND) | SCL, SDA, OTG, CSIN, VREG, VBAT, SLRST, DIS, LED | -0.3 | 7 | V |
| Output voltage range (with respect to and GND) | PMID1, PMID2, STAT | -0.3 | 20 | V |
| | VREF | | 6.5 | |
| | BOOT, BOOT1 | -0.7 | 20 | |
| | SW1, SW2 | -0.7 | 12 | |
| Voltage difference between CSIN and VBAT inputs (VCSIN -VBAT) | | | ±7 | V |
| Output sink | STAT | | 10 | mA |
| Output current (average) | SW1, SW2 | | 1.5 ⁽²⁾ | A |
| T _A | Operating free-air temperature range | -30 | +85 | °C |
| T _J | Junction temperature range | -40 | +125 | °C |
| T _{stg} | Storage temperature | -45 | +150 | °C |
| ESD Rating ⁽³⁾ | Human body model at all pins | ±2000 | | V |
| | Machine model | ±100 | | |
| | Charge device model | ±500 | | |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Duty cycle for output current should be less than 50% for 10- year life time when output current is above 1.25A

(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | bq24140 | | UNITS |
|-------------------------------|--|--------------|--|-------|
| | | WCSP PACKAGE | | |
| | | 30 PINS | | |
| θ_{JA} | Junction-to-ambient thermal resistance | 79.5 | | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance | 0.3 | | |
| θ_{JB} | Junction-to-board thermal resistance | 44.4 | | |
| ψ_{JT} | Junction-to-top characterization parameter | 0.3 | | |
| ψ_{JB} | Junction-to-board characterization parameter | 44.4 | | |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance | n/a | | |

(1) 有关传统和新的热度的更多信息，请参阅 IC 封装热量量 应用报告 [SPRA953](#)。

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|------------------|--------------------------------------|-----|-----|------------------|------|
| V _{BUS} | Supply voltage | 4.0 | | 6 ⁽¹⁾ | V |
| V _{IN} | Supply voltage | 4.0 | | 9 ⁽¹⁾ | V |
| T _J | Operating junction temperature range | -40 | | 125 | °C |

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A tight layout minimizes switching noise.

ELECTRICAL CHARACTERISTICS

Circuit of [Figure 1](#), V_{BUS} = 5V, HZ_MODE=0, OPA_MODE=0, CD=0, T_J = -40°C–125°C and T_J = 25°C for typical values

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|--------|-----|-------|------|
| INPUT CURRENTS | | | | | | |
| I _{VBUS} | VBUS supply current for control | VBUS > V _{MIN} , PWM switching | 10 | | | mA |
| | | VBUS > V _{MIN} , PWM NOT switching | 5 | | | |
| | | 0°C < T _J < 85°C, CD = 1 or HZ_MODE = 1 | 33 | 80 | | μA |
| I _{VIN} | VIN supply current for control | VIN > V _{MIN} , PWM switching | 10 | | | mA |
| | | VIN > V _{MIN} , PWM NOT switching | 5 | | | |
| | | 0°C < T _J < 85°C, CD = 1 or HZ_MODE = 1, No load on VREG | | 150 | | μA |
| I _{IN_LEAK} | Leakage current from battery to VBUS pin and / or VIN | 0°C < T _J < 85°C, V _{VBAT} = 4.2 V, High Impedance mode | | 5 | | μA |
| | Battery discharge current in high impedance mode, (CSIN, VBAT, SW pins) | 0°C < T _J < 85°C, V _{VBAT} = 4.2 V, High Impedance mode, SCL,SDA,OTG=0V or 1.8V | | 23 | | μA |
| VOLTAGE REGULATION | | | | | | |
| V _{OREG} | Output charge voltage | Operating in voltage regulation, programmable | 3.5 | | 4.44 | V |
| | Voltage regulation accuracy | T _A = 25°C | -0.5% | | 0.5% | |
| | | Over recommended operating temperature | -0.75% | | 0.75% | |
| | | 4.1 V – 4.35 V range, over recommended operating temperature | -0.6% | | 0.4% | |
| CURRENT REGULATION -FAST CHARGE | | | | | | |
| I _{OCHARGE} | Output charge current | VIN, V _{LOWV} ≤ V _{VBAT} < V _{OREG} , VIN > VSLP, RSNS = 68 mΩ, LOW_CHG=0, Programmable | 550 | | 1550 | mA |
| | | VBUS, V _{LOWV} ≤ V _{VBAT} < V _{OREG} , VBUS > VSLP, RSNS = 68 mΩ LOW_CHG = 0, Programmable | 550 | | 1250 | |
| | | V _{LOWV} ≤ V _{VBAT} < V _{OREG} , VBUS > VSLP, RSNS=68 mΩ LOW_CHG=1 | | 325 | 350 | |
| | Regulation accuracy for charge current across RSNS, V _{IREG} = I _{OCHARGE} × R _{SNS} | 37.4 mV ≤ V _{IREG} | -3% | | 3% | |
| WEAK BATTERY DETECTION | | | | | | |
| V _{LOWV} | Weak battery voltage threshold | Programmable | 3.4 | | 3.7 | V |
| | Weak battery voltage accuracy | | -5% | | 5% | |

ELECTRICAL CHARACTERISTICS (continued)

 Circuit of Figure 1, $V_{BUS} = 5V$, $HZ_MODE=0$, $OPA_MODE=0$, $CD=0$, $T_J = -40^{\circ}C-125^{\circ}C$ and $T_J = 25^{\circ}C$ for typical values

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|--|--|-----------------------------------|------|-------|---------|----|
| | Deglintch time for weak battery threshold | Rising voltage, 2-mV over drive, $t_{RISE} = 100$ ns | | 30 | | ms | |
| | Hysteresis for V_{LOWV} | Battery voltage falling | | 100 | | mV | |
| DIS, SLRST and OTG PIN LOGIC LEVEL | | | | | | | |
| V_{IL} | Input low threshold level | | | | 0.4 | V | |
| V_{IH} | Input high threshold level | | 1.3 | | | V | |
| CHARGE TERMINATION DETECTION | | | | | | | |
| I_{TERM} | Termination charge current | $V_{VBAT} > V_{OREG}-V_{RCH}$, $V_{BUS} > V_{SLP}$, $R_{SNS} = 68$ m Ω , Programmable | 50 | | 400 | mA | |
| | Deglintch time for charge termination | Both rising and falling, 2-mV overdrive, t_{RISE} , $t_{FALL} = 100$ ns | | 30 | | ms | |
| | Regulation accuracy for termination current across R_{SNS} $V_{IREG_TERM} = I_{OTERM} \times R_{SNS}$ | 3.4 mV $\leq V_{IREG_TERM} \leq 6.8$ mV | -35% | | 35% | | |
| | | 6.8 mV $< V_{IREG_TERM} \leq 13.6$ mV | -12.5% | | 12.5% | | |
| | | 13.6 mV $< V_{IREG_TERM} \leq 30$ mV | -6% | | 6% | | |
| BAD ADAPTOR DETECTION | | | | | | | |
| $V_{IN(MIN)}$ | Input voltage lower limit | Bad adaptor detection | 3.7 | 3.8 | 4.0 | V | |
| | Deglintch time for VBUS rising above $V_{IN(MIN)}$ | Rising voltage, 2-mV overdrive, $t_{RISE} = 100$ ns | | 30 | | ms | |
| | Hysteresis for $V_{IN(MIN)}$ | Input voltage rising | 100 | | 200 | mV | |
| I_{SHORT} | Current source to GND | During bad adaptor detection | 20 | 30 | 40 | mA | |
| T_{INT} | Detection interval | Input power source detection | | 2 | | S | |
| INPUT BASED DYNAMIC POWER MANAGEMENT | | | | | | | |
| V_{IN_LOW} | The threshold when input based DPM loop kicks in | Charge mode, programmable | 4.2 | | 4.76 | V | |
| | DPM loop kick-in threshold tolerance | | -2% | | +2% | | |
| INPUT CURRENT LIMITING | | | | | | | |
| I_{IN_LIMIT} | Input current limit | $I_{IN} = 100$ mA | $T_J = 0^{\circ}C-125^{\circ}C$ | 88 | 93 | 98 | mA |
| | | | $T_J = -40^{\circ}C-125^{\circ}C$ | 86 | 93 | 98 | |
| | | $I_{IN} = 500$ mA | $T_J = 0^{\circ}C-125^{\circ}C$ | 450 | 475 | 500 | mA |
| | | | $T_J = -40^{\circ}C-125^{\circ}C$ | 440 | 475 | 500 | |
| VREF BIAS REGULATOR | | | | | | | |
| V_{REF} | Internal bias regulator voltage | $V_{IN} > V_{REF}$, $I_{VREF} = 1$ mA, $C_{VREF} = 1$ μ F | 5.5 | | 6.5 | V | |
| | V_{REF} output short current limit | | | 30 | | mA | |
| BATTERY RECHARGE THRESHOLD | | | | | | | |
| V_{RCH} | Recharge threshold voltage | Below V_{OREG} | 90 | 120 | 160 | mV | |
| | Deglintch time | V_{VBAT} decreasing below threshold, $t_{FALL} = 100$ ns, 10-mV overdrive | | 130 | | ms | |
| STAT OUTPUT | | | | | | | |
| V_{OL} | Low-level output saturation voltage, STAT pin | $I_O = 10$ mA, sink current | | | 0.55 | V | |
| | High-level leakage current for STAT | Voltage on STAT pin is 5V | | | 1 | μ A | |
| LED OUTPUT | | | | | | | |
| V_{LED_MIN} | Minimum LED operating voltage | | 2.5 | | | V | |
| I_{LED} | LED current, programmable | $I_{LED1} = L$, $I_{LED0} = L$ | | 0 | | mA | |
| | | $I_{LED1} = L$, $I_{LED0} = H$ | | 1.35 | | | |
| | | $I_{LED1} = H$, $I_{LED0} = L$ | | 2.7 | | | |
| | | $I_{LED1} = H$, $I_{LED0} = H$ | | 5.4 | | | |
| | LED current accuracy | | -20% | | +20% | | |
| V_{DO} | Drop-out voltage of LED | $V_{BAT} = 2.5$ V | | 100 | 200 | mV | |
| T_{ON} | Turn on time for current source (10%–90%) | | | 100 | | μ s | |
| T_{OFF} | Turn off time for current source (90%–10%) | | | 100 | | μ s | |
| I²C BUS LOGIC LEVELS AND TIMING CHARACTERISTICS | | | | | | | |

ELECTRICAL CHARACTERISTICS (continued)

Circuit of Figure 1, $V_{BUS} = 5V$, $HZ_MODE=0$, $OPA_MODE=0$, $CD=0$, $T_J = -40^{\circ}C-125^{\circ}C$ and $T_J = 25^{\circ}C$ for typical values

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|--|------|-------|------|--------------|
| V_{OL} | Output low threshold level | $I_O = 10$ mA, sink current | | 0.4 | | V |
| V_{IL} | Input low threshold level | $V_{(pull-up)} = 1.8$ V, SDA and SCL | | 0.4 | | V |
| V_{IH} | Input high threshold level | $V_{(pull-up)} = 1.8$ V, SDA and SCL | 1.2 | | | V |
| $I_{(bias)}$ | Input bias current | $V_{(pull-up)} = 1.8$ V, SDA and SCL | | 1 | | μA |
| f_{SCL} | SCL clock frequency | | | 3.4 | | MHz |
| BATTERY DETECTION | | | | | | |
| I_{DETECT} | Battery detection current before charge done (sink current) ⁽¹⁾ | Begins after termination detected | -0.5 | | | mA |
| t_{DETECT} | Battery detection time | | 262 | | | ms |
| $t_{DETECT2}$ | Battery detection time after linear charge is complete and PWM starts | | 262 | | | ms |
| SLEEP COMPARATOR | | | | | | |
| V_{SLP} | Sleep-mode entry threshold, $V_{BUS}-V_{VBAT}$ or $V_{IN} - V_{VBAT}$ | $2.3 V \leq V_{VBAT} \leq V_{OREG}$, V_{BUS} or V_{IN} falling | 0 | 40 | 100 | mV |
| $V_{SLP-EXIT}$ | Sleep-mode exit hysteresis | $2.3 V \leq V_{VBAT} \leq V_{OREG}$ | 70 | 110 | 200 | mV |
| | Deglitch time for V_{BUS} or V_{IN} rising above $V_{SLP}+V_{SLP-EXIT}$ | Rising voltage, 2-mV over drive, $t_{RISE} = 100$ ns | | 30 | | ms |
| UNDER-VOLTAGE LOCKOUT (UVLO) | | | | | | |
| V_{UVLO} | IC active threshold voltage | V_{BUS} or V_{IN} rising | 3.05 | 3.3 | 3.65 | V |
| V_{UV-HYS} | IC active hysteresis | V_{BUS} or V_{IN} falling from above V_{UVLO} | 90 | 100 | | mV |
| PWM | | | | | | |
| V_{BOOT} | Voltage from BOOT1 pin to SW1 pin, or Voltage from BOOT2 pin to SW2 pin | | | | 6.5 | V |
| R_{ON-Q1} | Internal top reverse blocking MOSFET on-resistance | $I_{IN_LIMIT} = 500$ mA, Measured from V_{IN} to PMID2 | | 100 | 150 | m Ω |
| R_{ON-Q2} | Internal top N-channel Switching MOSFET on-resistance | Measured from PMID2 to SW2, $V_{BOOT2} - V_{SW2} = 4$ V | | 120 | 200 | m Ω |
| R_{ON-Q3} | Internal bottom N-channel MOSFET on-resistance | Measured from SW2 to GND | | 110 | 200 | m Ω |
| R_{ON-Q4} | Internal top reverse blocking MOSFET on-resistance | $I_{IN_LIMIT} = 500$ mA, Measured from V_{BUS} to PMID1 | | 100 | 150 | m Ω |
| R_{ON-Q5} | Internal top N-channel Switching MOSFET on-resistance | Measured from PMID1 to SW1, $V_{BOOT1} - V_{SW1} = 4$ V | | 120 | 200 | m Ω |
| R_{ON-Q6} | Internal bottom N-channel MOSFET on-resistance | Measured from SW1 to GND | | 110 | 200 | m Ω |
| f_{OSC} | Oscillator frequency | | | 3.0 | | MHz |
| | Frequency accuracy | | -10% | | 10% | |
| D_{MAX} | Maximum duty cycle | | | 99.5% | | |
| D_{MIN} | Minimum duty cycle | | 0 | | | |
| | Synchronous mode to non-synchronous mode transition current threshold ⁽²⁾ | Low-side MOSFET cycle-by-cycle current sensing | | 100 | | mA |
| CHARGE MODE PROTECTION | | | | | | |
| $V_{OVP-VIN}$ | Input OVP for V_{IN} | Rising edge | 9.6 | 9.8 | 10.0 | V |
| | $V_{OVP-VIN}$ hysteresis | | | 140 | | mV |
| $V_{OVP-VBUS}$ | Input OVP for V_{BUS} | Rising edge | 6.3 | 6.5 | 6.7 | V |
| | $VOVP-VBUS$ hysteresis | | | 170 | | mV |
| V_{OVP} | Output OVP threshold voltage | V_{VBAT} threshold over V_{OREG} to turn off charger during charge | 110 | 117 | 121 | % V_{OREG} |
| | $VOVP$ hysteresis | Lower limit for V_{VBAT} falling from above V_{OVP} | | 11 | | % V_{OREG} |
| I_{LIMIT} | Cycle-by-cycle current limit for charge | Charge mode operation | 1.8 | 2.4 | 3.0 | A |
| V_{SHORT} | Trickle to fast charge threshold | V_{VBAT} rising | 2.0 | 2.1 | 2.2 | V |
| | V_{SHORT} hysteresis | | | 100 | | mV |
| I_{SHORT} | Trickle charge charging current | $V_{VBAT} \leq V_{SHORT}$ | 20 | 30 | 40 | mA |

(1) Negative charge current means the charge current flows from the battery to charger (discharging battery).

(2) Bottom N-channel MOSFET always turns on for -60 ns and then turns off if current is too low.

ELECTRICAL CHARACTERISTICS (continued)

 Circuit of [Figure 1](#), $V_{BUS} = 5V$, $HZ_MODE=0$, $OPA_MODE=0$, $CD=0$, $T_J = -40^{\circ}C-125^{\circ}C$ and $T_J = 25^{\circ}C$ for typical values

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|---|------|------|------|-------------|
| BOOST MODE OPERATION FOR V_{BUS} ($OPA_MODE=1$, $HZ_MODE=0$, V_{BUS} input only) | | | | | | |
| V_{BUS_BOOST} | Boost output voltage (to V_{BUS} pin) | $2.5 V < V_{VBAT} < 4.5 V$ | | 5.05 | | V |
| | Boost output voltage accuracy | Including line and load regulation | -3% | | +3% | |
| I_{BOOST} | Maximum output current for boost | $V_{BUS} = 5.05 V$, $2.5 V < V_{VBAT} < 4.5 V$ | 650 | | | mA |
| I_{BLIMIT} | Cycle by cycle current limit for boost | $V_{BUS} = 5.05 V$, $2.5 V < V_{VBAT} < 4.5 V$ | | 1.0 | | A |
| V_{BUSOVP} | Over voltage protection threshold for boost (V_{BUS} pin) | Threshold over V_{BUS} to turn off converter during boost | 5.8 | 6.0 | 6.2 | V |
| | V_{BUSOVP} hysteresis | V_{BUS} falling from above V_{BUSOVP} | | 162 | | mV |
| V_{BATMAX} | Maximum battery voltage for boost (V_{BAT} pin) | V_{VBAT} rising edge during boost | 4.65 | 4.75 | 4.85 | V |
| | V_{BATMAX} hysteresis | V_{VBAT} falling from above V_{BATMAX} | | 70 | | mV |
| V_{BATMIN} | Minimum battery voltage for boost (V_{BAT} pin) | During boosting | | 2.3 | | V |
| | | Before boost starts | | 2.8 | 2.97 | |
| | Boost output resistance at high-impedance mode (From V_{BUS} to $PGND$) | $CD = 1$ or $HZ_MODE = 1$ | 500 | | | k Ω |
| I_{CC_BOOST} | Operation quiescent current in boost mode | No load at V_{BUS} , power save mode, $V_{VBAT} = 4 V$, boosting | | 650 | | μA |
| PROTECTION | | | | | | |
| T_{SHTDWN} | Thermal trip | | | 165 | | $^{\circ}C$ |
| | Thermal hysteresis | | | 10 | | $^{\circ}C$ |
| T_{CF} | Thermal regulation threshold | Charge current begins to taper down | | 120 | | $^{\circ}C$ |
| T_{32S} | Time constant for the 32-second timer | 32 second mode | 15 | 32 | | S |
| T_{15M} | Time constant for the 15-minute timer | 15 minute mode | 12 | | 15 | Minute |
| VREG | | | | | | |
| V_{REG} | VREG Regulator | $I_{LOAD} = 1mA$, $C_{REG} = 0.1\mu F$, $V_{IN} > V_{UVLO}$ | 2.34 | 2.6 | 2.86 | V |
| I_{LIM_VREG} | Current limit VREG | $V_{REG} = 0V$ | 10 | | | mA |

TYPICAL APPLICATION CIRCUITS

$V_{IN}=5V$ or $V_{BUS}=5V$, $I_{CHARGE} = 1550mA$, $V_{BAT} = 3.5\text{--}4.44V$ (Adjustable), Safety Timer = 15 minutes or 32 seconds

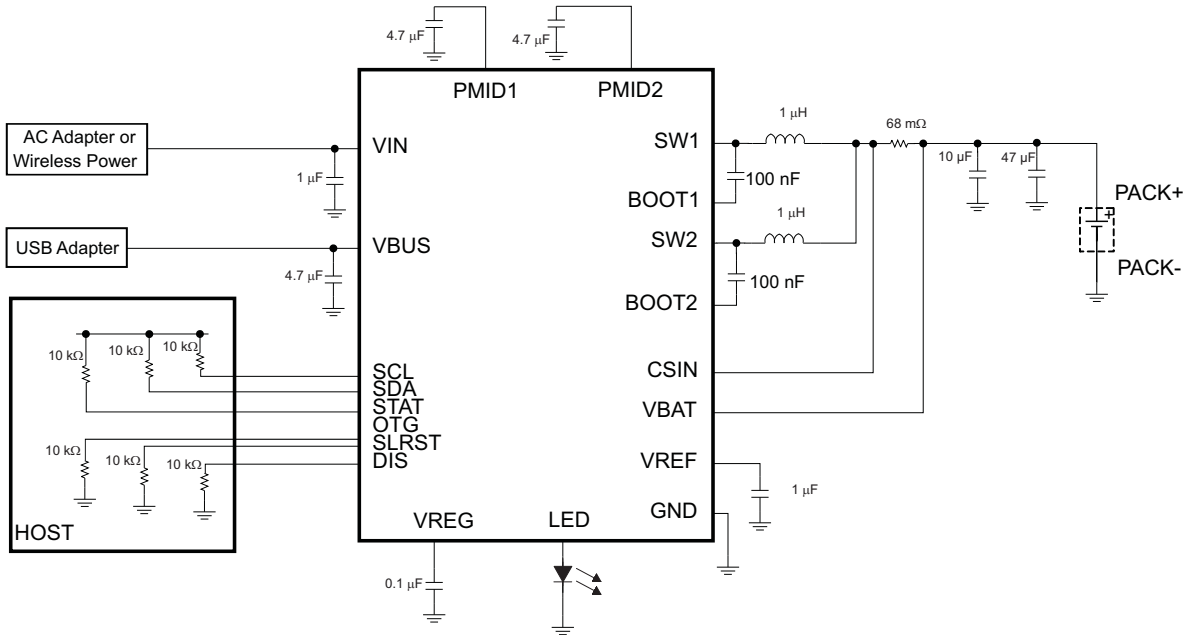


Figure 1. I²C Controlled 1-Cell USB and AC or Wireless Power Charger Application Circuit

$V_{IN}=5V$ or $V_{BUS}=5V$, $I_{CHARGE} = 1550mA$, $V_{BAT} = 3.5\text{--}4.44V$ (Adjustable), Safety Timer = 15 minutes or 32 seconds

BLOCK DIAGRAM

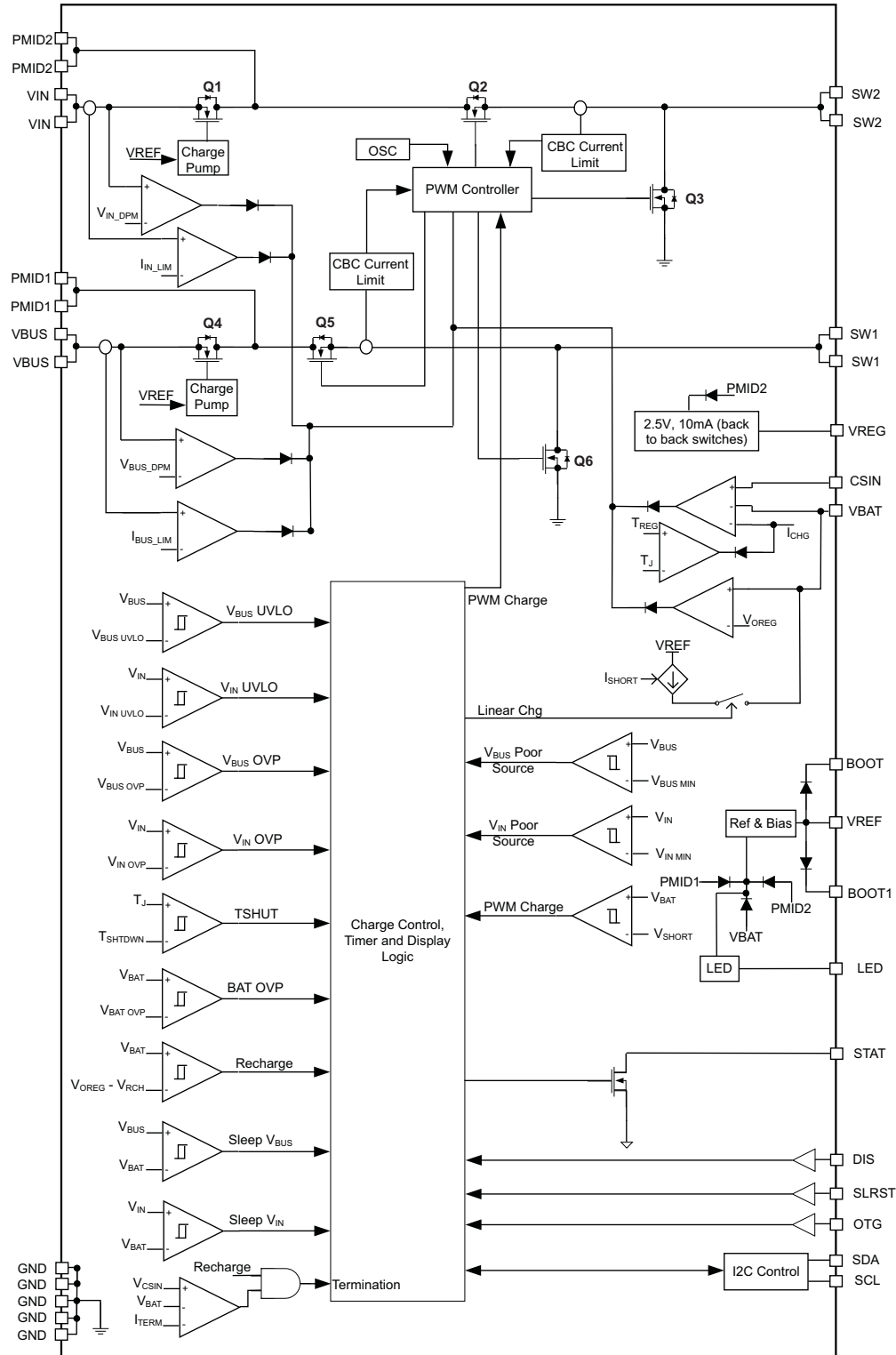


Figure 2. bq24140 Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

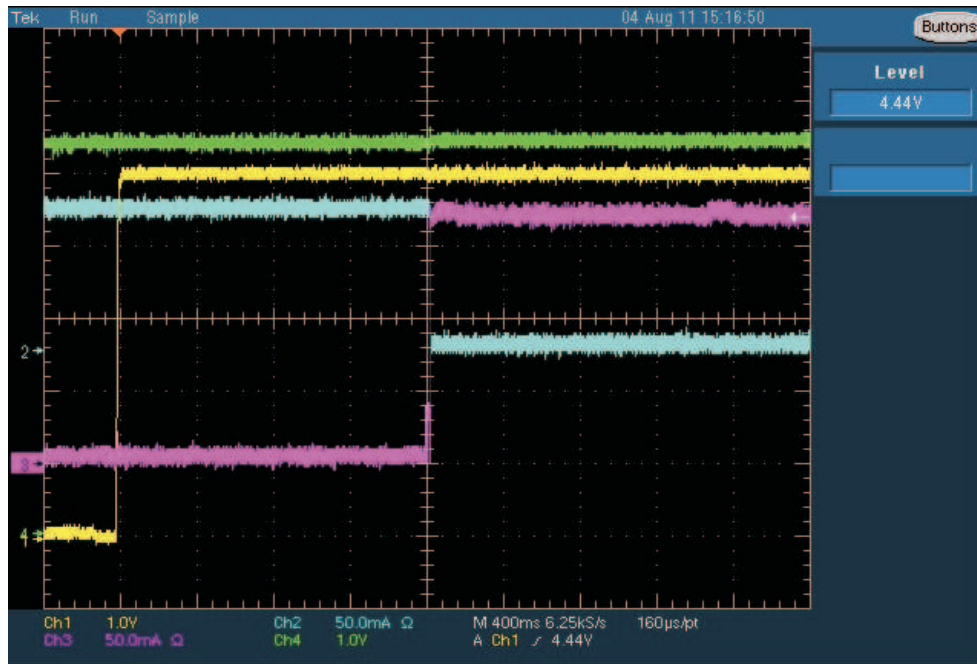


Figure 3. VBUS to VIN Charging – Default Mode C1:VIN, CH2: IVBUS, CH3: IVIN, CH4: VBUS

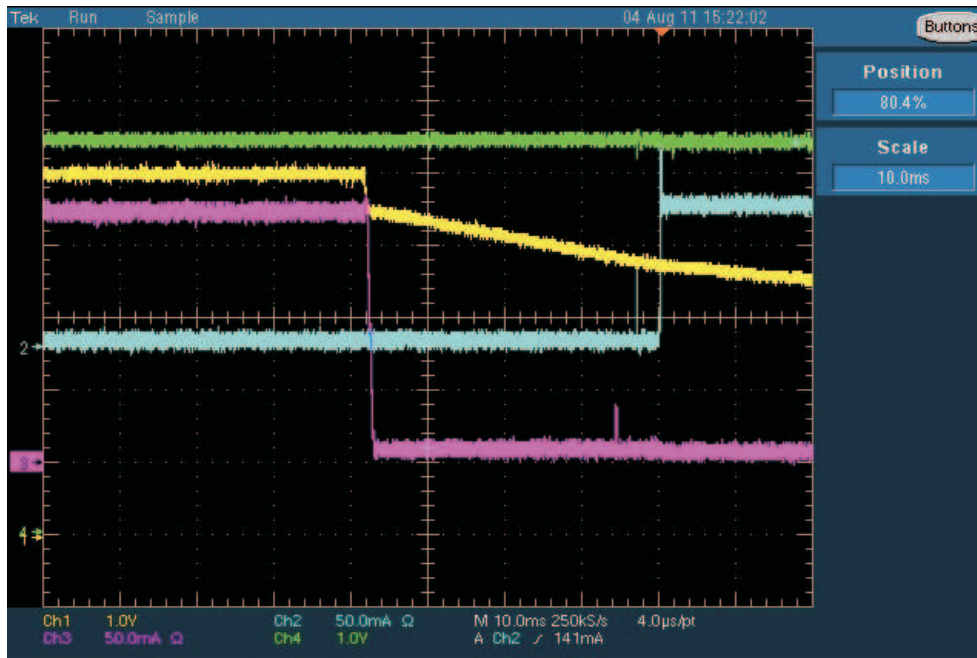


Figure 4. VIN Charging and removed, switch to VBUS – Default Mode C1:VIN, CH2: IVBUS, CH3: IVIN, CH4: VBUS

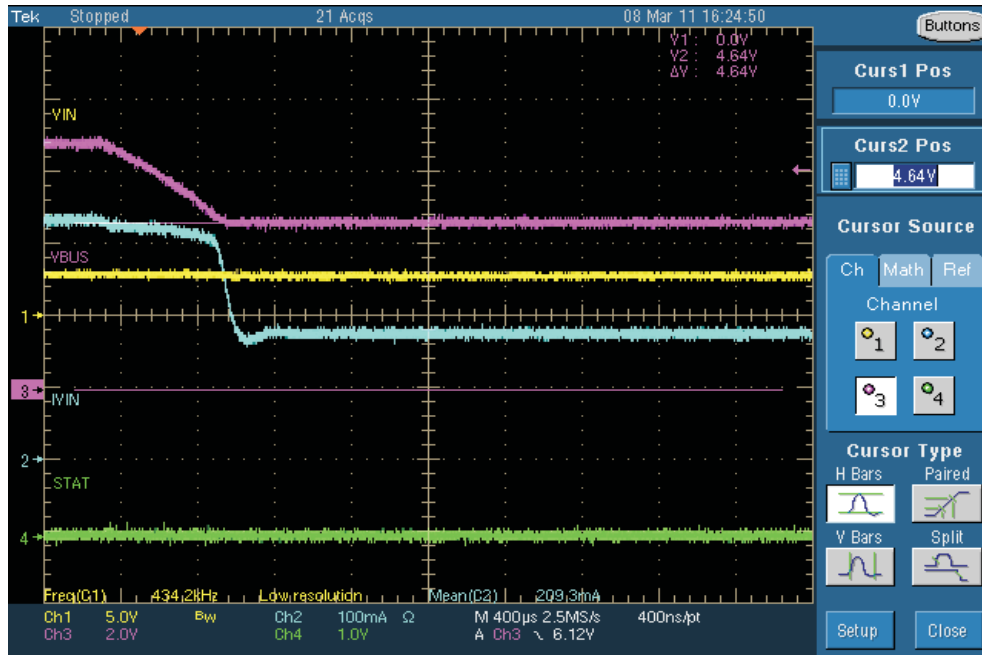


Figure 5. VBUS Dynamic Power Management (DPM) – C1:VIN, CH2: IVBUS, CH3: VBUS, CH4: STAT

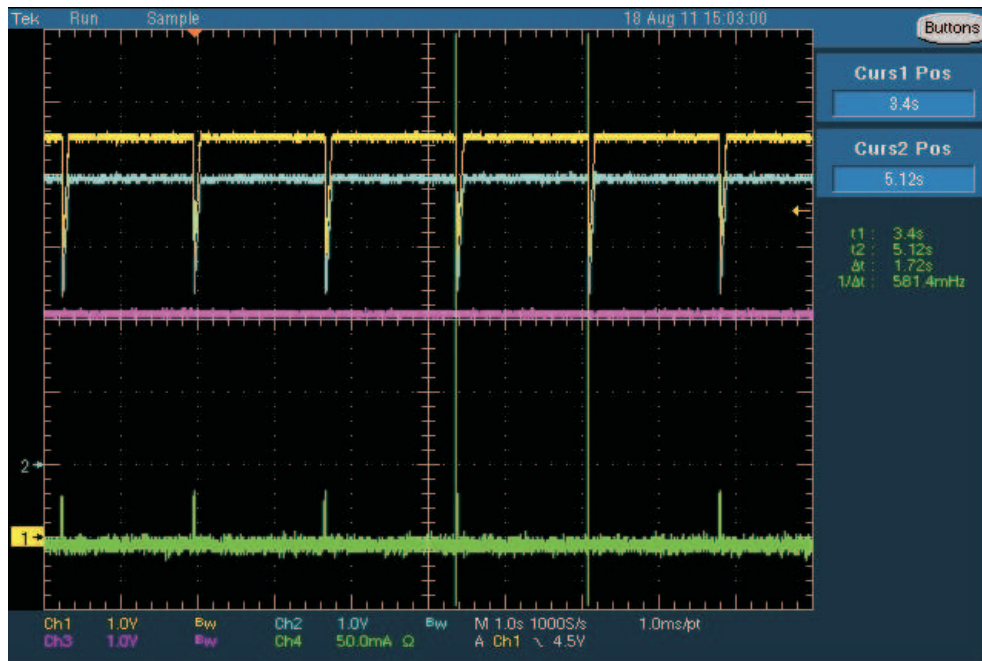


Figure 6. VBUS Dynamic Power Management (DPM) – CH1:VIN, CH2: STAT, CH3: VBAT, CH4: IVIN

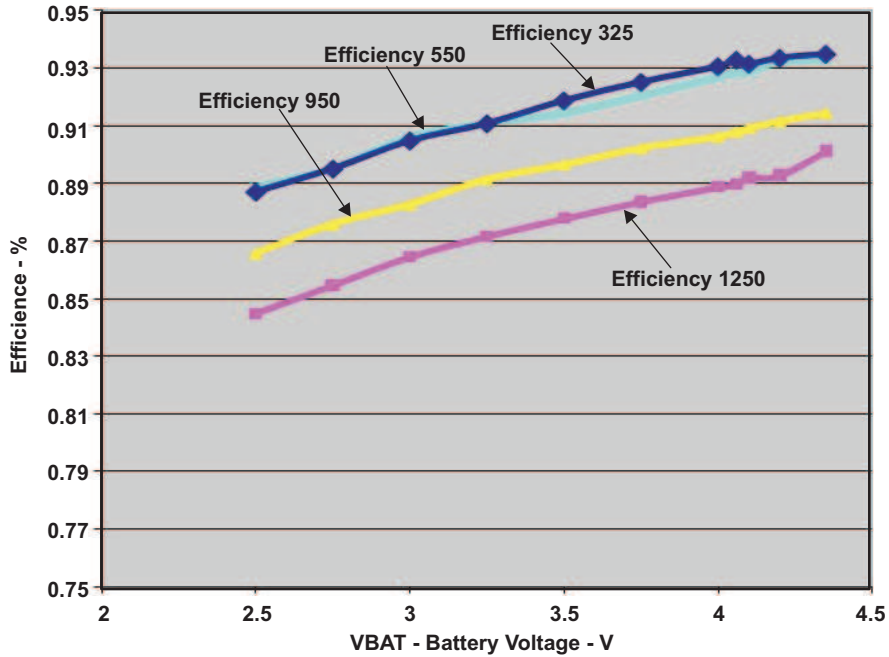


Figure 7. VBUS Efficiency versus Battery Voltage

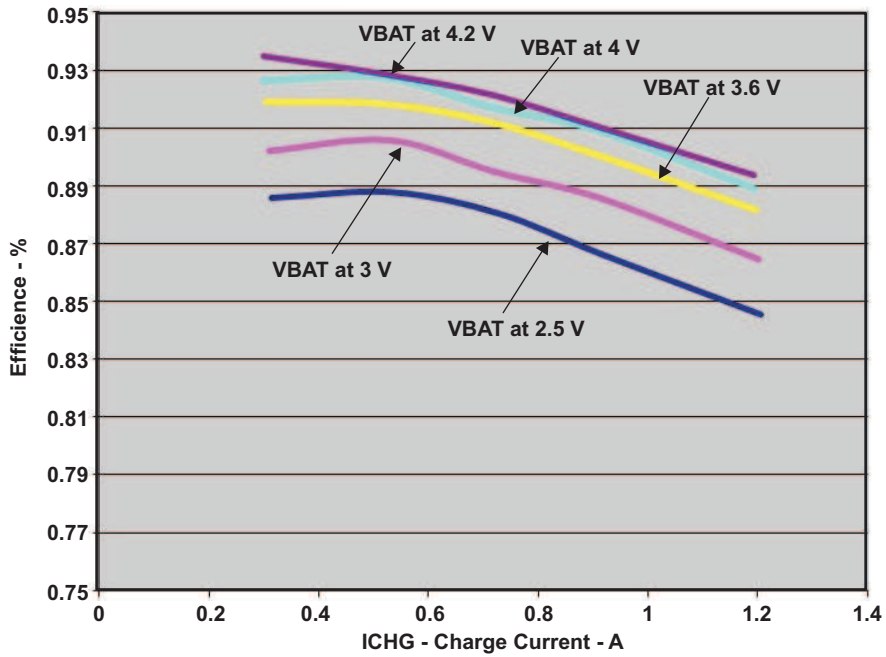


Figure 8. VBUS Efficiency versus Charge Current

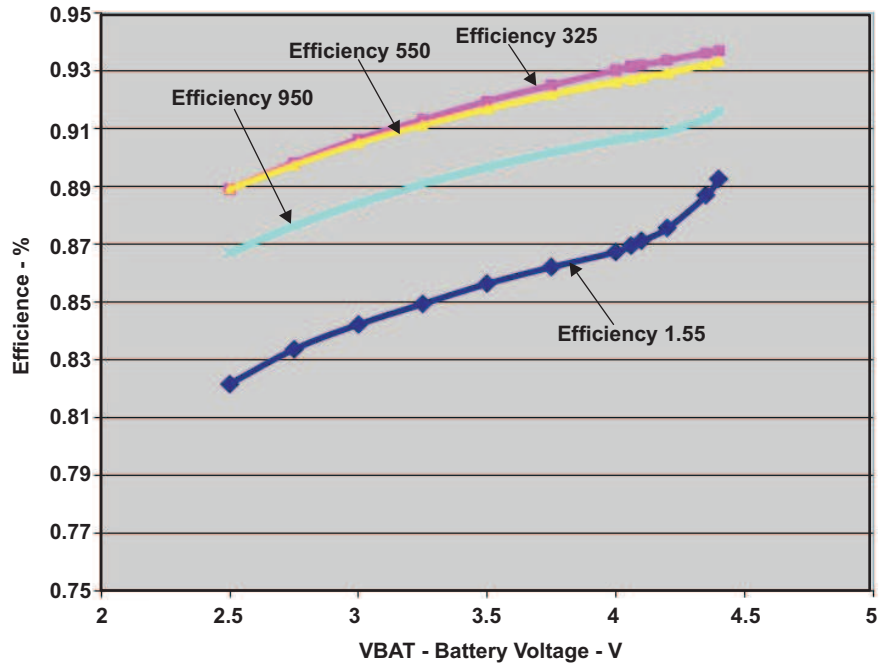


Figure 9. VIN Efficiency versus Battery Voltage

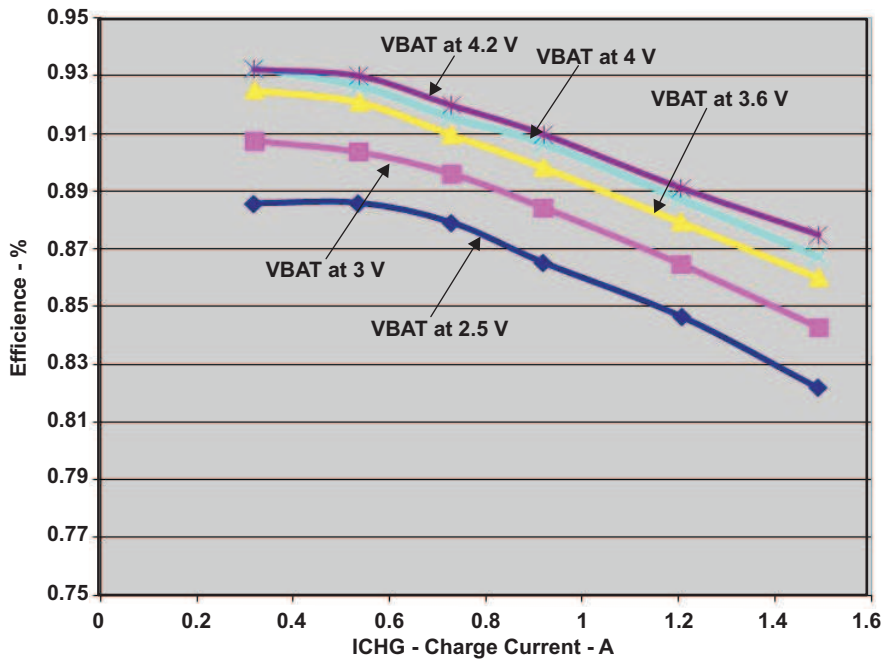


Figure 10. VIN Efficiency versus Charge Current

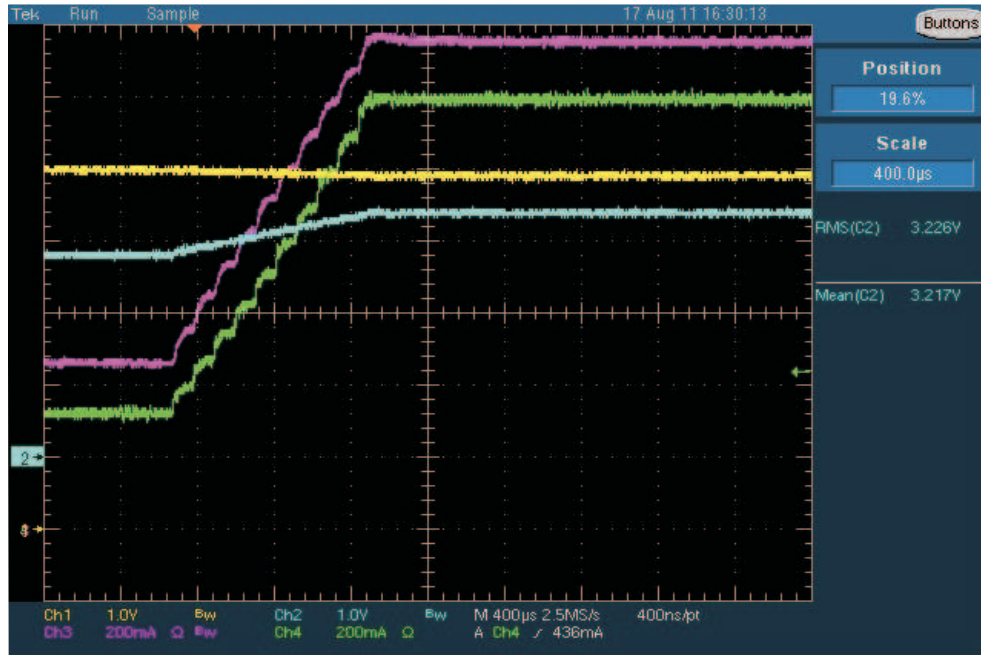


Figure 11. Charge Current Response – 550mA to 1.55A
CH1: VIN, CH2: VBAT, CH3: IBAT, CH4: IVIN

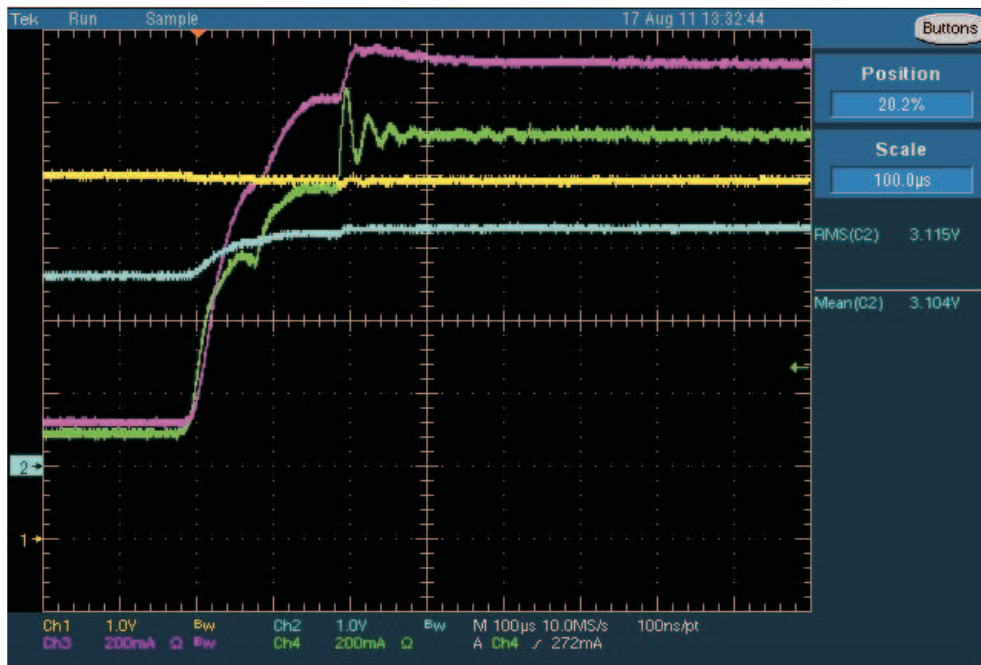


Figure 12. Input Current Regulation Response – 100mA to No Limit
CH1: VIN, CH2: VBAT, CH3: IBAT, CH4: IVIN

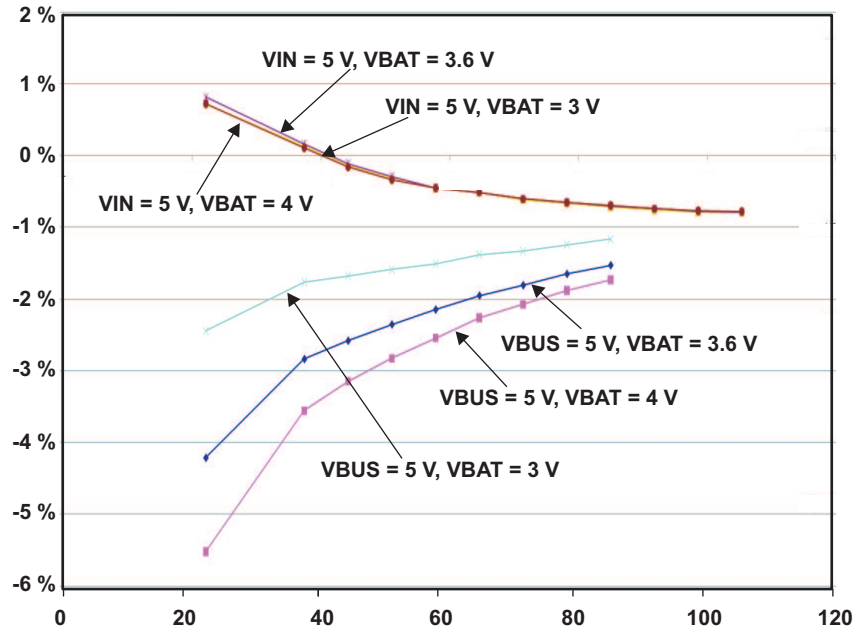


Figure 13. Typical Charge Current Accuracy

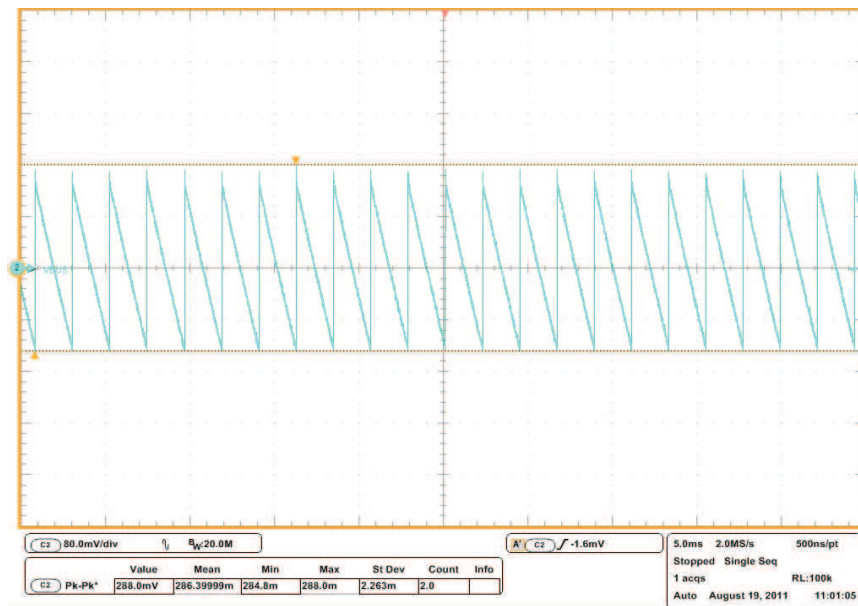


Figure 14. VBUS OTG in PFM Mode

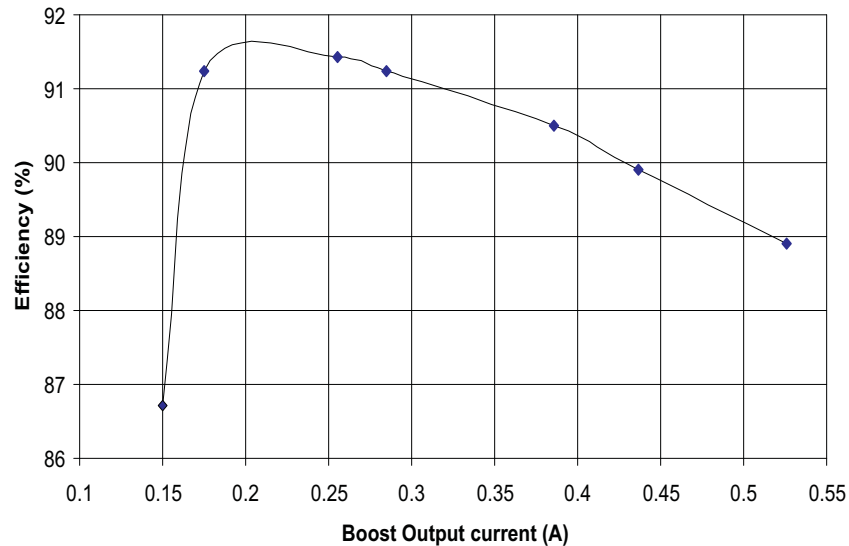


Figure 15. VBUS OTG Efficiency

DETAILED FUNCTIONAL DESCRIPTION

The bq24140 is a highly integrated dual input switch-mode battery charger with USB-OTG support. Due to the switch-mode architecture, it provides the capability of charging the battery faster than traditional linear chargers in the event that the power source is current limited, such as USB ports. In addition to the reduced charge time, higher efficiencies reduce the power losses through the charger and allows for better thermal management of the end product.

The bq24140 integrates a dual input 3MHz synchronous switching charger that targets space limited portable applications powered by a single cell Li based battery pack. In addition to charge the battery, the bq24140 provides support for simultaneously boosting the battery voltage back to the USB input for USB-OTG support.

The bq24140 has two operation modes: default mode and host-control mode. In default mode, the charger will start a charge cycle with the default parameters and wait for an I2C write to the IC before entering host-mode. In host-control mode, the charger will switch to a 32s watchdog timer and the charge parameters will follow the information set on the registers.

The bq24140 provides three ways of configuring the charger, charge mode, boost mode and high impedance mode. These 3 configuration allows for multiple possible settings of the charge systems, including charging the battery and providing power to an accessory. The high impedance mode reduces the quiescent current from the device, effectively reducing the power consumption when the portable device is in standby mode. Integrated control loops ensure smooth transitions between the different operating modes.

PWM Buck Charger

The IC provides an integrated, fixed 3 MHz frequency voltage-mode controller to regulate charge current or voltage. This type of controller is used to improve line transient response, thereby, simplifying the compensation network used for both continuous and discontinuous current conduction operation. The voltage and current loops are internally compensated using a Type-III compensation scheme that provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with very low ESR. The device operates between 0% to 99.5% duty cycles.

The IC has back to back common-drain N-channel FETs at the high side and one N-channel FET at low side for both VIN and VBUS inputs. The input N-FETs (Q1, Q4) prevents battery discharge when VIN and/or VBUS is lower than VBAT. The second high-side N-FET (Q2, Q5) are the switching FETs. A charge pump circuit is used to provide gate drive for Q1 and Q4, while a bootstrap circuit with an external bootstrap capacitor is used to supply the gate drive voltage for Q2 and Q5.

Cycle-by-cycle current limit is sensed through FETs Q4 and Q5 for the high side current limit and through Q3 and Q6 for the low side current limit. The high side current limit threshold is set to a nominal 2.4-A peak current. The low-side current limit decides if the PWM Controller will operate in synchronous or non-synchronous mode. This threshold is set to 100mA and it turns off the low-side N-channel FETs (Q3 and/or Q6) before the current reverses, preventing the battery from discharging. Synchronous operation is used when the current of the low-side FET is greater than 100mA to minimize power losses.

If the battery voltage is below the $V_{(SHORT)}$ threshold, the bq24140 applies the short circuit current, $I_{(SHORT)}$, to the battery. The purpose of this current is to close an open protector on the battery pack. Once the battery voltage rises above V_{SHORT} , the bq24140 ramps up the charge current to the programmed I_{CHARGE} value. If the programmed charge current requires an input current that is higher than the programmed I_{IN_LIMIT} value, then the bq24140 will regulate the input current and the charge current will be limited by the input current loop. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. Both the input current limit, I_{IN_LIMIT} , and fast charge current, I_{CHARGE} , can be set by the host. Once the battery voltage reaches the programmed regulation voltage, V_{OREG} , the charge current is tapered down. (See [Figure 16](#) and [Figure 17](#).)

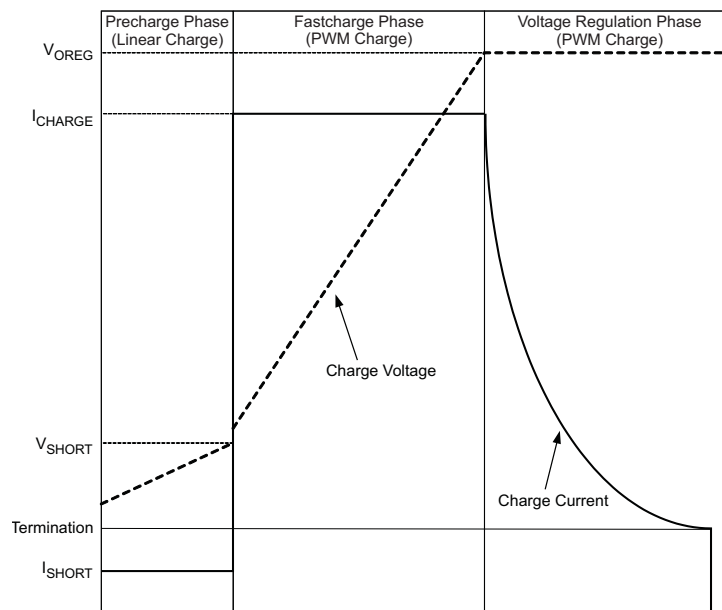


Figure 16. Typical Charging Profile for No Input Current Limit

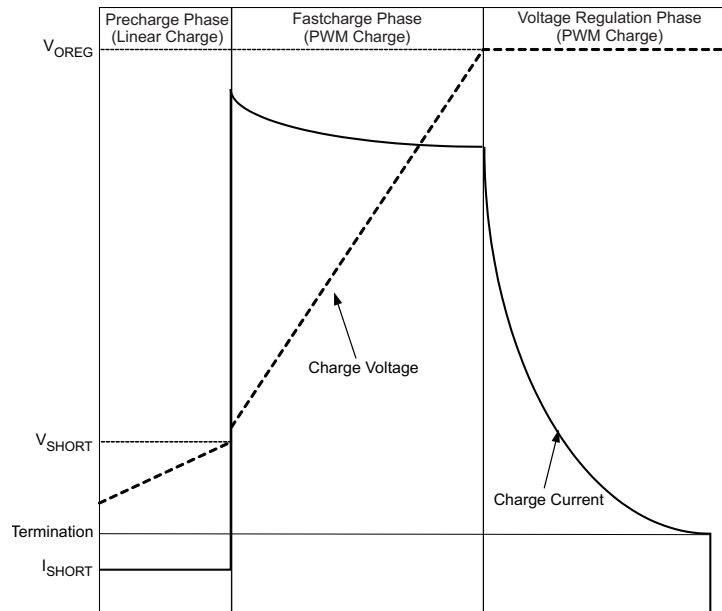


Figure 17. Typical Charging Profile With Input Current Limit

The voltage regulation feedback occurs by monitoring the battery-pack voltage between the VBAT and GND pins. The regulation voltage is adjustable (3.5V to 4.44V) and is programmed through I²C interface. The IC monitors the charging current during the voltage regulation phase. When the termination is enabled, once the termination threshold, I_{TERM} , is detected and the battery voltage is above the recharge threshold, the IC terminates charge. The termination current level is programmable. To disable the charge current termination, the host can set the charge termination bit (TE) of charge control register to 0, refer to I²C section for detail.

A new charge cycle is initiated when one of the following conditions is detected:

- The battery voltage falls below the $V_{(OREG)} - V_{(RCH)}$ threshold.
- VBUS or VIN Power-on reset (POR), if battery voltage is below the $V_{(LOWV)}$ threshold.
- CE bit toggle or RESET bit is set (Host controlled)

Figure 18 shows an operational flow chart of the bq24140 in charge mode.

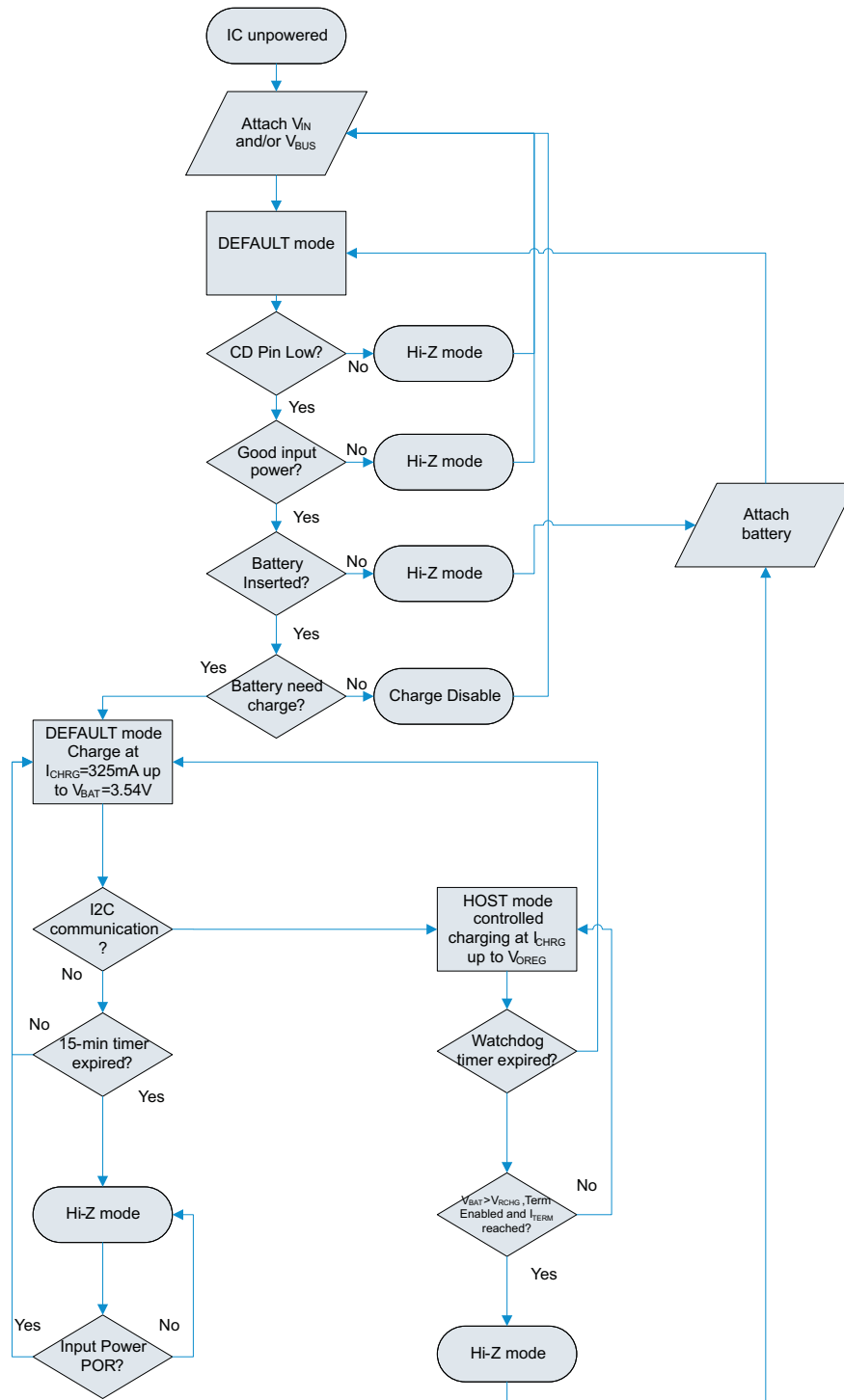


Figure 18. Operational Flowchart

POWER UP

When a power source is first connected to the bq24140, the IC will go to default mode for 15 minutes. In default mode, the bq24140 is configured with safe charging parameters for charge current, charge voltage and input current. Once a write event is done to the bq24140 through I²C, the device enters host mode and the device will then follow the parameters as they are written by the host.

During initial power up in default mode, the device will look at the battery voltage. If the battery voltage is less than the V_{LOWV} , the device will charge the battery with a default charge current of 325mA and a default battery charge voltage of 3.54V. The input current limit value depends on which power source was used. In the case the bq24140 is powered up from the VIN source, the input current limit is set to 500mA. If the device is powered up from the VBUS source, the input current limit depends on the status of the OTG pin. If the OTG pin is low, the input current limit is set to 100mA. If the OTG pin is high, the input current limit is set to 500mA.

INPUT POWER SOURCE PRIORITY

When two power supplies are detected in default mode, the bq24140 will default to VIN operation and the VBUS input will go to high impedance. There is a blanking time between switching from one power source to the other power source of 10ms ($t_{HANDOFF}$). The state diagram below describes the operation (Figure 19).

Input Power Source Switch Over State Diagram

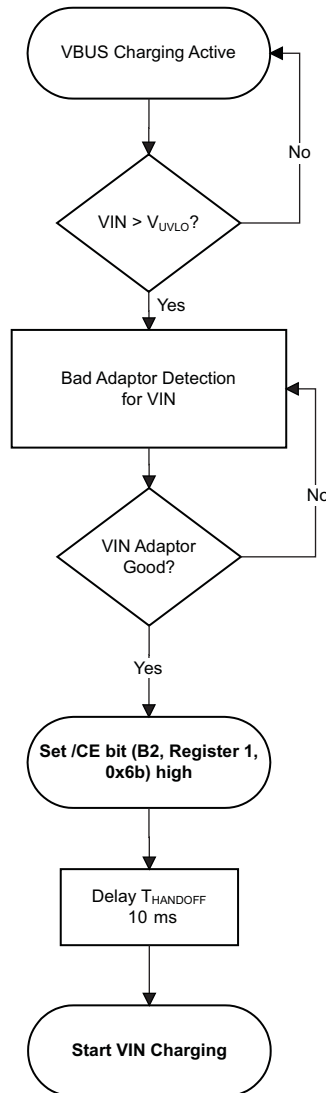


Figure 19. Input power source selection in default mode

In the case where the bq24140 is in host mode, power priority will be dictated by the Host by setting one input to high impedance and activating the other input using the HZ_MODE bit of the control register.

BAD ADAPTOR DETECTION

At POR of VBUS or VIN, the IC performs the bad adaptor detection by applying a current sink of 30mA to the valid power pin. If the power pin is higher than VIN(MIN) for 30ms, the adaptor is good and the charge process begins. Otherwise, if the power pin drops below VIN(MIN), a bad adaptor is detected. Once a bad adaptor is detected, the IC disables the current sink, sends a send fault pulse in FAULT pin and sets the bad adaptor flag (B2-B0=011 for Register 0x00). After a delay of T_{INT} , the IC repeats the adaptor detection process, as shown in the flowchart below:

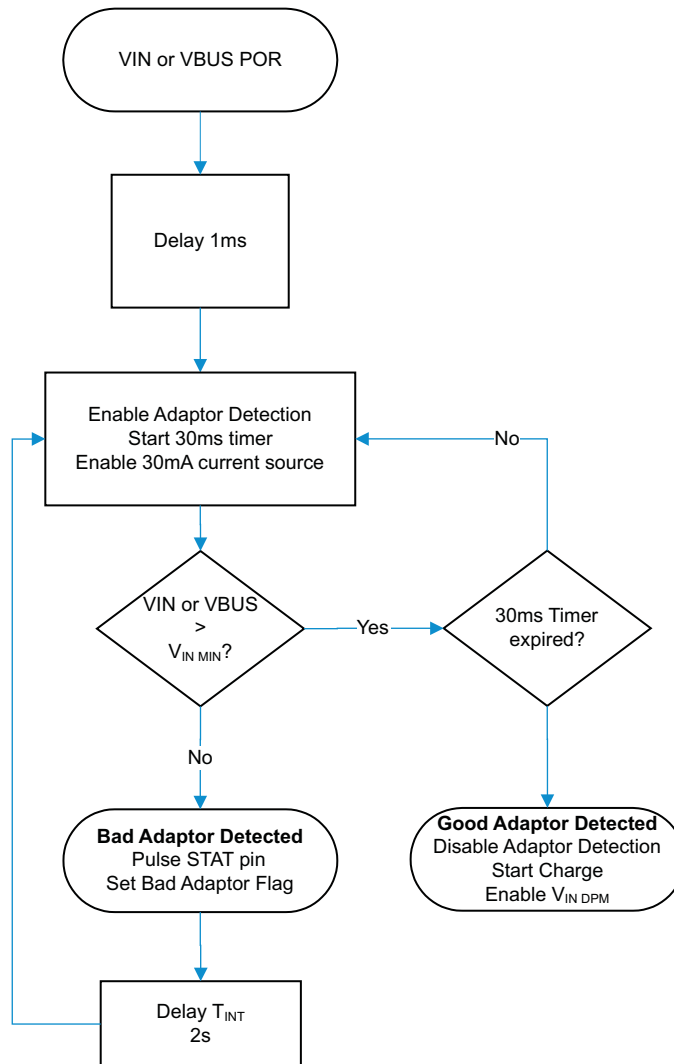


Figure 20. Bad Adaptor Detection

BATTERY DETECTION

Battery detection during charging

During normal charging process with host control, once the voltage at the VBAT pin is above the battery recharge threshold, $V_{OREG}-V_{RCH}$, and the termination charge current is detected, the IC turns off the PWM charge and enables a discharge current, I_{DETECT} , for a period of t_{DETECT} , then checks the battery voltage. If the battery voltage is still above recharge threshold, the IC concludes that the battery is present and charge is completed. On the other hand, if the battery voltage is below battery recharge threshold, the IC concludes that the battery was removed. Under this condition, the charge parameters (such as input current limit) are reset to the default values and charge resumes after a delay of t_{INT} . This function ensures that the charge parameters are reset whenever the battery is replaced.

Battery detection during power-up

The bq24140 also has a unique battery detection scheme during the start up of the charger. At power up, if the timer is in 15-minute mode, bq24140 will start a 262ms timer when exiting from short circuit mode to PWM charge mode. If the battery voltage is charged to recharge threshold ($V_{OREG}-V_{RCH}$) and the 262ms timer has not expired yet, or battery voltage is above output OVP threshold during short-circuit mode, bq24140 will consider the battery is not present; then stop charging and go to high impedance mode immediately. However, if the 262ms timer has expired before the recharge threshold is reached, the charging process will continue as normal.

HIGH-SIDE LED DRIVER

The LED pin is a high-side LED driver. This LED function needs to run from the battery and the expected output current can be programmed through I²C. There are 2 bits for programming the output current from the LED pin. In addition, there is extra programmability for the LED function. Since there is only one LED driver used by both the VIN and VBUS charger cores, there is only one LED register that can be accessed through the addresses 6AH and 6BH. When one of the two addresses is written, the settings for both cores will be set. Refer to the Register Description Section for details on the LED programmable timings and current options.

BOOST CONVERTER OPERATION

The bq24140 support USB-OTG for the VBUS pin when OTG mode is enabled. In this configuration, the battery voltage is boosted to 5.05V ($\pm 3\%$). The maximum output current for the boost converted is increased to 650mA minimum current.

Boost Start Up

To prevent the inductor saturation and limit the inrush current, a soft-start control is applied during the boost start up.

PFM Mode at Light Load

In boost mode, the IC operates in pulse skipping mode (PFM mode) to reduce the power loss and improve the converter efficiency at light load condition. During boosting, the PWM converter is turned off if the inductor current falls below than 200mA. The PWM is turned back on only when the voltage at PMID pin drops to 99.5% of the typical rated output voltage. A unique pre-set circuit is used to make the smooth transition between PWM and PFM mode.

Safety Timer in Boost Mode

At the beginning of boost operation, the IC starts a 32-second timer that is reset by the host using the I²C interface. Writing “1” to reset bit of TMR_RST in control register will reset the 32-second timer and TMR_RST is automatically set to “0” after the 32-second timer is reset. Once the 32-second timer expires, the IC turns off the boost converter, enunciates the fault pulse from the STAT pin and sets fault status bits in the status register. The fault condition is cleared by POR or host control.

Charge Status Output, STAT Pin

The STAT pin is used to indicate operation conditions for bq24140. STAT is pulled low during charging when EN_STAT bit in control register (00H) is set to “1”. Under other conditions, STAT pin behaves as a high impedance (open-drain) output. Under fault conditions, a 128- μ s pulse will be sent out to notify the host. The status of STAT pin at different operation conditions is summarized in [Table 1](#). The STAT pin can be used to drive an LED or communicate to the host processor.

Table 1. STAT Pin Summary

| CHARGE STATE | STAT |
|---|--|
| Charge in progress and EN_STAT = 1 | Low |
| Other normal conditions | Open-Drain |
| Charge mode faults and input not in HiZ | 128 μ s pulse, then open-drain |
| Boost mode faults and input not in HiZ | 128 μ s pulse, then open-drain |
| VIN Present bit change (H→L or L→H) regardless of HiZ status | 128 μ s pulse, then normal per above cases |
| VBUS Present bit change (H→L or L→H) regardless of HiZ status | 128 μ s pulse, then normal per above cases |

Safety Limit Registers

The bq24140 includes safety limit registers which are used as an extra level of security for devices that allow applications to be developed by third party vendors (i.e. Android OS). The purpose of the safety limit registers is to program the maximum allowable battery regulation voltage and charge current. These two registers need to be written before any other write actions are sent to the bq24140. Once a write action to a register other than the safety limit registers, the values on the safety limit registers will be locked.

SLRST Pin

When SLRST=0, the bq24140 will reset all the safety limits to default values, regardless of the write actions to safety limits registers (06H). When SLRST=1, the bq24140 can program the safety limit register until any write action to other registers locks the programmed safety limits.

VREG LDO

The bq24140 includes a 2.6V LDO that can be used as an indication of the VIN input being connected. This LDO is active all the time when there is a power source connected to the VIN input. The current limit on the LDO guarantees up to 10mA.

SERIAL INTERFACE DESCRIPTION

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The IC works as a slave and is compatible with the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.2 V (typical). I²C is asynchronous, which means that it runs off of SCL. The device has no noise or glitch filtering on SCL, so SCL input needs to be clean. Therefore, it is recommended that SDA changes while SCL is LOW.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as HS-mode. The IC supports 7-bit addressing only. **The device has two 7-bit addresses, defined as '1101011' (6BH) for USB portion and, and '1101010' (6AH) for AC portion.**

REGISTER DESCRIPTION

For I2C address 6BH (USB Charger)

Status/Control Register (READ/WRITE)

Memory location: 00, Reset state: x1xx 0xxx

| BIT | NAME | Read/Write | FUNCTION |
|---------|-------------|------------|---|
| B7(MSB) | TMR_RST/OTG | Read/Write | Write: TMR_RST function, write "1" to reset the safety timer (auto clear) Read: OTG pin status, 0-OTG pin at Low level, 1-OTG pin at High level; |
| B6 | EN_STAT | Read/Write | 0-Disable STAT pin function, 1-Enable STAT pin function (default 1) |
| B5 | STAT2 | Read only | 00-Ready, 01-Charge in progress, 10-Charge done, 11-Fault |
| B4 | STAT1 | Read only | |
| B3 | BOOST | Read only | Boost mode, 0—Not in boost mode. |
| B2 | FAULT_3 | Read only | Charge mode: 000-Normal, 001-VBUS OVP, 010-Sleep mode, 011-Bad Adaptor or VBUS<VUVLO, 100-Output OVP, 101-Thermal shutdown, 110-Timer fault, 111-No battery |
| B1 | FAULT_2 | Read only | |
| B0(LSB) | FAULT_1 | Read only | Boost mode: 000-Normal, 001-V _{BUS} OVP, 010-Over load, 011-Battery voltage is too low, 100-Battery OVP, 101-Thermal shutdown, 110-Timer fault, 111-NA |

Control Register (READ/WRITE)

Memory location: 01, Reset state: 0011 0000

| BIT | NAME | Read/Write | FUNCTION |
|---------|------------------------|------------|---|
| B7(MSB) | lin_Limit_2 | Read/Write | 00-USB host with 100-mA current limit, 01-USB host with 500-mA current limit, 10-USB host/charger with 800-mA current limit, 11-No input current limit (default 00) |
| B6 | lin_Limit_1 | Read/Write | |
| B5 | VLOWV_2 ⁽¹⁾ | Read/Write | 200 mV weak battery voltage threshold (default 1) |
| B4 | VLOWV_1 ⁽¹⁾ | Read/Write | 100 mV weak battery voltage threshold (default 1) |
| B3 | TE | Read/Write | 1-Enable charge current termination, 0-Disable charge current termination (default 0) |
| B2 | \overline{CE} | Read/Write | 1-Charger is disabled, 0-Charger enabled (default 0) |
| B1 | HZ_MODE | Read/Write | 1-High impedance mode, 0-Not high impedance mode (default 0) |
| B0(LSB) | OPA_MODE | Read/Write | 1-Boost mode, 0-Charger mode (default 0) |

(1) The range of weak battery voltage threshold (VLOWV) is 3.4V–3.7V with the offset of 3.4V and step of 100mV (default 3.7V).

Control/Battery Voltage Register (READ/WRITE)

Memory location: 02, Reset state: 0000 1010

| BIT | NAME | Read/Write | FUNCTION |
|---------|--------------------|------------|---|
| B7(MSB) | V _{OREG5} | Read/Write | Battery Regulation Voltage: 640 mV (default 0) |
| B6 | V _{OREG4} | Read/Write | Battery Regulation Voltage: 320 mV (default 0) |
| B5 | V _{OREG3} | Read/Write | Battery Regulation Voltage: 160 mV (default 0) |
| B4 | V _{OREG2} | Read/Write | Battery Regulation Voltage: 80 mV (default 0) |
| B3 | V _{OREG1} | Read/Write | Battery Regulation Voltage: 40 mV (default 1) |
| B2 | V _{OREG0} | Read/Write | Battery Regulation Voltage: 20 mV (default 0) |
| B1 | OTG_PL | Read/Write | Active at High level, 0-Active at Low level (default 1) |
| B0(LSB) | OTG_EN | Read/Write | Enable OTG Pin, 0-Disable OTG pin (default 0) |

- Charge voltage range is 3.5V–4.44V with the offset of 3.5V and step of 20mV (default 3.54V).

Vender/Part/Revision Register (READ only)

Memory location: 03, Reset state: 0101 0000

| BIT | NAME | Read/Write | FUNCTION |
|---------|-----------|------------|--------------------------------|
| B7(MSB) | Vender2 | Read only | Vender Code: bit 2 (default 0) |
| B6 | Vender1 | Read only | Vender Code: bit 1 (default 1) |
| B5 | Vender0 | Read only | Vender Code: bit 0 (default 0) |
| B4 | PN1 | Read only | 10 |
| B3 | PN0 | Read only | |
| B2 | Revision2 | Read only | 000: Revision 1.0 |
| B1 | Revision1 | Read only | |
| B0(LSB) | Revision0 | Read only | |

Battery Termination/Fast Charge Current Register (READ/WRITE)

Memory location: 04, Reset state: 0000 0001

| BIT | NAME | Read/Write | FUNCTION |
|---------|---------------------|------------|---|
| B7(MSB) | Reset | Write only | Write: 1-Charger in reset mode, 0-No effect Read: always get "0" |
| B6 | V _{ICHRG3} | Read/Write | Charge current sense voltage: 27.2mV |
| B5 | V _{ICHRG2} | Read/Write | Charge current sense voltage: 13.6mV |
| B4 | V _{ICHRG1} | Read/Write | Charge current sense voltage: 6.8mV |
| B3 | V _{ICHRG0} | Read/Write | Charge current sense voltage: NA |
| B2 | V _{ITERM2} | Read/Write | Termination current sense voltage: 13.6mV (default 0) |
| B1 | V _{ITERM1} | Read/Write | Termination current sense voltage: 6.8mV (default 0) |
| B0(LSB) | V _{ITERM0} | Read/Write | Termination current sense voltage: 3.4mV (default 1) |

- Charge current sense voltage offset is 37.4mV and default charge current is 550mA, if 68-mΩ sensing resistor is used and LOW_CHG=0.
- The maximum charge current is 1.25A (Rsns=68mΩ) when charging from VBUS. If a higher value is programmed, the 1.25A or maximum safety limit charge current is selected

Special Charger Voltage/Enable Pin Status Register

Memory location: 05, Reset state: 001X X100

| BIT | NAME | Read/Write | FUNCTION |
|---------|--------------------|------------|---|
| B7(MSB) | NA | Read/Write | NA |
| B6 | VBUS_PRESENT | Read Only | 0—VBUS not connected, 1—VBUS present |
| B5 | LOW_CHG | Read/Write | 0—Normal charge current sense voltage at 04H, 1—Low charge current sense voltage of 22.1mV (default 1) |
| B4 | DPM_STATUS | Read Only | 0—DPM mode is not active, 1—DPM mode is active |
| B3 | VIN_PRESENT | Read Only | 0—VIN not connected, 1—Vin present |
| B2 | V _{SREG2} | Read/Write | Special charger voltage: 320 mV (default 1) |
| B1 | V _{SREG1} | Read/Write | Special charger voltage: 160 mV (default 0) |
| B0(LSB) | V _{SREG0} | Read/Write | Special charger voltage: 80 mV (default 0) |

- Special charger voltage offset is 4.2V and default special charger voltage is 4.52V.
- Default charge current will be 325mA, if 68-mΩ sensing resistor is used, since default LOW_CHG=1.

Safety Limit Register (READ/WRITE, Write only once after reset!)

Memory location: 06, Reset state: 01000000

| BIT | NAME | Read/Write | FUNCTION |
|---------|----------|------------|---|
| B7(MSB) | V_MCHRG3 | Read/Write | Maximum charge current sense voltage: 54.4 mV (default 0) |
| B6 | V_MCHRG2 | Read/Write | Maximum charge current sense voltage: 27.2 mV (default 1) |
| B5 | V_MCHRG1 | Read/Write | Maximum charge current sense voltage: 13.6 mV (default 0) |
| B4 | V_MCHRG0 | Read/Write | Maximum charge current sense voltage: 6.8 mV (default 0) |
| B3 | V_MREG3 | Read/Write | Maximum battery regulation voltage: 160 mV (default 0) |
| B2 | V_MREG2 | Read/Write | Maximum battery regulation voltage: 80 mV (default 0) |
| B1 | V_MREG1 | Read/Write | Maximum battery regulation voltage: 40 mV (default 0) |
| B0(LSB) | V_MREG0 | Read/Write | Maximum battery regulation voltage: 20 mV (default 0) |

- Maximum charge current sense voltage offset is 550mA (default at 950mA) and the maximum charge current option is 1.55A, if 68-mΩ sensing resistor is used.
- Maximum battery regulation voltage offset is 4.2V (default at 4.2V) and maximum battery regulation voltage option is 4.44V.

LED Configuration Register

Memory location: 07, Reset state: 10000010

| BIT | NAME | Read/Write | FUNCTION |
|---------|-----------|------------|--|
| B7(MSB) | I_LED1 | Read/Write | 00 – LED Off |
| B6 | I_LED0 | Read/Write | 01 – LED current 1.25mA 10 – LED current 2.5mA (default) 11 – LED current 5mA |
| B5 | NA | Read Only | Returns 0 |
| B4 | LED_CTRL | Read/Write | 0 – LED On when charging is Active (default) 1 – LED On regardless of charging status |
| B3 | t_LEDON1 | Read/Write | 00 – LED On time 130ms (default) |
| B2 | t_LEDON0 | Read/Write | 01 – LED On time 260ms 10 – LED On time 520ms 11 – LED Constant On |
| B1 | t_LEDOFF1 | Read/Write | 00 – LED Off time 390ms 01 – LED Off time 780ms 10 – LED Off time 1560ms (default) 11 – LED Off time 3120ms |
| B0(LSB) | t_LEDOFF0 | Read/Write | |

For I2C address 6AH (AC Charger)
Status/Control Register (READ/WRITE)

Memory location: 00, Reset state: x1xx 0xxx

| BIT | NAME | Read/Write | FUNCTION |
|---------|-------------|------------|---|
| B7(MSB) | TMR_RST/OTG | Read/Write | Write: TMR_RST function, write "1" to reset the safety timer (auto clear) Read: SLRST pin status, 0-SLRST pin at LOW level, 1-SLRST pin at HIGH level. |
| B6 | EN_STAT | Read/Write | 0-Disable STAT pin function, 1-Enable STAT pin function (default 1) |
| B5 | STAT2 | Read only | 00-Ready, 01-Charge in progress, 10-Charge done, 11-Fault |
| B4 | STAT1 | Read only | |
| B3 | NA | Read only | NA |
| B2 | FAULT_3 | Read only | Charge mode: 000-Normal, 001-VBUS OVP, 010-Sleep mode, 011-Bad Adaptor or VBUS<VUVLO, 100-Output OVP, 101-Thermal shutdown, 110-Timer fault, 111-No battery |
| B1 | FAULT_2 | Read only | |
| B0(LSB) | FAULT_1 | Read only | |

Control Register (READ/WRITE)

Memory location: 01, Reset state: 0111 0000

| BIT | NAME | Read/Write | FUNCTION |
|---------|------------------------|------------|---|
| B7(MSB) | Iin_Limit_2 | Read/Write | 00-USB host with 100-mA current limit, 01-USB host with 500-mA current limit, 10-USB host/charger with 800-mA current limit, 11-No input current limit (default 01) |
| B6 | Iin_Limit_1 | Read/Write | |
| B5 | VLOWV_2 ⁽¹⁾ | Read/Write | 200mV weak battery voltage threshold (default 1) |
| B4 | VLOWV_1 ⁽¹⁾ | Read/Write | 100mV weak battery voltage threshold (default 1) |
| B3 | TE | Read/Write | 1-Enable charge current termination, 0-Disable charge current termination (default 0) |
| B2 | /CE | Read/Write | 1-Charger is disabled, 0-Charger enabled (default 0) |
| B1 | HZ_MODE | Read/Write | 1-High impedance mode, 0-Not high impedance mode (default 0) |
| B0(LSB) | NA | Read/Write | NA |

(1) The range of weak battery voltage threshold (VLOWV) is 3.4V–3.7V with the offset of 3.4V and step of 100mV (default 3.7V).

Control/Battery Voltage Register (READ/WRITE)

Memory location: 02, Reset state: 0000 1010

| BIT | NAME | Read/Write | FUNCTION |
|---------|--------------------|------------|--|
| B7(MSB) | V _{OREG5} | Read/Write | Battery Regulation Voltage: 640 mV (default 0) |
| B6 | V _{OREG4} | Read/Write | Battery Regulation Voltage: 320 mV (default 0) |
| B5 | V _{OREG3} | Read/Write | Battery Regulation Voltage: 160 mV (default 0) |
| B4 | V _{OREG2} | Read/Write | Battery Regulation Voltage: 80 mV (default 0) |
| B3 | V _{OREG1} | Read/Write | Battery Regulation Voltage: 40 mV (default 1) |
| B2 | V _{OREG0} | Read/Write | Battery Regulation Voltage: 20 mV (default 0) |
| B1 | NA | Read/Write | NA |
| B0(LSB) | NA | Read/Write | NA |

- Charge voltage range is 3.5V–4.44V with the offset of 3.5V and step of 20mV (default 3.54V).

Vender/Part/Revision Register (READ only)

Memory location: 03, Reset state: 0100 0000

| BIT | NAME | Read/Write | FUNCTION |
|---------|-----------|------------|--------------------------------|
| B7(MSB) | Vender2 | Read only | Vender Code: bit 2 (default 0) |
| B6 | Vender1 | Read only | Vender Code: bit 1 (default 1) |
| B5 | Vender0 | Read only | Vender Code: bit 0 (default 0) |
| B4 | PN1 | Read only | 00 |
| B3 | PN0 | Read only | |
| B2 | Revision2 | Read only | 000: Revision 1.0 |
| B1 | Revision1 | Read only | |
| B0(LSB) | Revision0 | Read only | |

Battery Termination/Fast Charge Current Register (READ/WRITE)

Memory location: 04, Reset state: 0000 0001

| BIT | NAME | Read/Write | FUNCTION |
|---------|---------|------------|---|
| B7(MSB) | Reset | Write only | Write: 1-Charger in reset mode, 0-No effect Read: always get "0" |
| B6 | VICHRG3 | Read/Write | Charge current sense voltage: 54.4 mV (default 0) |
| B5 | VICHRG2 | Read/Write | Charge current sense voltage: 27.2 mV (default 0) |
| B4 | VICHRG1 | Read/Write | Charge current sense voltage: 13.6 mV (default 0) |
| B3 | VICHRG0 | Read/Write | Charge current sense voltage: 6.8 mV (default 0) |
| B2 | VITERM2 | Read/Write | Termination current sense voltage: 13.6 mV (default 0) |
| B1 | VITERM1 | Read/Write | Termination current sense voltage: 6.8 mV (default 0) |
| B0(LSB) | VITERM0 | Read/Write | Termination current sense voltage: 3.4 mV (default 1) |

- Charge current sense voltage offset is 37.4mV and default charge current is 550mA, if 68-mΩ sensing resistor is used and LOW_CHG=0.
- The maximum charge current is 1.55A when charging from VIN. If a higher value is programmed, the 1.55A or maximum safety limit charge current is selected.

Special Charger Voltage/Enable Pin Status Register

Memory location: 05, Reset state: 001X X100

| BIT | NAME | Read/Write | FUNCTION |
|---------|-------------|------------|--|
| B7(MSB) | NA | Read/Write | NA |
| B6 | VIN_PRESENT | Read Only | 0—VIN not connected, 1—Vin present |
| B5 | LOW_CHG | Read/Write | 0—Normal charge current sense voltage at 04H, 1—Low charge current sense voltage of 22.1mV (default 1) |
| B4 | DPM_STATUS | Read Only | 0—DPM mode is not active, 1—DPM mode is active |
| B3 | CD_STATUS | Read Only | 0—CD pin at LOW level, 1—CD pin at HIGH level |
| B2 | V_SREG2 | Read/Write | Special charger voltage: 320mV (default 1) |
| B1 | V_SREG1 | Read/Write | Special charger voltage: 160mV (default 0) |
| B0(LSB) | V_SREG0 | Read/Write | Special charger voltage: 80mV (default 0) |

- Special charger voltage offset is 4.2V and default special charger voltage is 4.52V.
- Default charge current will be 325mA, if 68-mΩ sensing resistor is used, since default LOW_CHG=1.

Safety Limit Register (READ/WRITE, Write only once after reset!)

Memory location: 06, Reset state: 01000000

| BIT | NAME | Read/Write | FUNCTION |
|---------|---------------------|------------|---|
| B7(MSB) | V _{MCHRG3} | Read/Write | Maximum charge current sense voltage: 54.4 mV (default 0) |
| B6 | V _{MCHRG2} | Read/Write | Maximum charge current sense voltage: 27.2 mV (default 1) |
| B5 | V _{MCHRG1} | Read/Write | Maximum charge current sense voltage: 13.6 mV (default 0) |
| B4 | V _{MCHRG0} | Read/Write | Maximum charge current sense voltage: 6.8 mV (default 0) |
| B3 | V _{MREG3} | Read/Write | Maximum battery regulation voltage: 160 mV (default 0) |
| B2 | V _{MREG2} | Read/Write | Maximum battery regulation voltage: 80 mV (default 0) |
| B1 | V _{MREG1} | Read/Write | Maximum battery regulation voltage: 40 mV (default 0) |
| B0(LSB) | V _{MREG0} | Read/Write | Maximum battery regulation voltage: 20 mV (default 0) |

- Maximum charge current sense voltage offset is 550mA (default at 950mA) and the maximum charge current option is 1.55A, if 68-mΩ sensing resistor is used.
- Maximum battery regulation voltage offset is 4.2V (default at 4.2V) and maximum battery regulation voltage option is 4.44V.
- Memory location 06 resets only when V_{BAT} voltage drops below V_{SHORT} threshold (typ.2.05V) or SLRST (pin C3) goes to logic '0'. After reset, the maximum values for battery regulation voltage and charge current can be programmed many times until any writing to other register locks the safety limits. Programmed values exclude higher values from memory locations 02 (battery regulation voltage), and from memory location 04 (Fast charge current).

If host accesses (write command) to some other register before safety limit register, the default values hold!

LED Configuration Register

Memory location: 07, Reset state: 10000010

| BIT | NAME | Read/Write | FUNCTION |
|---------|----------------------|------------|--|
| B7(MSB) | I _{LED1} | Read/Write | 00 – LED Off |
| B6 | I _{LED0} | Read/Write | 01 – LED current 1.25 mA 10 – LED current 2.5 mA (default) 11 – LED current mA |
| B5 | NA | Read Only | Returns 0 |
| B4 | LED_CTRL | Read/Write | 0 – LED On when charging is Active (default) 1 – LED On regardless of charging status |
| B3 | t _{LEDON1} | Read/Write | 00 – LED On time 13 ms (default) |
| B2 | t _{LEDON0} | Read/Write | 01 – LED On time 260 ms 10 – LED On time 520 ms 11 – LED Constant On |
| B1 | t _{LEDOFF1} | Read/Write | 00 – LED Off time 390 ms |
| B0(LSB) | t _{LEDOFF0} | Read/Write | 01 – LED Off time 780 ms 10 – LED Off time 1560 ms (default) 11 – LED Off time 3120 ms |

APPLICATION SECTION

Charge Current Sensing Resistor Selection Guidelines

Both the termination current range and charge current range depend on the sensing resistor (R_{SNS}). The termination current step ($I_{O(TERM_STEP)}$) can be calculated using [Equation 1](#):

$$I_{O(TERM_STEP)} = \frac{V_{I(TERM0)}}{R_{(SNS)}} \quad (1)$$

[Table 2](#) shows the termination current settings for three sensing resistors.

Table 2. Termination Current Settings for 55-m Ω , 68-m Ω , 100-m Ω Sense Resistors

| BIT | $V_{I(TERM)}$ (mV) | $I_{(TERM)}$ (mA) $R_{(SNS)} = 55m\Omega$ | $I_{(TERM)}$ (mA) $R_{(SNS)} = 68m\Omega$ | $I_{(TERM)}$ (mA) $R_{(SNS)} = 100m\Omega$ |
|----------------|--------------------|--|--|---|
| $V_{I(TERM2)}$ | 13.6 | 247 | 200 | 136 |
| $V_{I(TERM1)}$ | 6.8 | 124 | 100 | 68 |
| $V_{I(TERM0)}$ | 3.4 | 62 | 50 | 34 |
| Offset | 3.4 | 62 | 50 | 34 |

The charge current step ($I_{O(CHARGE_STEP)}$) is calculated using [Equation 2](#):

$$I_{O(CHARGE_STEP)} = \frac{V_{I(CHRG0)}}{R_{(SNS)}} \quad (2)$$

[Table 3](#) shows the charge current settings for three sensing resistors.

Table 3. Charge Current Settings for 55-m Ω , 68-m Ω and 100-m Ω Sense Resistors

| BIT | $V_{I(REG)}$ (mV) | $I_{O(CHARGE)}$ (mA) $R_{(SNS)} = 55m\Omega$ | $I_{O(CHARGE)}$ (mA) $R_{(SNS)} = 68m\Omega$ | $I_{O(CHARGE)}$ (mA) $R_{(SNS)} = 100m\Omega$ |
|----------------|-------------------|---|---|--|
| $V_{I(CHRG3)}$ | 54.4 | 989 | 800 | 544 |
| $V_{I(CHRG2)}$ | 27.2 | 495 | 400 | 272 |
| $V_{I(CHRG1)}$ | 13.6 | 247 | 200 | 136 |
| $V_{I(CHRG0)}$ | 6.8 | 124 | 100 | 68 |
| Offset | 37.4 | 680 | 550 | 374 |

Output Inductor and Capacitance Selection Guidelines

The IC provides internal loop compensation. With the internal loop compensation, the highest stability occurs when the LC resonant frequency, f_o , is approximately 40 kHz (20 kHz to 80 kHz). [Equation 3](#) can be used to calculate the value of the output inductor, L_{OUT} , and output capacitor, C_{OUT} .

$$f_o = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 4.7 μ F and 47 μ F is recommended for C_{OUT} , see the application section for components selection.

POWER TOPOLOGIES

System Load After Sensing Resistor

One of the simpler high-efficiency topologies connects the system load directly across the battery pack, as shown in Figure 21. The input voltage has been converted to a usable system voltage with good efficiency from the input. When the input power is on, it supplies the system load and charges the battery pack at the same time. When the input power is off, the battery pack powers the system directly.

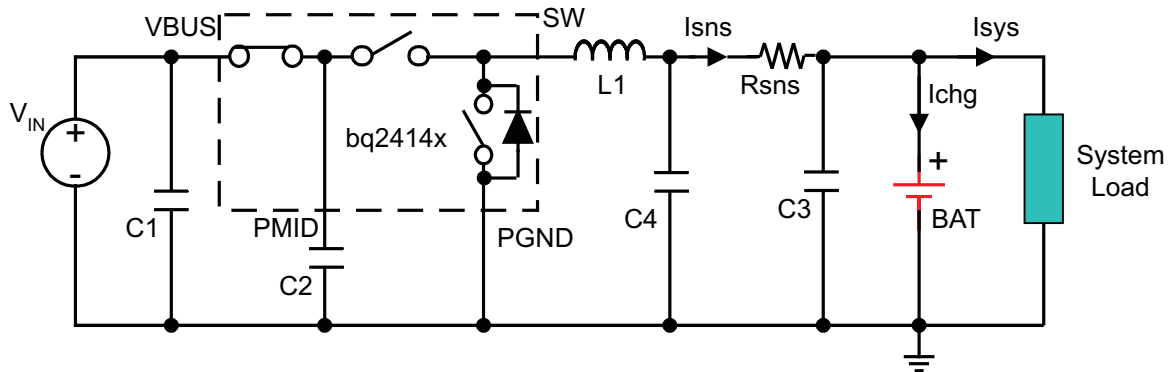


Figure 21. System Load After Sensing Resistor

The advantages:

1. When the AC adapter is disconnected, the battery pack powers the system load with minimum power dissipation. Consequently, the time that the system runs on the battery pack can be maximized.
2. It reduces the number of external path selection components and offers a low-cost solution.
3. Dynamic power management (DPM) can be achieved. The total of the charge current and the system current can be limited to a desired value by setting the charge current value. When the system current increases, the charge current drops by the same amount. As a result, no potential over-current or over-heating issues are caused by excessive system load demand.
4. The total input current can be limited to a desired value by setting the input current limit value. USB specifications can be met easily.
5. The supply voltage variation range for the system can be minimized.
6. The input current soft-start can be achieved by the generic soft-start feature of the IC.

Design considerations and potential issues:

1. If the system always demands a high current (but lower than the regulation current), the battery charging never terminates. Thus, the battery is always charged, and its lifetime may be reduced.
2. Because the total current regulation threshold is fixed and the system always demands some current, the battery may not be charged with a full-charge rate and thus may lead to a longer charge time.
3. If the system load current is large after the charger has been terminated, the IR drop across the battery impedance may cause the battery voltage to drop below the refresh threshold and start a new charge cycle. The charger would then terminate due to low charge current. Therefore, the charger would cycle between charging and terminating. If the load is smaller, the battery has to discharge down to the refresh threshold, resulting in a much slower cycling.
4. In a charger system, the charge current is typically limited to about 30mA, if the sensed battery voltage is below 2V short circuit protection threshold. This results in low power availability at the system bus. If an external supply is connected and the battery is deeply discharged, below the short circuit protection threshold, the charge current is clamped to the short circuit current limit. This then is the current available to the system during the power-up phase. Most systems cannot function with such limited supply current, and the battery supplements the additional power required by the system. Note that the battery pack is already at the depleted condition, and it discharges further until the battery protector opens, resulting in a system shutdown.
5. If the battery is below the short circuit threshold and the system requires a bias current budget lower than the short circuit current limit, the end-equipment will be operational, but the charging process can be affected

depending on the current left to charge the battery pack. Under extreme conditions, the system current is close to the short circuit current levels and the battery may not reach the fast-charge region in a timely manner. As a result, the safety timers flag the battery pack as defective, terminating the charging process. Because the safety timer cannot be disabled, the inserted battery pack must not be depleted to make the application possible.

6. If the battery pack voltage is too low, highly depleted, totally dead or even shorted, the system voltage is clamped by the battery and it cannot operate even if the input power is on.

System Load Before Sensing Resistor

The second circuit is similar to first one; the difference is that the system load is connected before the sense resistor, as shown in [Figure 22](#).

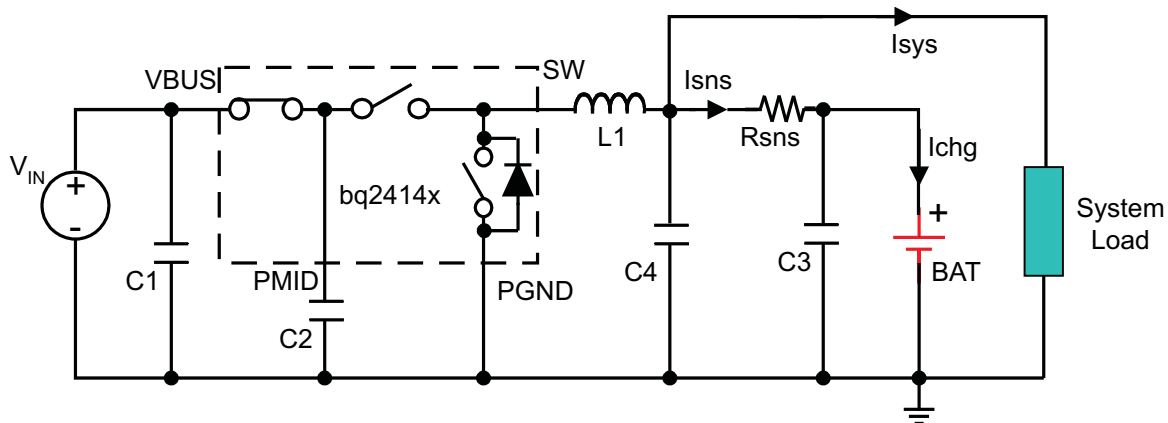


Figure 22. System Load Before Sensing Resistor

The advantages of system load before sensing resistor to system load after sensing resistor:

1. The charger controller is based only on the current going through the current-sense resistor. So, the constant current fast charge and termination functions operate without being affected by the system load. This is the major advantage of having the system load connected before the sense resistor.
2. A depleted battery pack can be connected to the charger without the risk of the safety timer expiration caused by high system load.
3. The charger can disable termination and keep the converter running to keep battery fully charged; or let the switcher terminate when the battery is full and then allow the system to run off of the battery through the sense resistor.

Design considerations and potential issues:

1. The total current is limited by the IC input current limit, or peak current protection, but not the charge current setting. The charge current does not drop when the system current load increases until the input current limit is reached. This solution is not recommended if the system requires a high current.
2. Efficiency declines when discharging through the sense resistor to the system.
3. No thermal regulation. Therefore, the system design should ensure the maximum junction temperature of the IC is below 125°C during normal operation.

DESIGN EXAMPLE FOR TYPICAL APPLICATION CIRCUIT

Systems Design Specifications:

- $V_{BUS} = 5\text{ V}$
 - $V_{BAT} = 4.2\text{ V}$ (1-Cell)
 - $I_{(charge)} = 1.25\text{ A}$
 - Inductor ripple current = 30% of fast charge current
1. Determine the inductor value (L_{OUT}) for the specified charge current ripple:

$$L_{OUT} = \frac{V_{BAT} \times (V_{BUS} - V_{BAT})}{V_{BUS} \times f \times \Delta I_L}$$
, the worst case is when battery voltage is as close as to half of the input voltage.

$$L_{OUT} = \frac{2.5 \times (5 - 2.5)}{5 \times (3 \times 10^6) \times 1.25 \times 0.3} \quad (4)$$

$$L_{OUT} = 1.11\ \mu\text{H}$$

Select the output inductor to standard 1 μH . Calculate the total ripple current with using the 1- μH inductor:

$$\Delta I_L = \frac{V_{BAT} \times (V_{BUS} - V_{BAT})}{V_{BUS} \times f \times L_{OUT}} \quad (5)$$

$$\Delta I_L = \frac{2.5 \times (5 - 2.5)}{5 \times (3 \times 10^6) \times (1 \times 10^{-6})} \quad (6)$$

$$\Delta I_L = 0.42\text{ A}$$

Calculate the maximum output current:

$$I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

$$I_{LPK} = 1.25 + \frac{0.42}{2} \quad (8)$$

$$I_{LPK} = 1.46\text{ A}$$

Select 2.5mm by 2mm 1- μH 1.5-A surface mount multi-layer inductor. The suggested inductor part numbers are shown as following.

Table 4. Inductor Part Numbers

| PART NUMBER | INDUCTANCE | SIZE | MANUFACTURER |
|----------------|------------|--------------|-----------------|
| LQM2HPN1R0MJ0 | 1 μ H | 2.5 x 2.0 mm | Murata |
| MIPS2520D1R0 | 1 μ H | 2.5 x 2.0 mm | FDK |
| MDT2520-CN1R0M | 1 μ H | 2.5 x 2.0 mm | TOKO |
| CP1008 | 1 μ H | 2.5 x 2.0 mm | Inter-Technical |

2. Determine the output capacitor value (C_{OUT}) using 40 kHz as the resonant frequency:

$$f_0 = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (9)$$

$$C_{OUT} = \frac{1}{4\pi^2 \times f_0^2 \times L_{OUT}} \quad (10)$$

$$C_{OUT} = \frac{1}{4\pi^2 \times (40 \times 10^3)^2 \times (1 \times 10^{-6})} \quad (11)$$

$$C_{OUT} = 15.8 \mu\text{F}$$

Select two 0603 X5R 6.3V 10- μ F ceramic capacitors in parallel i.e., Murata GRM188R60J106M.

3. Determine the sense resistor using the following equation:

$$R_{(SNS)} = \frac{V_{(RSNS)}}{I_{(CHARGE)}} \quad (12)$$

The maximum sense voltage across the sense resistor is 85 mV. In order to get a better current regulation accuracy, $V_{(RSNS)}$ should equal 85mV, and calculate the value for the sense resistor.

$$R_{(SNS)} = \frac{85\text{mV}}{1.25\text{A}} \quad (13)$$

$$R_{(SNS)} = 68 \text{ m}\Omega$$

This is a standard value. If it is not a standard value, then choose the next close value and calculate the real charge current. Calculate the power dissipation on the sense resistor:

$$P_{(RSNS)} = I_{(CHARGE)}^2 \times R_{(SNS)}$$

$$P_{(RSNS)} = 1.25^2 \times 0.068$$

$$P_{(RSNS)} = 0.106 \text{ W}$$

Select 0402 0.125-W 68-m Ω 2% sense resistor, i.e. Panasonic ERJ2BWGR068.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| BQ24140YFFR | ACTIVE | DSBGA | YFF | 30 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24140 | Samples |
| BQ24140YFFT | ACTIVE | DSBGA | YFF | 30 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24140 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

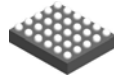
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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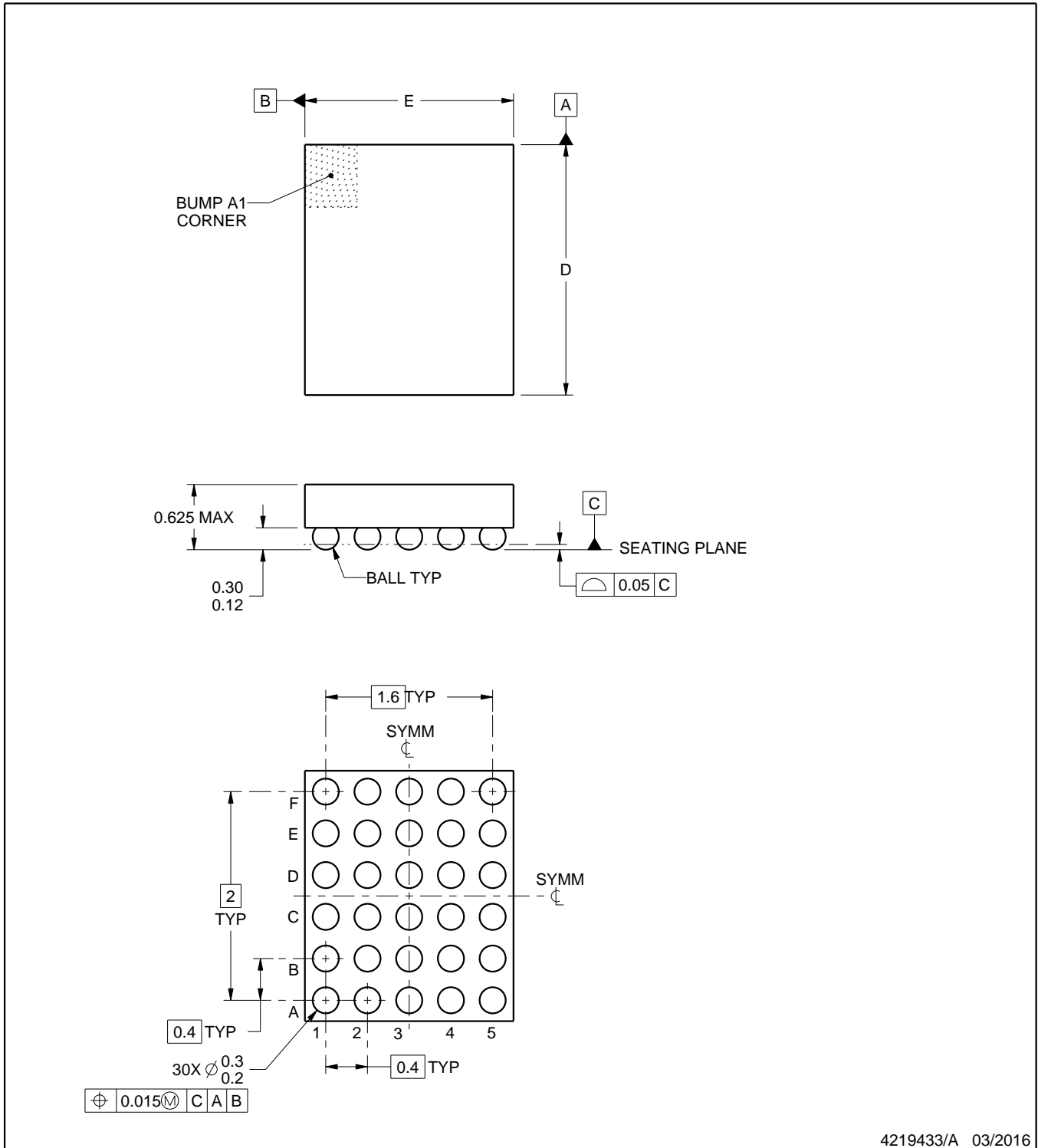
YFF0030



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4219433/A 03/2016

NOTES:

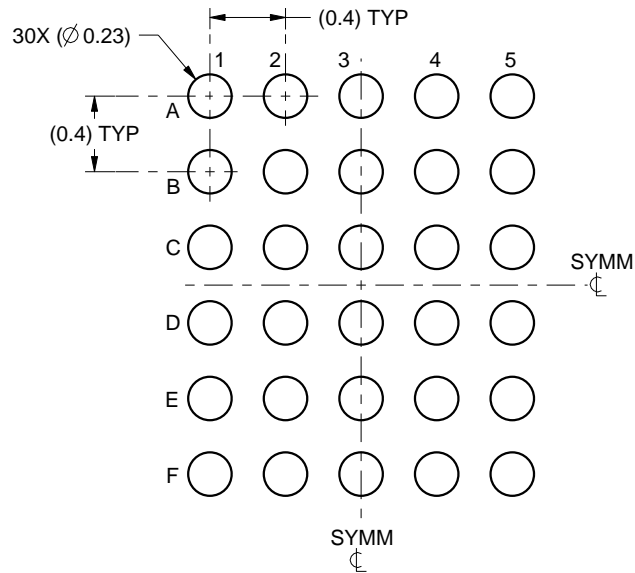
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

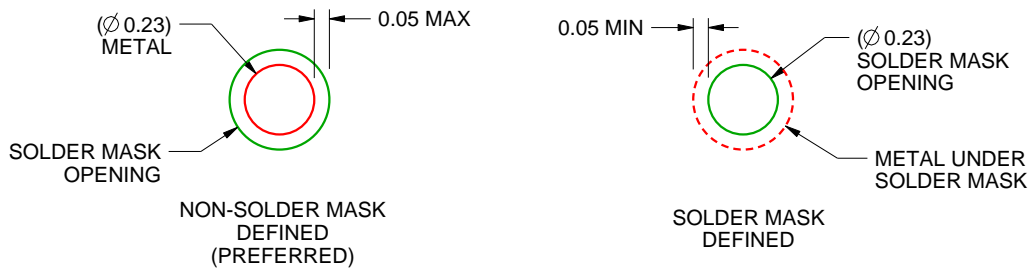
YFF0030

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

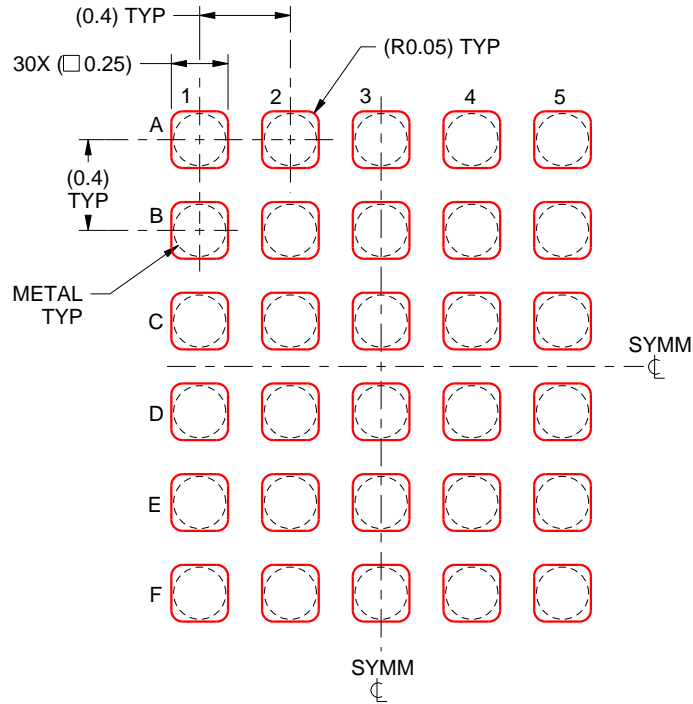
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0030

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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