TPS735-Q1 500mA 低静态电流、低噪声、高 PSRR 低压降线性稳压器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：–40°C 至 125°C 的环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 输入电压：2.7V 至 6.5V
- 带 EN 引脚的 500mA 低压降稳压器
- 低 I_Q：46µA
- 提供了多个输出电压版本：
  - 1V 至 4.3V 固定输出
  - 1.25V 至 6V 可调节输出
- 高 PSRR：1kHz 频率下为 68dB
- 低噪声：13.2µV_{RMS}
- 快速启动时间：45µs
- 与低 ESR 2µF 输出电容器一起工作时保持稳定
- 出色的负载和线路瞬态响应
- 2% 的总体精度（负载、线路、温度，V_{OUT} > 2.2V）
- 低压降：500mA 时为 280mV
- 3mm × 3mm VSON-8 封装

2 应用

- 车用信息娱乐
- 导航系统
- WiFi、WiMax 模块
- 远程信息处理系统
- 微处理器电源

3 说明

TPS735-Q1 低压降 (LDO)，低功耗线性稳压器系列产品能够提供出色的交流性能，同时还能保证极低的接地电流。可提供高电源抑制比 (PSRR)、低噪声、快速启动以及出色的线路和负载瞬态响应，同时消耗极低的 46µA（典型值）接地电流。

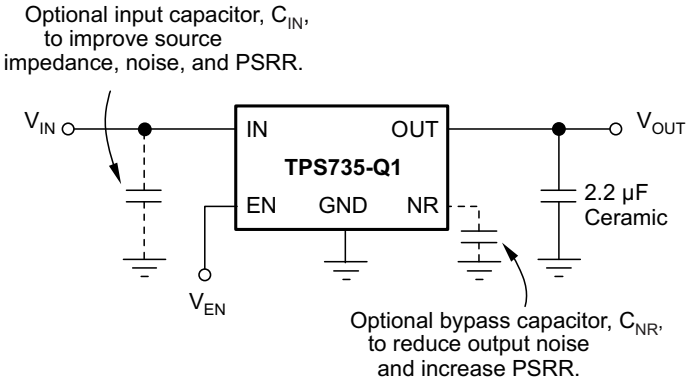
TPS735-Q1 系列器件与陶瓷电容器搭配使用时可保持稳定，并且该器件使用先进的 BiCMOS 制造工艺，能够在输出 500mA 输出电流时产生 280mV 的典型压降。TPS735-Q1 系列器件使用一个精度电压基准和反馈环路来实现 2% 的整体精度（包括全部负载、线路、过程和温度变化，V_{OUT} > 2.2V）。该系列器件的额定 T_A 为 –40°C 至 125°C，采用薄型 3mm × 3mm VSON 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS735-Q1	VSON (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用



目录

4 修订历史记录

Changes from Revision A (January 2015) to Revision B **Page**

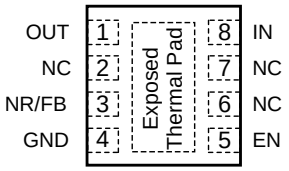
- 已添加 为第 1 页的图添加了标题 1
- Changed time scale from 10 ms to 10 µs in *TPS73525-Q1 Turn-On Response (V_{IN} = V_{EN})* figure 13
- Changed time scale from 10 ms to 10 µs in *TPS73525-Q1 Turn-On Response Using EN* figure 13

Changes from Original (October 2014) to Revision A **Page**

- 更改了产品预览文档 1

5 Pin Configuration and Functions

DRB Package
8-Pin VSON With Exposed Thermal Pad
Top View



NC = No internal connection.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. The EN pin can be connected to the IN pin if not used.
FB	3	I	This pin is only available for the adjustable version. The FB pin is the input to the control-loop error amplifier, and is used to set the output voltage of the device.
GND	4	—	Ground
IN	8	I	Input supply
NC	2, 6, 7	—	Not internally connected
NR	3	—	This pin is only available for the fixed voltage versions. Connecting an external capacitor to this pin bypasses noise generated by the internal band gap and allows the output noise to be reduced to very low levels. The maximum recommended capacitor is 0.01 µF.
OUT	1	O	This pin is the output of the regulator. A small 2-µF ceramic capacitor is required from this pin to ground to assure stability.
Exposed thermal pad		—	The pad must be tied to the GND pin.

6 Specifications

6.1 Absolute Maximum Ratings

At –40°C ≤ T_J and T_A ≤ 125°C (unless otherwise noted). All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	7	V
	V_{EN}	–0.3	V_{IN} + 0.3	V
	V_{FB}	–0.3	1.6	V
	V_{OUT}	–0.3	V_{IN} + 0.3	V
Current	I_{OUT}	Internally limited		A
Continuous total power dissipation	Continuous, $P_{D(tot)}$	See the *Power Dissipation* section		
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed as *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	2.7	6.5	V
V_{OUT}	Output voltage	V_{FB}	6	V
I_{OUT}	Output current(1)	0	500	mA
T_A	Operating free-air temperature	–40	125	°C

(1) When operating at T_J near 125°C, $I_{OUT(min)}$ is 500 µA.

6.4 Thermal Information

THERMAL METRIC(1)		TPS735-Q1 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

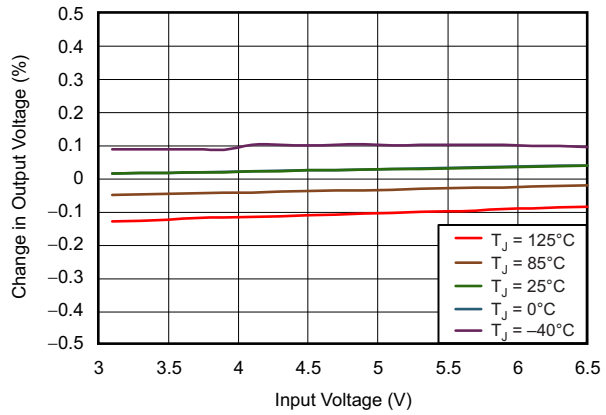
Over operating temperature range (–40°C ≤ T_J, T_A ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted.
For the adjustable version (TPS73501-Q1), V_{OUT} = 3 V. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage(1)			2.7		6.5	V
V_{FB}	Internal reference (TPS73501-Q1)	T_J = 25°C		1.196	1.208	1.220	V
V_{OUT}	Output voltage range (TPS73501-Q1)			V_{FB}		6	V
	DC output accuracy(1)	1 mA ≤ I_{OUT} ≤ 500 mA, V_{OUT} + 0.5 V ≤ V_{IN} < 6.5 V	V_{OUT} > 2.2 V	–2%	±1%	2%	
			V_{OUT} ≤ 2.2 V	–3%	±1%	3%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)	V_{OUTnom} + 0.5 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	500 µA ≤ I_{OUT} ≤ 500 mA			0.005		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = V_{OUTnom} – 0.1 V)	I_{OUT} = 500 mA			280	500	mV
I_{LIM}	Output current limit	V_{OUT} = 0.9 × V_{OUTnom}, V_{IN} = V_{OUTnom} + 0.9 V, V_{IN} ≥ 2.7 V		800	1170	1900	mA
I_{GND}	Ground pin current	10 mA ≤ I_{OUT} ≤ 500 mA			45	65	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0 V			0.15	1	µA
I_{FB}	Feedback pin current (TPS73501-Q1)	V_{OUTnom} = 1.2 V		–0.5		0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.85 V, V_{OUT} = 2.85 V, C_{NR} = 0.01 µF, I_{OUT} = 100 mA	f = 100 Hz		60		dB
			f = 1k Hz		68		dB
			f = 10 kHz		41		dB
			f = 100 kHz		21		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	C_{NR} = 0.01 µF		11 × V_{OUT}		μV_{RMS}
			C_{NR} = none		95 × V_{OUT}		μV_{RMS}
t_{STR}	Startup time	C_{NR} = none			45		µs
		C_{NR} = 0.001 µF			45		µs
		C_{NR} = 0.01 µF			50		µs
		C_{NR} = 0.047 µF			50		µs
$V_{EN(HI)}$	Enable high (enabled)			1.2			V
$V_{EN(LO)}$	Enable low (shutdown)					0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1	µA
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		°C
UVLO	Undervoltage lockout	V_{IN} rising		1.9	2.2	2.65	V
V_{hys}	Hysteresis	V_{IN} falling			70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater.
(2) V_{DO} is not measured for this family of devices with V_{OUTnom} < 2.8 V because the minimum V_{IN} = 2.7 V.

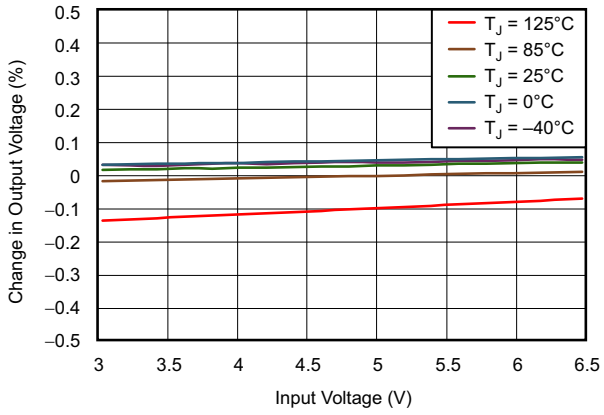
6.6 Typical Characteristics

Over operating temperature range (–40°C ≤ T_J, T_A ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted. T_A = 25°C, unless otherwise noted.



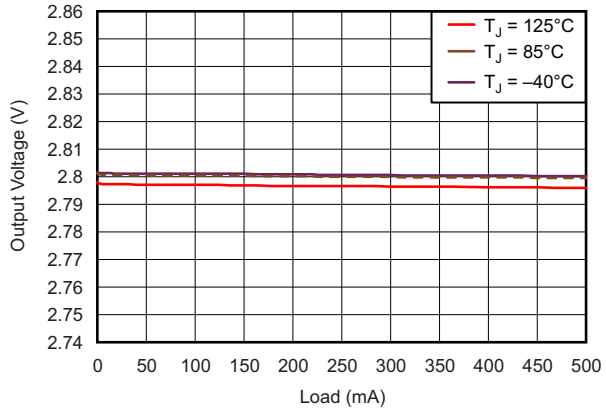
I_{OUT} = 100 mA

Figure 1. TPS73501-Q1 Line Regulation



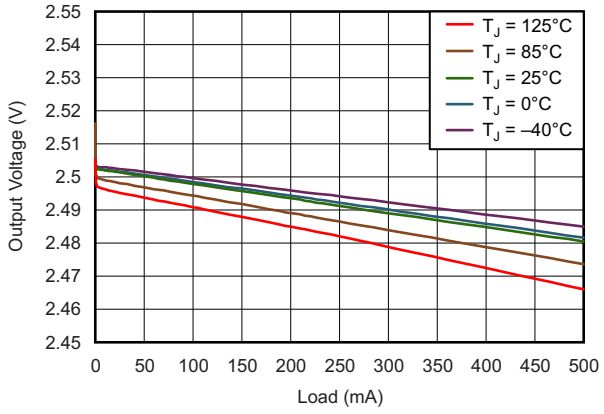
I_{OUT} = 100 mA

Figure 2. TPS73525-Q1 Line Regulation



The y-axis range is ±2% of 2.8 V

Figure 3. TPS73501-Q1 Load Regulation



The y-axis range is ±2% of 2.5 V

Figure 4. TPS73525-Q1 Load Regulation

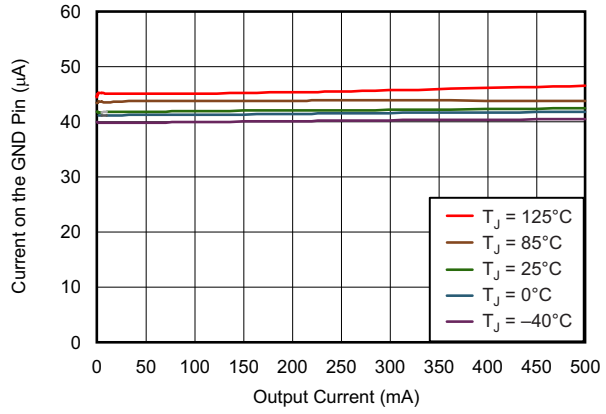
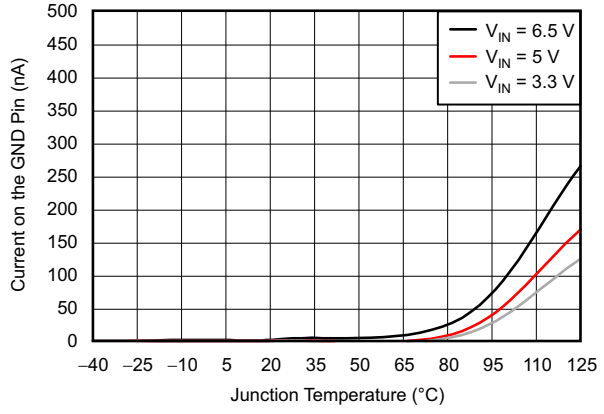


Figure 5. TPS73525-Q1 Ground Pin Current vs Output Current



V_{EN} = 0.4 V

Figure 6. TPS73525-Q1 Ground Pin Current (Disable) vs Temperature

Typical Characteristics (continued)

Over operating temperature range (–40°C ≤ T_J, T_A ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted. T_A = 25°C, unless otherwise noted.

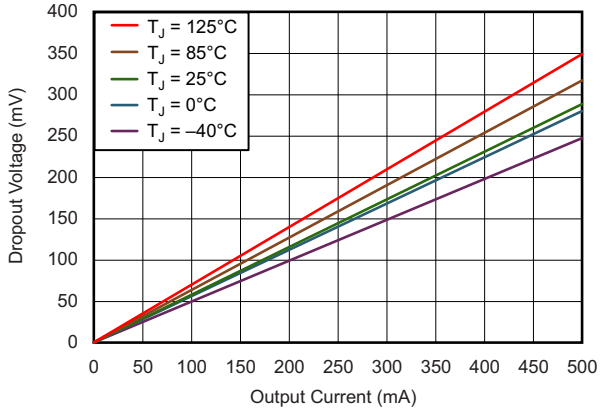


Figure 7. TPS73501-Q1 Dropout Voltage vs Output Current

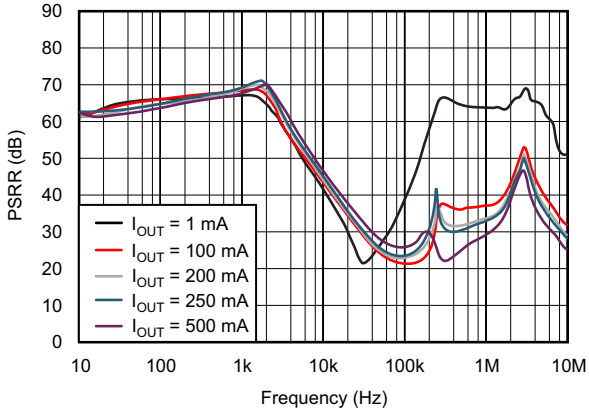


Figure 8. Power-Supply Ripple Rejection vs Frequency (V_{IN} – V_{OUT} = 1 V)

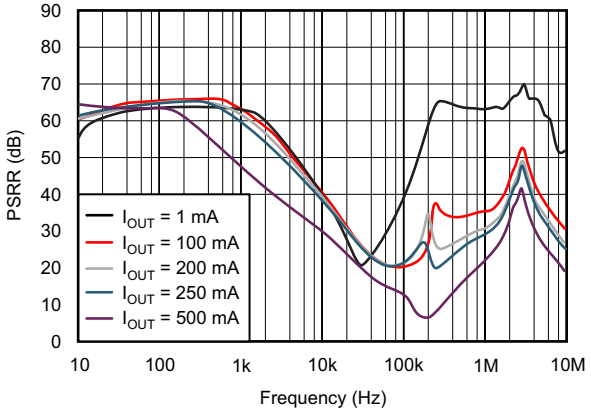


Figure 9. Power-Supply Ripple Rejection vs Frequency (V_{IN} – V_{OUT} = 0.5 V)

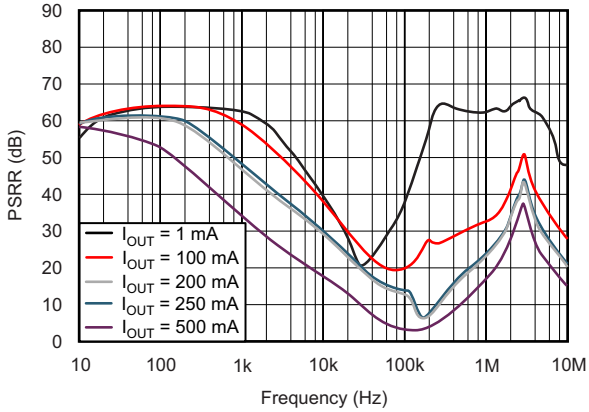


Figure 10. Power-Supply Ripple Rejection vs Frequency (V_{IN} – V_{OUT} = 0.3 V)

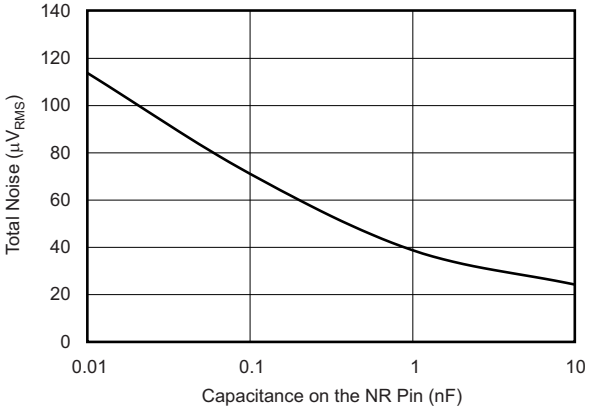
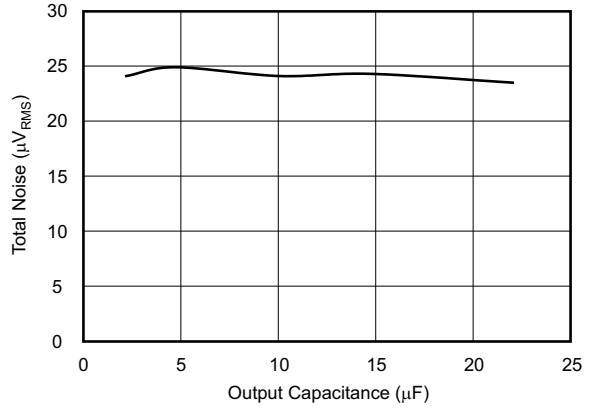


Figure 11. TPS73525-Q1 RMS Noise vs C_{NR}



C_{NR} = 0.01 µF, I_{OUT} = 1 mA

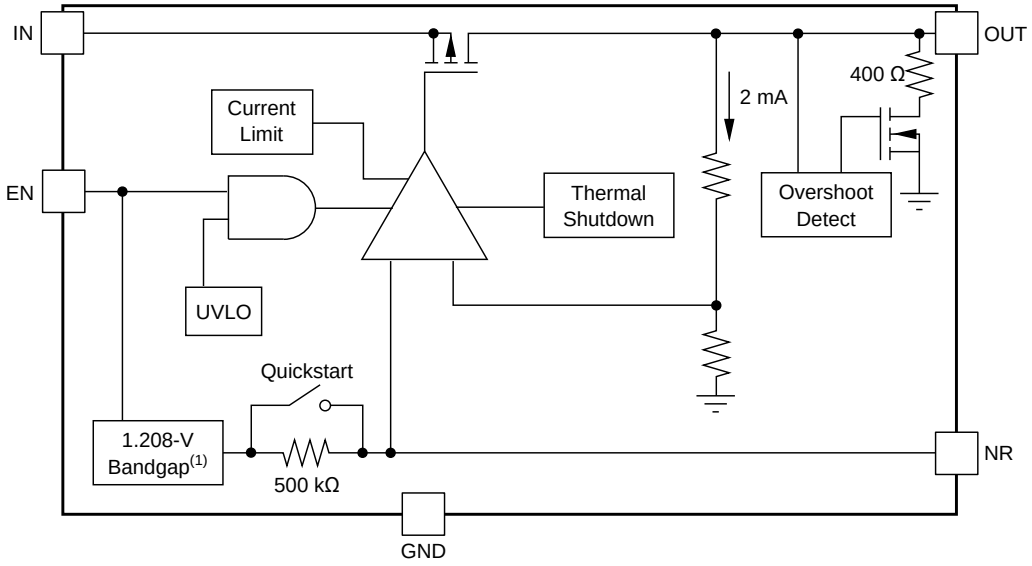
Figure 12. TPS73525-Q1 RMS Noise vs C_{OUT}

7 Detailed Description

7.1 Overview

The TPS735-Q1 family of low dropout (LDO) regulators combines the high performance required by many radio frequency (RF) and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection and very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS735-Q1 family of devices an excellent choice for portable applications. All versions have thermal and overcurrent protection and are fully specified from –40°C ≤ T_J, T_A ≤ 125°C.

7.2 Functional Block Diagram



NOTE: Fixed voltage versions between 1 V to 1.2 V have a 1-V band-gap circuit instead of a 1.208-V band-gap circuit.

Figure 13. Fixed Voltage Versions

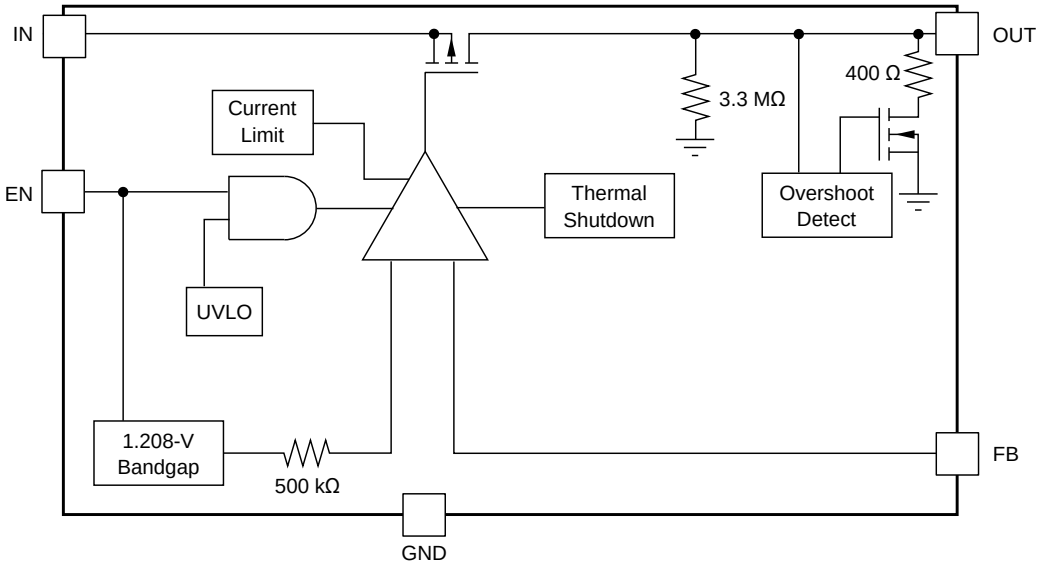


Figure 14. Adjustable Voltage Versions

7.3 Feature Description

7.3.1 Internal Current-Limit

The TPS735-Q1 internal current-limit helps protect the regulator during fault conditions. During current-limit, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in current-limit for extended periods of time.

The PMOS pass element in the TPS735-Q1 family of devices has a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting can be appropriate.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can be connected to the IN pin.

7.3.3 Dropout Voltage

The TPS735-Q1 family of devices uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance ($R_{(IN/OUT)}$) of the PMOS pass element. V_{DO} scales with the output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the *Typical Characteristics* section (see Figure 8 through Figure 10).

7.3.4 Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS735-Q1 family of devices use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see the *Functional Block Diagram* section). This architecture allows the combination of very-low output noise and fast startup times. The NR pin is high impedance so a low-leakage C_{NR} capacitor must be used. Most ceramic capacitors are appropriate in this configuration. A high-quality, COG-type (NPO) dielectric ceramic capacitor is recommended for C_{NR} when used in environments where abrupt changes in temperature can occur.

Note that for fastest start-up, apply V_{IN} first, then drive the enable pin (EN) high. If the EN pin is tied to the IN pin, start-up is somewhat slower. Refer to the *Typical Application* section (see Figure 17 and Figure 18). The quick-start switch is closed for approximately 135 μs. To ensure that C_{NR} is charged during the quick-start time, use a capacitor with a value of no more than 0.01 μF.

7.3.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the transient response duration. In the adjustable version, adding C_{FB} between the OUT and FB pins improves stability and transient response performance. The transient response of the TPS735-Q1 family of devices is enhanced by an active pulldown that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 400-Ω resistor to ground.

7.3.6 Undervoltage Lockout (UVLO)

The TPS735-Q1 family of devices uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that the UVLO typically ignores undershoot transients on the input if the transients are less than 50 μs in duration.

7.3.7 Minimum Load

The TPS735-Q1 family of devices is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. Below 500 μA and at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown to turn on. The output pulldown limits voltage drift to 5% (typically) but ground current can increase by approximately 50 μA. In most applications, the junction does not reach high temperatures at light loads because very little power is dissipated. Therefore, the specified ground current is valid at no load in most applications.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO voltage and has not decreased below the UVLO threshold minus V_{hys}.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the thermal shutdown temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is equal to the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and the LDO behaves like a resistor. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus V_{hys}, or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUTnom} + V_{DO}$ and $V_{IN} >$ UVLO	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 165°C$
Dropout mode	UVLO $< V_{IN} < V_{OUTnom} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	—	$T_J < 165°C$
Disabled mode (any true condition disables the device)	$V_{IN} <$ UVLO $– V_{hys}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > 165°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS735-Q1 family of automotive-qualified LDO regulators provides a design with an ultra-low noise, high PSRR, low-dropout linear regulation with a very small ground current (46 µA, typical).

The devices are stable with ceramic capacitors, and have a dropout voltage of 280 mV at the full output rating of 500 mA. The features of the TPS735-Q1 family of devices enables the LDO regulators to be suitable for a wide variety of applications, with minimal design complexity.

8.2 Typical Application

Figure 15 shows the basic circuit connections for fixed-voltage models. Figure 16 gives the connections for the adjustable output version (TPS73501-Q1). Use the equation in Figure 16 to calculate the value of R1 and R2 for any output voltage.

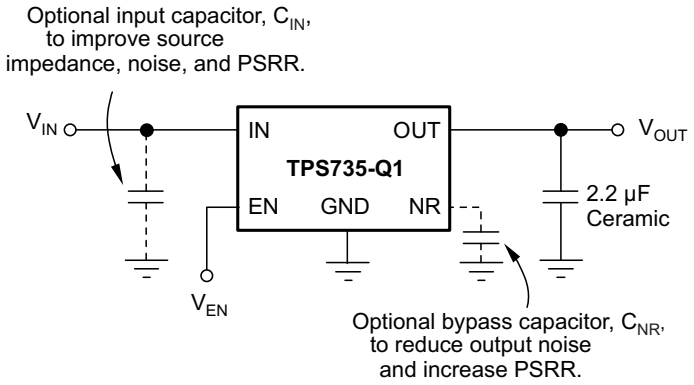


Figure 15. Typical Application Circuit for Fixed Voltage Versions

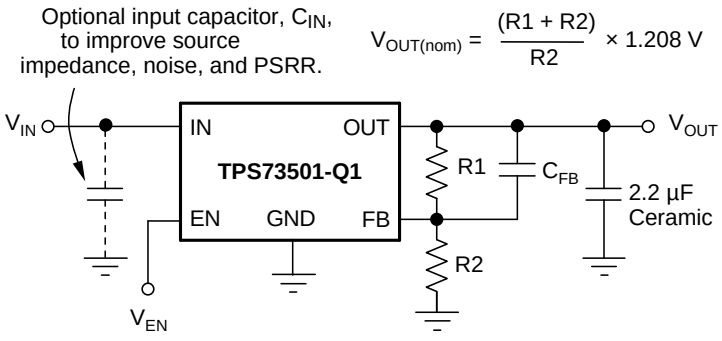


Figure 16. Typical Application Circuit for Adjustable Voltage Versions

Typical Application (continued)

8.2.1 Design Requirements

8.2.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a 0.1-μF to 1-μF low-equivalent series-resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher-value capacitor can be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor can be necessary to ensure stability.

The TPS735-Q1 family of devices is designed to be stable with standard ceramic output capacitors of values 2 μF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor is < 1 Ω and, therefore, the output capacitor type must either be ceramic or conductive polymer electrolytic.

8.2.1.2 Feedback Capacitor Requirements (TPS73501-Q1 only)

The feedback capacitor (C_{FB}), shown in Figure 16, is required for stability. For a parallel combination of R1 and R2 equal to 250 kΩ, any value between 3 pF to 1 nF can be used. Fixed voltage versions have an internal 30-pF feedback capacitor that is quick-charged at start-up. Larger value capacitors also improve noise slightly. The TPS73501-Q1 device is stable in unity-gain configurations (the OUT pin is tied to the FB pin) without C_{FB}.

8.2.2 Detailed Design Procedure

8.2.2.1 Output Noise

In most LDO regulators, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS735-Q1 family of devices, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output-resistor divider and the error-amplifier input. To minimize noise in a given application, use a 0.01-μF noise reduction capacitor. For the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2 μA of divider current has the same noise performance as a fixed voltage version with a C_{NR}. To further optimize noise, ESR of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing the total output noise up to 10%. The maximum recommended capacitor is 0.01 μF.

Equation 1 calculates the approximate integrated output noise from 10 Hz to 100 kHz with a C_{NR} value of 0.01 μF.

$$V_n\ (\mu V_{RMS}) = 11\ (\mu V_{RMS} / V) \times V_{OUT}\ (V) \quad (1)$$

The TPS73501-Q1 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the previously listed recommendations.

Typical Application (continued)

8.2.3 Application Curves

At V_{IN} = V_{OUTnom} + 0.5 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF, and T_A = 25°C, unless otherwise noted.

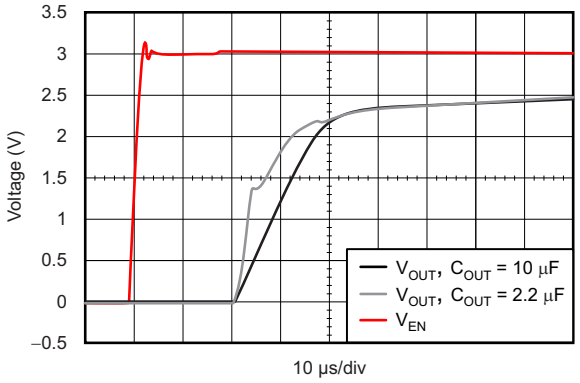


Figure 17. TPS73525-Q1 Turn-On Response (V_{IN} = V_{EN})

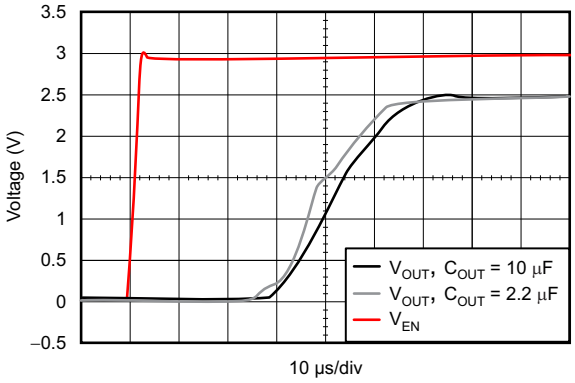


Figure 18. TPS73525-Q1 Turn-On Response Using EN

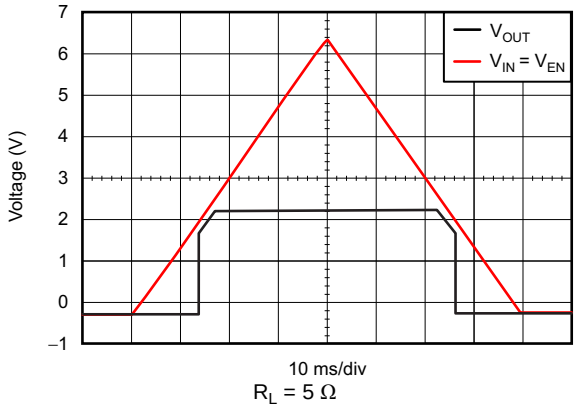


Figure 19. TPS73525-Q1 Power-Up and Power-Down (V_{IN} = V_{EN})

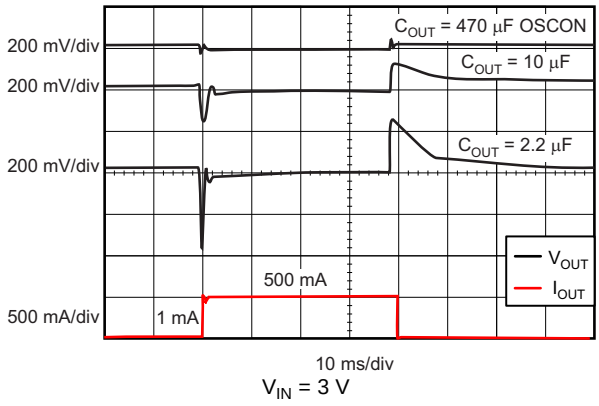


Figure 20. TPS73525-Q1 Load Transient Response

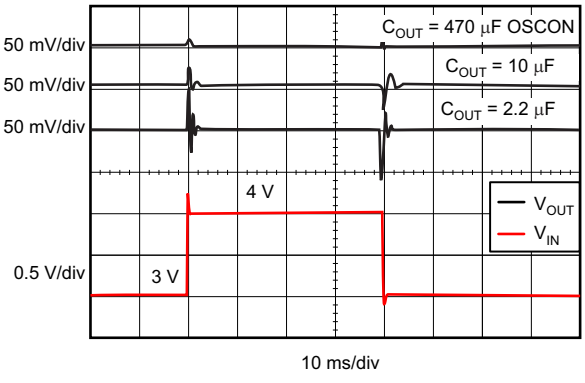


Figure 21. TPS73525-Q1 Line Transient Response

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the PowerPAD™. In most applications, this ground plane is necessary to meet thermal requirements.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for V_{IN} and V_{OUT} is recommended, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

10.1.2 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the thermal margin in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 40°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS735-Q1 family of devices is designed to protect against overload conditions. This protection circuitry is not intended to replace proper heatsinking. Continuously running the TPS735-Q1 family of devices into thermal shutdown degrades device reliability.

10.1.3 Package Mounting

Solder pad footprint recommendations for the TPS735-Q1 family of devices are available from the Texas Instruments web site at www.ti.com.

10.1.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Layout Guidelines (continued)

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

NOTE

When the device is used in a condition of high input and low output voltages, P_D can exceed the junction temperature rating even when the ambient temperature is at room temperature.

Equation 3 is an example calculation for the power dissipation (P_D) of the DRB package.

$$P_D = (6.5\ V – 1.2\ V) \times 500\ mA = 2.65\ W \quad (3)$$

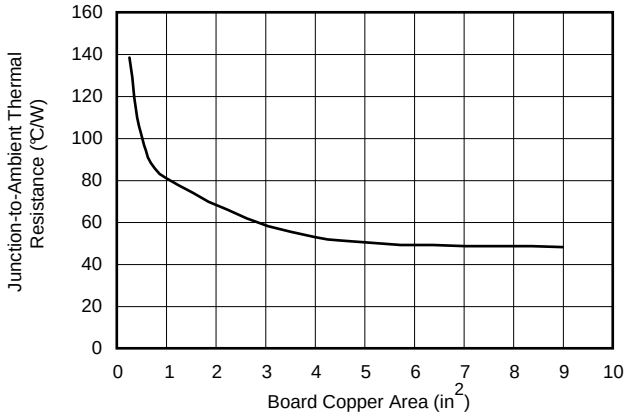
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output performance.

On the DRB package, the primary conduction path for heat is through the exposed thermal pad to the PCB. The pad can be connected to ground or left floating; however, the pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum allowable junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. Use Equation 4 to calculate the maximum junction-to-ambient thermal resistance.

$$R_{\theta JA} = \frac{(125°C – T_A)}{P_D} \quad (4)$$

Layout Guidelines (continued)

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 22.



NOTE: The $R_{\theta JA}$ value at a board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

Figure 22. $R_{\theta JA}$ vs Board Size

Figure 22 shows the variation of $R_{\theta JA}$ as a function of copper area in the board that is connected to the thermal pad. Figure 22 is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not to be used to calculate actual thermal performance.

NOTE

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

10.1.5 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with the corresponding formulas (given in Equation 5).

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipation calculated with Equation 2,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB temperature measured 1 mm away from the device package on the PCB surface (as shown in Figure 23). (5)

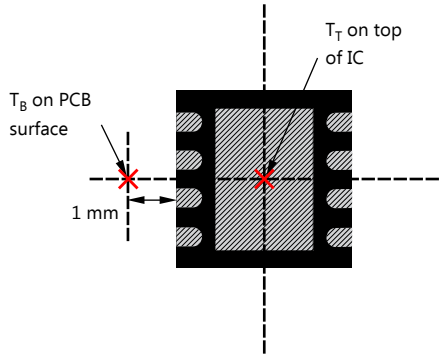


Figure 23. Measuring Points for T_T and T_B

Layout Guidelines (continued)

NOTE

Both T_T and T_B can be measured on actual application boards using an infrared thermometer.

For more information about measuring T_T and T_B, see the application note, *Using New Thermal Metrics*, SBVA025.

According to Figure 24, the thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on copper area. Using Ψ_{JT} or Ψ_{JB} with Equation 5 is a good way to estimate T_J by simply measuring T_T or T_B on an application board.

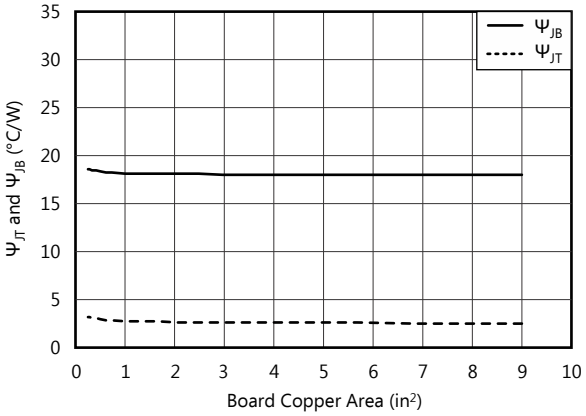
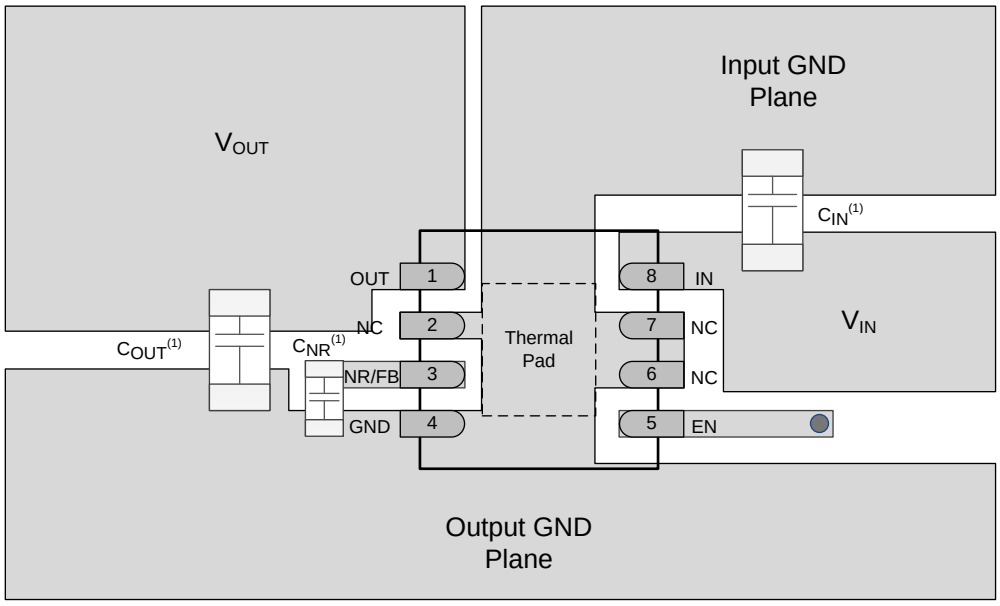


Figure 24. Ψ_{JT} and Ψ_{JB} vs Board Size

10.2 Layout Example



(1) C_{IN} and C_{OUT} are 0603 capacitors and C_{NR} is a 0402 capacitor. The footprint is shown to scale with package size.

Figure 25. TPS735-Q1 Fixed Version Layout Reference Diagram

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

表 2. 器件命名规则(1)

产品	V_{OUT}
TPS735**xx(x)***yyyz*	**XX(X)** 是标称输出电压。对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，33 = 3.3V；125 = 1.25V）。 **YYY** 为封装标识符。 **Z** 为卷带数量（R = 3000，T = 250）。 **01** 为可调版本。

(1) 要获得最新的封装和订购信息，请参阅本文档末尾的封装选项附录，或者访问 TI 网站 www.ti.com.cn。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《半导体和 IC 封装热指标应用报告》*
- 德州仪器 (TI)，*《TPS735xxEVM-276 用户指南》*
- 德州仪器 (TI)，*《使用新的热指标应用报告》*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

E2E is a trademark of Texas Instruments.
PowerPAD is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

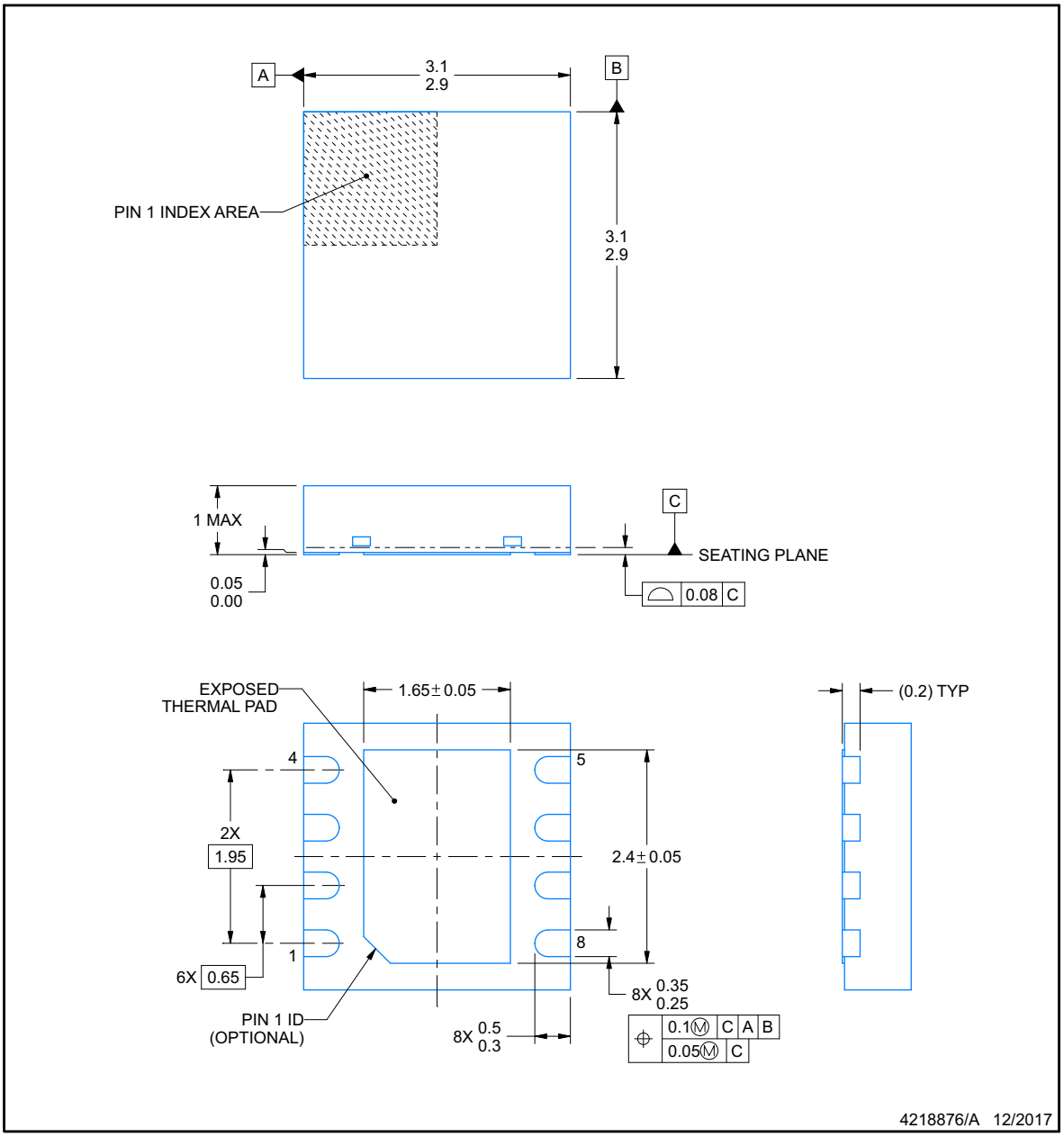
以下页面包含机械、封装和可订购信息。这些信息是针对指定器件系列提供的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

DRB0008B

PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

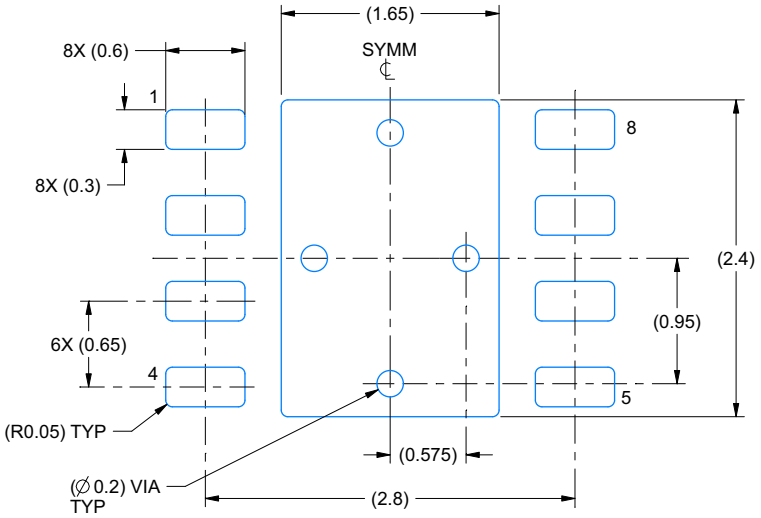
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

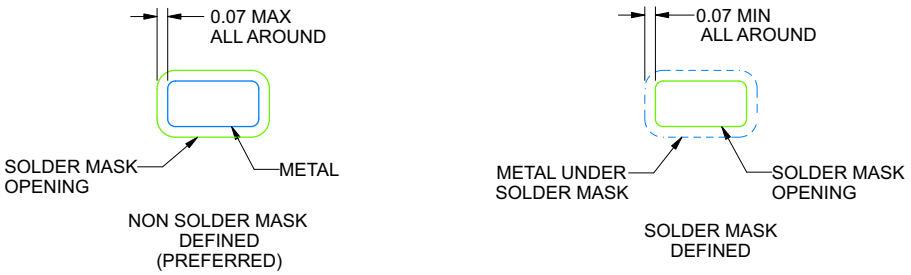
DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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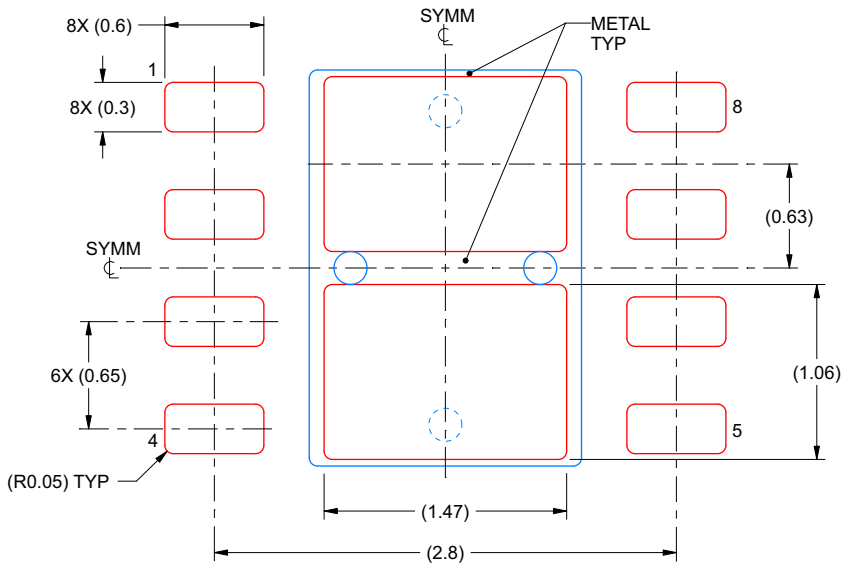
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008B — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73501QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	501DRB	Samples
TPS73512QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	512DRB	Samples
TPS73515QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	515DRB	Samples
TPS73518QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	518DRB	Samples
TPS73525QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	525DRB	Samples
TPS73527QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	527DRB	Samples
TPS73530QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	530DRB	Samples
TPS73533QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	533DRB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

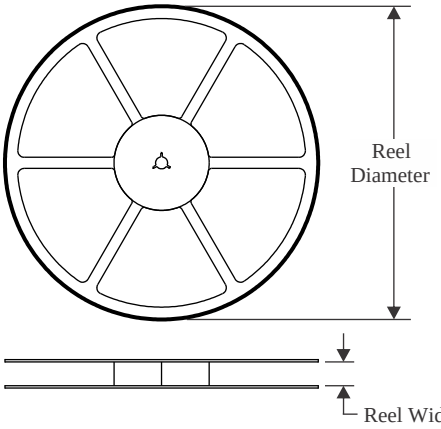
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

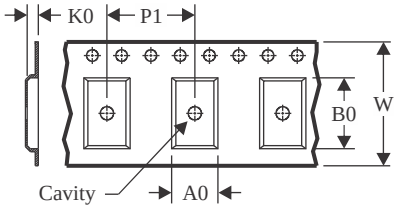
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

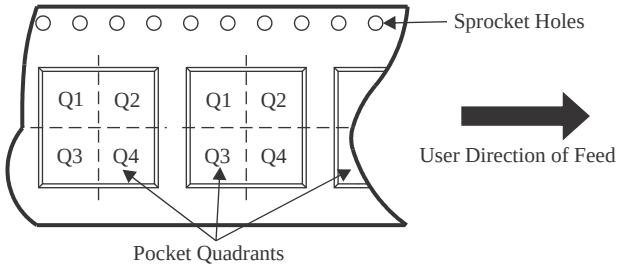


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

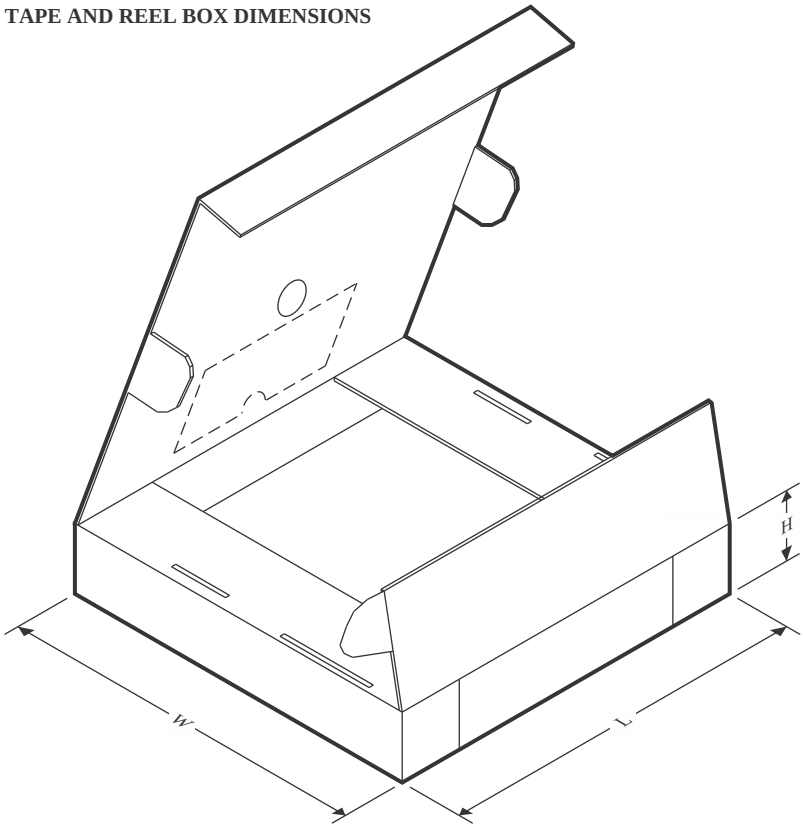
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73501QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73512QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73515QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73518QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73527QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73530QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73533QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73501QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73512QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73515QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73518QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73525QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73527QDRBRQ1	SON	DRB	8	3000	356.0	356.0	35.0
TPS73530QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73533QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

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