DRV421 用于闭环电流感测的集成磁通门传感器

1 特性

- 高精度、集成磁通门传感器
  - 偏移和漂移：±8μT（最大值），±5nT/°C（典型值）
- 扩展电流测量范围
  - H 桥输出驱动：5V 时的典型值为 ±250mA
- 精密分流感测放大器
  - 偏移和漂移（最大值）：±75μV，±2μV/°C
  - 增益误差和漂移（最大值）：±0.3%，±5ppm/°C
- 精密基准
  - 精度和漂移（最大值）：±2%，±50ppm/°C
  - 引脚可选电压：2.5V 或 1.65V
  - 可选比例模式：VDD/2
- 磁芯消磁功能
- 诊断 特性：超限和错误标志
- 电源电压范围：3.0V 至 5.5V
- 在 -40°C 至 +125°C 的扩展工业温度范围内完全额定运行

2 应用

- 闭环直流和交流电流传感器模块
- 泄漏电流传感器
- 工业用监控和控制系统
- 过流检测
- 频率、电压和太阳能逆变器

3 说明

DRV421 设计用于闭环磁流传感解决方案，可实现精密的隔离式直流和交流电流测量。该器件提供专有的集成磁通门传感器以及所需的模拟信号调节功能，从而最大限度减少组件数量和成本。磁通门传感器具有低偏移和漂移，再搭配上优化的前端电路，可提供无与伦比的测量精度。

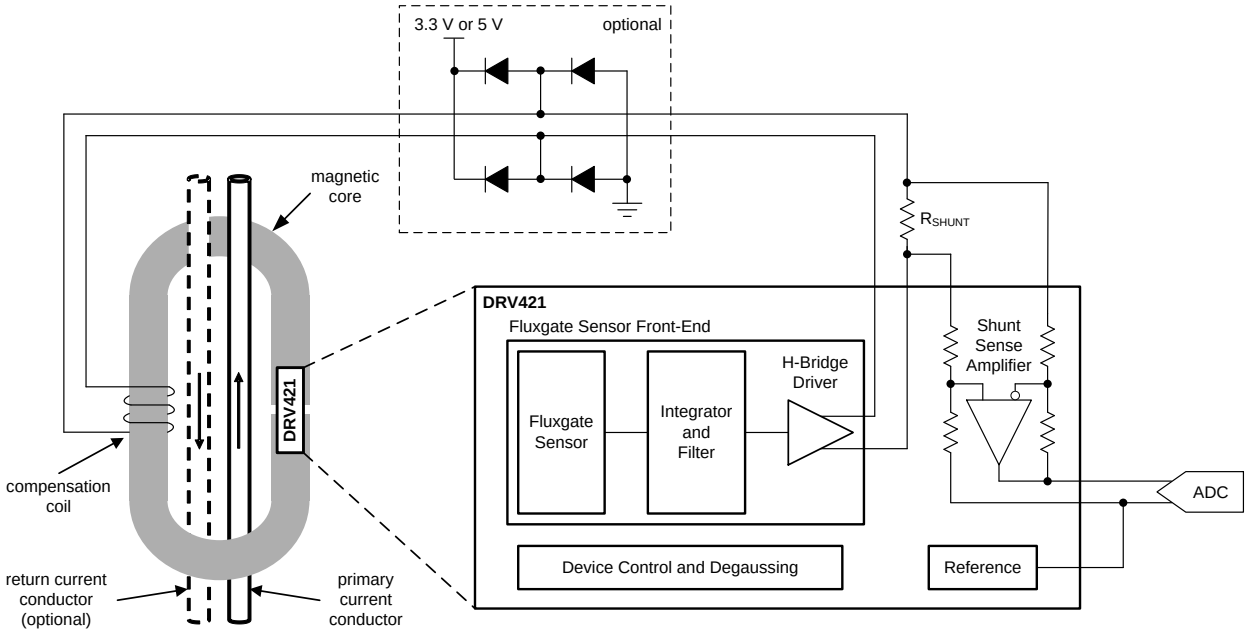
DRV421 提供驱动电流感测反馈环路所需的全部电路模块。传感器前端电路后跟一个滤波器，经配置可与各种磁芯搭配使用。该器件通过集成的 250mA H 桥来驱动补偿线圈，相比传统的单端驱动方式，可使电流测量范围扩大一倍。该器件同时提供精密基准电压和分流感测放大器，用以生成并驱动模拟输出信号。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV421	WQFN (20)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的封装选项附录。

典型应用



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (July 2015) to Revision B **Page**

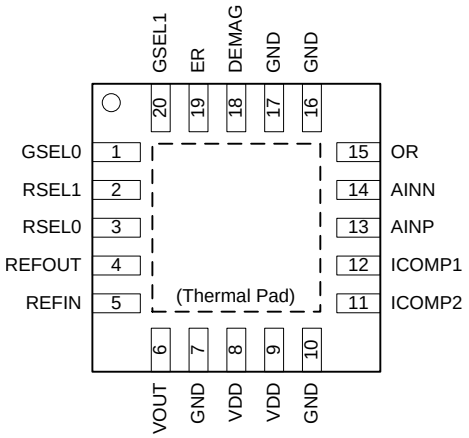
- 已添加 TI 设计 ... 1
- 已添加后两个*应用* 要点的措辞 ... 1
- Changed QFN to WQFN in pin configuration drawing ... 3
- Changed QFN to WQFN in *Thermal Information* table ... 4
- Changed QFN to WQFN in *Power Dissipation* section ... 34

Changes from Original (May 2015) to Revision A **Page**

- 已发布为量产数据 ... 1

5 Pin Configuration and Functions

RTJ Package
20-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AINN	14	I	Inverting input of shunt sense amplifier
AINP	13	I	Noninverting input of shunt sense amplifier
DEMAG	18	I	Degauss control input
ER	19	O	Error flag; open-drain, active low output
GND	7, 10, 16, 17	—	Ground reference
GSEL0	1	I	Gain and bandwidth selection input 0
GSEL1	20	I	Gain and bandwidth selection input 1
ICOMP1	12	O	Output 1 of compensation coil driver
ICOMP2	11	O	Output 2 of compensation coil driver
OR	15	O	Shunt sense amplifier overrange indicator; open-drain, active-low output
REFIN	5	I	Common-mode reference input for the shunt sense amplifier
REFOUT	4	O	Voltage reference output
RSEL0	3	I	Voltage reference mode selection input 0
RSEL1	2	I	Voltage reference mode selection input 1
VDD	8, 9	—	Supply voltage, 3.0 V to 5.5 V. Decouple both pins using 1-µF ceramic capacitors placed as close as possible to the device. See the *Power-Supply Decoupling* and *Layout* sections for further details.
VOUT	6	O	Shunt sense amplifier output
PowerPAD™		—	Connect thermal pad to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply voltage (VDD to GND)		–0.3	7	V
	Input voltage, except pins AINP and AINN (2)		GND – 0.5	V_{DD} + 0.5	
	Shunt sense amplifier inputs (pins AINP and AINN) (3)		GND – 6.0	V_{DD} + 6.0	
Current	Pins ICOMP1 and ICOMP2 (short circuit current I_{SC}) (4)		–300	300	mA
	Shunt sense amplifier inputs	pins AINP and AINN	–5	5	
		All remaining pins	–25	25	
Temperature	Junction, T_J max		–50	150	°C
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited, except for the shunt sense amplifier input pins.
(3) These inputs are not diode-clamped to the power supply rails.
(4) Power-limited; observe maximum junction temperature.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.0	5.0	5.5	V
T_A	Specified ambient temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		SBOS704 RTJ (WQFN) 20 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All minimum and maximum specifications at T_A = +25°C, V_{DD} = 3.0 V to 5.5 V, and I_{COMP1} = I_{COMP2} = 0 mA (unless otherwise noted). Typical values are at V_{DD} = 5.0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLUXGATE SENSOR FRONT-END						
	Offset (1)	No magnetic field	–8	±2	8	µT
	Offset drift	No magnetic field		±5		nT/°C
	Noise	f = 0.1 Hz to 10 Hz		17		nTrms
	Noise density	f = 1 kHz		1.5		nT/√Hz
	Saturation trip level for pin ER			1.7		mT
A_{OL}	DC open-loop gain			16		V/µT
	AC open-loop gain	GSEL[1:0] = 00, at 3.8 kHz, integration-to-flatband corner frequency		8.5		V/mT
		GSEL[1:0] = 01, at 3.8 kHz, integration-to-flatband corner frequency		38		
		GSEL[1:0] = 10, at 1.9 kHz, integration-to-flatband corner frequency		25		
		GSEL[1:0] = 11, at 1.9 kHz, integration-to-flatband corner frequency		70		
I_{ICOMP}	Peak current at pins ICOMP1 and ICOMP2	$V_{ICOMP1} – V_{ICOMP2}$ = 4.2 V_{PP}, V_{DD} = 5 V, T_A = –40°C to +125°C	210	250		mA
		$V_{ICOMP1} – V_{ICOMP2}$ = 2.5 V_{PP}, V_{DD} = 3.3 V, T_A = –40°C to +125°C	125	150		
V_{ICOMP}	Voltage swing at pins ICOMP1 and ICOMP2	20-Ω load, V_{DD} = 5 V, T_A = –40°C to +125°C	4.2			V_{PP}
		20-Ω load, V_{DD} = 3.3 V, T_A = –40°C to +125°C	2.5			
	Common-mode output voltage at pins ICOMP1 and ICOMP2			V_{REFOUT}		V
SHUNT SENSE AMPLIFIER						
V_{OO}	Output offset voltage	V_{AINP} = V_{AINN} = V_{REFIN}, V_{DD} = 3.0 V	–0.075	±0.01	0.075	mV
	Output offset voltage drift		–2	±0.4	2	µV/°C
CMRR	Common-mode rejection ratio, RTO (2)	V_{CM} = −1 V to V_{DD} + 1 V, V_{REFIN} = V_{DD} / 2	–250	±50	250	µV/V
$PSRR_{AMP}$	Power-supply rejection ratio, RTO	V_{DD} = 3.0 V to 5.5 V, V_{CM} = V_{REFIN}	–50	±4	50	µV/V
V_{IC}	Common-mode input voltage range		–1		V_{DD} + 1	V
Z_{IND}	Differential input impedance		16.5	20	23.5	kΩ
Z_{IC}	Common-mode input impedance		40	50	60	kΩ
G	Gain, V_{OUT} / (V_{AINP} – V_{AINN})			4		V/V
E_G	Gain error		–0.3%	±0.02%	0.3%	
	Gain error drift		–5	±1	5	ppm/°C
	Linearity error	R_L = 1 kΩ		12		ppm
	Voltage output swing from negative rail (OR pin trip level)	V_{DD} = 5.5 V, I_{VOUT} = 2.5 mA		48	85	mV
		V_{DD} = 3.0 V, I_{VOUT} = 2.5 mA		56	100	
	Voltage output swing from positive rail (OR pin trip level)	V_{DD} = 5.5 V, I_{VOUT} = –2.5 mA	V_{DD} – 85	V_{DD} – 48		mV
		V_{DD} = 3.0 V, I_{VOUT} = –2.5 mA	V_{DD} – 100	V_{DD} – 56		
I_{SC}	Short-circuit current	V_{OUT} connected to GND		–18		mA
		V_{OUT} connected to VDD		20		
	Signal overrange indication delay (OR pin)	V_{IN} = 1-V step		2.5 to 3.5		µs
$BW_{–3dB}$	Bandwidth			2		MHz
SR	Slew rate			6.5		V/µs
	Settling time, large-signal	ΔV = ± 2 V to 1% accuracy, no external filter		0.9		µs
	Settling time, small-signal	ΔV = ± 0.4 V to 0.01% accuracy		8		µs
e_n	Output voltage noise density, RTO	f = 1 kHz, compensation loop disabled		170		nV/√Hz
V_{REFIN}	Input voltage range at pin REFIN	T_A = –40°C to +125°C	GND		VDD	V

(1) Fluxgate sensor front-end offset can be reduced using the feature.
(2) Parameter value referred to output (RTO).

Electrical Characteristics (continued)

All minimum and maximum specifications at T_A = +25°C, V_{DD} = 3.0 V to 5.5 V, and I_{COMP1} = I_{COMP2} = 0 mA (unless otherwise noted). Typical values are at V_{DD} = 5.0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE						
V_{REFOUT}	Reference output voltage at pin REFOUT	RSEL[1:0] = 00, no load	2.45	2.5	2.55	V
		RSEL[1:0] = 01, no load	1.6	1.65	1.7	
		RSEL[1:0] = 1x, no load	45	50	55	% of VDD
	Reference output voltage drift	RSEL[1:0] = 00, 01	–50	±10	50	ppm/°C
	Voltage divider gain error drift	RSEL[1:0] = 1x	–50	±10	50	ppm/°C
$PSRR_{REF}$	Power-supply rejection ratio	RSEL[1:0] = 00, 01	–300	±15	300	µV/V
	Load regulation	RSEL[1:0] = 0x, load to GND or VDD, ΔI_{LOAD} = 0 mA to 5 mA, T_A = –40°C to +125°C		0.15	0.35	mV/mA
		RSEL[1:0] = 1x, load to GND or VDD, ΔI_{LOAD} = 0 mA to 5 mA, T_A = –40°C to +125°C		0.3	0.8	
I_{SC}	Short-circuit current	REFOUT connected to VDD		20		mA
		REFOUT connected to GND		–18		
DIGITAL INPUTS/OUTPUTS						
Logic Inputs (CMOS)						
V_{IH}	High-level input voltage	T_A = –40°C to +125°C	0.7 × VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage	T_A = –40°C to +125°C	–0.3		0.3 × VDD	V
	Input leakage current			0.01		µA
Logic Outputs (Open-Drain)						
V_{OH}	High-level output voltage		Set by external pull-up resistor			V
V_{OL}	Low-level output voltage	4-mA sink		0.3		V
POWER SUPPLY						
I_Q	Quiescent current	I_{ICOMP1} = I_{ICOMP2} = 0 mA, 3.0 V ≤ V_{DD} ≤ 3.6 V, T_A = –40°C to +125°C		6.5	9	mA
		I_{ICOMP1} = I_{ICOMP2} = 0 mA, 4.5 V ≤ V_{DD} ≤ 5.5 V, T_A = –40°C to +125°C		8.1	11	
V_{RST}	Power-on reset threshold			2.4		V

6.6 Typical Characteristics

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)

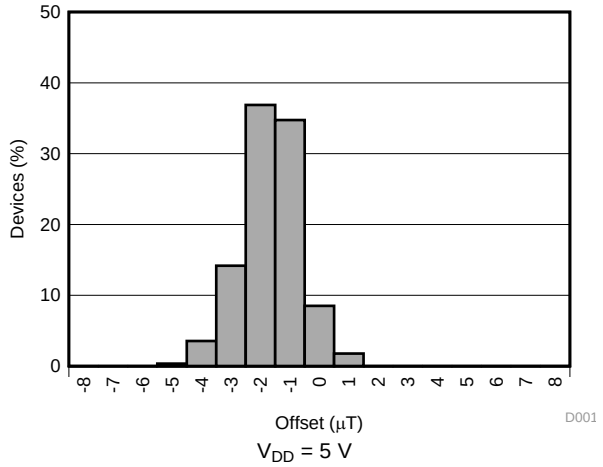


图 1. Fluxgate Sensor Front-End Offset Histogram

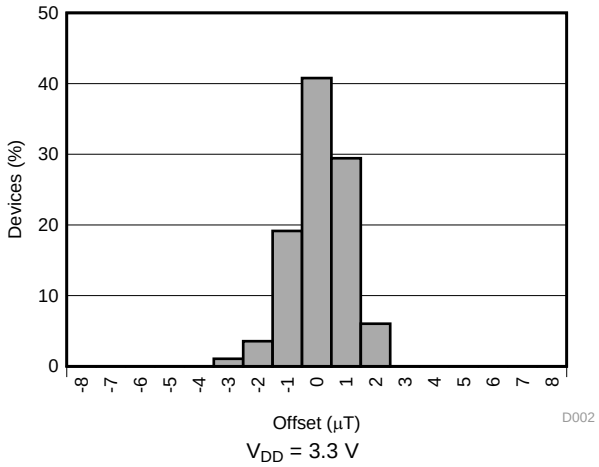


图 2. Fluxgate Sensor Front-End Offset Histogram

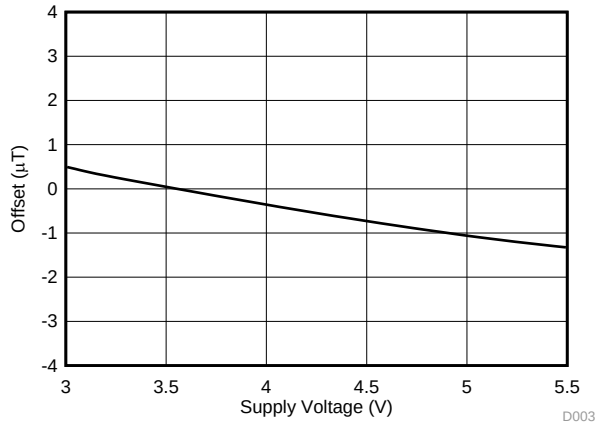


图 3. Fluxgate Sensor Front-End Offset vs Supply Voltage

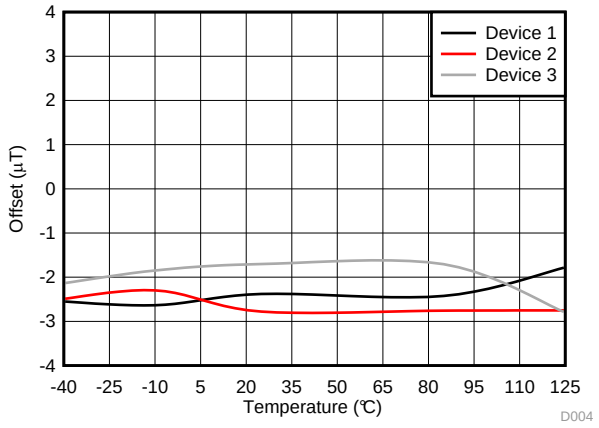


图 4. Fluxgate Sensor Front-End Offset vs Temperature

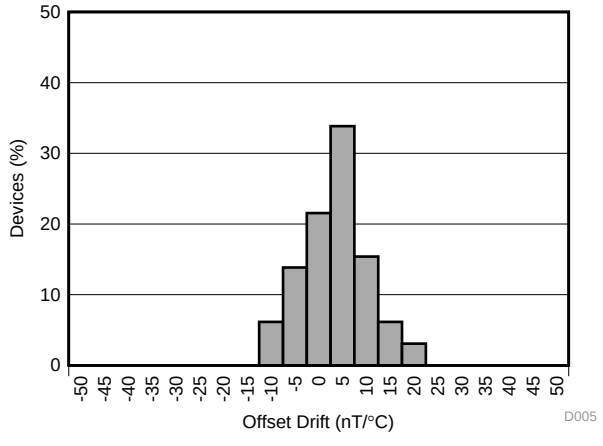


图 5. Fluxgate Sensor Front-End Offset Drift Histogram

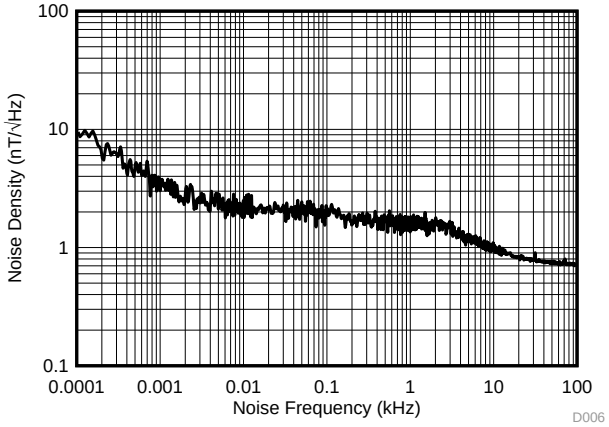


图 6. Fluxgate Sensor Front-End Noise Density vs Noise Frequency

Typical Characteristics (接下页)

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)

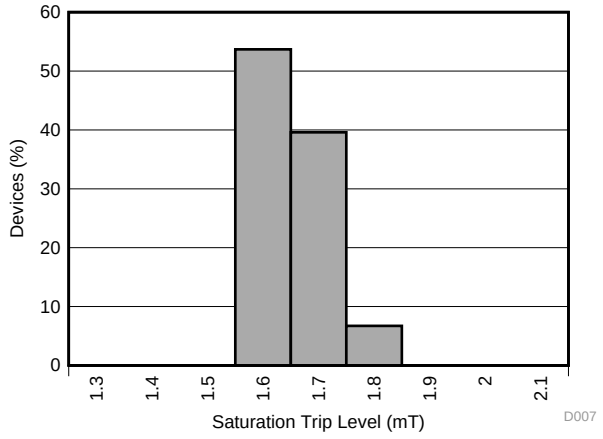


图 7. Fluxgate Sensor Saturation (ER Pin) Trip Level Histogram

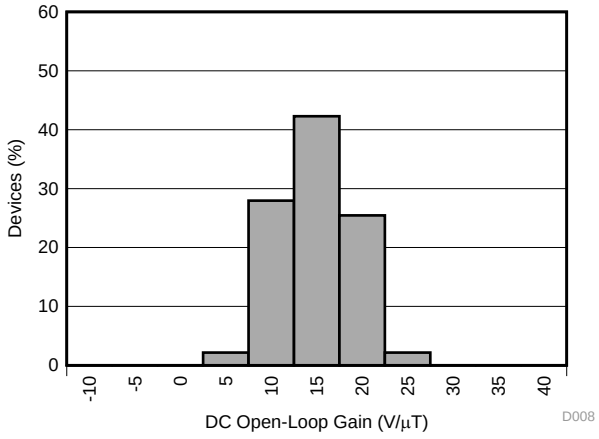


图 8. Fluxgate Sensor Front-End DC Open-Loop Gain Histogram

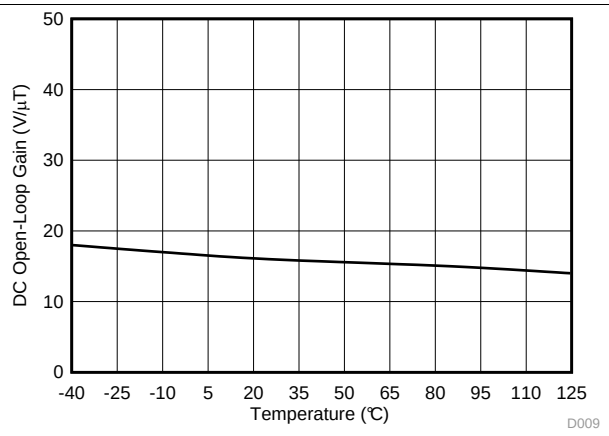


图 9. Fluxgate Sensor Front-End DC Open-Loop Gain vs Temperature

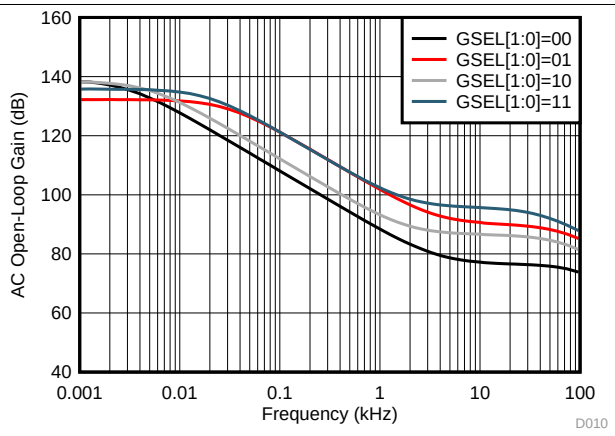


图 10. Fluxgate Sensor Front-End AC Open-Loop Gain vs Frequency

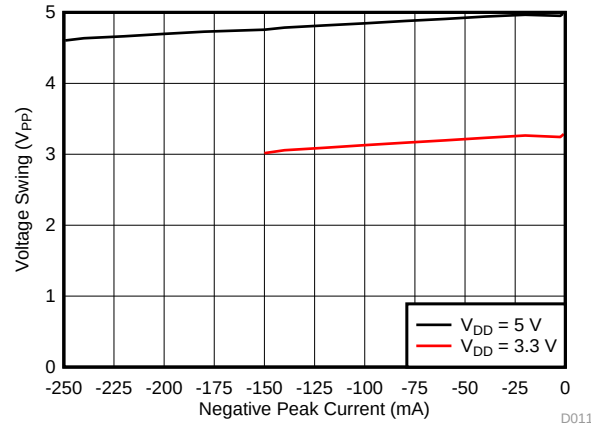


图 11. Voltage Swing at ICOMPx Pins vs Negative Peak Current

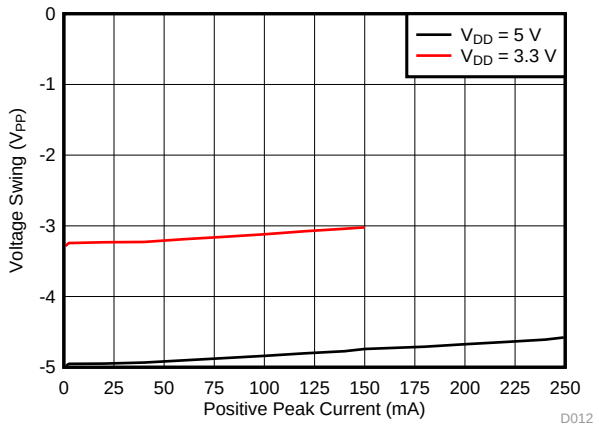
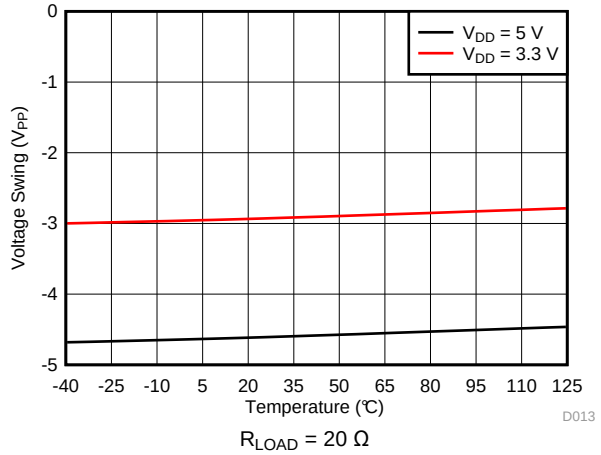


图 12. Voltage Swing at ICOMPx Pins vs Positive Peak Current

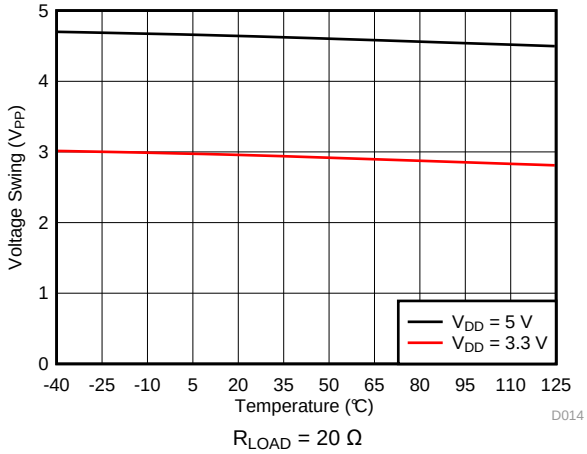
Typical Characteristics (接下页)

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)



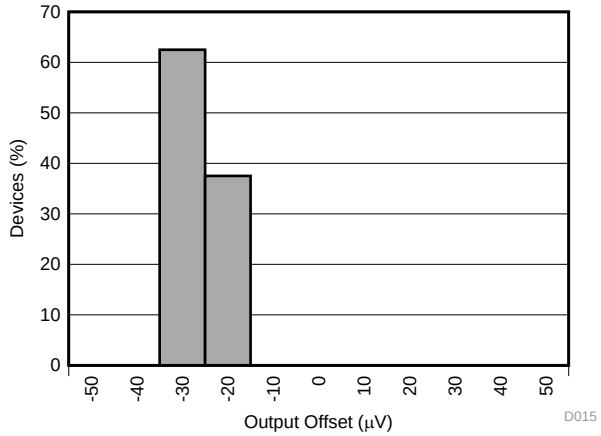
R_{LOAD} = 20 Ω

图 13. Negative Voltage Swing at ICOMPx Pins vs Temperature



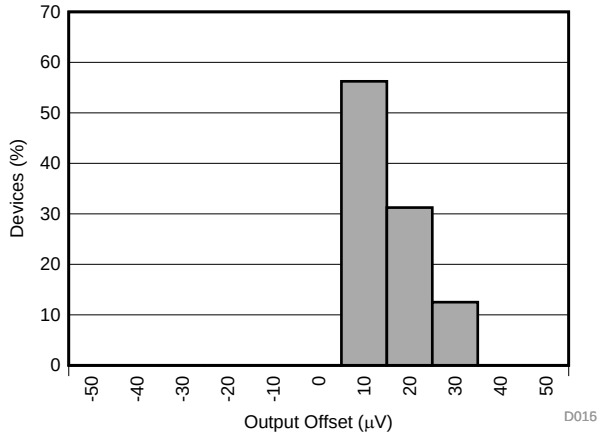
R_{LOAD} = 20 Ω

图 14. Positive Voltage Swing at ICOMPx Pins vs Temperature



V_{DD} = 5 V

图 15. Shunt Sense Amplifier Offset Histogram



V_{DD} = 3.3 V

图 16. Shunt Sense Amplifier Offset Histogram

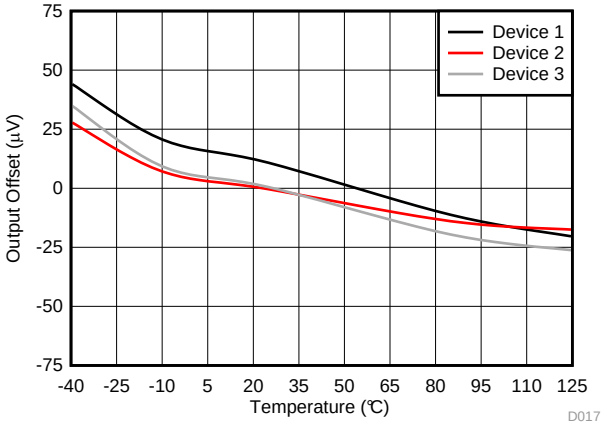


图 17. Shunt Sense Amplifier Offset vs Temperature

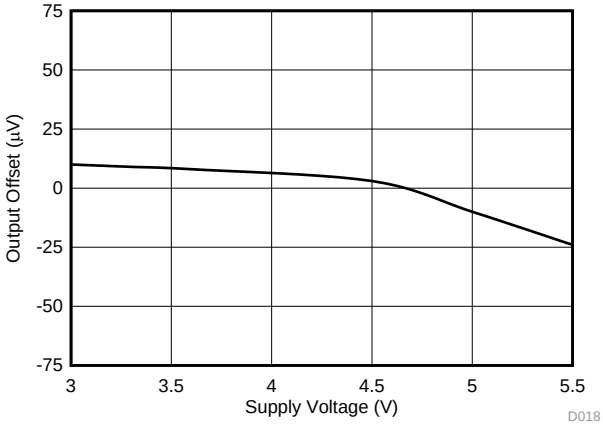


图 18. Shunt Sense Amplifier Offset vs Supply Voltage

Typical Characteristics (接下页)

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)

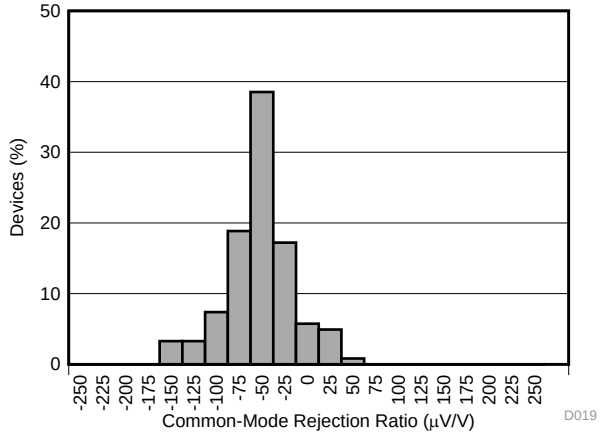


图 19. Shunt Sense Amplifier Common-Mode Rejection Ratio Histogram

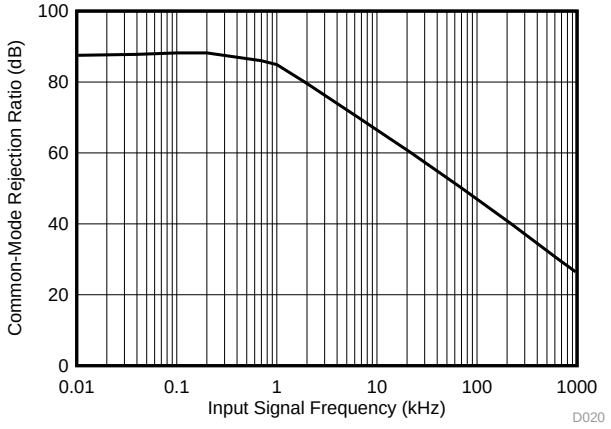


图 20. Shunt Sense Amplifier Common-Mode Rejection Ratio vs Input Signal Frequency

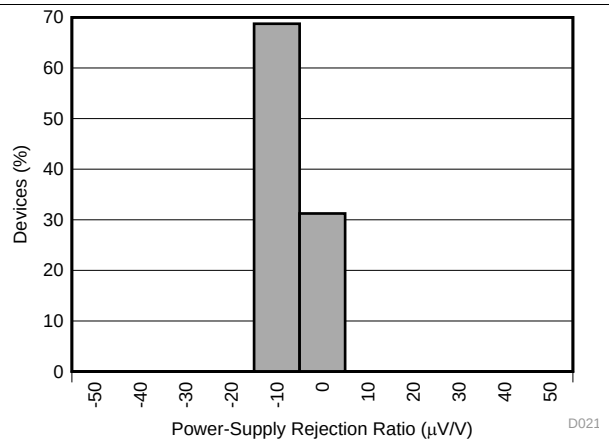


图 21. Shunt Sense Amplifier Power-Supply Rejection Ratio Histogram

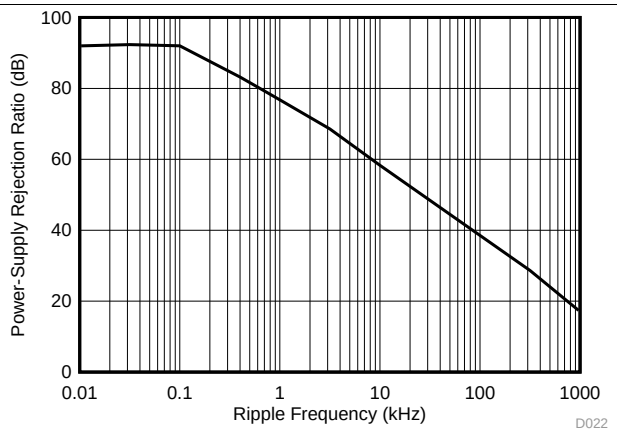


图 22. Shunt Sense Amplifier Power-Supply Rejection Ratio vs Ripple Frequency

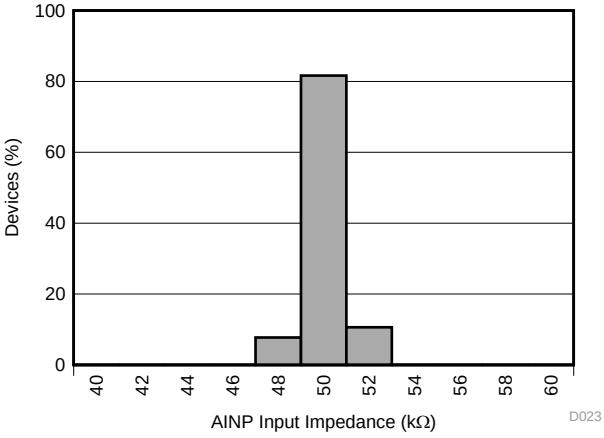


图 23. Shunt Sense Amplifier AINP Input Impedance Histogram

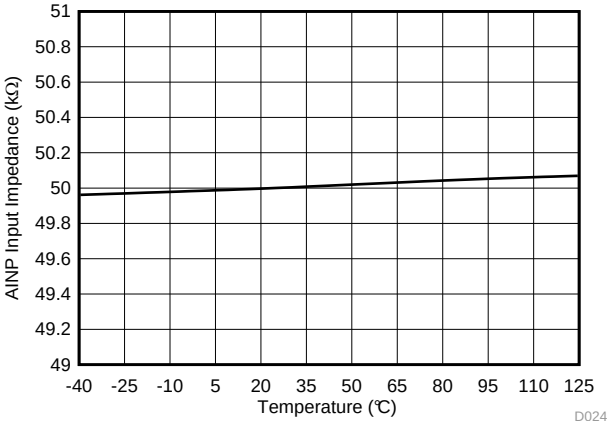


图 24. Shunt Sense Amplifier AINP Input Impedance vs Temperature

Typical Characteristics (接下页)

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)

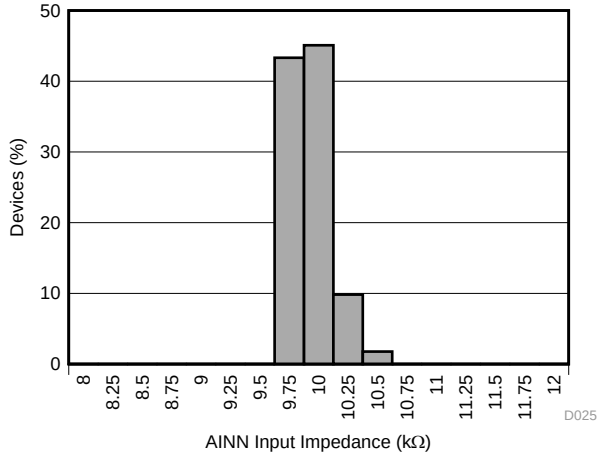


图 25. Shunt Sense Amplifier AINN Input Impedance Histogram

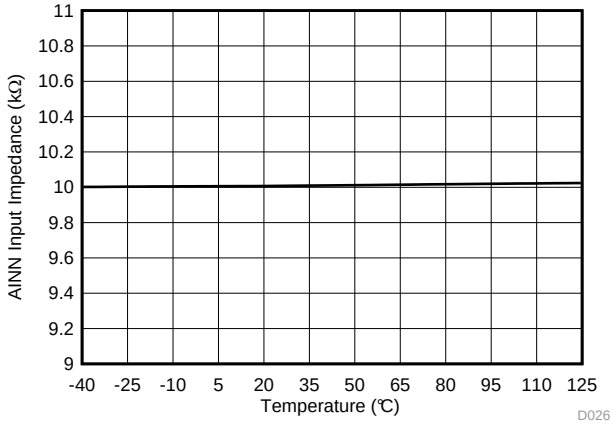


图 26. Shunt Sense Amplifier AINN Input Impedance vs Temperature

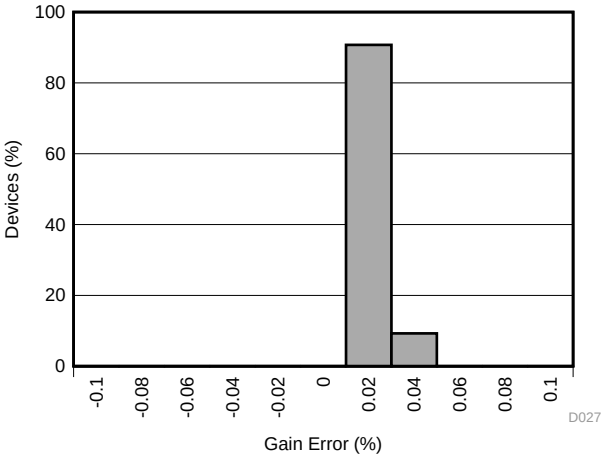


图 27. Shunt Sense Amplifier Gain Error Histogram

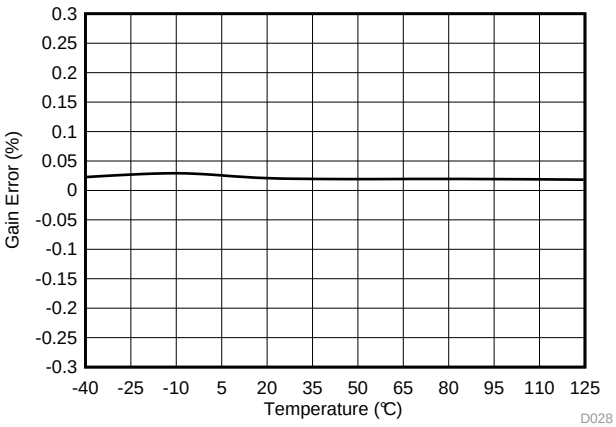


图 28. Shunt Sense Amplifier Gain Error vs Temperature

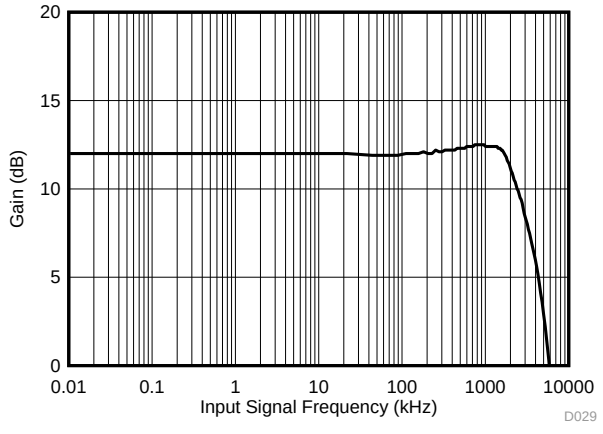


图 29. Shunt Sense Amplifier Gain vs Frequency

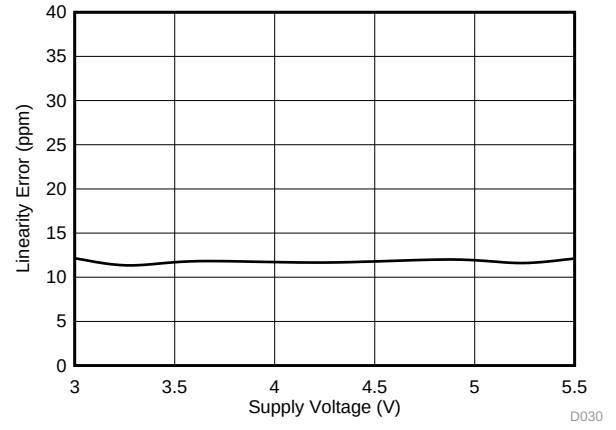


图 30. Shunt Sense Amplifier Linearity vs Supply Voltage

Typical Characteristics (接下页)

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)

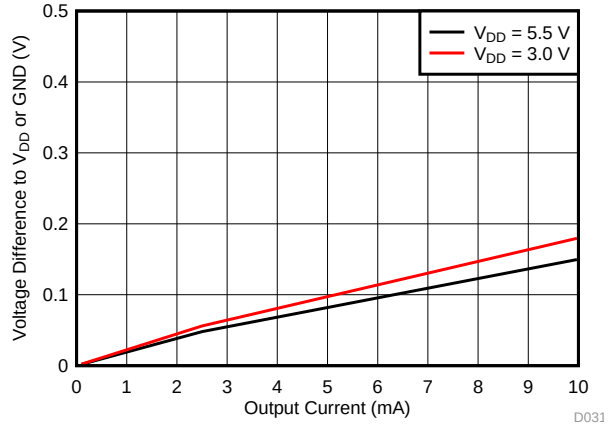


图 31. OR Pin Trip Level vs Output Current

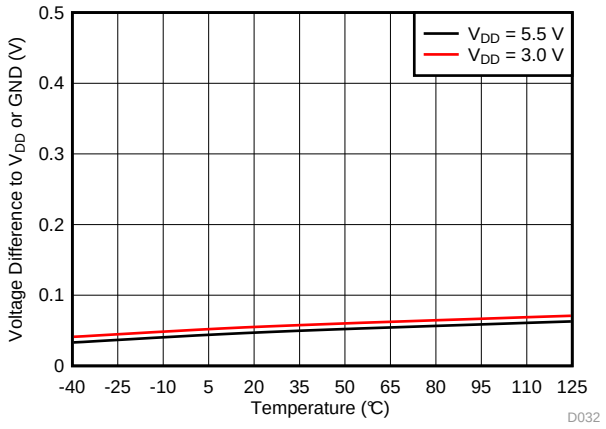


图 32. OR Pin Trip Level vs Temperature

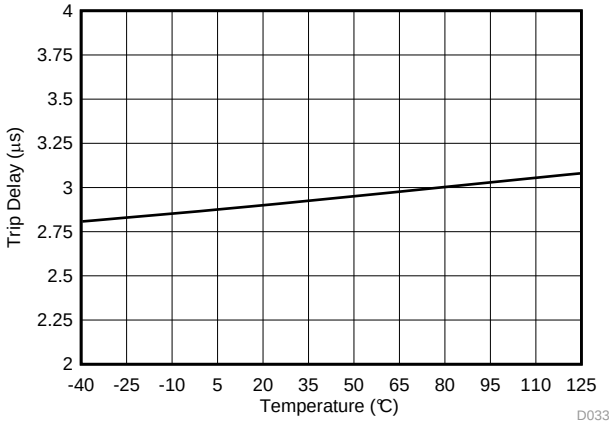


图 33. OR Pin Trip Delay vs Temperature

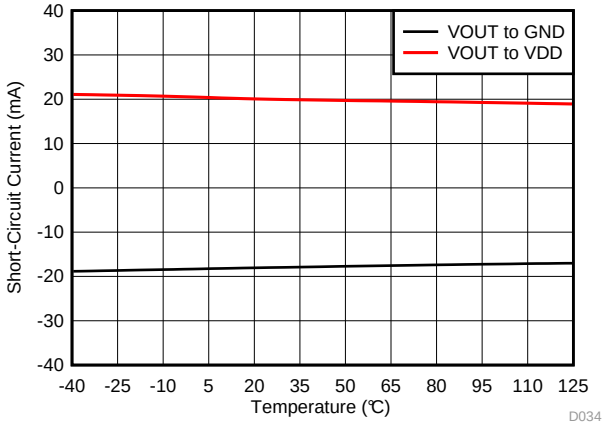


图 34. Shunt Sense Amplifier Output Short-Circuit Current vs Temperature

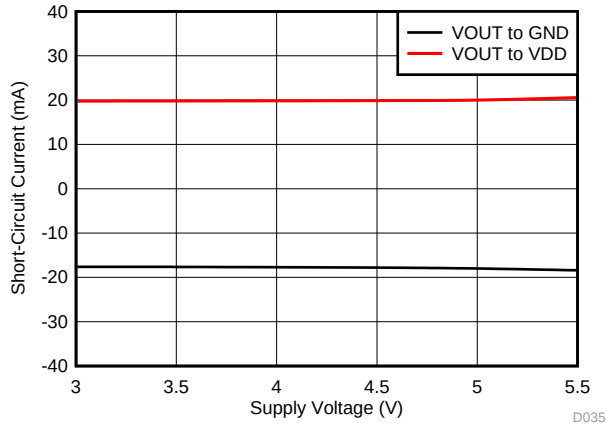


图 35. Shunt Sense Amplifier Output Short-Circuit Current vs Supply Voltage

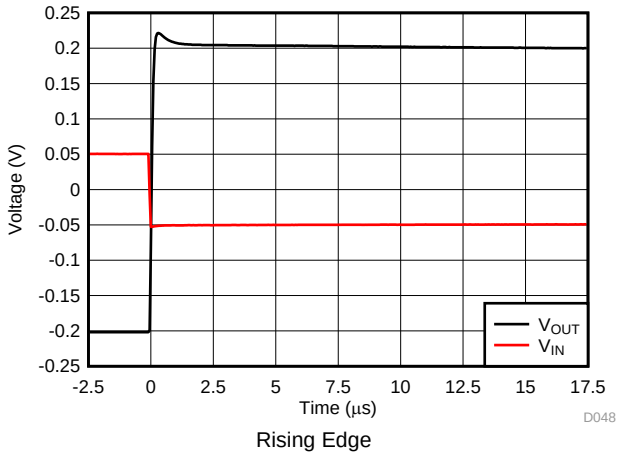
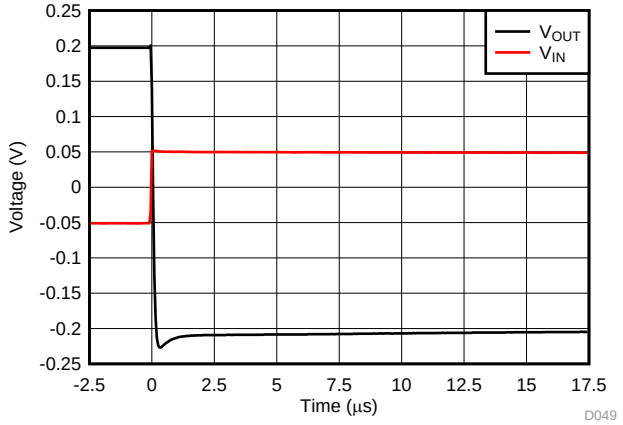


图 36. Shunt Sense Amplifier Small-Signal Settling Time

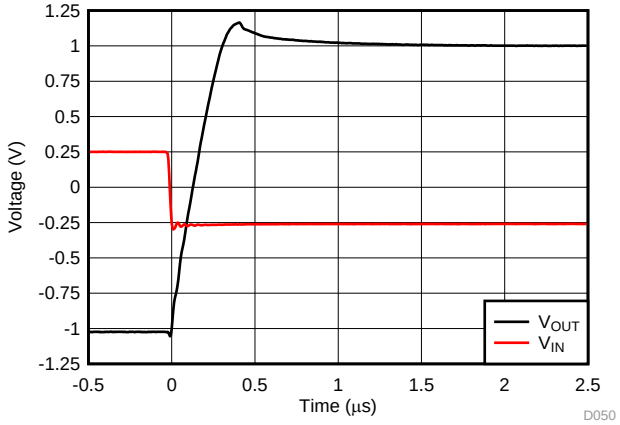
Typical Characteristics (接下页)

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)



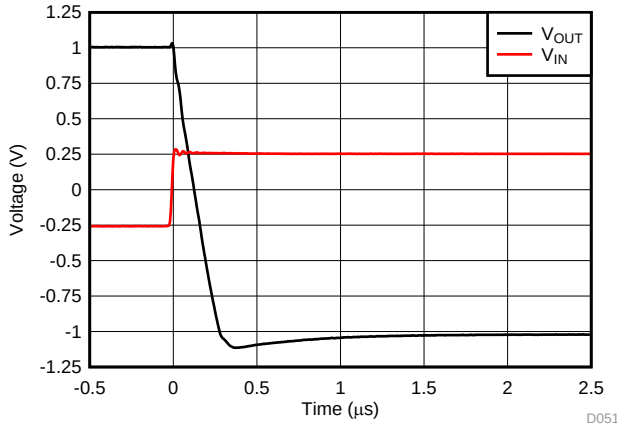
Falling Edge

图 37. Shunt Sense Amplifier Small-Signal Settling Time



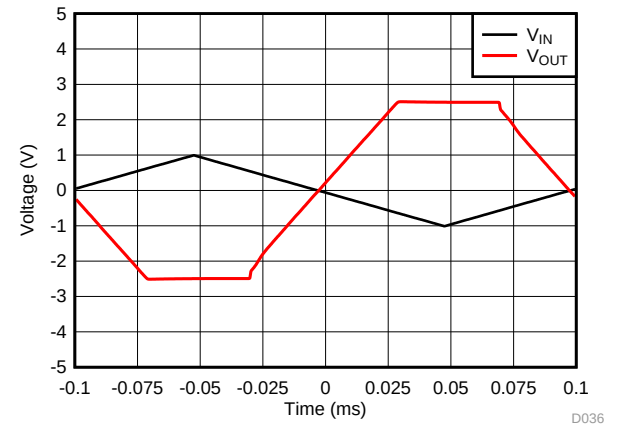
Rising Edge

图 38. Shunt Sense Amplifier Large-Signal Settling Time



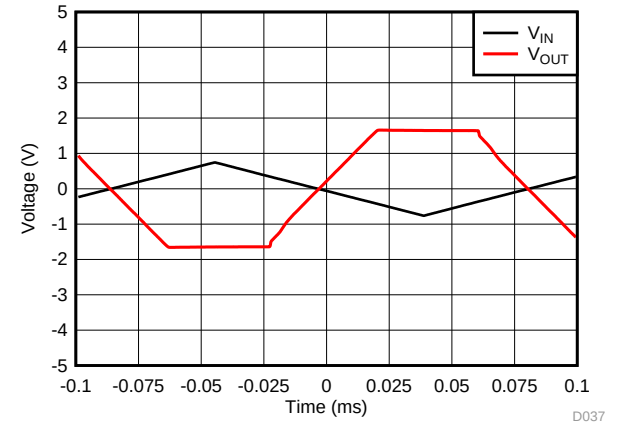
Falling Edge

图 39. Shunt Sense Amplifier Large-Signal Settling Time



V_{DD} = 5 V

图 40. Shunt Sense Amplifier Overload Recovery Response



V_{DD} = 3.3 V

图 41. Shunt Sense Amplifier Overload Recovery Response

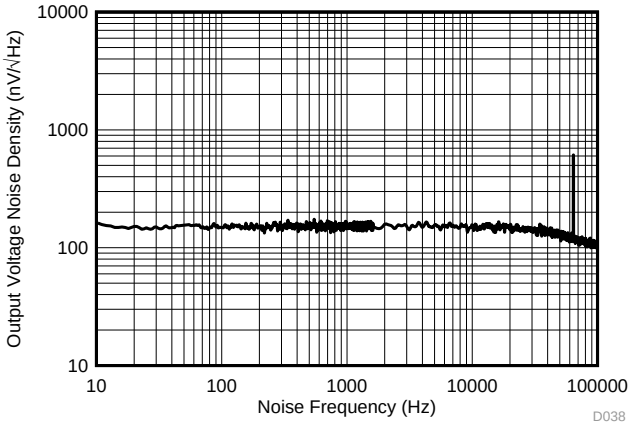


图 42. Shunt Sense Amplifier Output Voltage Noise Density vs Noise Frequency

Typical Characteristics (接下页)

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)

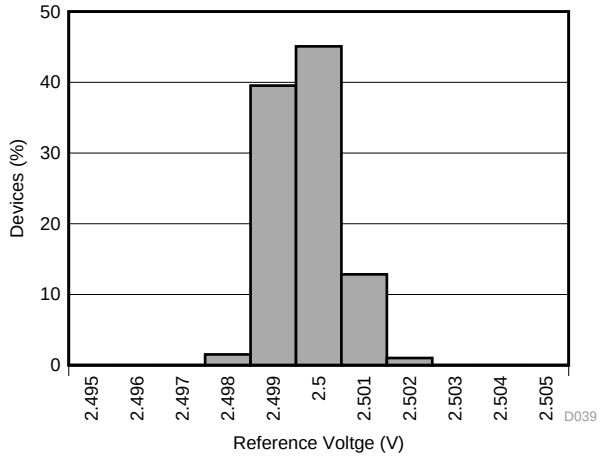


图 43. Reference Voltage Histogram

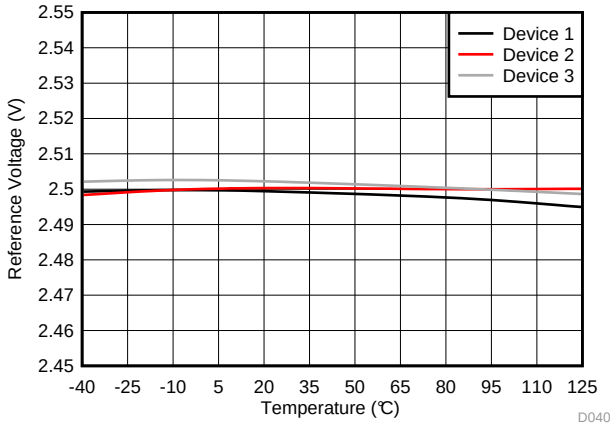


图 44. Reference Voltage vs Temperature

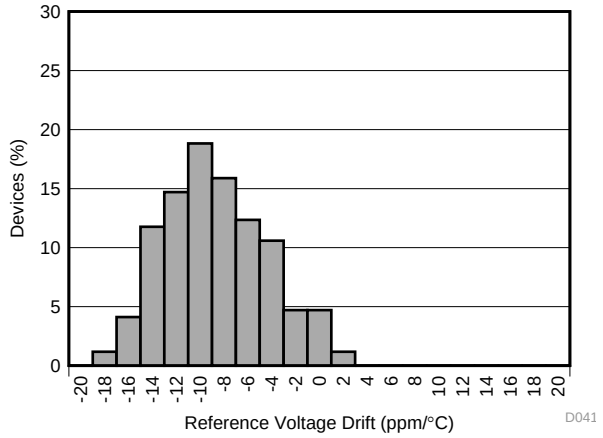


图 45. Reference Voltage Drift Histogram

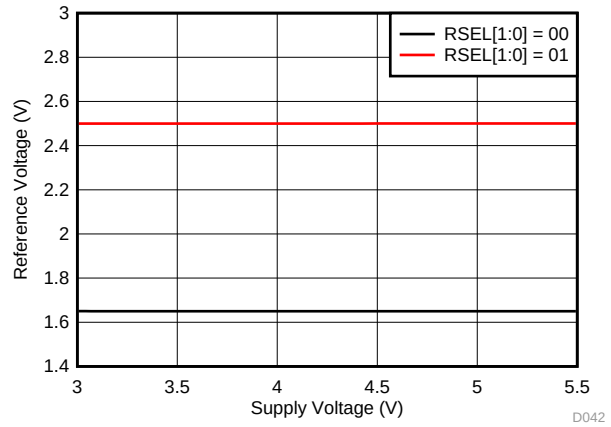


图 46. Reference Voltage vs Supply Voltage

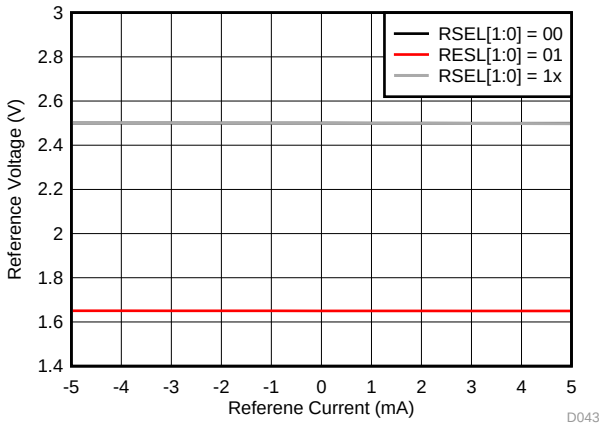


图 47. Reference Voltage vs Reference Output Current

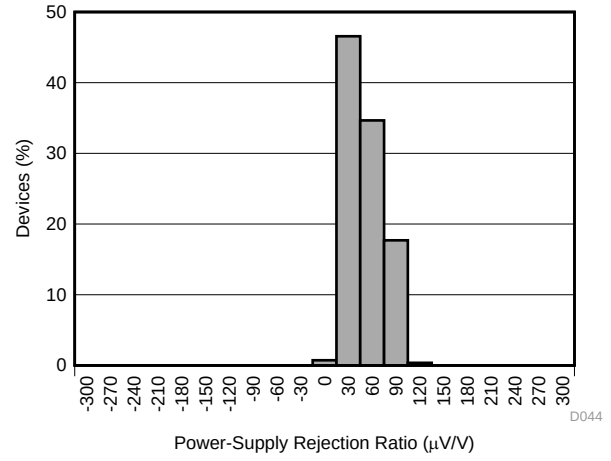


图 48. Reference Voltage Power-Supply Rejection Ratio Histogram

Typical Characteristics (接下页)

at V_{DD} = 5 V and T_A = +25°C (unless otherwise noted)

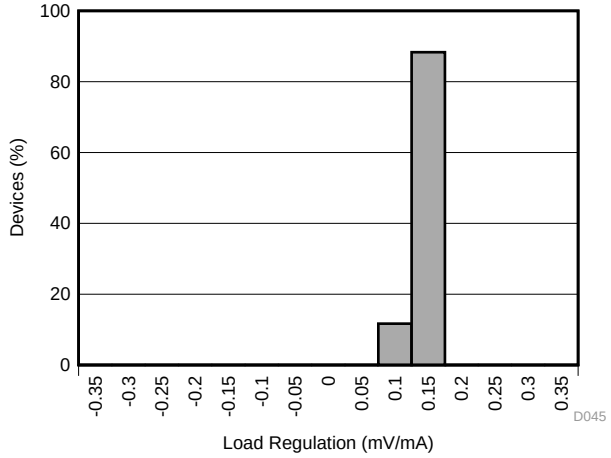


图 49. Reference Voltage Load Regulation Histogram

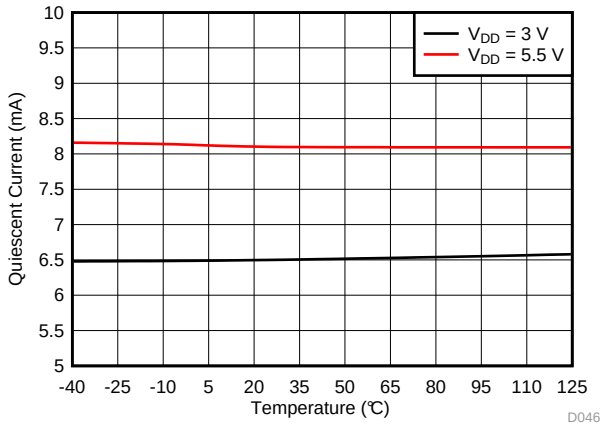


图 50. Quiescent Current vs Temperature

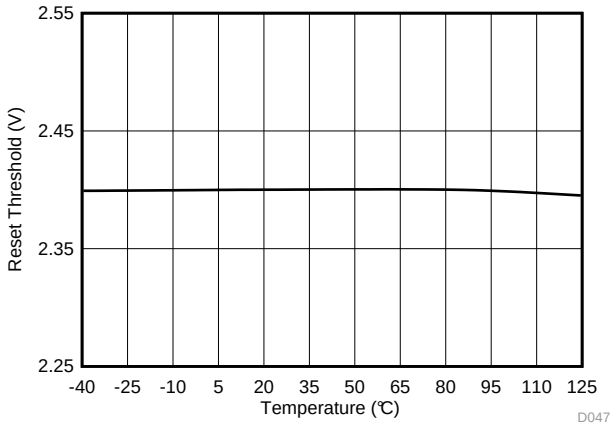


图 51. Power-On Reset Threshold vs Temperature

7 Detailed Description

7.1 Overview

The DRV421 is a fully-integrated, magnetic fluxgate sensor, with the necessary sensor conditioning and compensation circuitry for closed-loop current sensors. The device is inserted into an air gap of an external ferromagnetic toroid core to sense the magnetic field. A compensation coil wrapped around the magnetic core generates a magnetic field opposite to the one generated by the current flow to be measured.

At dc and low-frequencies, the magnetic field induced by the current in the primary conductor generates a flux in the magnetic core. The fluxgate sensor detects the flux in the DRV421. The device filters the sensor output to provide loop stability. The filter output connects to the built-in H-bridge driver that drives an opposing current through the external compensation coil. The compensation coil generates an opposite magnetic field that brings the original magnetic flux in the core back to zero.

At higher frequencies, the inductive coupling between the primary conductor and compensation coil directly drives a current through the compensation coil.

The compensation current is proportional to the primary current ($I_{PRIMARY}$), with a value that is calculated using 公式 1:

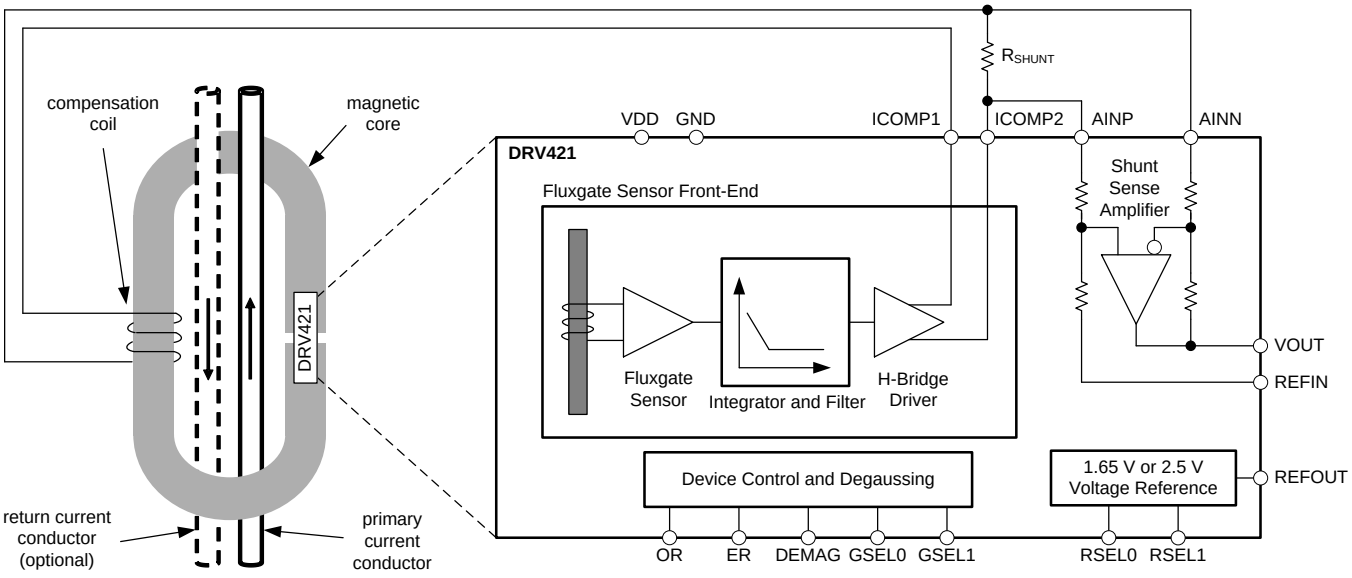
$$I_{ICOMP} = I_{PRIMARY} / N_{WINDING} \quad (1)$$

where

- $N_{WINDING}$ = the number of windings of the compensation coil

This compensation current generates a voltage drop across a small external shunt resistor, R_{SHUNT}. An integrated difference amplifier with a fixed gain of 4 V/V measures this voltage and generates an output voltage that is referenced to REFIN and proportional to the primary current. The *Functional Block Diagram* section shows the DRV421 used as a closed-loop current sensor, for both single-ended and differential primary currents.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fluxgate Sensor

The fluxgate sensor of the DRV421 is uniquely suited for closed-loop current sensors because of its high sensitivity, low noise, and low offset. The fluxgate principle relies on repeatedly driving the sensor in and out of saturation; therefore, the sensor is free of any significant magnetic hysteresis. The feedback loop accurately drives the magnetic flux inside the core to zero.

The DRV421 package is free of any ferromagnetic materials in order to prevent magnetization by external fields and to obtain accurate and hysteresis-free operation. Select nonmagnetizable materials for the printed circuit board (PCB) and passive components in the direct vicinity of the DRV421; see the *Layout Guidelines* section for more details.

图 52 shows the orientation of the fluxgate sensor and the direction of magnetic sensitivity inside of the package. This orientation is marked by a straight line on top of the package.

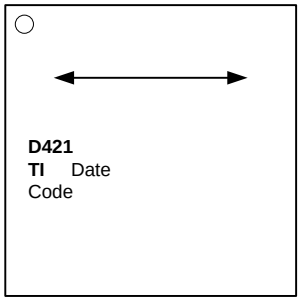


图 52. Orientation and Magnetic Sensitivity Direction of the Integrated Fluxgate Sensor

7.3.2 Integrator-Filter Function and Compensation Loop Stability

The DRV421 and the magnetic core are components of the system feedback loop that compensates the magnetic flux generated by the primary current. Therefore, the loop properties and stability depend on both components. Four key parameters determine the stability and effective loop gain at high frequencies:

GSEL[1:0] Filter gain setting pins of the DRV421

G_{CORE} Open-loop, current-to-field transfer of the magnetic core

Amount of magnetic field generated by 1 A of uncompensated primary current (unit is T/A).

$N_{WINDING}$ Number of compensation coil windings

L Compensation coil inductance

A minimum inductance of 100 mH is required for stability. Higher inductance improves overload current robustness (see the *Overload Detection and Control* section).

To properly select the filter gain of the DRV421, combine these three parameters into a modified gain factor (G_{MOD}) using 公式 2:

$$G_{MOD} = \frac{G_{CORE} \times N_{WINDING}}{L} \quad (2)$$

The effective loop gain is proportional to the current-to-field transfer of the magnetic core (larger field means larger gain) and number of compensation coil windings (larger number of windings means larger compensation field for a given input current). The compensation coil inductance adds a low-frequency pole to the system, thus a larger inductance reduces the effective loop gain at higher frequencies. A more detailed review of system loop stability is provided in application report SLOA224, *Designing with the DRV421: Control Loop Stability*.

For stable operation with a wide range of magnetic cores, the DRV421 features an adjustable loop filter controlled with pins GSEL1 and GSEL0. 表 1 lists the different filter settings and the related core properties. For standard closed-loop current transducer modules with medium inductance and small shunt resistor value, use gain setting 10. Gain setting 01 features a higher integrator-filter crossover frequency of 3.8 kHz, and is recommended for fault-current sensors with a large shunt resistor and medium inductance.

Feature Description (接下页)

表 1. DRV421 Loop Gain Filter Settings and Relation to Magnetic Core Parameters

GSEL1	GSEL0	COMPENSATION LOOP PROPERTIES		RANGE OF MODIFIED GAIN FACTOR G_{MOD}	RANGE OF COMPENSATION COIL INDUCTANCE L ($N_{WINDING}$ = 1000 and G_{CORE} = 0.6 mT/A)
		INTEGRATOR CORNER FREQUENCY	AC OPEN-LOOP GAIN		
0	0	3.8 kHz	8.5	$3 < G_{MOD} < 12$	100 mH < L < 200 mH
0	1	3.8 kHz	38	$1 < G_{MOD} < 3$	200 mH < L < 600 mH
1	0	1.9 kHz	25	$1 < G_{MOD} < 3$	200 mH < L < 600 mH
1	1	1.9 kHz	70	$0.3 < G_{MOD} < 1$	600 mH < L < 2 H

表 1 gives an initial gain-setting recommendation based on a simulation model of a generic magnetic core. Secondary magnetic effects, such as eddy current losses and core hysteresis, can lead to different optimal settings. Therefore, make sure to verify the correct gain setting by measuring the response of the current sensor to an input current step at compensation driver output pins ICOMP1 and ICOMP2. Examples of measurement results with a magnetic core of 300 mH, 1000 compensation coil windings, and different DRV421 gain settings are shown in 图 53 to 图 56.

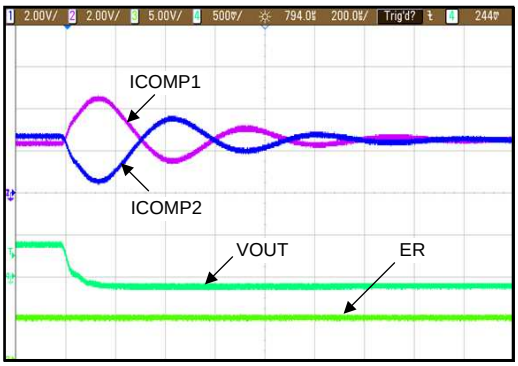


图 53. Settling of ICOMP1 and ICOMP2 with GSEL[1:0] = 00

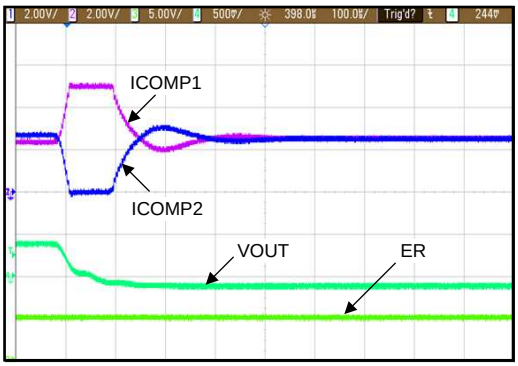


图 54. Settling of ICOMP1 and ICOMP2 with GSEL[1:0] = 01

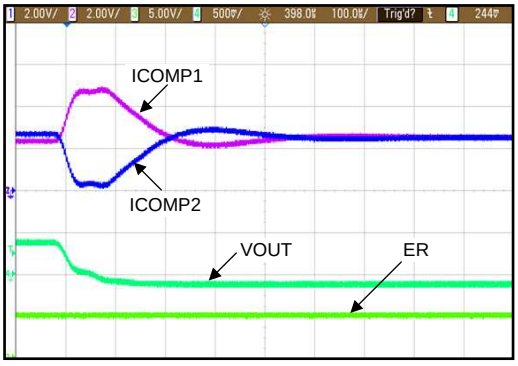


图 55. Settling of ICOMP1 and ICOMP2 with GSEL[1:0] = 10

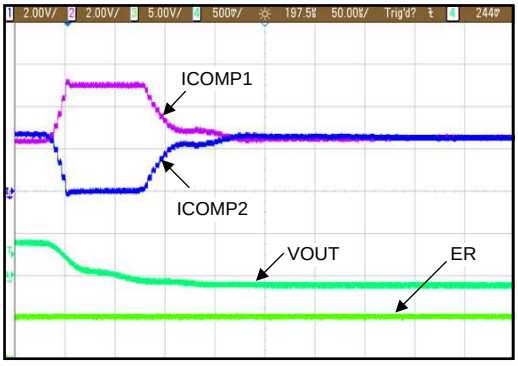


图 56. Settling of ICOMP1 and ICOMP2 with GSEL[1:0] = 11

These measurement examples show a stable response for both GSEL[1:0] = 10 and 11 settings. However, inductive coupling between the primary current and compensation coil makes it difficult to measure high-frequency instability. Therefore, use the lowest gain setting that yields a stable response; in this case, use gain setting 10.

7.3.3 H-Bridge Driver for Compensation Coil

The H-bridge compensation coil driver provides the current for the compensation coil at pins ICOMP1 and ICOMP2. A fully-differential driver stage maximizes the driving voltage that is needed to overcome the wire resistance and inductance of the coil with a single 3.3-V or 5-V supply. The low impedance of the H-bridge driver outputs over a wide frequency range provides a smooth transition between the compensation frequency range of the integrator-filter stage and the high-frequency range of the primary current that directly couples into the compensation coil according to the winding ratio (transformer effect).

The common-mode voltage of the H-bridge driver outputs is set by the RSEL pins (see the *Voltage Reference* section). Thus, the common-mode voltage of the shunt sense amplifier is matched if the internal reference is used.

The two compensation driver outputs are protected and accept inductive energy. However, for high-current sensors, add external protection diodes (see the *Protection Recommendations* section).

Consider the polarity of the compensation coil connection to the output of the H-bridge driver. If the polarity is incorrect, the H-bridge output drives to the power supply rails, even at low primary-current levels. In this case, interchange the connection of pins ICOMP1 and ICOMP2 to the compensation coil.

7.3.4 Shunt Sense Amplifier

The compensation coil current creates a voltage drop across the external shunt resistor, R_{SHUNT}. The internal differential amplifier senses this voltage drop. This differential amplifier offers wide bandwidth and a high slew rate for fast current sensors. Excellent dc stability and accuracy result from an autozero technique. The voltage gain is 4 V/V, set by precisely-matched and thermally-stable internal resistors.

Both AINN and AINP differential amplifier inputs are connected to the shunt resistor. This resistor, in series with the internal 10-kΩ resistor, affects the overall gain and causes an additional gain error; this gain error is often negligible. However, if a common-mode rejection of 70 dB is desired, the match of both divider ratios must be higher than 1/3000. Therefore, for best common-mode rejection performance, place a dummy shunt resistor (R_5) with a value higher than the shunt resistor in series with the REFIN pin to restore matching of both resistor dividers, as shown in 图 57.

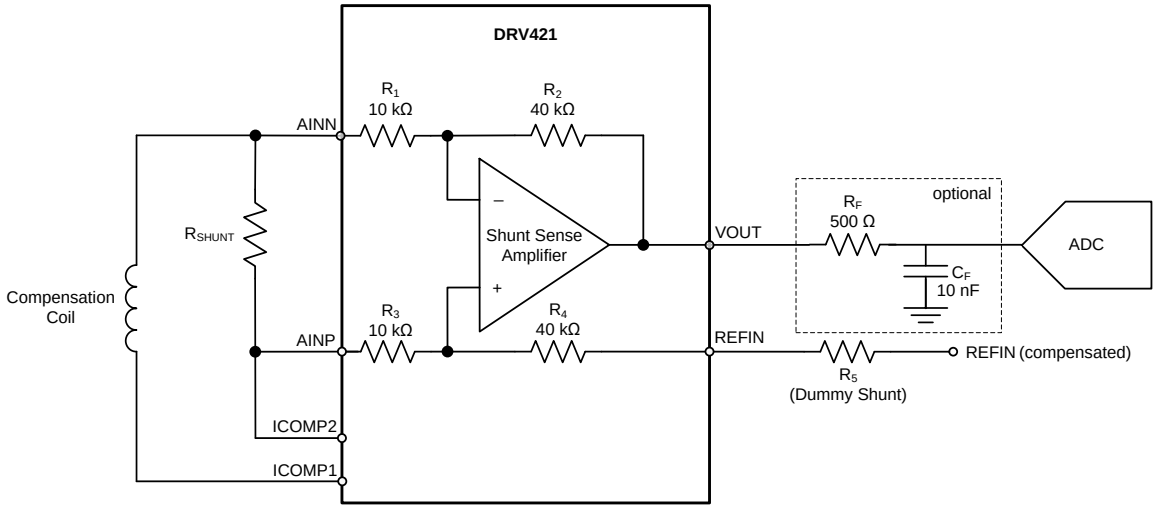


图 57. Internal Difference Amplifier with Example of a Decoupling Filter

For an overall gain of 4 V/V, calculate the value of R_5 using 公式 3:

$$4 = \frac{R_2}{R_1} = \frac{R_4 + R_5}{R_{SHUNT} + R_3} \quad (3)$$

where:

- $R_2 / R_1 = R_4 / R_3 = 4$
- $R_5 = R_{SHUNT} \times 4$

If the input signal is large, the amplifier output drives close to the supply rails. The amplifier output is able to drive the input of a successive approximation register (SAR) analog-to-digital converter (ADC). For best performance, add an RC low-pass filter stage between the shunt sense amplifier output and the ADC input. This filter limits the noise bandwidth and decouples the high-frequency sampling noise of the ADC input from the amplifier output. For filter resistor R_F and filter capacitor C_F values, refer to the specific converter recommendations in the respective product data sheet.

The shunt sense amplifier output drives 100 pF directly and shows 50% overshoot with a 1-nF capacitance. Filter resistor R_F extends the capacitive load range. Note that with an R_F of only 20 Ω, the load capacitor must be either less than 1 nF or more than 33 nF to avoid overshoot; with an R_F of 50 Ω, this transient area is avoided.

Reference input REFIN is the common-mode voltage node for output signal VOUT. Use the internal voltage reference of the DRV421 by connecting the REFIN pin to reference output REFOUT. To avoid mismatch errors, use the same reference voltage for REFIN and the ADC. Alternatively, use an ADC with a pseudodifferential input, with the positive input of the ADC connected to the VOUT and the negative input connected to REFIN of the DRV421.

7.3.5 Overrange Comparator

High peak current across the shunt resistor can generate a voltage drop that overloads the shunt sense amplifier input. The open-drain, active-low output overrange pin (OR) indicates an overvoltage condition of the amplifier. The output of this flag is suppressed for 3 µs, preventing unwanted triggering from transients and noise. This pin returns to high as soon as the overload condition is removed; an external pull-up resistor is required to return the OR pin to high.

This OR output can be used as a window comparator to actively shut off circuits in the system. The value of the shunt resistor defines the operating window for the current, and sets the ratio between the nominal signal and the trip level of the overrange comparator. The trip level (I_{MAX}) of this window comparator is calculated using 公式 4:

$$I_{MAX} = \text{Input Voltage Swing} / R_{SHUNT}$$

where

- Input Voltage Swing = Output Voltage Swing / Gain (4)

For example, with a 5-V supply, the output voltage swing is approximately ±2.45 V (load and supply voltage-dependent).

The gain of 4 V/V enables an input voltage swing of ±0.6125 V.

The resulting trip level is $I_{MAX} = 0.6125\ V / R_{SHUNT}$.

See 图 32 and 图 33 in the *Typical Characteristics* section for details.

Common window comparators use a preset level to detect an overrange condition. The DRV421 internally detects an overrange condition as soon as the amplifier exceeds the linear operating range, not just at a preset voltage level. Therefore, the error is reliably indicated in faults such as output-short, low-load, or low-supply conditions. This configuration is a safety improvement if compared to a standard voltage-level comparator.

The internal resistance of the compensation coil may prevent high compensation current flow because of H-bridge driver overload; therefore, the shunt sense amplifier might not overload. However, a fast rate of change of the primary current transmitted through transformer effect safely triggers the overload flag.

7.3.6 Voltage Reference

The internal precision voltage reference circuit offers low drift performance at the REFOUT output pin and is used for internal biasing. The reference output is intended to be the common-mode voltage of the output (VOUT pin) to provide a bipolar signal swing. This low-impedance output tolerates sink and source currents of ±5 mA. However, fast load transients can generate ringing on this line. A small series resistor of a few ohms improves the response, particularly for capacitive loads equal to or greater than 1 µF.

Adjust the value of the voltage reference output to the power supply of the DRV421 using mode selection pins RSEL0 and RSEL1, as shown in 表 2.

表 2. Reference Output Voltage Selection

MODE	RSEL1	RSEL0	DESCRIPTION
V_{REFOUT} = 2.5 V	0	0	Use with sensor module supply of 5 V
V_{REFOUT} = 1.65 V	0	1	Use with sensor module supply of 3.3 V
Ratiometric output	1	x	Provides output centered on V_{DD} / 2

In ratiometric output mode, an internal resistor divider divides the power supply voltage by a factor of two.

For current sensor modules with a reference input pin, the DRV421 also allows overwriting the internal reference with an external reference voltage, V_{EXT}, as shown in 图 58. If there is a significant difference between the external and the internal voltage, resistor R_5 limits the current flow from the internal reference. In this case, the internal reference sources current I_{REFOUT} shown in 公式 5:

$$I_{REFOUT} = \frac{V_{REFOUT} - V_{EXT}}{600\ \Omega} \quad (5)$$

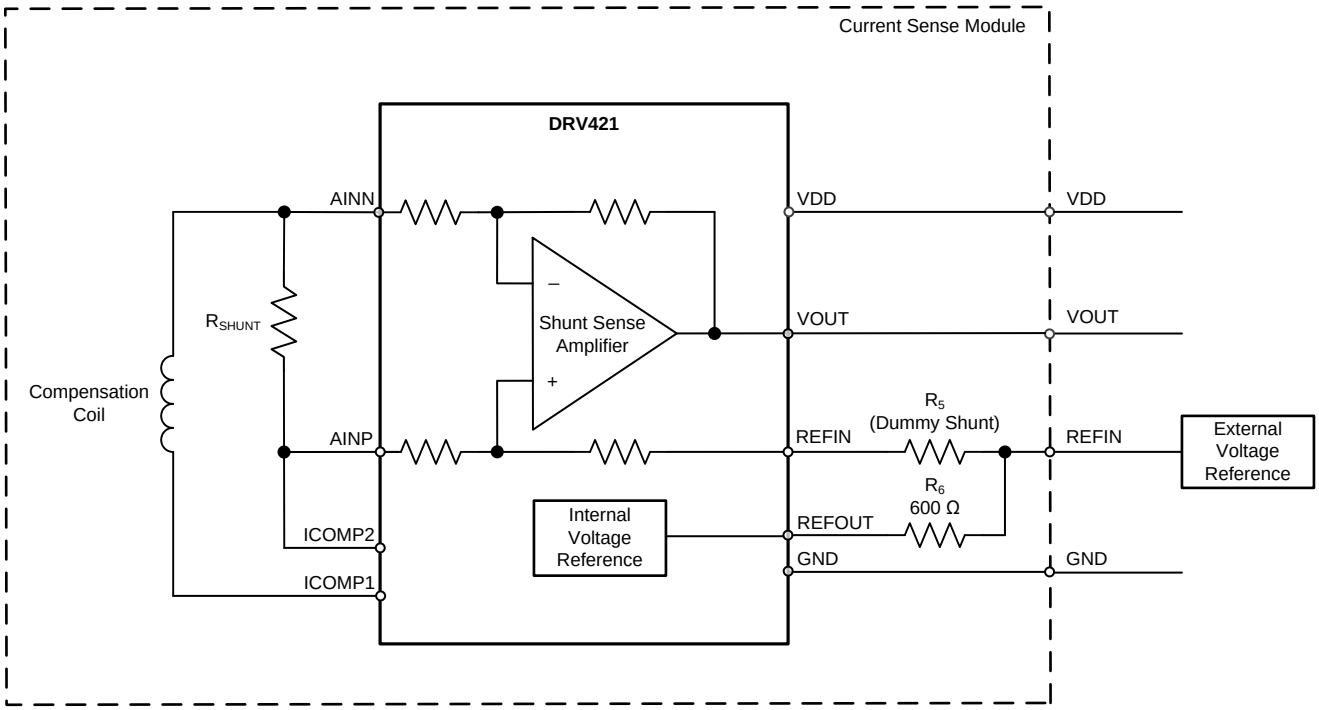


图 58. DRV421 with External Reference

The example of 600 Ω for R_6 was chosen for illustration purposes; different values are possible. If no external reference is connected, R_6 has little impact on the common-mode rejection of the shunt sense amplifier; therefore, use a resistor value that is as small as possible.

7.3.7 Overload Detection and Control

Magnetic fluxgate sensors have a very high sensitivity and allow detection of small magnetic fields. These sensors are ideally suited for use in closed-loop current modules appllications because the high sensitivity makes sure that the field inside the core gap is accurately driven to zero. However, for large fields, the fluxgate saturates and causes the output to return to zero, as shown in 图 59.

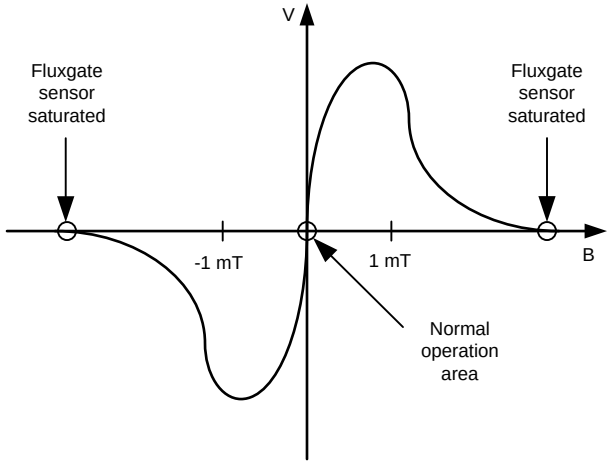


图 59. Typical Fluxgate Sensor Response to Magnetic Fields

In normal operation, the feedback loop keeps the magnetic field close to zero. However, large overload currents that exceed the measurement range (for example, short-circuit currents) saturates the fluxgate. The behavior is shown in 图 60, where the compensation current, magnetic field in the core, and fluxgate output are shown for the case of a 1000-A primary current step.

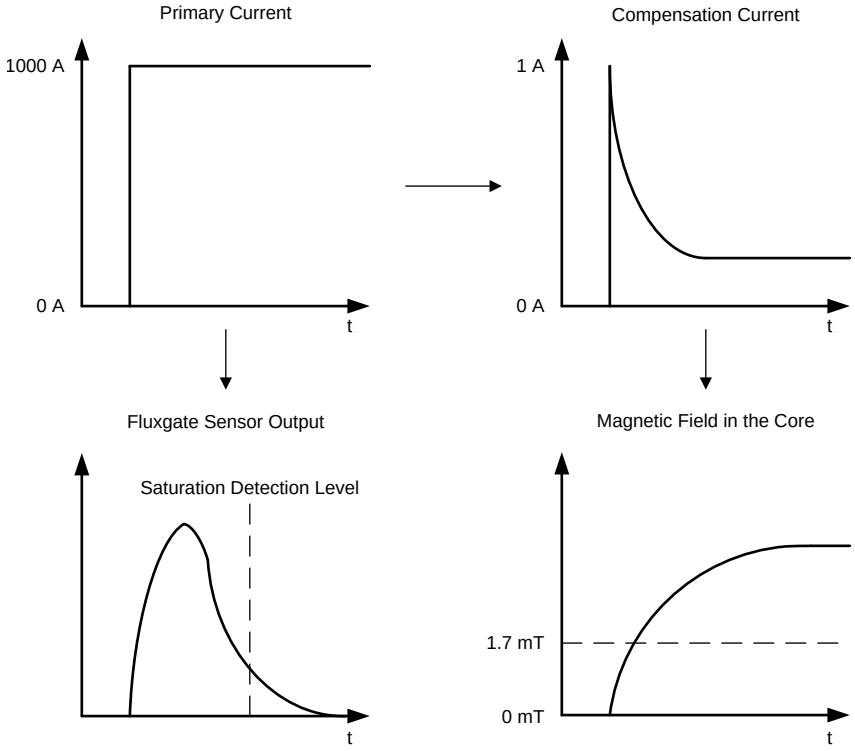


图 60. Closed-Loop Current Sensor Response to an Overloaded Step Current

Use the inverse of 公式 1 to calculate the current measurement range. For example, if the compensation coil has 1000 windings, the maximum measurement range is 210 A at a 5-V supply (210-mA minimum compensation driver capability × 1000 windings). The inductive coupling between primary current and compensation coil initially provides a correct compensation current. However, over time, the compensation current drops to 210 mA and the field inside the core increases beyond the measurement range of the fluxgate. Thus, the sensor output returns to zero because of saturation.

This zero output causes unpredictable behavior in the analog control loop. For example, as a result of an invalid fluxgate output, the H-bridge drives the wrong compensation current and generates a large magnetic field through the compensation coil. This magnetic field keeps the fluxgate in saturation and leads to system lockup. This unpredicatable behavior exists for any fluxgate-based current sensor.

For proper handling of overload currents, the DRV421 features a two-step overload detection and control function. Firstly, the polarity of the last four fluxgate sensor outputs exceeding a threshold value of approximately 13 µT are internally stored. Secondly, the DRV421 features an additional circuitry that verifies every 4 µs whether the fluxgate is saturated. If saturation is detected, digital circuitry overrides the fluxgate output and provides a high output according to the polarity detected during the last valid sensor output. As a result, the H-brigde drives the outputs to the supply rails, making sure that the magnetic field returns to within the fluxgate range as soon as the current returns to within the measurement range. After this happens, the fluxgate is no longer saturated, and normal analog feedback loop operation resumes. During fluxgate saturation, the error pin is pulled low to signal that the current exceeds the measurement range (see the *Error Flag* section).

For correct operation of this overload control feature, at least 10 µs are required between the time the field exceeds the polarity detection threshold (13 µT) and the saturation trip level (1.7 mT). Initially, fast primary current steps are inductively coupled to the compensation coil (transformer effect); therefore, the primary current rise time is not limited. Instead, the rise time is determined by the compensation coil inductance; a larger inductance leads to a slower compensation current decrease. The minimum required inductance is 100 mH; for optimal robustness, use 300 mH (see the *Magnetic Core Design* section for detailed requirements).

7.3.8 Magnetic Core Demagnetization

Ferromagnetic cores can have a significant remanence (residual magnetism in the absence of any currents). This core magnetization is caused by strong external magnetic fields, overcurrent conditions in the system, or if a significant primary current flows when the sensor is not powered. This remaining magnetic field is indistinguishable from an actual primary current, and creates a magnetic offset error. This magnetic offset error limits the precision and the dynamic range of the current sensor, and is independent of the fluxgate sensor front-end offset specified in this data sheet.

To reduce errors caused by core magnetization, the DRV421 features a unique closed-loop demagnetization feature. Conventional open-loop demagnetization techniques rely on driving a fixed ac waveform through the compensation coil. Instead, the DRV421 demagnetization feature first measures the magnetic offset using its integrated fluxgate sensor, and then drives a controlled ac waveform to reduce the measured magnetization. This method results in significantly better results. Moreover, any fluxgate offset is part of the closed-loop demagnetization measurement, and therefore removed along with core magnetization, leaving only fluxgate offset drift over temperature as an error source.

Start the demagnetization feature on demand by pulling the DEMAG pin high for at least 25 µs. This process starts a 500-ms demagnetization cycle. During this time, the error pin (ER) is pulled low to indicate that the output is not valid. When DEMAG is high during power up, the demagnetization cycle initiates immediately after the supply voltage crosses the power-up threshold. Hold DEMAG low to avoid this cycle during start up. To abort the demagnetization cycle, pull DEMAG low for longer than 25 µs. 图 61 shows the ICOMPx output behavior during a demagnetization sequence. 图 62 shows the reduced error resulting from core demagnetization.

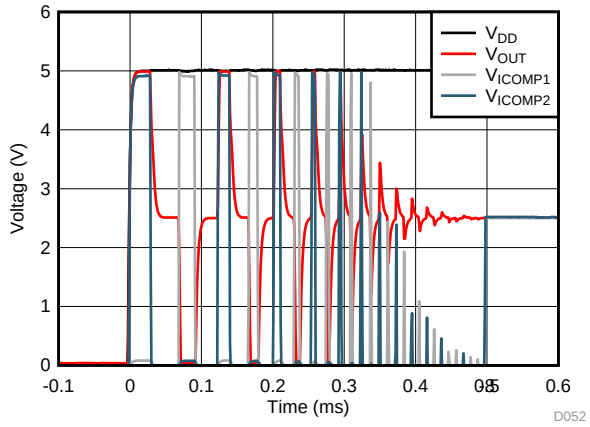


图 61. Demagnetization Sequence

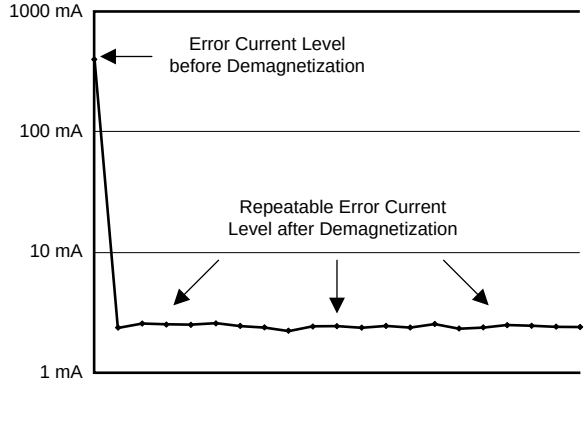


图 62. Impact of Demagnetization on Error Current

During a demagnetization cycle, the primary current must be zero because the resulting magnetic field cannot be distinguished from the remanence of the core. A demagnetization cycle in the presence of primary current (or any other sources of magnetic field) leads to residual errors because the demagnetization feature attempts to reduce the primary-generated field to zero, but significantly magnetizes the core instead of demagnetizing the core. If a primary current is present that is large enough to saturate the fluxgate sensor during start up, the DRV421 skips demagnetization (regardless of the level on the DEMAG pin), and the search function starts instead (see the *Search Function* section for more details).

To reduce effects from the earth's magnetic field, degauss in the same orientation as nominal operation of the system.

7.3.9 Search Function

Closed-loop current sensors usually require primary current to be applied only after the sensor is powered up. This requirement allows the feedback loop to start from zero current operation; the magnetic core is maintained at zero flux at all times, thus preventing magnetization. Moreover, the DRV421 integrated fluxgate has a limited measurement range of 1.7 mT. As a result, the presence of a significant primary current at power up saturates the fluxgate, and the system feedback loop does not work; similar to the presence of an overload current (see the *Overload Detection and Control* section).

The DRV421 search function allows for a power up in presence of primary dc current. If the fluxgate is saturated at power up, the digital logic of the DRV421 connects ICOMP1 to VDD and COMP2 to GND for 30 ms. Because of the compensation coil inductance, the compensation current slowly increases during this time, and depending on the primary current polarity, may at some point compensate the primary current. In this case, the fluxgate sensor desaturates and normal operation initiates. If the fluxgate sensor is still saturated after 30 ms, the voltage polarity on ICOMPx pins is inverted (ICOMP1 = GND, ICOMP2 = VDD) and the process repeats for opposite primary current polarity. If the fluxgate remains saturated after 60 ms, the error state persists and the error pin ER remains active low. 图 63 shows a search sequence starting with the wrong polarity.

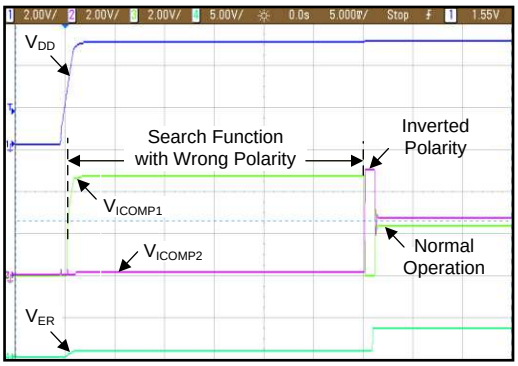


图 63. Search Sequence Starting with Wrong Polarity

The search funciton cannot be used for primary ac currents. Moreover, the presence of primary current before the sensor is powered up may lead to core magnetization, and thus offset shift. Therefore, for robust operation, do not power up in the presence of primary currents.

7.3.10 Error Flag

The DRV421 features an error output (ER pin) that is activated under multiple conditions. The error flag is active when the output voltage is not proportional to the primary current; during a power fail or brownout; during a demagnetization cycle; or when the magnetic field on the fluxgate is greater than 1.7 mT (saturation of the fluxgate). Saturation is usually caused by either the consequence of an overload current (see the *Overload Detection and Control* section) or results from a power-up in the presence of a primary current (see the *Search Function* section).

The error flag resets as soon as the error condition is no longer present and the circuit has returned to normal operation. The error flag is an open-drain logic output. Connect the error flag to the overrange flag for a wired-OR; for proper operation, use an external pull-up resistor. The following conditions result in error flag activation (ER asserts low):

1. For 80 µs after power-up
2. If a supply-voltage brownout condition (V_{DD} < 2.4 V) lasts for more than 20 µs
3. If the sensed magnetic field is > 1.7 mT because:
   – Overload control is active
   – Search function is active
4. Demagnetization cycle is active (see the *Magnetic Core Demagnetization* section)

7.4 Device Functional Modes

The DRV421 has a single functional mode and is operational when the power-supply voltage is greater than 3 V. The maximum power supply voltage for the DRV421 is 5.5 V.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Magnetic Core Design

The high sensitivity, low offset, and low noise of the DRV421 fluxgate sensor enable a high-performance closed-loop current sensor module. For good module performance, an appropriate magnetic core design is required.

表 3 lists the DRV421 and magnetic core specifications with relation to the overall current module specifications.

表 3. Current-Sensor Module Performance versus DRV421 Specifications and Magnetic Core Performance

CURRENT SENSOR MODULE PARAMETER	PERFORMANCE DETERMINED BY:
Offset and offset drift	DRV421 fluxgate sensor front-end: offset and offset drift
Offset on start-up and after overload condition	Magnetic core: magnetization (see the *Magnetic Core Demagnetization* section)
Noise	DRV421 fluxgate sensor front-end: noise
Linearity error	DRV421 fluxgate sensor front-end: AC open-loop gain
Gain error	Magnetic core: Permeability, geometry, and actual number of compensation coil windings
Measurement range	1) DRV421 fluxgate sensor front-end: H-bridge peak current 2) Compensation coil: number of windings and resistance 3) Value of the external shunt resistor
Neighbor-current rejection (crosstalk)	Magnetic core: permeability, sensor gap design, and magnetic shielding
Bandwidth and gain flatness	1) DRV421 fluxgate sensor front-end: AC open-loop gain setting 2) Magnetic core: high-frequency behavior of the core and inductance of the compensation coil 3) Value of the external shunt resistor
Common-mode current rejection (for fault current sensors)	Magnetic core: permeability, actual position of the primary current conductors, and magnetic shielding

For further details, see application report SLOA223, *Designing with the DRV421: Closed Loop Current Sensor Specifications*.

Application Information (接下页)

8.1.2 Protection Recommendations

Inputs AINP and AINN require external protection to limit the voltage swing to within 6 V beyond both supply rails. Driver outputs ICOMP1 and ICOMP2 handle high-current pulses protected by internal clamp circuits to the supply voltage. If large magnitude overcurrents are expected, connect external Schottky diodes to the supply rails to protect the DRV421 from damage.

CAUTION

Large overcurrents may drive the power supply above the normal operating voltage. Route large overcurrent pulses away from the device using diodes connected to the supply, as shown in the *typical application* on the front page. To prevent these pulses from driving up the supply voltage, and prevent damage to the DRV421 and other components in the circuit, use an additional supply clamp, as shown in 图 64. All other pins offer standard protection; see the *Absolute Maximum Ratings*.

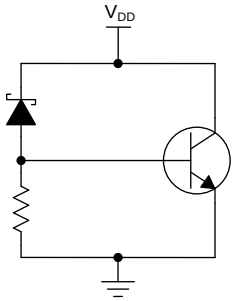


图 64. Additonal Supply Clamp for the DRV421

8.2 Typical Application

8.2.1 Closed-Loop Current Sensing Module

Closed-loop current sensor modules (图 65) measure currents over a wide frequency range, including dc currents. These sensor modules offer a contact-free sensing method and excellent galvanic isolation performance, combined with high resolution, accuracy, and reliability. The DRV421 is designed for use in this kind of application.

At dc and in low-frequency range, the magnetic field induced by the primary current is sensed by the DRV421 fluxgate sensor. The sensed signal is filtered by the DRV421 and the internal H-bridge driver generates a proportional compensation current. The compensation current flows through the compensation coil, and generates a magnetic field. This magnetic field drives the original magnetic flux in the core back to zero. The value of this magnetic field is increased by the number of compensation coil windings. Therefore, use 公式 1 to calculate the required compensation current for a given primary current.

At higher frequencies, the magnetic field induced by the primary current directly couples into the compensation coil and generates a current. The low impedance of the H-bridge driver does not influence the value of this current. Also in this case, the value of the compensation current is the value of the primary current divided by the number of compensation coil windings.

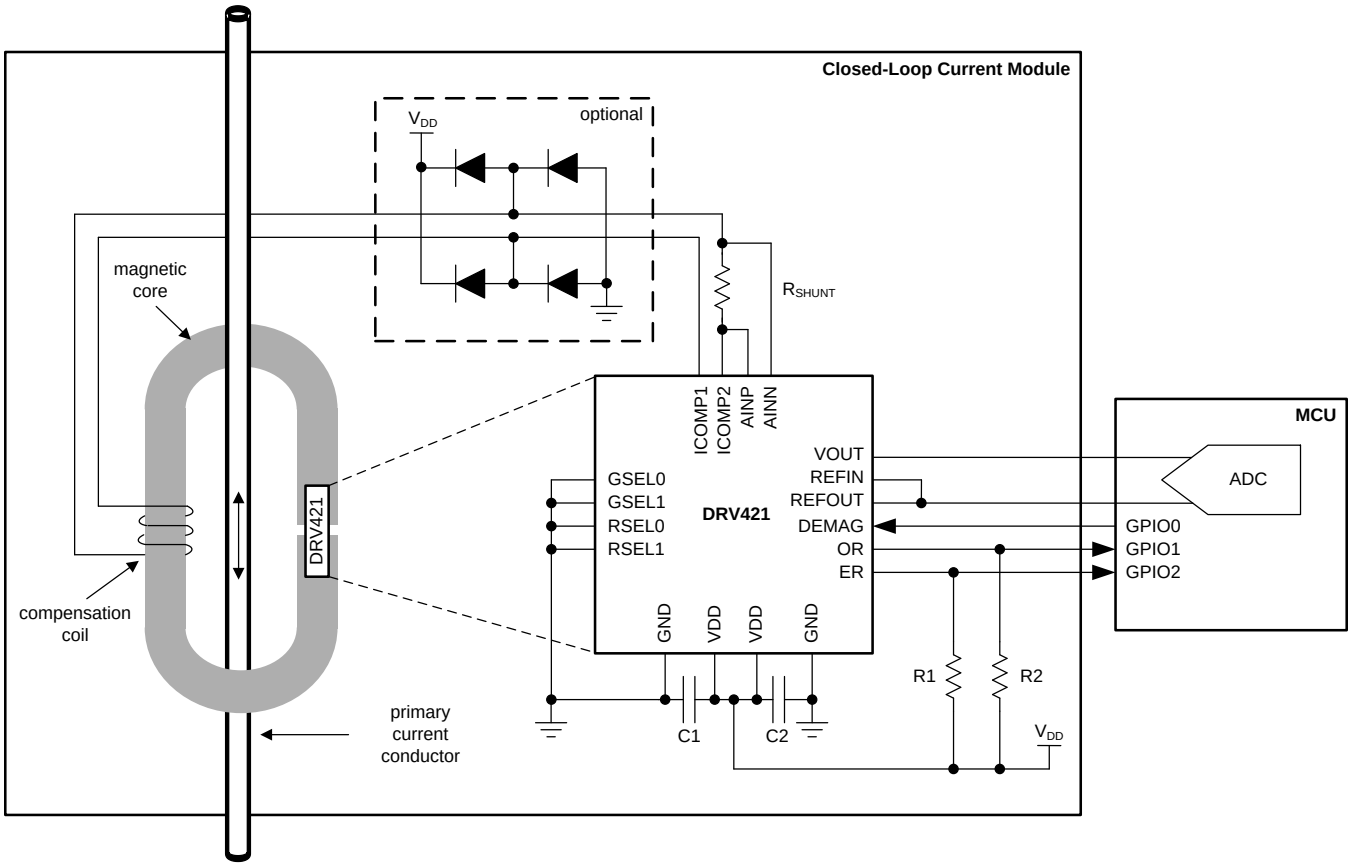


图 65. Closed-Loop Current Sensing Module

Typical Application (接下页)

8.2.1.1 Design Requirements

A closed-loop current sensing module contains the DRV421, the magnetic core with a compensation coil, and a shunt resistor. To increase the robustness of the module to high primary current peaks, use additional protection diodes. See application report SLOA223, *Designing with the DRV421: Closed Loop Current Sensor Specifications*, for additional information on the magnetic core and compensation coil design. The DRV421 output voltage is calculated as described in 公式 6:

$$V_{OUT} = I_{PRIM} \times \left(\frac{N_{PRIM}}{N_{WINDING}} \right) \times R_{SHUNT} \times G \quad (6)$$

where:

- I_{PRIM} = primary current value
- N_{PRIM} = the number of windings of the primary current conductor
- $N_{WINDING}$ = the number of windings of the compensation coil
- R_{SHUNT} = shunt resistor value
- G = shunt sense amplifier gain; default value is 4

8.2.1.2 Detailed Design Procedure

The compensation current creates a voltage drop across the shunt resistor. The maximum shunt resistor value is limited by supply voltage V_{DD}, the compensation current range, and the resistance of the compensation coil, as described in 公式 7:

$$R_{SHUNT} + R_{COIL} \leq \frac{V_{ICOMP(MIN)}}{I_{ICOMP}} \quad (7)$$

The voltage drop across the shunt resistor is sensed by the DRV421 shunt sense amplifier with a gain of four. For proper operation, keep the resulting output voltage at VOUT pin within the voltage output swing range specified in the *Electrical Characteristics*.

8.2.1.3 Application Curves

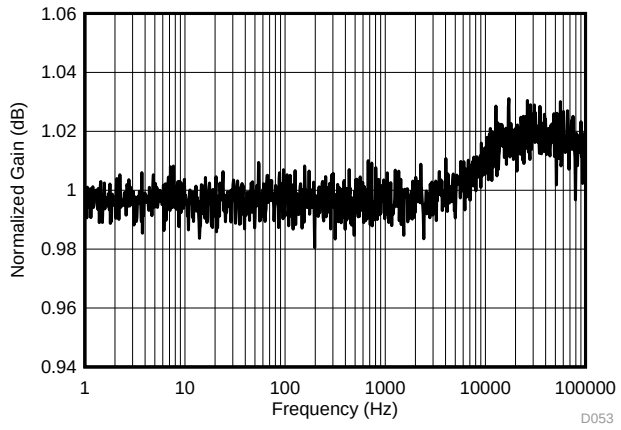


图 66. Gain Flatness of a DRV421-Based Closed-Loop Current Sensing Module

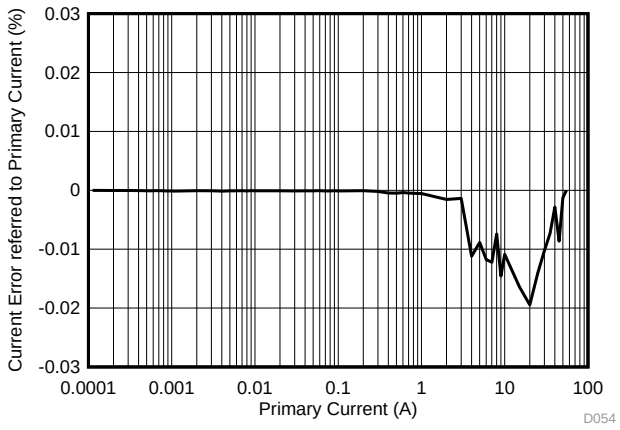


图 67. Current Error of a DRV421-Based Closed-Loop Current Sensing Module

Typical Application (接下页)

8.2.2 Differential Closed-Loop Current Sensing Module

The differential closed-loop current sensing module (图 68) measures the difference between two or more currents. Typical end-applications for such modules are leakage or residual current sensors. The high sensitivity of the fluxgate sensor and the low temperature drift make the DRV421 a suitable choice for this type of modules. The principle operation is the same as that of the closed-loop current module described in the *Closed-Loop Current Sensing Module* section. The compensation current corresponds to the current difference between the primary conductors.

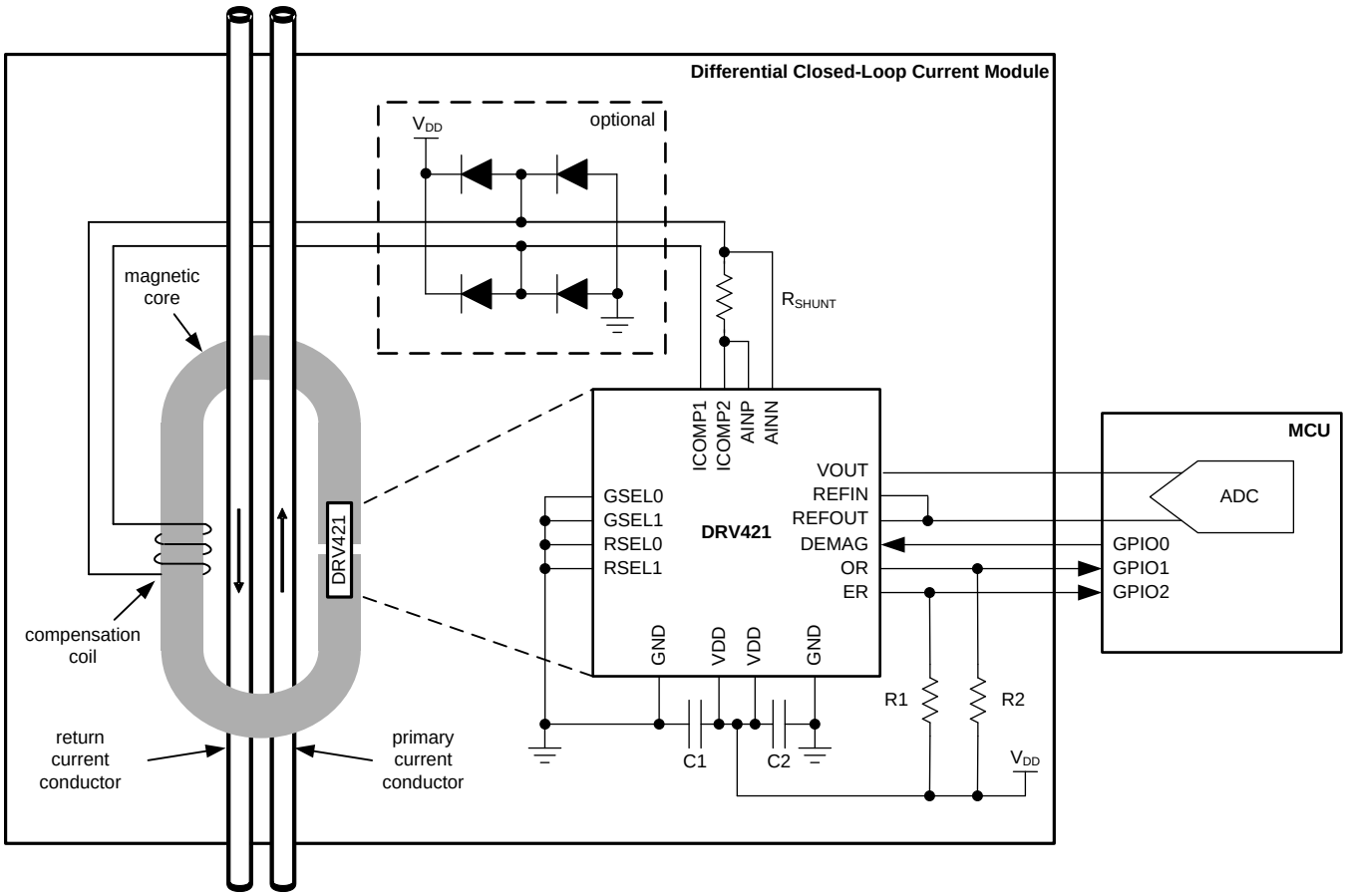


图 68. Differential Closed-Loop Current Sensing Module

Typical Application (接下页)

8.2.2.1 Design Requirements

As with the previous application, the compensation current creates a voltage drop across the shunt resistor. The maximum shunt resistor value is limited by supply voltage V_{DD}, the compensation current range, and the resistance of the compensation coil; see 公式 7.

However, in applications that sense leakage or residual currents, the difference between the primary currents is zero in normal operation. In fault condition only, there is a small difference current that is sensed in order to shut down the system to prevent damage to the device or the user. In this case, the compensation current is also very low, usually only in the range of few mA. Therefore, use a higher shunt resistor value in this case to support high sensitivity on system level. Consider the impact of shunt resistor value on gain and gain flatness as decribed in application report SLOA223, *Designing with the DRV421: Closed Loop Current Sensor Specifications*.

8.2.2.2 Detailed Design Procedure

For differential current sensing modules with a large shunt resistor and medium compensation coil inductance, use the gain setting that features the higher cross-over frequency of 3.8 kHz: GSEL[1:0] = 01.

8.2.2.3 Application Curve

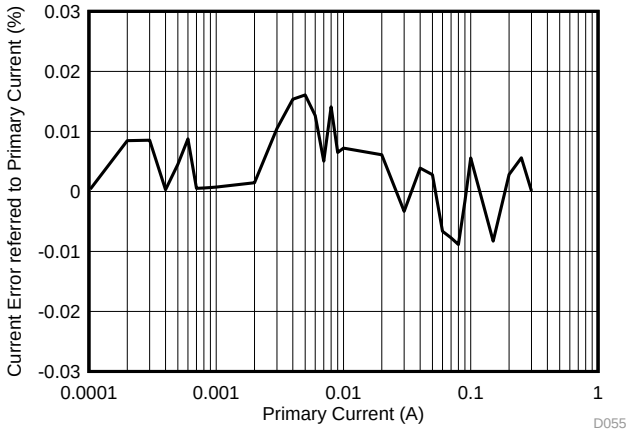


图 69. Current Error of a DRV421-Based Differential Closed-Loop Current Sensing Module

Typical Application (接下页)

8.2.3 Using the DRV421 in ±15-V Sensor Applications

The DRV421 is designed for 3.3-V or 5-V nominal operation. To support a wider module current range, the device is also used in ±15-V application, as shown in 图 70. In this application, an external regulator generates the 5-V supply for the DRV421. An additional external ±15-V power driver stage drives the compensation coil. These techniques allow the design of exceptionally precise and stable ±15-V current-sense modules.

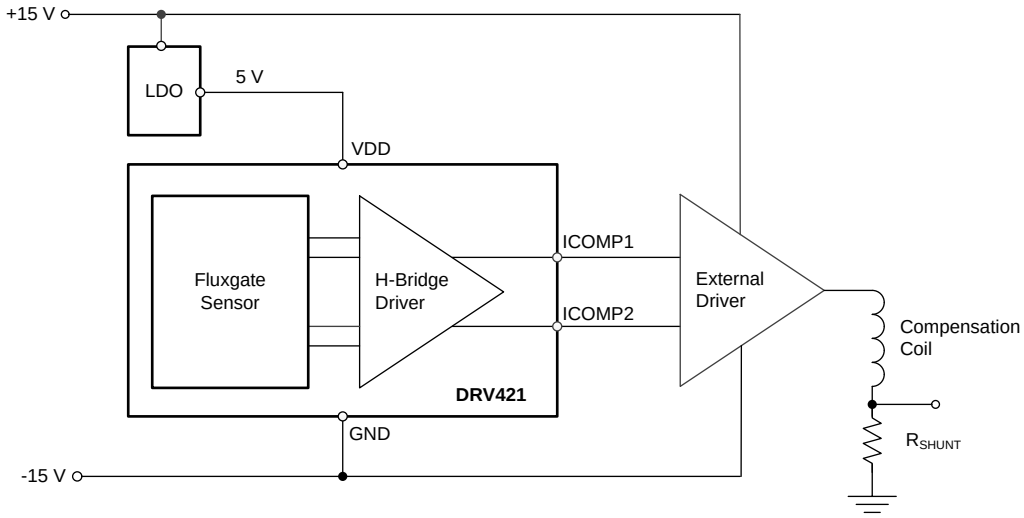


图 70. ±15-V Current-Sense Modules

9 Power-Supply Recommendations

9.1 Power-Supply Decoupling

Decouple both VDD pins of the DRV421 with 1-uF X7R-type ceramic capacitors to the adjacent GND pin as illustrated in 图 71. For best performance, place both decoupling capacitors as close to the related power-supply pins as possible. Connect these capacitors to the power-supply source in a way that allows the current to flow through the pads of the decoupling capacitors.

9.2 Power-On Start Up and Brownout

Power-on is detected when the supply voltage exceeds 2.4 V at VDD pin. At this point, DRV421 initiates following start-up sequence:

1. Digital logic starts up and waits for 26 µs for the supply to settle.
2. Fluxgate sensor powers up.
3. If fluxgate sensor saturation is detected, search function starts as described in the *Search Function* section.
4. If DEMAG pin is set high, demagnetization cycle starts as described in the *Magnetic Core Demagnetization* section.
5. The compensation loop is active after the demagnetization cycle, or 80 µs after the supply voltage exceeds 2.4 V.

During this startup sequence, the ICOMP1 and ICOMP2 outputs are pulled low to prevent undesired signals on the compensation coil, and the ER pin is asserted low.

The DRV421 tests for low supply voltages with a brownout voltage level of 2.4 V. Use a power-supply source capable of supporting large current pulses driven by the DRV421, and low ESR bypass capacitors for stable supply voltage in the system. A supply drop below 2.4-V that lasts longer than 20 µs generates a power-on reset; the device ignores shorter voltage drops. A voltage drop on the VDD pin to below 1.8 V immediately initiates a power-on reset. After the power supply returns to 2.4 V, the device initiates a start-up cycle, as described at the beginning of this section.

9.3 Power Dissipation

The thermally-enhanced, PowerPAD, WQFN package reduces the thermal impedance from junction to case. This package has a downset lead frame on which the die is mounted. The lead frame has an exposed thermal pad (PowerPAD) on the underside of the package, and provides a good thermal path for the heat dissipation.

The power dissipation on both linear outputs ICOMP1 and ICOMP2 is calculated with 公式 8:

$$P_{D(ICOMP)} = I_{ICOMP} \times (V_{ICOMP} - V_{SUPPLY}) \quad (8)$$

where

- V_{SUPPLY} = voltage potential closer to V_{ICOMP}, V_{DD}, or GND

CAUTION

Output short-circuit conditions are particularly critical for the H-bridge driver output pins ICOMP1 and ICOMP2. The full supply voltage occurs across the conducting transistor and the current is only limited by the current density limitation of the FET; permanent damage can occur. The DRV421 does not feature temperature protection or thermal shut-down.

9.3.1 Thermal Pad

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences the overall heat dissipation. Technical details are described in application report SLMA002, *PowerPad Thermally Enhanced Package,* available for download at www.ti.com.

10 Layout

10.1 Layout Guidelines

The DRV421 unique, integrated fluxgate has a very high sensitivity to magnetic fields in order to enable design of a closed-loop current sensor with best-in-class precision and linearity. Observe proper PCB layout techniques because any current-conducting wire in the direct vicinity of the DRV421 generates a magnetic field that may distort measurements. Common passive components and some PCB plating materials contain ferromagnetic materials that are magnetizable. For best performance, use the following layout guidelines:

- Route current conducting wires in pairs: route a wire with an incoming supply current next to, or on top of its return current path. The opposite magnetic field polarity of these connection cancel each other. To facilitate this layout approach, the DRV421 positive and negative supply pins are located next to each other.
- Route the compensation coil connections close to each other as a pair to reduce coupling effects.
- Route currents parallel to the fluxgate sensor sensitivity axis as shown in 图 71. As a result, magnetic fields are perpendicular to the fluxgate sensitivity, and have limited impact.
- Vertical current flow (for example, through vias) generates a field in the fluxgate-sensitive direction. Minimize the number of vias in vincinity of the DRV421.
- Place all passive components (for example, decoupling capacitors and the shunt resistor) outside of the portion of the PCB that is inserted into the magnetic core gap. Use nonmagnetic components to prevent magnetizing effects.
- Do not use PCB trace finishes using nickel-gold plating because of the potential for magnetization.
- Connect all GND pins to a local ground plane.

Ferrite beads in series to the power-supply connection reduce interaction with other circuits powered from the same supply voltage source. However, to prevent influence of the magnetic fields if ferrite beads are used, do not place them next to the DRV421.

The reference output (REFOUT pin) refers to GND. Use a low-impedance and star-type connection to reduce the driver current and the fluxgate sensor current modulating the voltage drop on the ground track. The REFOUT and VOUT outputs are able to drive some capacitive load, but avoid large direct capacitive loading because of increased internal pulse currents. Given the wide bandwidth of the shunt sense amplifier, isolate large capacitive loads with a small series resistor.

Solder the exposed PowerPAD, on the bottom of the package to the ground layer because the PowerPAD is internally connected to the substrate that must be connected to the most-negative potential.

图 71 illustrates a generic layout example that highlights the placement of components that are critical to the DRV421 performance. For specific layout examples, see SLOU409, *DRV421EVM Users Guide*, and TIDUA92, *TIPD196 Design Guide*.

10.2 Layout Example

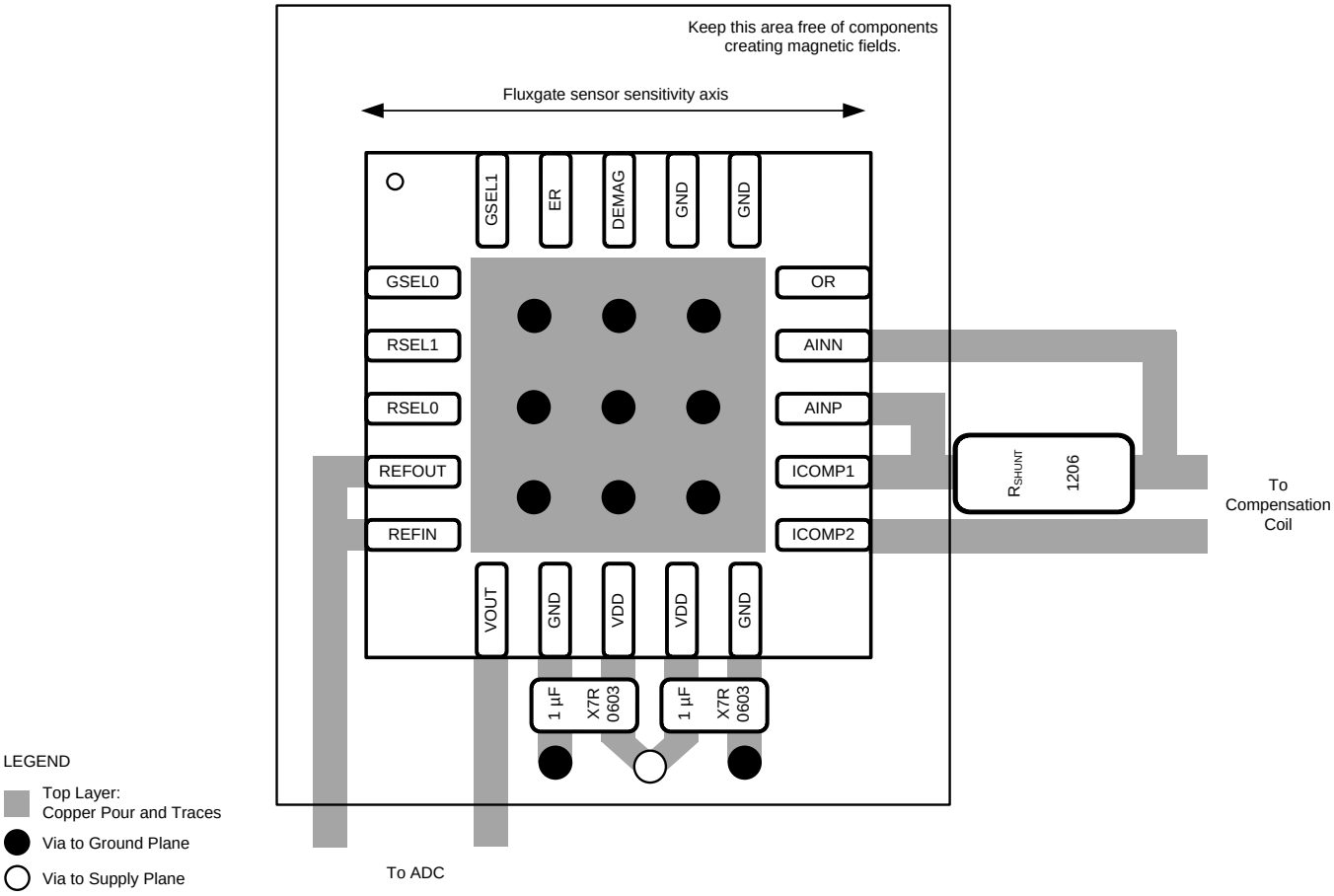


图 71. Generic Layout Example (Top View)

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

- 《DRV421EVM 用户指南》，SLOU409
- 《TIPD196 设计指南》，TIDUA92
- *《基于 DRV421 的设计：闭环电流传感器规范》*，SLOA223
- *《基于 DRV421 的设计：控制环路稳定性》*，SLOA224

11.2 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV421RTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	-----> DRV421	Samples
DRV421RTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	-----> DRV421	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

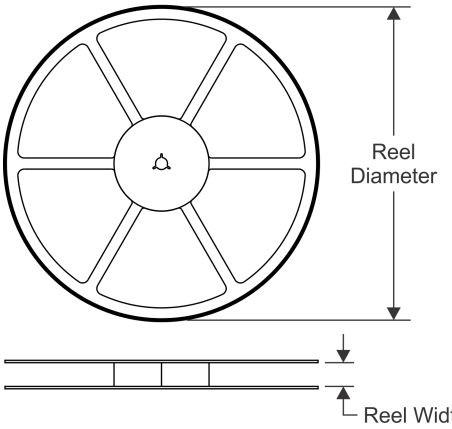
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

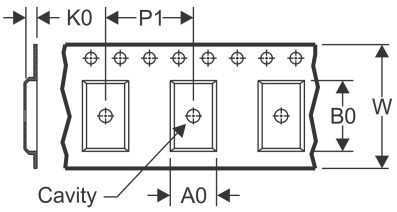
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

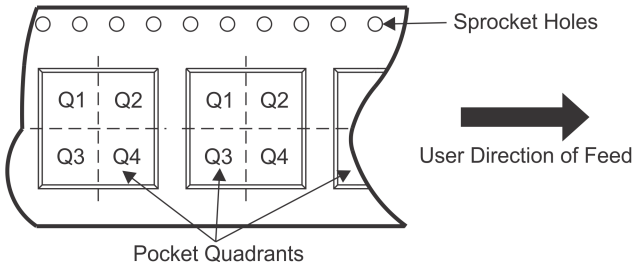


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

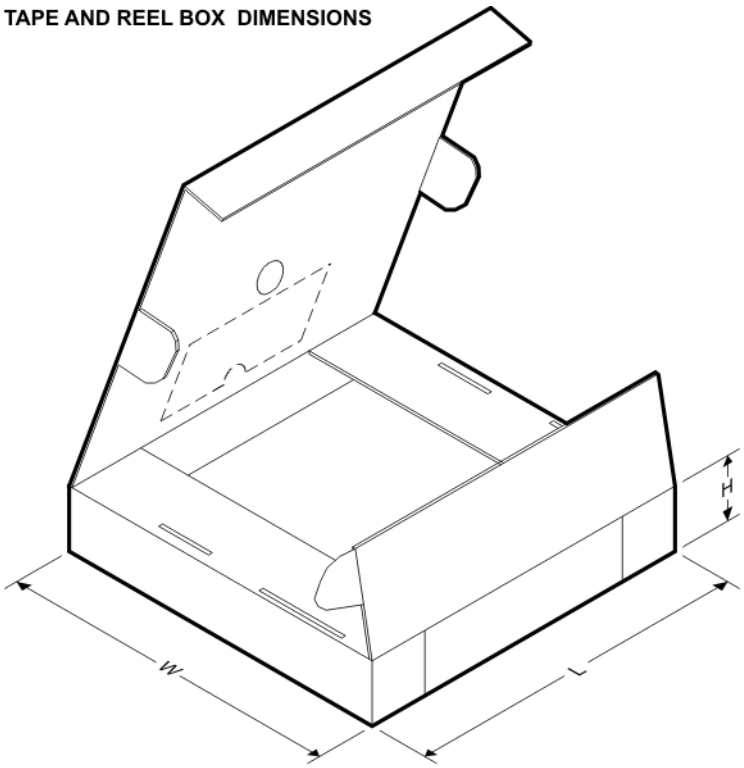
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV421RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV421RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV421RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
DRV421RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

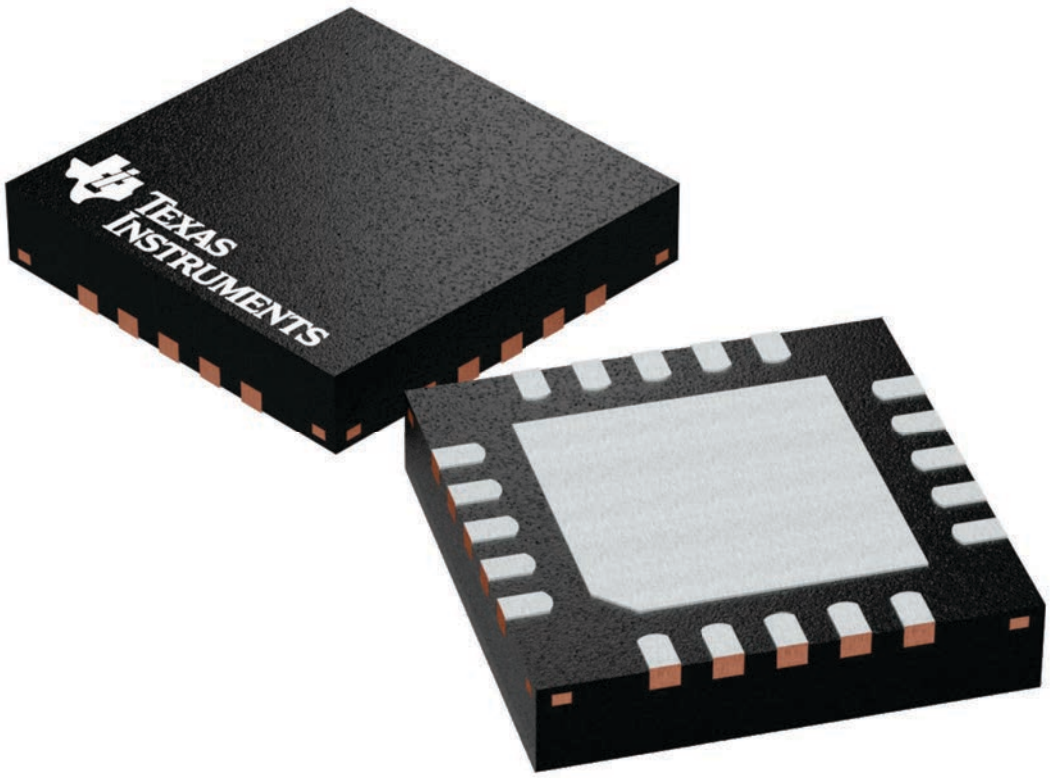
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

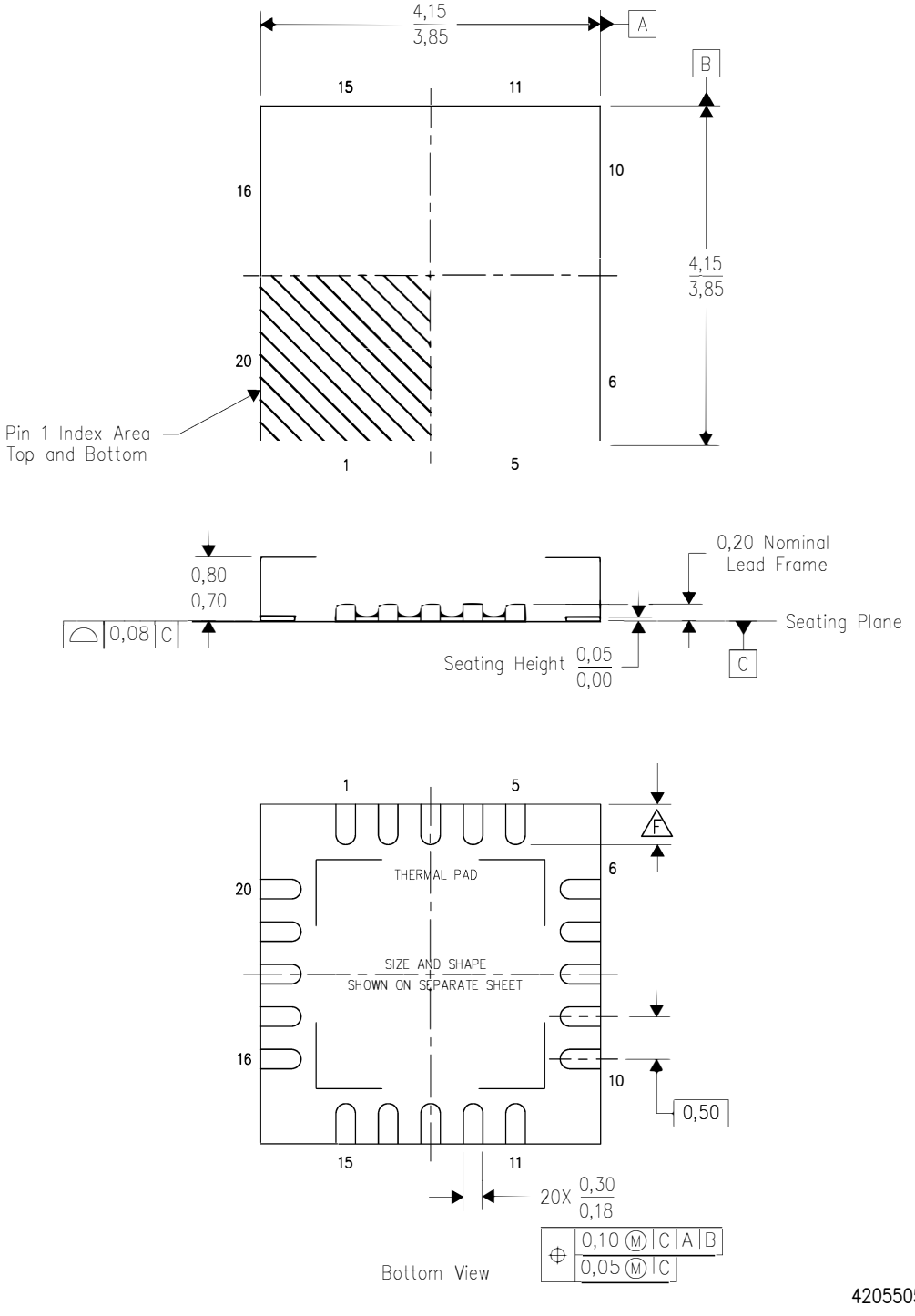
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

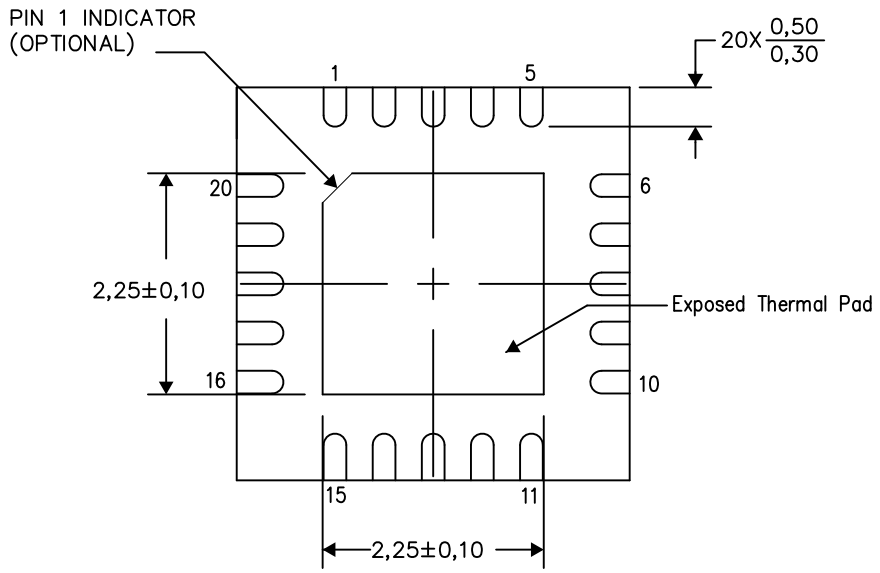
RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206256–8/V 05/15

NOTE: All linear dimensions are in millimeters

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