



门控 H 类、双端口 VDSL2 线路驱动器

 查询样品: [THS6226](#)

特性

- 数字式可调节静态电流:
7.6mA 至 23.0mA
- **1.0mA** 偏置电流步进
- 独立的升压和主线路驱动器停用
- 低功耗线路终端模式
- 完整的电容器再充电: **3ms**
- 低输出电压噪声密度:
6.3 nV/√Hz Input-Referred Voltage Noise
- 低 MTPR 失真:
70dB with +19.8dBm G.993.2—Profile 8b
- **-91dBc HD3 (1MHz, 60Ω 差分负载)**
- 高输出电流: (可向 **60Ω** 负载输送 **383mA** 的电流)
- 宽输出摆幅: **40V_{PP}** (+12V, 100Ω 差分负载和一个 **1:1.4** 变压器)
- 大带宽: **125MHz**
- 端口至端口隔离度: 在 **1MHz** 频率下为 **90dB**
- 在 **1MHz** 频率下提供了 **50dB** 的 **PSRR** 以实现优良的隔离

应用

- 非常适合于所有的 **VDSL2** 传输模式
- 返回兼容 **ADSL / ADSL2+ / ADSL2++** 系统

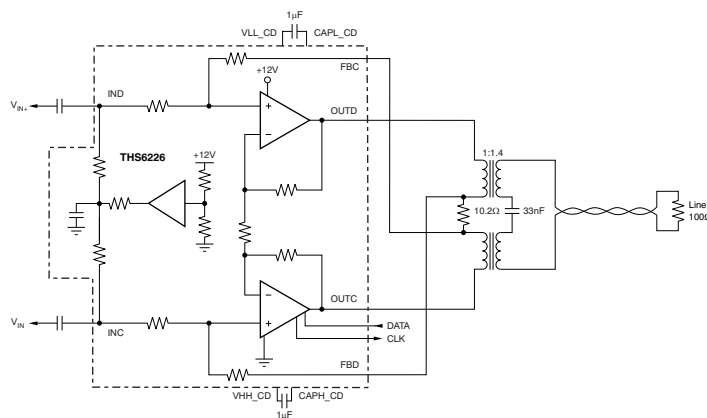
说明

THS6226 是一款双端口、H 类、电流反馈架构、差分线路驱动器放大器系统,非常适合于 xDSL 系统。该器件旨在应用于 VDSL2 (超高位速率数字用户线路 2) 线路驱动器系统,此类系统可启用本地 DTM 信号,同时支持高于 +20.5dBm 的线路功率(在高达 8.5MHz 的频率条件下)和上佳的线性度,从而支持 G.993.2 VDSL2 8b 传输模式。另外,它还拥有足以支持 +14.5dBm 线路功率(在高达 30MHz 的频率下)的中心局传输的高速度。

THS6226 的独特架构提供了极小的静态电流,同时仍然实现了超高的线性度。在全偏置条件和 1MHz 频率下,差分失真为 -91dBc,而在 5MHz 频率下则降至仅 -75dBc。对于并不需要放大器全部性能的线路长度,放大器的多种固定偏置设定值可提升节能效果。为了在所有的传输模式中提供更大的灵活性及节能幅度,可对静态电流进行数字式调节(调节范围从 7.67mA 至 23mA),并具有一个 1.0mA 的偏置电流步进。对于那些希望在不进行传输的时候实现更多节能的系统,THS6226 可在其线路终端模式中使用,以保持阻抗匹配。

采用 +12V 电源时的宽输出摆幅与出色的电流驱动能力相结合,提供了宽动态余量,从而将失真抑制在极低的水平上。

THS6226 采用 QFN-32 PowerPAD™ 封装。



利用 THS6226 的一个端口的典型 VDSL2 线路驱动器电路



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| PRODUCT ⁽²⁾ | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING | TRANSPORT MEDIA, QUANTITY |
|------------------------|--------------|--------------------|-----------------|---------------------------|
| THS6226IRHBT | VQFN-32 | RHB | THS6226IRHB | Tape and Reel, 250 |
| THS6226IRHBR | | | | Tape and Reel, 3000 |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
- (2) The PowerPAD is electrically isolated from all other pins.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

| PARAMETER | | THS6226 | UNIT |
|---|----------------------------|---|------|
| Supply voltage, GND to V_{S+} , class AB only | | 15 | V |
| Supply voltage, GND to V_{S+} , class H only | | 12.5 | V |
| Input voltage, V_I | | 15 | V |
| Output current, I_O : static dc ⁽²⁾ | | ±100 | mA |
| Continuous power dissipation | | See Thermal Information table | |
| Normal storage temperature | | –40 to +85 | °C |
| Maximum junction temperature, any condition, T_J ⁽³⁾ | | +150 | °C |
| Maximum junction temperature, continuous operation, long-term reliability, T_J ⁽⁴⁾ | | +130 | °C |
| Storage temperature range, T_{STG} | | –65 to +150 | °C |
| ESD ratings: | Human body model (HBM) | 2000 | V |
| | Charged device model (CDM) | 500 | V |
| | Machine model (MM) | 100 | V |

- (1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
- (2) The THS6226 incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief [SLMA002](#) for more information about utilizing the PowerPAD thermally-enhanced package. Under high-frequency ac operation (> 10kHz), the short-term output current capability is much greater than the continuous dc output current rating. This short-term output current rating is about 8.5x the dc capability, or approximately ±850mA.
- (3) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
- (4) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | THS6226 | UNITS |
|-------------------------------|--|---------|-------|
| | | RHB | |
| | | 32 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance | 35.1 | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance | 22.1 | |
| θ_{JB} | Junction-to-board thermal resistance | 7.0 | |
| Ψ_{JT} | Junction-to-top characterization parameter | 0.3 | |
| Ψ_{JB} | Junction-to-board characterization parameter | 6.9 | |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance | 1.3 | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

ELECTRICAL CHARACTERISTICS: $V_S = +12V$
Boldface limits are tested at **+25°C**.

 At $T_A = +25^\circ\text{C}$, with $R_{MATCH} = 10.2\Omega$, transformer turn ratio 1:1.4, $R_L = 100\Omega$ differential at transformer output, Full Bias Mode, and active impedance circuit configuration, unless otherwise noted. Each port is tested independently.

| PARAMETER | CONDITIONS | THS6226IRHB | | | UNIT | TEST LEVEL ⁽¹⁾ |
|---|--|-----------------------------|------------|------------|------------------------------|---------------------------|
| | | MIN | TYP | MAX | | |
| AC PERFORMANCE | | | | | | |
| Small-signal bandwidth, -3dB | $V_O = 2V_{PP}$, differential at OUTCD and OUTAB, gain = 19V/V | | 125 | | MHz | C |
| 0.1dB bandwidth flatness | $V_O = 2V_{PP}$ | | 37 | | MHz | C |
| Large-signal bandwidth | $V_O = 10V_{PP}$ | | 125 | | MHz | C |
| Slew rate (10% to 90% level) | $V_O = 15V$ step, differential | | 1500 | | V/ μs | C |
| Rise and fall time | $V_O = 2V_{PP}$ | | 2.8 | | ns | C |
| Harmonic distortion | $V_O = 2V_{PP}$, $R_L = 60\Omega$ differential | | | | | C |
| Second harmonic | Full bias, $f = 1\text{MHz}$ | | -91 | | dBc | C |
| Third harmonic | Full bias, $f = 1\text{MHz}$ | | -91 | | dBc | C |
| Second harmonic | Full bias, $f = 5\text{MHz}$ | | -70 | | dBc | C |
| | Low bias, $f = 5\text{MHz}$ | | -64 | | dBc | C |
| Third harmonic | Full bias, $f = 5\text{MHz}$ | | -75 | | dBc | C |
| | Low bias, $f = 5\text{MHz}$ | | -47 | | dBc | C |
| Differential input voltage noise | $f = 1\text{MHz}$, input-referred | | 6.3 | | nV/ $\sqrt{\text{Hz}}$ | C |
| DC PERFORMANCE | | | | | | |
| Differential gain | | | 19 | | V/V | C |
| Differential gain error ⁽²⁾ | | | | ± 2.5 | % | A |
| Input offset voltage | | | ± 1 | ± 5 | mV | A |
| | -40°C to +85°C | | | ± 6 | mV | B |
| Input offset voltage drift | | | | 15 | $\mu\text{V}/^\circ\text{C}$ | B |
| Input offset voltage matching | Channels 1 to 2 and 3 to 4 only | | ± 1 | ± 5 | mV | A |
| INPUT CHARACTERISTICS | | | | | | |
| Noninverting input resistance | | | 500 2 | | k Ω pF | C |
| Input bias voltage | | 5.8 | 6 | 6.2 | V | A |
| OUTPUT CHARACTERISTICS | | | | | | |
| Class H output voltage swing | $R_L = 60\Omega$ differential, class H operation ⁽³⁾⁽⁴⁾ , each output | +16/-4 | +17.5/-5.5 | | V | A |
| | -40°C to +85°C ⁽³⁾⁽⁴⁾ | +15.7/-3.7 | | | V | B |
| Class H output current (sourcing, sinking) | $R_L = 60\Omega$ differential, class H operation | ± 333 | ± 383 | | mA | A |
| | -40°C to +85°C | ± 323 | | | mA | B |
| Class AB output voltage swing | $R_L = 60\Omega$ differential, normal operation ⁽³⁾ , each output | +9.9/+2.1 | +10.1/+1.9 | | V | A |
| | -40°C to +85°C ⁽³⁾ | +9.8/+2.2 | | | V | B |
| Class AB output current (sourcing, sinking) | $R_L = 60\Omega$ differential, normal operation | ± 130 | ± 137 | | mA | A |
| | -40°C to +85°C | ± 126 | | | mA | B |
| Short-circuit output current | | | 1 | | A | C |
| Output impedance | $f = 1\text{MHz}$, differential | | 0.2 | | Ω | C |
| Crosstalk | $f = 1\text{MHz}$, $V_{OUT} = 2V_{PP}$, port 1 to port 2 | | -90 | | dB | C |

- (1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
- (2) Negative feedback loop only.
- (3) Measured at amplifier output (pin 17, 20, 21, and 24).
- (4) Capacitor fully charged, no droop.

ELECTRICAL CHARACTERISTICS: $V_S = +12V$ (continued)

Boldface limits are tested at **+25°C**.

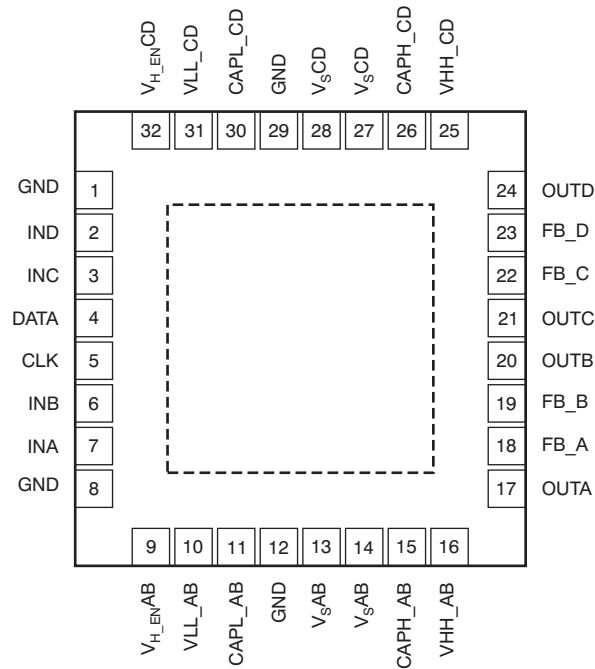
At $T_A = +25^\circ\text{C}$, with $R_{\text{MATCH}} = 10.2\Omega$, transformer turn ratio 1:1.4, $R_L = 100\Omega$ differential at transformer output, Full Bias Mode, and active impedance circuit configuration, unless otherwise noted. Each port is tested independently.

| PARAMETER | CONDITIONS | THS6226IRHB | | | UNIT | TEST LEVEL ⁽¹⁾ |
|--|---|-------------|---------|-------------|------------------|---------------------------|
| | | MIN | TYP | MAX | | |
| POWER SUPPLY | | | | | | |
| Maximum operating voltage | Class AB | +10 | +12 | +15 | V | A |
| | –40°C to +85°C | +10 | | +15 | V | B |
| | Class H | +10 | +12 | +12.5 | V | B |
| | –40°C to +85°C | +10 | | +12.5 | | B |
| I_{S+} quiescent current | Per port, full bias, class H enable (power supply connected together) | 22.5 | 23.5 | 24.5 | mA | A |
| | –40°C to +85°C | 21.8 | | 25.2 | mA | B |
| | Per port, full bias, class H disable (power supply connected together) | 22.0 | 23.0 | 24.0 | mA | A |
| | –40°C to +85°C | 21.3 | | 24.7 | mA | B |
| | Bias current step | | 1.0 | | mA | C |
| | Per port, low bias, class H disable (power supply connected together) | 7.2 | 7.6 | 8 | mA | A |
| | –40°C to +85°C | 6.9 | | 8.3 | mA | B |
| | Per port, line termination mode (B9 = B8 = B7 = B6 = 0) (power supply connected together) | | 4.4 | | mA | C |
| | Both ports, main amplifiers and class H disable (B9 = B8 = B7 = B6 = 0) | | 1.7 | 2.2 | mA | A |
| | –40°C to +85°C | | | 2.3 | mA | B |
| Power-supply rejection (PSRR) | Differential, from +12V, GND | 60 | 70 | | dB | A |
| | –40°C to +85°C | 58 | | | dB | B |
| LOGIC | | | | | | |
| Logic pin logic threshold | Logic 1, with respect to GND ⁽⁵⁾ | 1.9 | | | V | C |
| | Logic 0, with respect to GND ⁽⁵⁾ | | | 0.8 | V | C |
| Logic pin quiescent current | Logic X = 0.5V (logic 0) | | 10 | 25 | μA | A |
| | –40°C to +85°C | | | 30 | μA | B |
| | Logic X = 3.3V (logic 1) | | 66 | 125 | μA | A |
| | –40°C to +85°C | | | 130 | μA | B |
| Turn-on time delay (t_{ON}) | Time for I_S to reach 50% of final value | | 1 | | μs | C |
| Turn-off time delay (t_{OFF}) | Time for I_S to reach 50% of final value | | 1 | | μs | C |
| Logic pin input impedance | | | 50 1 | | k Ω pF | C |

(5) The GND pin usable range is from V_{S-} to $(V_{S+} - 5V)$.

PIN CONFIGURATIONS

**QFN-32⁽¹⁾⁽²⁾
RHB PACKAGE
(TOP VIEW)**



- (1) The PowerPAD is electrically isolated from all other pins and can be connected to any potential voltage range from V_{S-} to V_{S+} . Typically, the PowerPAD is connected to the GND plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.
- (2) The THS6226 defaults to the disabled mode at power-up.

PIN DESCRIPTIONS

| NAME | PIN | DESCRIPTION |
|---------------------|-----|--|
| GND | 1 | Analog ground |
| IND | 2 | Input D of amplifier CD |
| INC | 3 | Input C of amplifier CD |
| DATA | 4 | Serial interface data pin |
| CLK | 5 | Serial interface CLK pin |
| INB | 6 | Input B of amplifier AB |
| INA | 7 | Input A of amplifier AB |
| GND | 8 | Analog ground |
| V _{H_ENAB} | 9 | Class H mode control pin for amplifier AB |
| VLL_AB | 10 | Amplifier AB low pump supply |
| CAPL_AB | 11 | Amplifier AB negative voltage pump capacitor pin |
| GND | 12 | Analog ground |
| V _{SAB} | 13 | Amplifier AB supply voltage |
| V _{SAB} | 14 | Amplifier AB supply voltage |
| CAPH_AB | 15 | Amplifier AB positive voltage pump capacitor pin |
| VHH_AB | 16 | Amplifier AB high pump supply |
| OUTA | 17 | Output A of amplifier AB |
| FB_A | 18 | Feedback for active output impedance of amplifier AB |
| FB_B | 19 | Feedback for active output impedance of amplifier AB |
| OUTB | 20 | Output B of amplifier AB |
| OUTC | 21 | Output C of amplifier CD |
| FB_C | 22 | Feedback for active output impedance of amplifier CD |
| FB_D | 23 | Feedback for active output impedance of amplifier CD |
| OUTD | 24 | Output D of amplifier CD |
| VHH_CD | 25 | Amplifier CD high pump supply |
| CAPH_CD | 26 | Amplifier CD positive voltage pump capacitor pin |
| V _{SCD} | 27 | Amplifier CD supply voltage |
| V _{SCD} | 28 | Amplifier CD supply voltage |
| GND | 29 | Analog ground |
| CAPL_CD | 30 | Amplifier CD negative voltage pump capacitor pin |
| VLL_CD | 31 | Amplifier CD low pump supply |
| V _{H_ENCD} | 32 | Class H mode control pin for amplifier CD |

TIMING CHARACTERISTICS

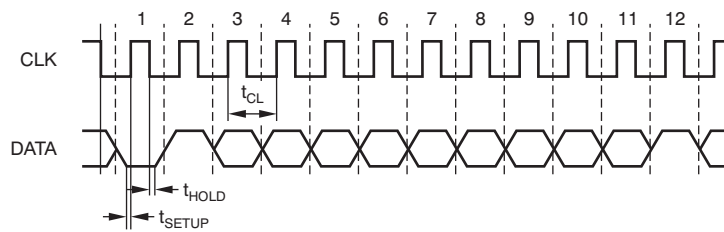


Figure 1. Serial Interface Timing

| PARAMETER | DESCRIPTION | THS6226 | | UNITS |
|--------------------|--------------|---------|-----|-------|
| | | MIN | MAX | |
| t _{SETUP} | Setup time | 3 | | ns |
| t _{HOLD} | Hold time | 0.5 | | ns |
| t _{CL} | Clock period | 200 | | ns |

TYPICAL CHARACTERISTICS: $V_S = +12V$

At $T_A = +25^\circ C$ and Full Bias Mode, unless otherwise noted

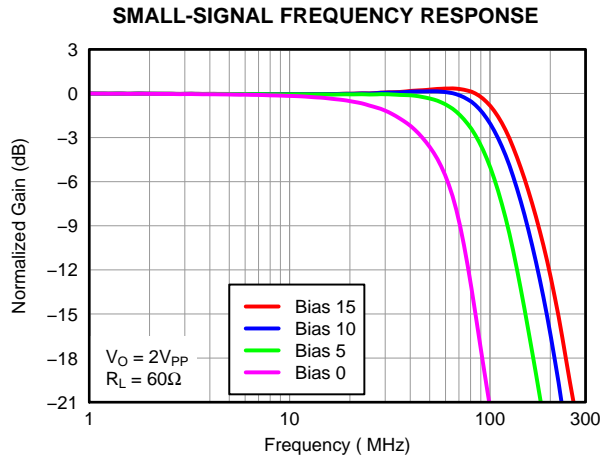


Figure 2.

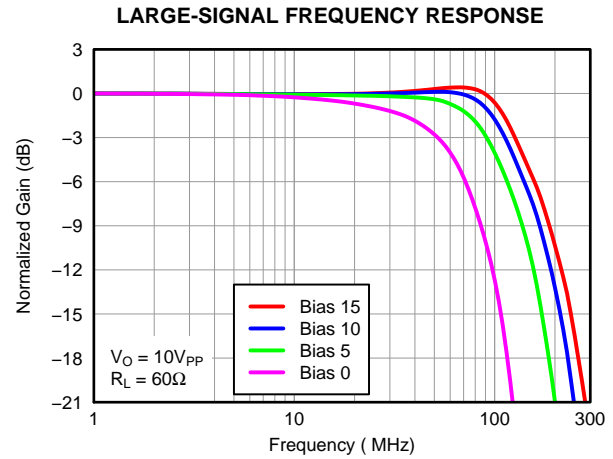


Figure 3.

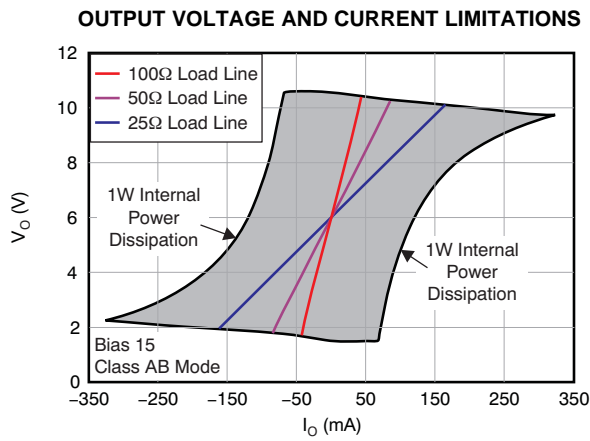


Figure 4.

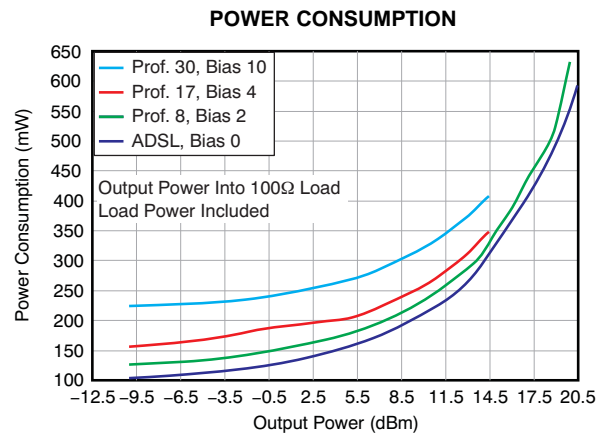


Figure 5.

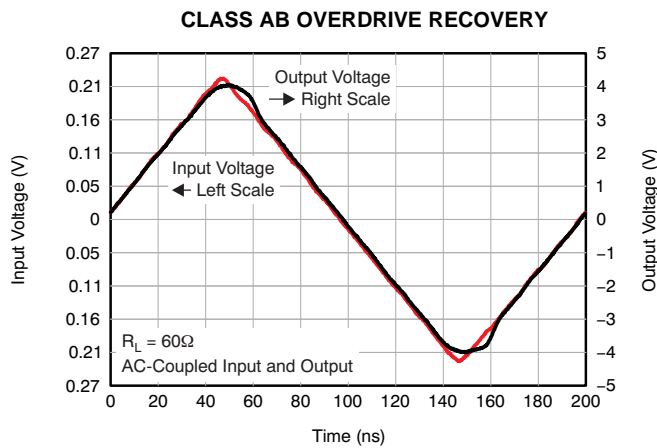


Figure 6.

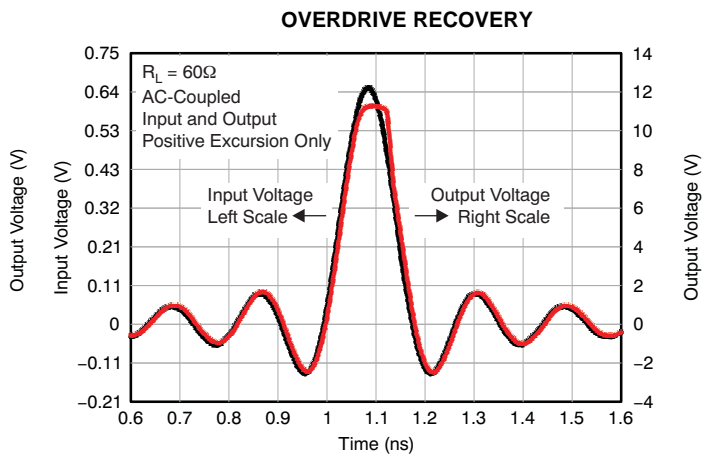


Figure 7.

TYPICAL CHARACTERISTICS: $V_S = +12V$ (continued)

At $T_A = +25^\circ C$ and Full Bias Mode, unless otherwise noted

INPUT NOISE DENSITY

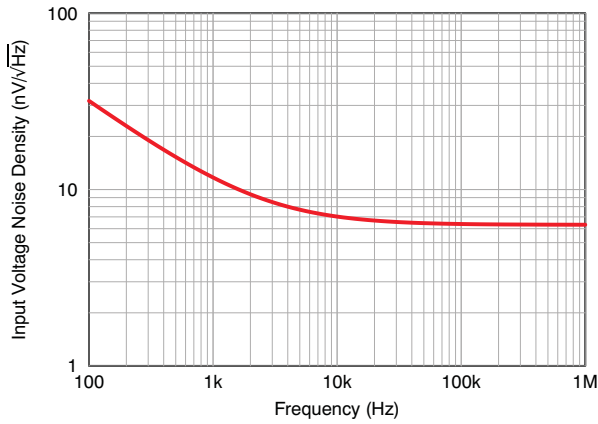


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

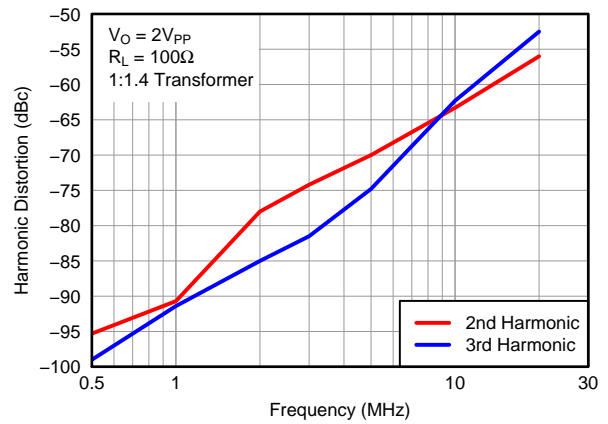


Figure 9.

HARMONIC DISTORTION vs LOAD

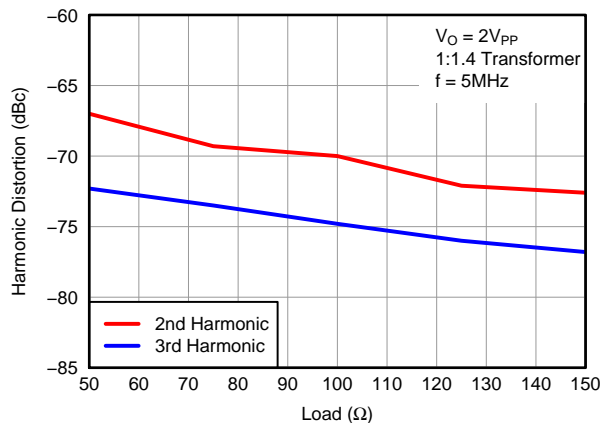


Figure 10.

TWO-TONE, THIRD-ORDER INTERMODULATION SPURIOUS

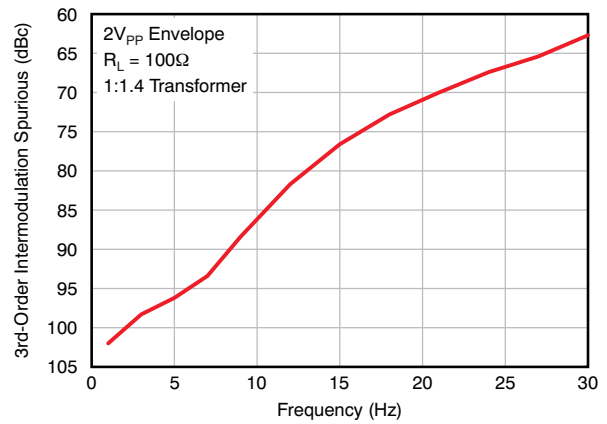


Figure 11.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

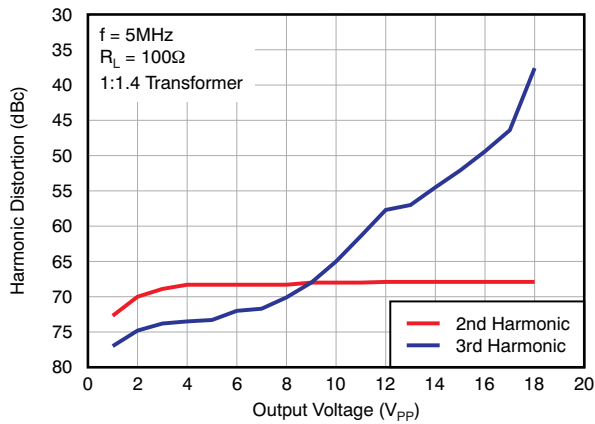


Figure 12.

HARMONIC DISTORTION vs BIAS CURRENT

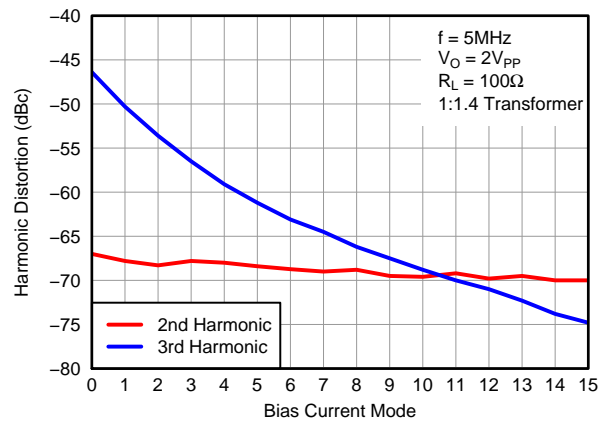


Figure 13.

TYPICAL CHARACTERISTICS: $V_S = +12V$ (continued)

At $T_A = +25^\circ C$ and Full Bias Mode, unless otherwise noted

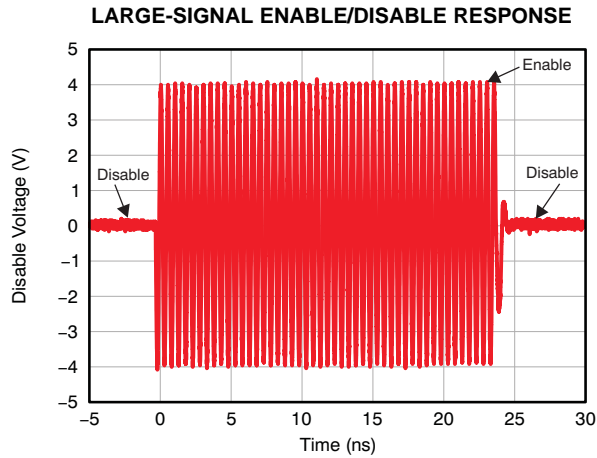


Figure 14.

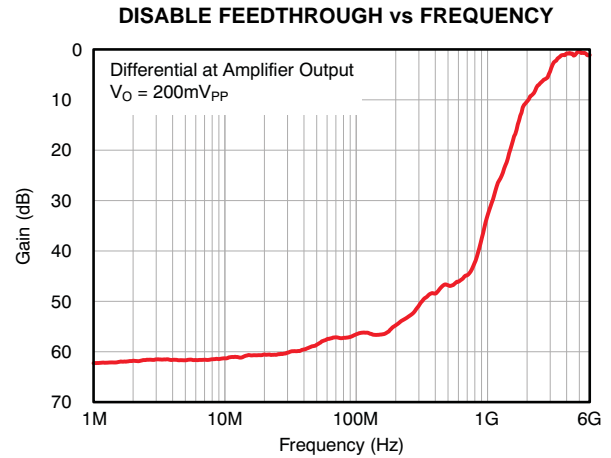


Figure 15.

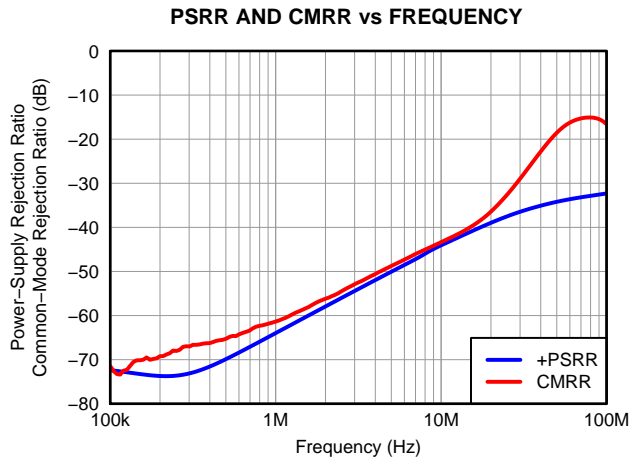


Figure 16.

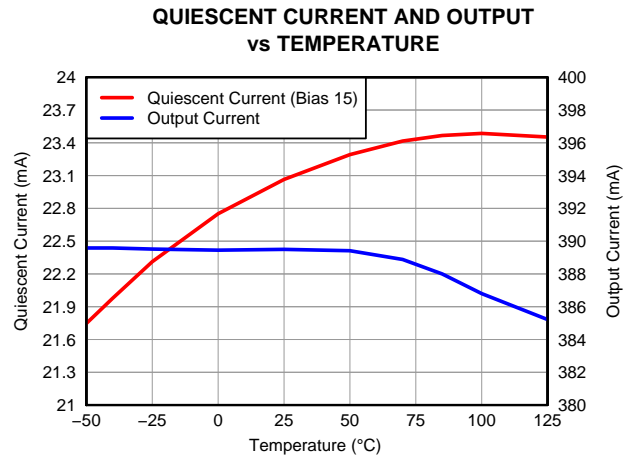


Figure 17.

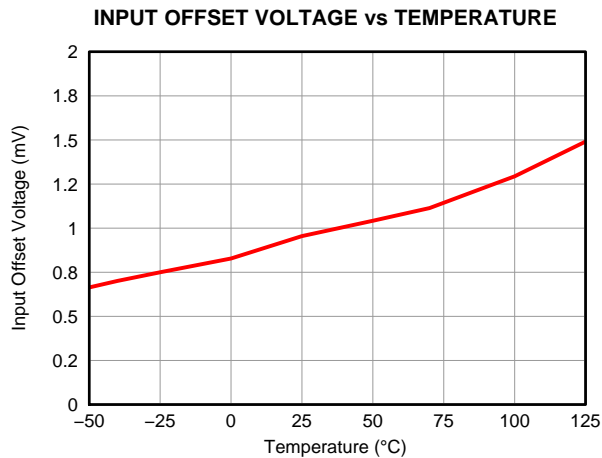


Figure 18.

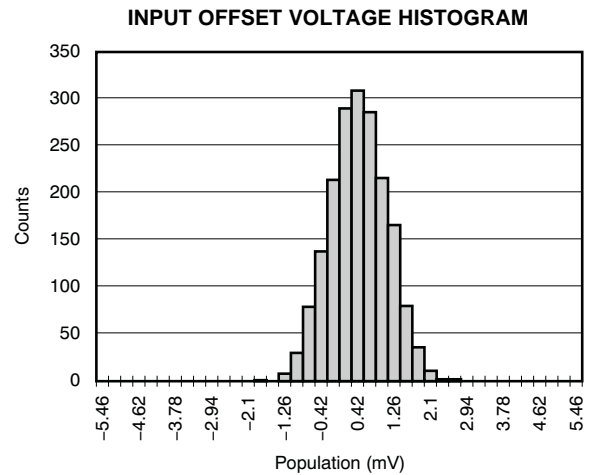


Figure 19.

APPLICATION INFORMATION

The THS6226 class H line driver provides exceptional ac performance in conjunction with wide output voltage swing. The class H operation allows voltage swings to exceed the power supply for short intervals limited only by the charge in the capacitor. In class AB mode, the THS6226 is capable of driving a 60Ω load from +1.9V to +10.1V. In class H mode, under the same conditions, the output voltage range becomes an impressive –5.5V to +17.5V, or 46V_{PP} differentially with the capacitor fully charged.

Figure 20 shows a fully-differential, noninverting amplifier configuration with active impedance. In this configuration, the 10.2Ω matching resistance appears through the transformer as 100Ω, minimizing reflection on the line, while also minimizing transmission losses. The THS6226 gain is fixed and equal to 19V/V from input of the amplifier to the output of the amplifier (IN_{CD} to OUT_{CD}), not including the transformer-turn ratio.

To simplify the implementation as well as provide design flexibility, the THS6226 contains an integrated mid-supply buffer that provides the correct biasing to the amplifier core without requiring any external components. Also present is a two-pin serial interface that provides exceptional design flexibility and allows minimal power consumption for each xDSL profile.

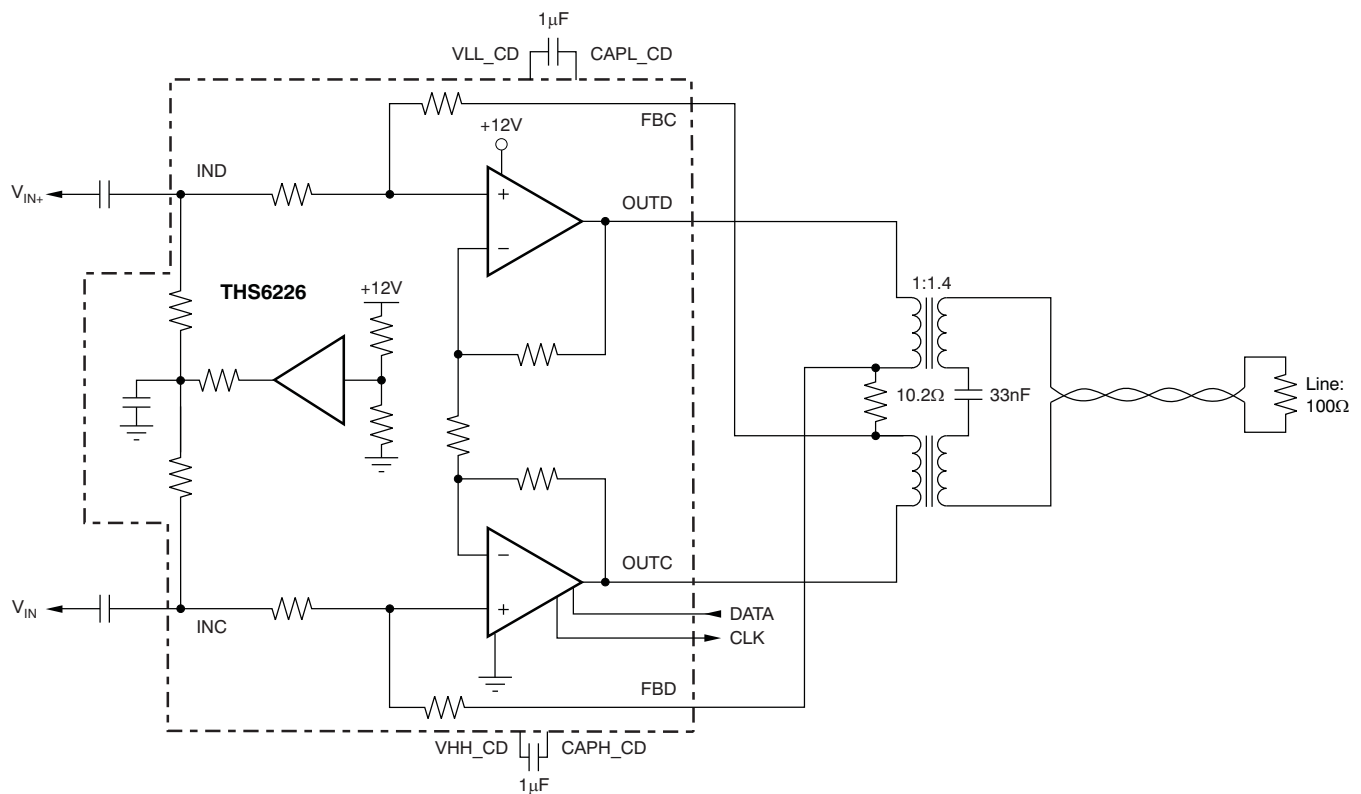


Figure 20. Multi-Tone Power Ratio (MTPR) Test Circuit

PROGRAMMING THE THS6226

Programming of the THS6226 is realized through a serial interface (pins 4 and 5) and proceeds in the following sequence.

Two start bits are required B0 = 0 followed by B1 = 1.

B2 through B9 are used to program the THS6226.

Refer to [Table 1](#) for the bit descriptions.

B10 (refer to [Table 2](#)) is the parity bit that controls if the word is or is not loaded.

B11 is the stop bit and should be set to B11 = 1. [Figure 21](#) shows the sequence to be adopted.

Table 1. SDATA

| PARAMETER | DESCRIPTION |
|-----------|---------------------------|
| B0, B1 | Start bit |
| B2, B3 | Channel select |
| B4, B5 | Power-down features |
| B6-B9 | Quiescent current setting |
| B10 | Parity bit |
| B11 | Stop bit |

Table 2. Parity Bit

| B10 | ODD PARITY BIT |
|-----|--|
| 0 | If odd, number of high bits in B2 to B9 |
| 1 | If even, number of high bits in B2 to B9 |

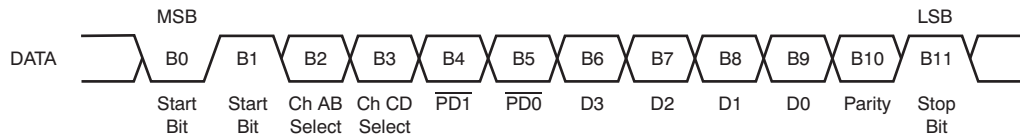


Figure 21. DATA Description

QUIESCENT CURRENT

The quiescent current of the THS6226 is dissipated in two main modules of the THS6226: the class AB and the charge pump. B4 and B5 select the mode of operation, class AB operating with or without the charge pump enabled, powering down the entire port, or operating in a line termination mode. [Table 4](#) lists the details on each bit functionality and the approximate quiescent current.

The class AB quiescent current is set by bits B6 to B9, using B4 and B5 for the power-down function, and B2 and B3 for channel select. The approximate quiescent current for the amplifier core is shown in [Table 3](#).

Table 3. Class AB Quiescent Current

| B6 (D3) | B7 (D2) | B8 (D1) | B9 (D0) | QUIESCENT CURRENT SETTING | APPROXIMATE I_Q (mA/Port) |
|---------|---------|---------|---------|---------------------------|-----------------------------|
| 0 | 0 | 0 | 0 | ADSL2+ mode | 7.6 |
| 0 | 0 | 0 | 1 | | 8.7 |
| 0 | 0 | 1 | 0 | Profile 8b mode | 9.8 |
| 0 | 0 | 1 | 1 | | 10.9 |
| 0 | 1 | 0 | 0 | Profile 17a mode | 12 |
| 0 | 1 | 0 | 1 | | 13 |
| 0 | 1 | 1 | 0 | | 14 |
| 0 | 1 | 1 | 1 | | 15 |
| 1 | 0 | 0 | 0 | | 16 |
| 1 | 0 | 0 | 1 | | 17 |
| 1 | 0 | 1 | 0 | Profile 30a mode | 18 |
| 1 | 0 | 1 | 1 | | 19 |
| 1 | 1 | 0 | 0 | | 20 |
| 1 | 1 | 0 | 1 | | 21 |
| 1 | 1 | 1 | 0 | | 22 |
| 1 | 1 | 1 | 1 | | 23 |

The various power modes are shown in [Table 4](#). For all modes, when B6 through B9 are not defined, set B9 = B8 = B7 = B6 = 0 to achieve the lowest power dissipation possible.

Table 4. Power Modes

| B4 (PD1) | B5 (PD0) | POWER-DOWN MODE | APPROXIMATE I_Q (mA/Port) |
|----------|----------|---|-----------------------------|
| 0 | 0 | Power-down (B9, B8, B7, B6 = 0) | 0.85 |
| 0 | 1 | Line termination mode (B9, B8, B7, B6 = 0) | 4.4 |
| 1 | 0 | Class AB driver I_Q set by B6 to B9, class H disabled | — |
| 1 | 1 | Class AB driver I_Q set by B6 to B9, class H enabled | — |

Channel selection is shown in [Table 5](#). Each channel can be programmed independently, or together if both B2 and B3 are set to '1'.

Table 5. Channel Selection

| B2 (Channel AB) | B3 (Channel CD) | CHANNEL SELECT |
|-----------------|-----------------|---|
| 0 | 0 | Bits B4 to B9 are ignored |
| 0 | 1 | Channel B programmed with B4 to B9 |
| 1 | 0 | Channel A programmed with B4 to B9 |
| 1 | 1 | Channels A and B programmed with B4 to B9 |

At startup, the internal register is set as shown in [Table 6](#).

Table 6. Internal Register

| B2 (Channel AB) | B3 (Channel CD) | B4 (PD1) | B5 (PD0) | B6 (D3) | B7 (D2) | B8 (D1) | B9 (D0) |
|-----------------|-----------------|----------|----------|---------|---------|---------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

In this condition, the total quiescent power dissipation is 10.2mW/port on a +12V supply.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (February 2011) to Revision C | Page |
|--|-------------|
| • Changed LOGIC, <i>Logic pin input impedance</i> typical specification and unit in Electrical Characteristics table | 4 |
| • Changed Timing Characteristics section | 6 |

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| THS6226IRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | THS6226 IRHB |  |
| THS6226IRHBT | ACTIVE | VQFN | RHB | 32 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | THS6226 IRHB |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| THS6226IRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| THS6226IRHBT | VQFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| THS6226IRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| THS6226IRHBT | VQFN | RHB | 32 | 250 | 210.0 | 185.0 | 35.0 |

GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

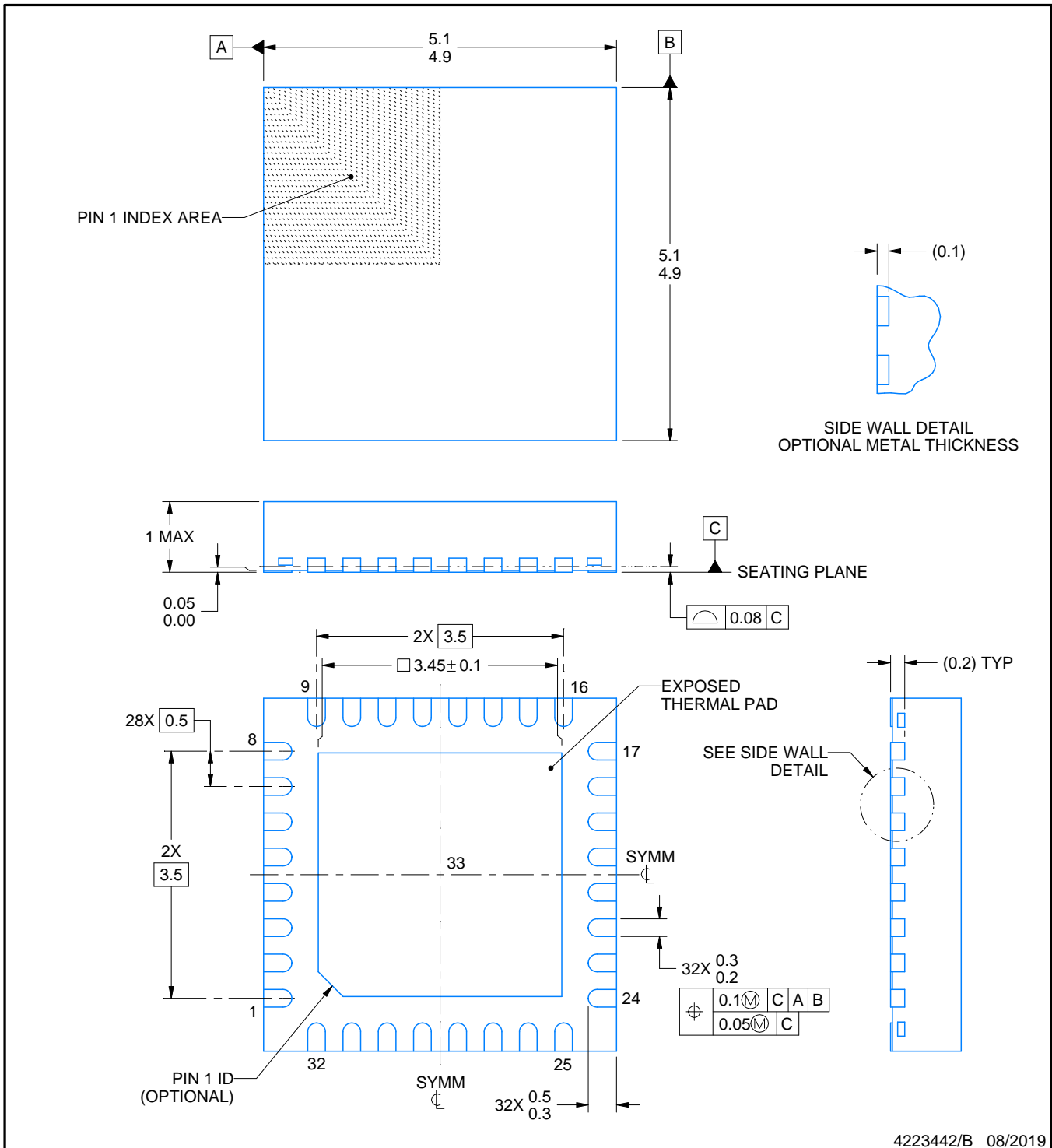
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A



4223442/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

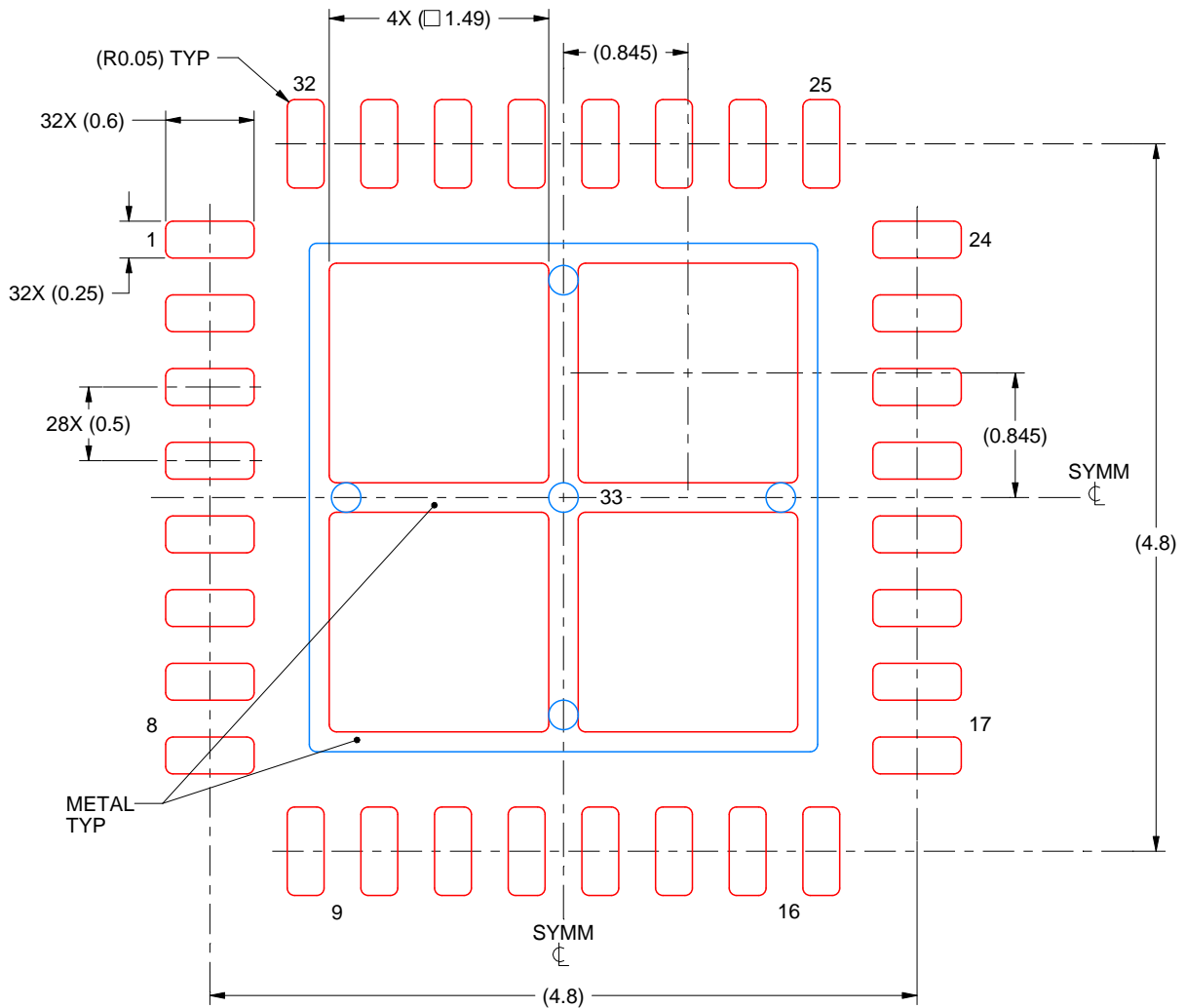
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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