LP3910 Power Management IC for Hard-Drive-Based Portable Media Players

1 Features

- Two Low-Dropout Regulators With Programmable Output Voltages:
  - LDO1 for General Purpose Applications
  - LDO2 for Low-Noise Analog Applications
- Green and Red LED-Charger Status Drivers
- 4-Channel 8-Bit Dual Slope Analog-to-Digital (ADC) Converter
- 2 High-Efficiency DVS Buck Converters
- Wide Load Range Buck-Boost DC-DC Converter
- 400-kHz I^2C-Compatible Interface
- Linear Constant-Current and Constant-Voltage Charger for Single-Cell Lithium-Ion Batteries
- USB and Adapter Charging
- System Power Supply Management
- Voltage and Thermal Supervisory Circuits
- Continuous Battery Voltage Monitoring
- Interrupt Request Output With 8 Sources
- 50-mΩ Battery Path Resistance
- 100-mA to 1000-mA Full-Rate Charge Current Using Wall Adapter
- Selectable 0.05C and 0.1C End-of-Charge (EOC) Current
- USB Current Limits of 100, 500, and 800 mA
- USB Pre-Qualification Current of 50 mA
- Selectable 4.1-V, 4.2-V or 4.38-V Battery-Termination Voltages
- 0.35% Battery-Termination Accuracy
- ±1 LSB INL/DNL on 8-Bit ADC

2 Applications

- Hard Drive-Based Media Players
- Portable Gaming Players
- Portable Navigation Devices

3 Description

The LP3910 is a programmable system power management unit optimized for HDD-based portable media players. The device incorporates two low-dropout LDO voltage regulators, two integrated buck DC-DC converters with dynamic voltage scaling (DVS), one wide load-range buck-boost DC-DC converter with programmable output voltage, a 4-channel, 8-bit ADC, and a dual-source lithium-ion or lithium-polymer battery charger.

The LP3910 also incorporates some advanced battery management functions such as battery temperature measurement, reverse current blocking for USB, LED-charger status indication, thermally regulated internal power FETs, battery-voltage monitoring, overcurrent protection, and a 10-hour safety timer. The device is programmable through a 400-kHz I2C-compatible interface.

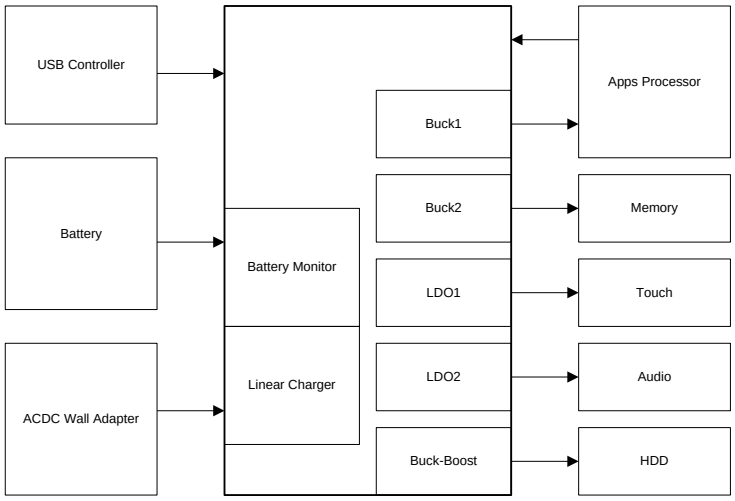
The LP3910 is available in a thermally-enhanced 6-mm × 6-mm × 0.8-mm 48-pin WQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3910	WQFN (48)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (March 2013) to Revision M — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

Changes from Revision K (February 2012) to Revision L — **Page**

- Changed layout of National Data Sheet to TI format ... 68

5 Device Comparison Tables

Table 1. Device Default Voltage Options

ORDER NUMBER	LDO1	LDO2	BUCK1	BUCK2	BUCK-BOOST	I_{CHRG}
LP3910SQ-AA	2 V	3.3 V	1.2 V	3.3 V	3.3 V	100 mA
LP3910SQX-AA	2 V	3.3 V	1.2 V	3.3 V	3.3 V	100 mA
LP3910SQ-AK	2.5 V	3 V	1.6 V	1.8 V	3.3 V	100 mA
LP3910SQX-AK	2.5 V	3 V	1.6 V	1.8 V	3.3 V	100 mA
LP3910SQ-AM	3.3 V	3.3 V	1.5 V	1.8 V	3.3 V	100 mA
LP3910SQX-AM	3.3 V	3.3 V	1.5 V	1.8 V	3.3 V	100 mA
LP3910SQ-AN	1.2 V	2.5 V	1 V	1.8 V	3.3 V	1000 mA
LP3910SQX-AN	1.2 V	2.5 V	1 V	1.8 V	3.3 V	1000 mA

Table 2. Device Option Parameters for AP Option

SYMBOL	DESCRIPTION	VALUE
LDO1	Default LDO1	2.8 V
LDO2	Default LDO2	1.5 V
Buck1	Default Buck1	1.45 V
Buck2	Default Buck2	1.8 V
Buck-Boost	Default Buck-Boost	3.3 V
I_{CHRG}	Default charge current	100 mA
T1	Turnon delay for LDO1 and LDO2	6 ms
T2	Turnon delay for Buck1	3 ms
T3	Turnon delay for Buck2	1 ms
T4	Turnon delay for Buck-Boost	0 ms
T5	Turnon delay for NRST	10 ms
T1	Turnoff delay for LDO1 and LDO2	10 ms
T2	Turnoff delay for Buck1	10 ms
T3	Turnoff delay for Buck2	10 ms
T4	Turnoff delay for Buck-Boost	10 ms
T5	Turnoff delay for NRST	3 ms
$V_{BATTLOW}$	battery low threshold	2.5 V
$V_{FULLRATE}$	Full-rate threshold	2.55 V
I_{LED}	Default LED current	2 V

The following options are programmed for the LP3910. The system designer that needs specific options is advised to contact the local Texas Instruments sales office.

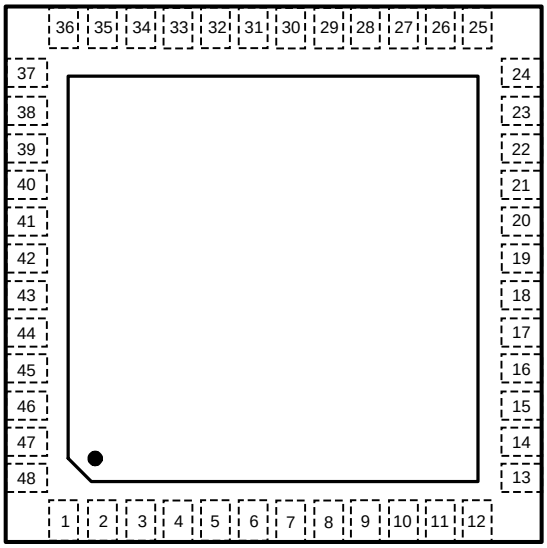
Table 3. Factory Programmable Options

FACTORY PROGRAMMABLE OPTIONS	DEFAULT VALUE (AA)
LDO1 output voltage after power up	2 V
LDO2 output voltage after power up	3.3 V
BUCK1 output voltage after power up	1.2 V
BUCK2 output voltage after power up	3.3 V
BUCK-BOOST power voltage after power up	3.3 V
Battery low threshold	2.9 V
Delay for LDO1 and LDO2	5 ms
Delay for BUCK1	15 ms
Delay for BUCK2	20 ms
Delay for BUCK-BOOST	25 ms
Delay for NRST	60 ms
Default full-rate charge current	100 mA
EOC default	0.1C
V_{TERM} default	4.2 V
ONOFF edge/level	Level
ONOFF polarity	Positive
BUCK1 enable polarity	Positive
LDO2 enable polarity	Positive
Ignore ten-hour timer	No
LED default current	10 mA
Buck-boost 500-mA output current	No
Thermistor 10 k/100 k	100 k

The I^2C Chip ID address is offered as a metal mask option. The current value equals 60 hex.

6 Pin Configuration and Functions

NJV Package
48-Pin WQFN
Top View



Pin Functions

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	TS	I	A	Battery temperature sense pin. This pin is normally connected to the thermistor pin of the battery cell.
2	VBATT1	O	A	Positive battery terminal. This pin must be externally shorted to VBATT2 and VBATT3
3	AGND	—	G	Analog ground
4	VREFH	O	A	Connection to bypass capacitor for internal high reference
5	LDO2EN	I	D	Digital input to enable/disable LDO2
6	VLDO2	O	A	LDO2 output
7	VIN1	I	PWR	Power input to LDO1 and LDO2. VIN1 pin must be externally shorted to the VDD pins.
8	VLDO1	O	A	LDO1 output
9	POWERACK	I	D	Digital power acknowledgement input (see *Power-On, Power-Off Sequencing*)
10	ISENSE	I	A	A 4.64-kΩ resistor must be connected between this pin and GND. A fraction of the charge current flows through this resistor to enable the ADC to measure the charge current.
11	ADC2	I	A	Channel 2 input to ADC
12	ADC1	I	A	Channel 1 input to ADC
13	IRQB	O	Open Drain	Open drain active low interrupt request
14	NRST	O	Open Drain	Open drain active low reset during standby
15	CHG	O	D	This output indicates that a valid charger supply source (USB adapter) has been detected, and the device is charging. (Red LED)
16	STAT	O	D	Battery Status output indicator - off during constant current (CC), 50% duty cycle during constant voltage (CV), 100% duty cycle with a fully charged Li-ion battery (Green LED)
17	BUCK1EN	I	D	Digital input to enable/disable BUCK1
18	VFB1	I	A	Buck1 Feedback input terminal
19	BCKGND1	—	G	Buck1 Ground
20	VBUCK1	O	A	Buck1 Output

(1) A: Analog; D: Digital: G: Ground; PWR: Power

Pin Functions (continued)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
21	VIN2	I	PWR	Power input to Buck1. VIN2 pin must be externally shorted to the VDD pins.
22	VIN3	I	PWR	Power input to Buck2. VIN3 pin must be externally shorted to the VDD pins.
23	VBUCK2	O	A	Buck2 Output
24	BCKGND2	—	G	Buck2 Ground
25	VFB2	I	A	Buck2 Feedback input terminal
26	ONOFF	I	D	Power ONOFF pin configured either as level (High or Low) triggered or edge (High or Low) triggered.
27	I^2C_SCL	I	D	I^2C-compatible interface clock terminal
28	VDDIO	I	D	Supply to input / output stages of digital I/O
29	I^2C_SDA	I/O	D	I^2C-compatible interface data terminal
30	ONSTAT	O	Open Drain	Open Drain output that reflects the debounced state of ONOFF pin.
31	VBBFB	I	A	Buck-Boost Feedback input terminal
32	VBBOUT	O	A	Buck-Boost Output voltage
33	VBBL2	I	A	Buck-Boost inductor
34	BBGND1	—	G	Buck-Boost high current ground
35	VBBL1	I	A	Buck-Boost inductor
36	VIN4	I	PWR	Power input to Buck-Boost. VIN4 pin must be externally shorted to the VDD pins.
37	USBSUSP	I	D	This pin must be pulled high during USB suspend mode.
38	USBISEL	I	D	Pulling this pin low limits the USB charge current to 100 mA. Pulling this pin high limits the USB charge current to 500 mA.
39	BBGND2	—	G	BUCK-BOOST Core Ground
40	DGND	—	G	Digital ground
41	VDD3	I	PWR	Power input to supply application. This pin must be externally shorted to VDD1 and VDD2.
42	VDD2	I	PWR	Power input to supply application This pin must be externally shorted to VDD1 and VDD3.
43	VBATT3	O	A	Positive battery terminal. This pin must be externally shorted to V\BATT1 and VBATT2.
44	VBATT2	O	A	Positive battery terminal. This pin must be externally shorted to VBATT1 and VBATT3.
45	USBPWR	I	PWR	USB power input pin
46	VDD1	I	PWR	Power input to supply application This pin is shorted to VDD2 and VDD3.
47	CHG_DET	I	A	Wall adapter power input pin
48	IREF	I	A	A 121-kΩ resistor must be connected between this pin and AGND. The resistor value determines the reference current for the internal bias generator.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply voltage	CHG_DET	–0.3	6.5	V
Battery voltage	VBATT1, 2, 3	–0.3	5	V
Voltage	USBPWR, VIN1,VIN2,VIN3,VIN4, VDD1,VDD2,VDD3	–0.3	6.2	V
	All other pins	–0.3	V_{DD} + 0.3	V
Power dissipation (T_A = 70°C)(4)			2.6	W
Storage temperature, T_{stg}		–45	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typical) and disengages at T_J = 140°C (typical).

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	NOM	MAX	UNIT
CHG_DET	4.5		6	V
USBPWR	4.35		6	V
VBATT1, 2, 3	0		4.5	V
VIN1, VIN2, VIN3, VIN4, VDD1, VDD2, VDD3	2.5		6	V
VDDIO	2.5		V_{DD}	V
Junction temperature, T_J	–40		125	°C
Ambient temperature, T_A	–40		85	°C
Power dissipation, T_{J-MAX} and T_{A-MAX}		1.6		W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) Minimum and maximum limits are specified by design, test, or statistical analysis. Nominal numbers are not ensured, but do represent the most likely norm.
(3) Nominal values and limits are for T_J = 25°C.

7.4 Thermal Information

THERMAL METRIC(1)		LP3910 NJV (WQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

Unless otherwise noted, V_{DD} = 5 V, V_{BATT} = 3.6 V, and limits apply for T_J = 25°C. (1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_BATT}	Battery standby supply current	All circuits off except for POR and battery monitor. No adapter or USB power connected.		6	20	µA
I_{Q_BATT}	Battery standby supply current	All circuits off except for POR and battery monitor. No adapter or USB power connected. T_J = 0°C to 125°C			20	µA
V_{POR}	Power-on reset threshold	V_{DD} falling edge		1.9		V
T_{SD}	Thermal shutdown threshold			160		°C
T_{SDH}	Thermal shutdown hysteresis			20		°C
$T_{TH\text{-}ALERT}$	Thermal interrupt threshold			115		°C
VDDIO	IO supply		2.5		V_{DD}	V
F_{CLK}	Internal system clock frequency			2		MHz

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) Low ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(4) This specification is ensured by design. Not tested during production.

7.6 Electrical Characteristics: I²C Interface

Unless otherwise noted, VDDIO = 3.6 V, and minimum and maximum limits apply for T_J = 0°C to 125°C. (1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low level input voltage	I^2C_SDA & I^2C_SCL			0.3 × VDDIO	V
V_{IH}	High level input voltage	I^2C_SDA & I^2C_SCL	0.7 × VDDIO			V
V_{OL}	Low level output voltage	I^2C_SDA & I^2C_SCL	0		0.2 × VDDIO	V
V_{HYS}	Schmitt trigger input hysterisis	I^2C_SDA & I^2C_SCL	0.1 × VDDIO			V

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are specified by design, test, or statistical analysis.
(3) Low ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(4) This specification is ensured by design.

7.7 Electrical Characteristics: Li-Ion Battery Charger

Unless otherwise noted, V_{DD} = 5 V, V_{BATT} = 3.6 V, C_{BATT} = 4.7 µF, C_{CHG_DET} = 10 µF, R_{IREF} = 121 kΩ. Typical limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{USB}	Minimum external USB supply voltage	T_J = 25°C USB current limit = 500 mA	4.15	4.25	4.35	V
V_{USB_HYST}	USBPWR detect hysteresis			110		mV
CHG_DET	Minimum external adapter supply voltage range	T_J = 25°C Adapter current limit = 1 A V_{FWD} Schottky = 350 mV	4.4	4.5	4.6	V
V_{CHG_HYST}	CHG_DET input hysteresis			150		mV
I_{USB_SUSP}	Quiescent current in USB suspend mode	USB suspend mode, V_{USB} = 5 V USBSUSP = USBPWR USBISEL = 0 V		30	60	µA
V_{TERM_TOL}	Battery charge termination voltage tolerance (selected in *CHCTL Register (01)H Charger Control Register*)	T_J = 25°C I_{PROG} = 500 mA, I_{CHG} = 50 mA	–0.35% −0.5% −0.5%	4.2 4.1 4.38	0.35% 0.5% 0.5%	V
		T_J = 0°C to 125°C I_{PROG} = 500 mA, I_{CHG} = 50 mA	–1% –1.5% –1.5%	4.2 4.1 4.38	1% 1.5% 1.5%	V
I_{CHG_WA}	Full-rate charging current from wall adapter input (see *Full-Rate Charging Mode*)	CHG_DET = 5.25 V V_{BATT} = 3.6 V, I_{PROG} = 500 mA	450	500	550	mA
I_{CHG_USB}	Full-rate charging current from usbpwr input (see *Full-Rate Charging Mode*)	USB = 5 V, V_{BATT} = 3.6 V I_{PROG} = 500 mA, USB_ISEL = 800 mA	450	500	550	mA
		USB = 5 V, V_{BATT} = 3.6 V I_{PROG} = 500 mA, USB_ISEL = 500 mA	405	450	495	mA
USB I_{LIMIT}	USB charge-current limit	USB_ISEL = 100 mA	90	95	100	mA
		USB_ISEL = 500 mA	450	475	500	
		USB_ISEL = 800 mA	720	760	800	
$I_{PREQUAL}$	Pre-qualification current	V_{BATT} = 2.5 V, wall-adapter charge current Percentage of programmed full-rate current	8%	10%	12%	
		V_{BATT} = 2.5 V, USB charge current	40	50	60	mA
V_{FULL_RATE}	Full-rate qualification threshold	V_{BATT} rising, transition from pre-qualification to full-rate charging (standard)	2.75	2.85	2.95	V
		V_{BATT} rising, transition from pre-qualification to full-rate charging (AP version only)	2.45	2.55	2.65	
V_{TH_H}	Upper T_S comparator limit		2.82	2.87	2.93	V
V_{TH_L}	Lower T_S comparator limit	45°C CHSPV Reg D3 = 0	0.315	0.33	0.345	V
		50°C CHSPV Reg D3 = 1	0.255	0.27	0.285	
I_{TSENSE}	Battery temperature sense current		7.75	8	8.25	µA
T_{REG}	Regulated charger junction temperature	T_J = 25°C	105	115	125	°C

(1) All voltages are with respect to the potential at the GND pin.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(3) Minimum and maximum limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(4) Low ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

7.8 Detection and Timing

Typical limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EOC}	End-of-charge current	I_{PROG} = 500 mA 10% EOC setting	40	50	60	mA
		I_{PROG} = 500 mA 5% EOC setting	20	25	30	mA
$V_{RESTART}$	Battery restart charging voltage	V_{TERM} = 4.1 V	3.82	3.9	3.94	V
		V_{TERM} = 4.2 V	3.94	4	4.06	
		V_{TERM} = 4.38 V	4.14	4.2	4.26	

7.9 Output Electrical Characteristics: CHG, STAT

Unless otherwise noted, V_{DD} = 5 V, V_{BATT} = 3.6 V. C_{BATT} = 4.7 µF, C_{CHG_DET} = 10 µF. Typical limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LED}	Output high level	V_{LED} = 2 V CHSPV Register (02)h bit 5 = 1 (standard)	4	5	6	mA
		V_{LED} = 2 V CHSPV Register (02)h bit 5 = 1 (AP version only)	0.75	1	1.25	
I_{LED}	Output high level	V_{LED} = 2 V CHSPV Register (02)h bit 5 = 0 (standard)	8	10	12	mA
		V_{LED} = 2 V CHSPV Register (02)h bit 5 = 0 (AP version only)	1.6	2	2.4	
$I_{LEAKAGE}$	Leakage current	V_{LED} = 1.5 V, LED off		0.1	5	µA
LED_{FREQ}	Blinking frequency		0.8	1	1.2	Hz

(1) All voltages are with respect to the potential at the GND pin.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(3) Minimum and maximum limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(4) Low ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

7.10 Output Electrical Characteristics: NRST, IRQB, ONSTAT

Unless otherwise noted, V_{DD} = 5 V, V_{BATT} = 3.6 V, C_{BATT} = 4.7 µF, C_{CHG_DET} = 10 µF. Minimum and maximum limits apply over the entire junction temperature range for operation, T_J = 0°C to 125°C.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low level	I_{OL} = 4 mA			0.4	V
$I_{LEAKAGE}$	Leakage current	V_{DD} = 2.5 V, output logic high	–1		1	µA

(1) All voltages are with respect to the potential at the GND pin.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(3) Minimum and maximum limits are specified by design, test, or statistical analysis.
(4) Low ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

7.11 Input Electrical Characteristics: USBSUSP, USBISEL

Unless otherwise noted, V_{USB} = 5 V, V_{BATT} = 3.6 V, C_{BATT} = 4.7 µF, C_{CHG_DET} = 10 µF. Minimum and maximum limits apply over the entire junction temperature range for operation, T_J = 0°C to 125°C.(1)(2)(3)(4)(5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low level				0.3 × V_{USB}	V
V_{IH}	Input high level		0.7 × V_{USB}			V
$I_{LEAKAGE}$	Input leakage		−1		1	µA

(1) LDO2EN, BUCK1EN, and USBSUSP have weak internal pulldowns while pins POWERACK, ONOFF do not have weak pulldowns.
(2) All voltages are with respect to the potential at the GND pin.
(3) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(4) Minimum and maximum limits are specified by design, test, or statistical analysis.
(5) Low ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

7.12 Input Electrical Characteristics: POWERACK, ONOFF, LDO2EN, BUCK1EN

Unless otherwise noted, V_{DD} = 5 V, V_{BATT} = 3.6 V, C_{BATT} = 4.7 µF, C_{CHG_IN} = 10 µF. Minimum and maximum limits apply over the entire junction temperature range for operation, T_J = 0°C to 125°C.(1)(2)(3)(4)(5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.4			V
$I_{LEAKAGE}$	Input leakage		–1		1	µA

(1) LDO2EN, BUCK1EN, and USBSUSP have weak internal pulldowns, while pins POWERACK, ONOFF do not have this.
(2) All voltages are with respect to the potential at the GND pin.
(3) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(4) Minimum and maximum limits are specified by design, test, or statistical analysis.
(5) Low ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

7.13 Electrical Characteristics: LDO1 Low Dropout Linear Regulators

Unless otherwise noted, VIN1 = 3.6 V, I_{MAX} = 150 mA, V_{OUT} = default value, C_{VDD} = 10 µF, C_{LDO1} = 1 µF, ESR = 5 mΩ – 500 mΩ, C_{VREFH} = 100 nF. Typical limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN1	Operational voltage		2.5		6	V
V_{OUT} Range	Output voltage programming range	T_J = 25°C 1.2 V to 3.3 V in 100-mV steps	1.2		3.3	V
V_{OUT} Accuracy	Output voltage accuracy	1 mA ≤ I_{OUT} ≤ I_{MAX} over full line and load regulation. V_{OUT} = default value	–3%		3%	
ΔV_{OUT}	Line regulation	V_{IN} = (V_{OUT} + 500 mV) to 5.5 V Load current = I_{MAX}		3		mV
	Load regulation	V_{IN} = 3.6 V, Load current = 1 mA to I_{MAX}		10		mV
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V	600	750		mA
$V_{IN} – V_{OUT}$	Dropout voltage	Load current = I_{MAX}		60	150	mV
PSRR	Power supply ripple rejection	F = 10 kHz, load current = I_{MAX}		30		dB
R_{SHUNT}	LDO output impedance	LDO disabled, V_{OUT} = default value			200	Ω

7.14 Electrical Characteristics: LDO2 Low Dropout Linear Regulator

Unless otherwise noted VIN1 = 3.6V, I_{MAX} = 150 mA, V_{OUT} = default value, C_{VDD} = 10 µF, C_{LDO2} = 1 µF, ESR = 5 mΩ to 500 mΩ, C_{VREFH} = 100 nF. Typical limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN2	Operational voltage		2.5		6	V
V_{OUT} range	Output voltage programming range	T_A = 25°C 1.3 V to 3.3 V in 100-mV steps	1.3		3.3	V
V_{OUT} accuracy	Output voltage accuracy (default V_{OUT})	1 mA ≤ I_{OUT} ≤ I_{MAX} over full line and load regulation	–3%		3%	
ΔV_{OUT}	Line regulation	V_{IN} = (V_{OUT} + 500 mV) to 5.5 V, Load current = I_{MAX}		3		mV
	Load regulation	V_{IN} = 3.6 V, Load current = 1 mA to I_{MAX}		10		mV
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V	600	750		mA
$V_{IN} – V_{OUT}$	Dropout voltage	Load current = I_{MAX}		60	150	mV
PSRR	Power supply ripple rejection	F = 1 kHz, load current = I_{MAX}		50		dB
		F = 10 kHz, load current = I_{MAX}		35		
e_N	Analog supply output noise voltage	10 Hz < F < 100 kHz		50		μV_{RMS}
R_{SHUNT}	LDO output impedance	LDO disabled, V_{OUT} = default value			200	Ω

7.15 Electrical Characteristics: Buck1 Converter

Unless otherwise noted, VIN2 = 3.6 V, V_{OUT} = default value, C_{VIN2} = 10 µF, C_{SW1} = 10 µF, L_{SW1} = 2.2 µH. Typical limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified. Modulation mode is PWM mode with automatic switch to PFM at light loads.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN2	Input voltage		2.7		6	V
V_{OUT} range	Output voltage programming range	T_J = 25°C 0.8 V to 2 V in 50-mV Steps	0.8		2	V
ΔV_{OUT}	Static output voltage tolerance	I_{OUT} = 200 mA including line and load regulation	–3%		3%	
	Line regulation	I_{OUT} = 10 mA V_{IN2} = 2.5 V − V_{DD}		0.2		%/V
	Load regulation	100 mA < I_{OUT} < 300 mA		0.002		%/mA
I_{OUT}	Continuous output current		600			mA
	Peak output current limit		850	1000	1150	mA
I_{PFM}	Maximum I_{LOAD}, PFM mode			75		mA
I_Q	Quiescent current	I_{OUT} = 0 mA		30	90	µA
		BUCK1 disabled			1	
F_{OSC}	Internal oscillator frequency	PWM mode		2		MHz
η	Peak efficiency			90%		
T_{ON}	Turnon time	To 95% level(1)			1	ms

(1) This specification is ensured by design.

7.16 Electrical Characteristics: Buck2 Converter

Unless otherwise noted, VIN3 = 3.6 V, V_{OUT} = default value, C_{VIN3} = 10 µF, C_{SW1} = 10 µF, L_{SW2} = 2.2 µH. Typical limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified. Modulation mode is PWM mode with automatic switch to PFM at light loads.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN3	Input voltage		2.7		6	V
V_{OUT} Range	Output voltage programming range	1.8 V – 3.3 V in 100-mV steps	0.8		2	V
ΔV_{OUT}	Static output voltage tolerance	I_{OUT} = 200 mA including line and load regulation	–3%		3%	
	Line regulation	I_{OUT} = 10 mA V_{IN3} = 2.5 V − V_{DD}		0.2		%/V
	Load regulation	100 mA < I_{OUT} < 300 mA		0.002		%/mA
I_{OUT}	Continuous output current		600			mA
	Peak output current limit		850	1000	1150	mA
I_{PFM}	Maximum I_{LOAD}, PFM mode			75		mA
I_Q	Quiescent current	I_{OUT} = 0 mA		30	90	µA
		Buck2 disabled			1	
F_{OSC}	Internal oscillator frequency	PWM mode		2		MHz
η	Peak efficiency			90%		
T_{ON}	Turnon time	To 95% level(1)			1	ms

(1) This specification is ensured by design..

7.17 Electrical Characteristics: Buck-Boost

Unless otherwise noted, VIN4 = 3.6 V, C_{VIN4} = 10 µF, C_{BB} = 22 µF, L_{BB} = 2.2 µH. Typical limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified. Modulation mode is PWM mode with automatic switch to PFM at light loads.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN4	Input voltage	I_{OUTMAX} = 1000 mA	2.9		5.7	V
		I_{OUTMAX} = 800 mA	2.7		5.7	V
V_{OUT} Range	Output voltage programming range	T_J = 25°C 1.80 V to 3.30 V in 50-mV steps	1.8		3.3	V
ΔV_{OUT}	Static output voltage tolerance	I_{OUT} = 0 mA to 1000 mA including line and load regulation	–4%		4%	
	Line regulation	I_{OUT} = 10 mA		0.2		%/V
	Load regulation	100 mA < I_{OUT} < 1000 mA		0.0016		%/mA
I_{OUT}	Continuous output current		1000			mA
	Peak inductor current limit	V_{OUT} = 3.3 V 1-A load at V_{IN} = 2.7 V	1800		2400	mA
I_{PFM}	Maximum I_{LOAD}, PFM mode			75		mA
I_Q	Quiescent current	I_{OUT} = 0 mA PFM no switching		80		µA
		Buck-Boost disabled			1	
F_{OSC}	Internal oscillator frequency	PWM mode		2		MHz
η	Peak efficiency			93%		
T_{ON}	Turnon time	To 95% level(1)			1	ms

(1) This specification is ensured by design.

7.18 Electrical Characteristics: ADC

All limits apply for T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	T_J = 25°C	1.22	1.225	1.23	V
		T_J = 0°C to 125°C	1.2	1.225	1.23	V
INL	Core ADC integral non-linearity	V_{REF} = 1.225 (1)	–1		1	LSB
DNL	Core ADC differential non-linearity	V_{REF} = 1.225 (1)	–0.5		0.5	LSB
V_{GP_IN}	General purpose ADC input voltage range		V_{REF}		2 × V_{REF}	V
V_{BATT}, RANGE 0	Battery maximum voltage scalar output	VBATT = 3.5 V	2.435	2.45	2.465	V
	Battery minimum voltage scalar output	VBATT = 2.6 V	1.217	1.225	1.232	V
V_{BATT}, RANGE 1	Battery maximum voltage scalar output	VBATT = 4.4 V	2.435	2.45	2.465	V
	Battery minimum voltage scalar output	V_{REF} = 2.6 V	1.217	1.225	1.232	V
V_{ISENSE} , RANGE 0	ISENSE maximum voltage scalar output	V_{ISENSE} = 0.6463 V I_{CHG} = 0.605 A, R_{SENSE} = 4.64 kΩ	2.373	2.45	2.519	V
	ISENSE minimum voltage scalar output	V_{ISENSE} = 0 V I_{CHG} = 0 A, R_{SENSE} = 4.64 kΩ	1.186	1.225	1.260	V
V_{ISENSE}, RANGE 1	ISENSE maximum voltage scalar output	V_{ISENSE} = 1.175 V I_{CHG} = 1.1 A, R_{SENSE} = 4.64 kΩ	2.373	2.45	2.519	V
	ISENSE minimum voltage scalar output	V_{ISENSE} = 0 V I_{CHG} = 0 A, R_{SENSE} = 4.64 kΩ	1.186	1.225	1.26	V
ADC1 and $ADC2_{MIN}$	ADC1 and ADC2 minimum voltage scalar output	V_{REFH} = 1.225 V	1.218	1.225	1.23	V
ADC1 and $ADC2_{MAX}$	ADC1 and ADC2 maximum voltage scalar output	V_{REFH} = 1.225 V	2.436	2.45	2.46	V
t_{CONV}	Conversion time (1)				5	ms
t_{WARM}	Warm-up time			2		ms

(1) This specification is ensured by design.

7.19 I^2C Timing Requirements

Unless otherwise noted, VDDIO = 3.6 V and minimum and maximum limits apply for T_J = 0°C to 125°C. (1)

		MIN	NOM	MAX	UNIT
F_{CLK}	Clock frequency			400	kHz
t_{BF}	Bus-free time between START and STOP	1.3			µs
t_{HOLD}	Hold time repeated START condition	0.6			µs
t_{CLK-LP}	CLK low period	1.3			µs
t_{CLK-HP}	CLK high period	0.6			µs
t_{SU}	Set-up time repeated START condition	0.6			µs
$t_{DATA-HOLD}$	Data hold time	0			µs
$t_{DATA-SU}$	Data set-up time	100			ns
t_{SU}	Set-up time for STOP condition	0.6			µs
t_{TRANS}	Maximum pulse width of spikes that must be suppressed by the input filter of both data and CLK signals T_J = 25°C	50			µs

(1) These specifications are ensured by design.

7.20 USB Timing Requirements

Nominal limits apply for T_J = 25°C; minimum and maximum limits apply for T_J = 0°C to 125°C, unless otherwise specified.

		MIN	NOM	MAX	UNIT
T_{CHG_IN}	Deglitch adapter insertion	28	32	36	ms
T_{USB}	Deglitch USB power insertion	28	32	36	ms
T_{PQ_FULL}	Deglitch time for pre-qualification to full-rate charge transition	8	10	12	ms
T_{FULL_PQ}	Deglitch time for full-rate to pre-qualification transition	8	10	12	ms
$T_{BATTLOWF}$	Deglitch time for V_{BATT} falling below $V_{BATTLOW}$ threshold	4	5	6	ms
$T_{BATTLOWR}$	Deglitch time for V_{BATT} rising above $V_{BATTLOW}$ threshold	4	5	6	ms
$T_{BATTEMP}$	Deglitch time for recovery from battery temperature fault	8	10	12	ms
T_{ONOFF_F}	Deglitching on falling edge of ONOFF pin	28	32	36	ms
T_{ONOFF_R}	Deglitching on rising edge of ONOFF pin	28	32	36	ms
$T_{RESTART}$	Deglitching on falling V_{BATT} crossing $V_{RESTART}$	8	10	12	ms
T_{CCCV}	Deglitching of CC→CV charging transition	8	10	12	ms
T_{CVEOC}	Deglitching of CV→EOC (End of Charge)	8	10	12	ms
$T_{POWERACK}$	Deglitching of POWERACK pin	4	5	6	ms
T_{TSHD}	Deglitching of thermal shutdown		2		ms
T_{TOPOFF}	Topoff timer	17	21	25	min
T_{10HR}	10-hour safety timer	9	10	11	hours
T_{1HR}	1-hour prequalification safety timer	0.9	1	1.1	hour

7.21 Typical Characteristics

T_A = 25°C unless otherwise noted

7.21.1 Battery-Charger Characteristics

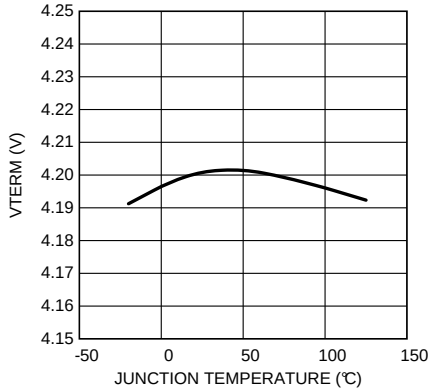


Figure 1. V_{TERM} 4.2 V vs Temperature

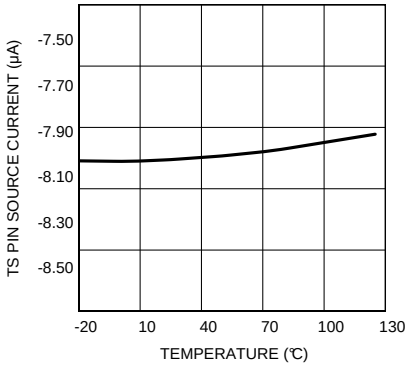


Figure 2. TS Pin Current vs Temperature

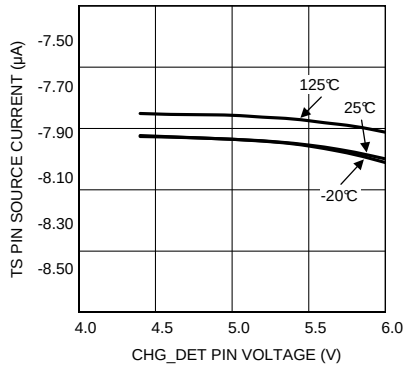
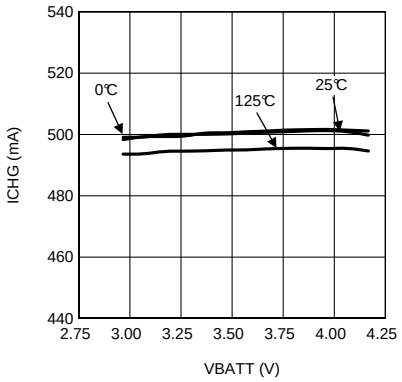
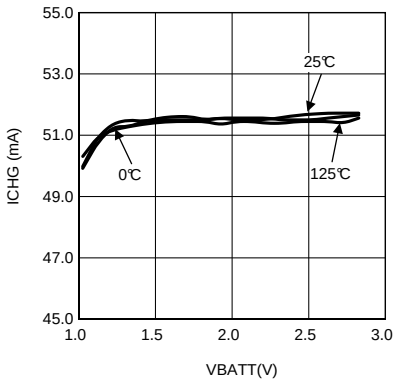


Figure 3. TS Pin Current vs CHG_DET



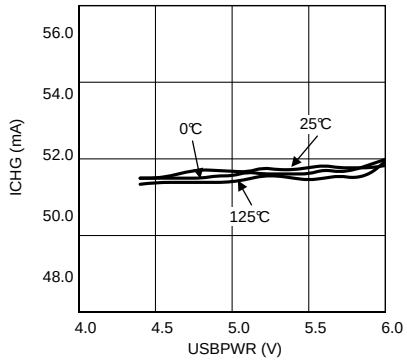
CHG_DET = 5 V CC

Figure 4. CHG vs VBATT



Prequal I_{PROG} = 500 mA CHG_DET = 5 V

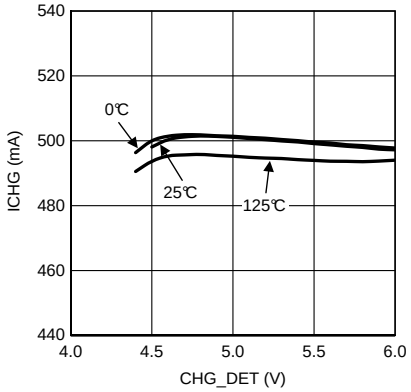
Figure 5. IU vs VBATT



V_{BATT} = 2.5 V Prequal

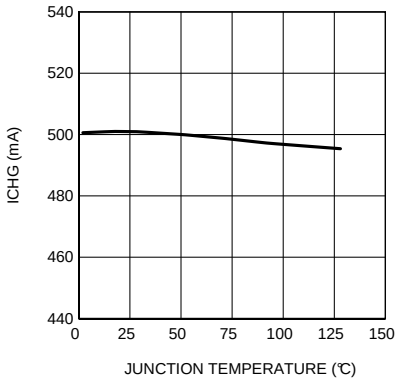
Figure 6. ICHG vs USBPWR

Battery-Charger Characteristics (continued)



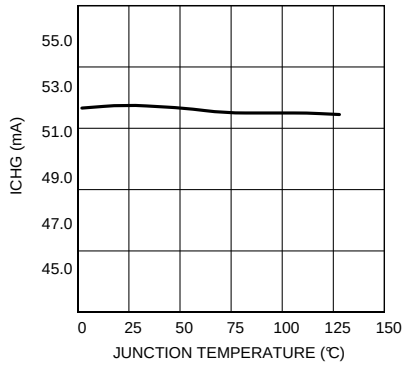
V_{BATT} = 3.5 V, CC

Figure 7. ICHG vs CHG_DET



V_{BATT} = 3.75 V, CC CHG_DET = 5 V

Figure 8. ICHG vs Temperature



V_{BATT} = 3.75 V, Prequal CHG_DET = 5 V

Figure 9. ICHG vs Temperature

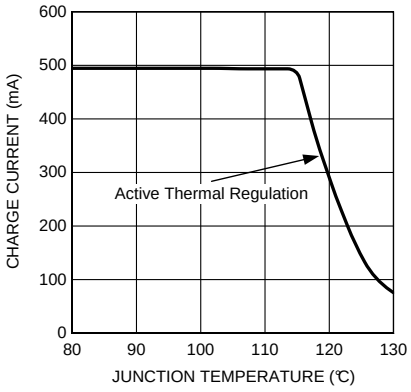


Figure 10. Thermal Regulation of Charge Current

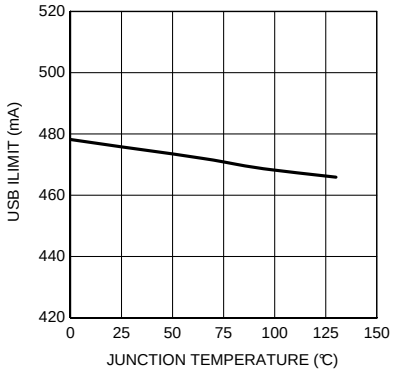
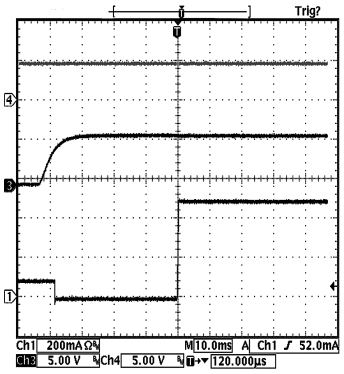


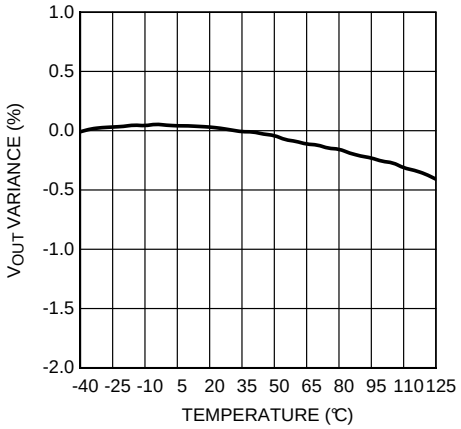
Figure 11. USB I_{LIMIT} vs Temperature



Ch1 = Charge Current (mA) Ch4 = USBPWR (V)
Ch3 = CHG_DET (V)

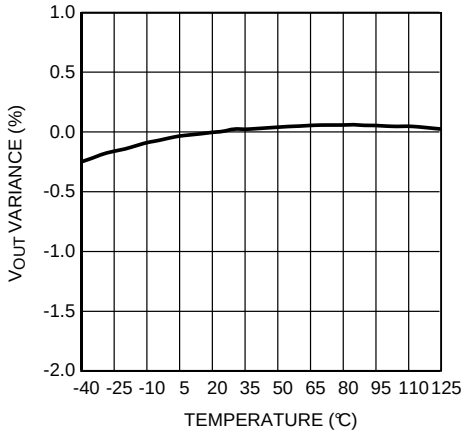
Figure 12. Wall Adapter Insertion With USBPWR Present

7.21.2 LDO Characteristics



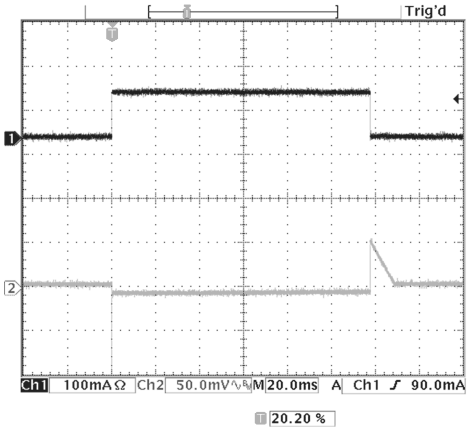
V_{IN} = 4.3 V V_{OUT} = 3.3 V Load = 100 mA

Figure 13. Output Voltage Change vs Temperature (LDO1)



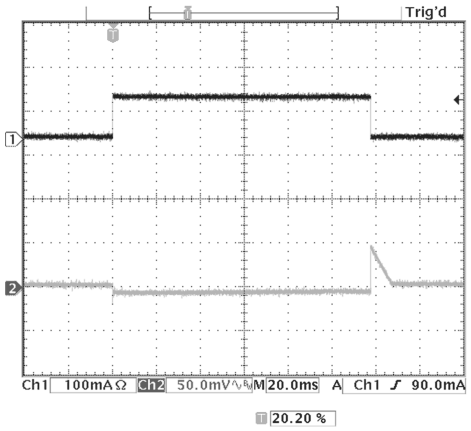
V_{IN} = 4.3 V V_{OUT} = 1.8 V Load = 100 mA

Figure 14. Output Voltage Change vs Temperature (LDO2)



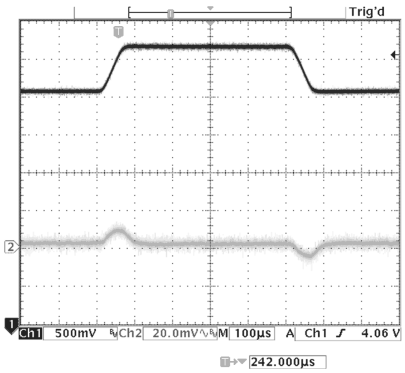
V_{IN} = 3.6 V V_{OUT} = 3.3 V Load = 0 to 100 mA

Figure 15. Load Transient (LDO1)



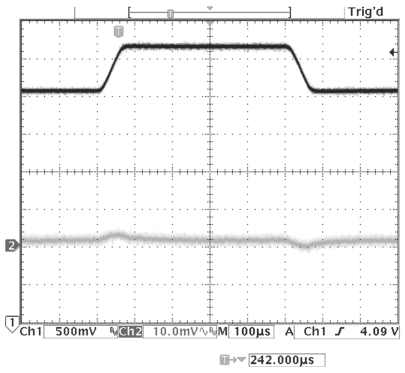
V_{IN} = 3.6 V V_{OUT} = 1.8 V Load = 0 to 100 mA

Figure 16. Load Transient (LDO2)



V_{IN} = 3.6 to 4.5 V V_{OUT} = 3.3 V Load = 150 mA

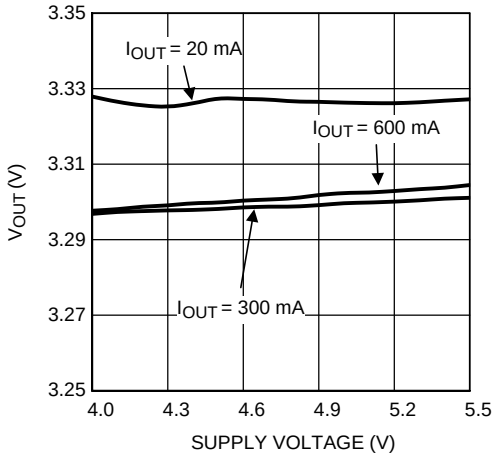
Figure 17. Line Transient (LDO1)



V_{IN} = 3 to 4.2 V V_{OUT} = 1.8 V Load = 150 mA

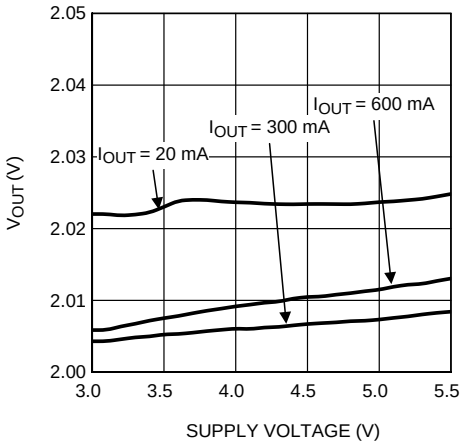
Figure 18. Line Transient (LDO2)

7.21.3 Buck Characteristics



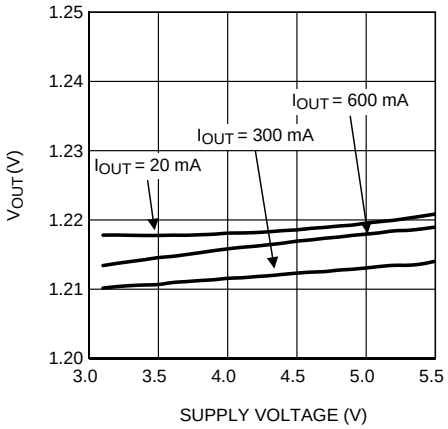
V_{OUT} = 3.3 V

Figure 19. Output Voltage vs Supply Voltage



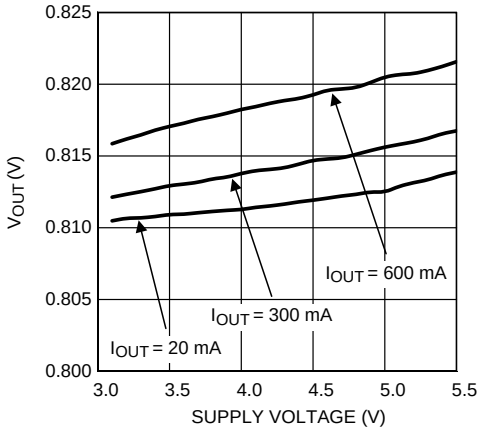
V_{OUT} = 2 V

Figure 20. Output Voltage vs Supply Voltage



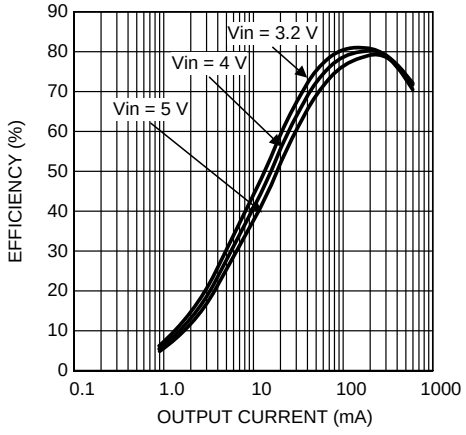
V_{OUT} = 1.2 V

Figure 21. Output Voltage vs Supply Voltage



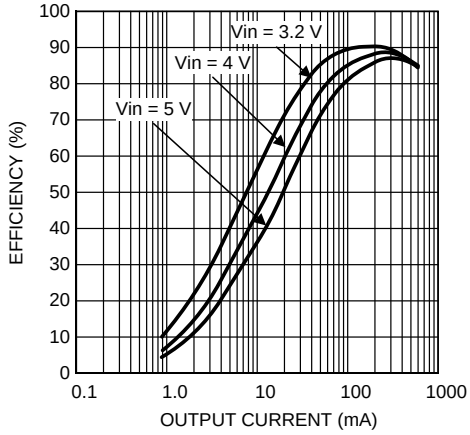
V_{OUT} = 0.8 V

Figure 22. Output Voltage vs Supply Voltage



V_{OUT} = 1.2 V L = 2.2 µH Forced PWM Mode

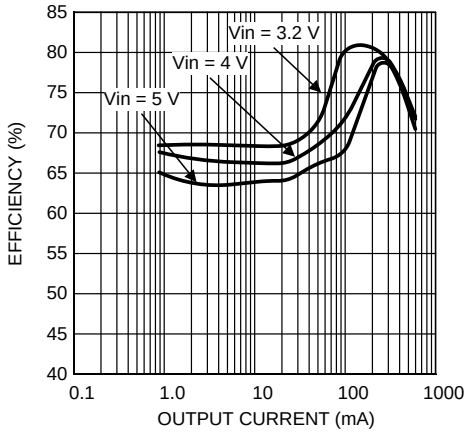
Figure 23. Buck1 Efficiency vs Output Current



V_{OUT} = 2 V L = 2.2 µH Forced PWM Mode

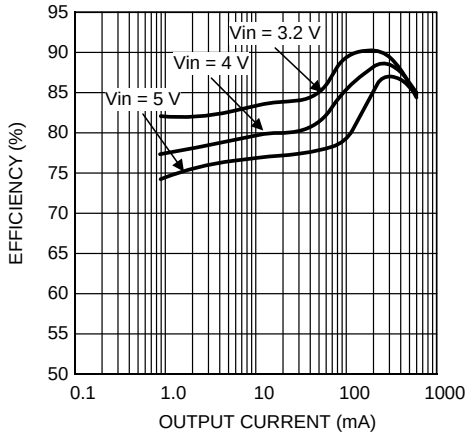
Figure 24. Buck 1 Efficiency vs Output Current

Buck Characteristics (continued)



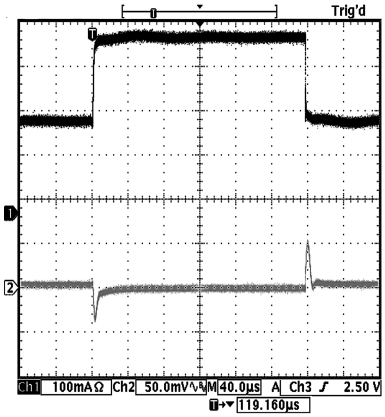
V_{OUT} = 1.2 V L = 2.2 µH PFM-to-PWM Mode

Figure 25. Buck1 Efficiency vs Output Current



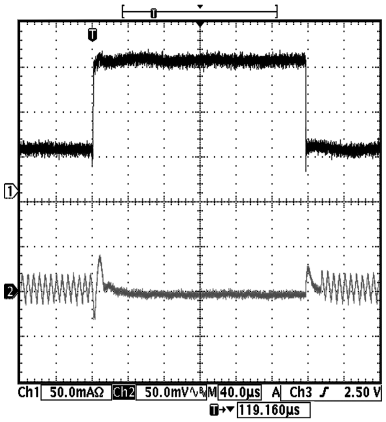
V_{OUT} = 2 V L = 2.2 µH PFM-to-PWM Mode

Figure 26. Buck1 Efficiency vs Output Current



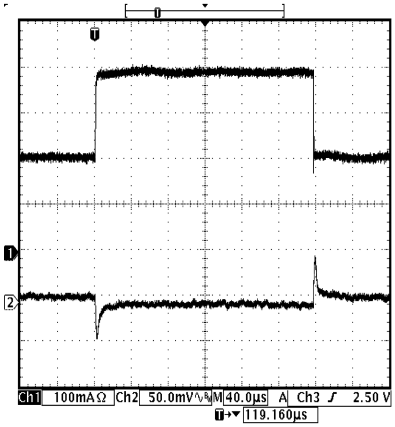
V_{IN} = 4.2 V V_{OUT} = 1.2 V Load = 200 to 400 mA
PWM Mode

Figure 27. Buck1 Load Transient Response



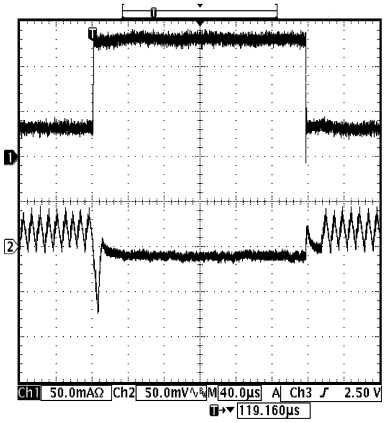
V_{IN} = 4.2 V V_{OUT} = 1.2 V Load = 50 to 150 mA
PFM-to-PWM Mode

Figure 28. Buck1 Load Transient Response



V_{IN} = 4.2 V V_{OUT} = 3.3 V Load = 0 to 400 mA
PWM Mode

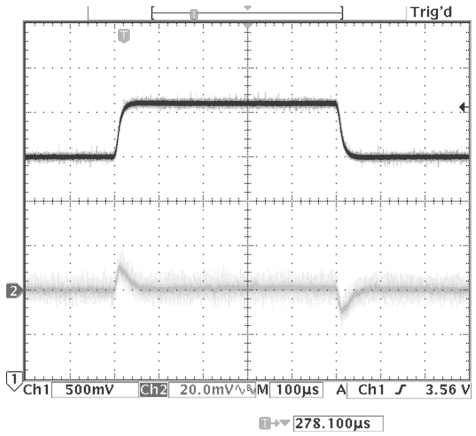
Figure 29. Buck2 Load Transient Response



V_{IN} = 4.2 V V_{OUT} = 3.3 V Load = 50 to 150 mA
PFM-to_PWM Mode

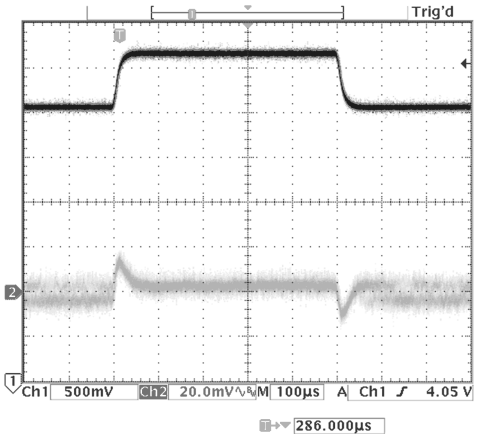
Figure 30. Buck2 Load Transient Response

Buck Characteristics (continued)



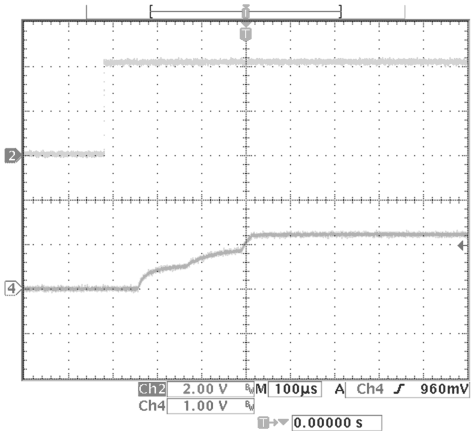
V_{IN} = 3 to 3.6 V V_{OUT} = 1.2 V Load = 250 mA

Figure 31. Line Transient Response



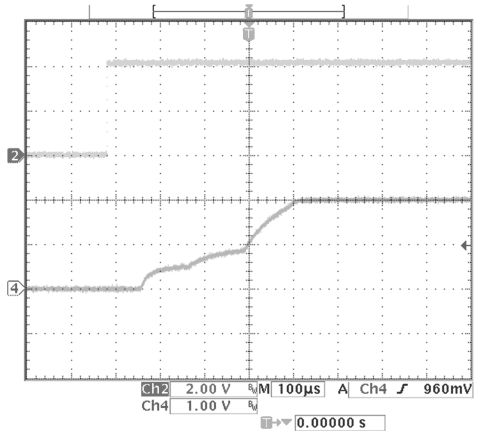
V_{IN} = 3 to 3.6 V V_{OUT} = 3.3 V Load = 250 mA

Figure 32. Line Transient Response



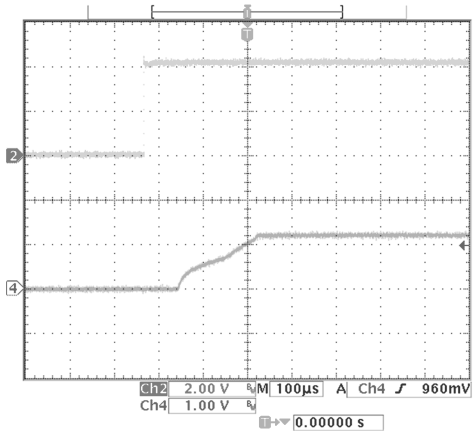
V_{OUT} = 1.8 V Load = 30 mA

Figure 33. Start-up into PWM Mode



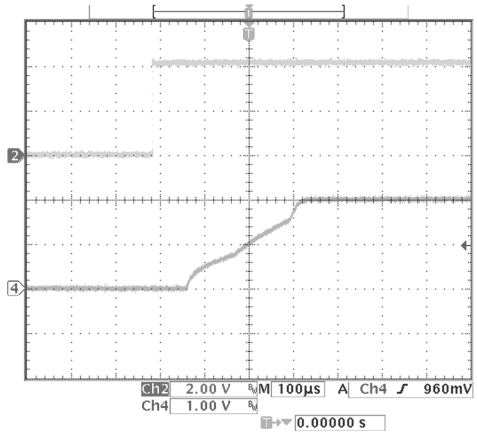
V_{OUT} = 3.3 V Load = 30 mA

Figure 34. Start-up into PWM Mode



V_{OUT} = 1.8 V Load = 30 mA

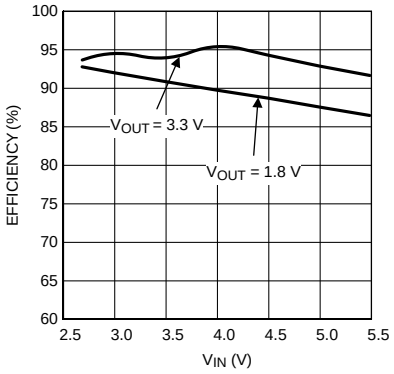
Figure 35. Start-up Into PFM Mode



V_{OUT} = 3.3 V Load = 30 mA

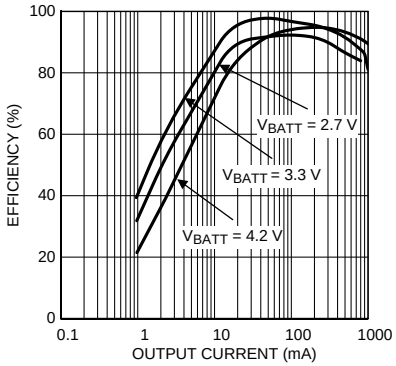
Figure 36. Start-up Into PFM Mode

7.21.4 Buck-Boost Characteristics



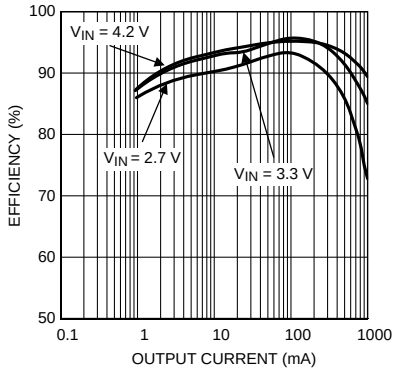
I_{LOAD}= 100 mA

Figure 37. Efficiency vs VIN



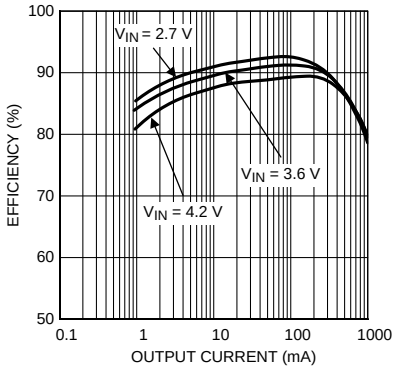
V_{OUT} = 3.3 V

Figure 38. Forced PWM Efficiency vs I_{LOAD}



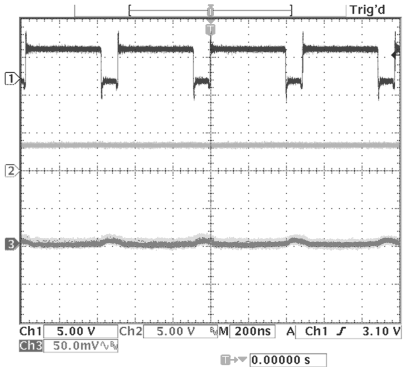
V_{OUT} = 3.3 V

Figure 39. Automode Efficiency vs I_{LOAD}



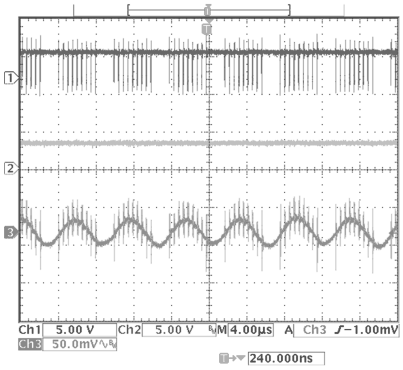
V_{OUT} = 1.8 V

Figure 40. Automode Efficiency vs I_{LOAD}



V_{IN} = 4.2 V V_{OUT} = 3.3 V I_{LOAD} = 250 mA

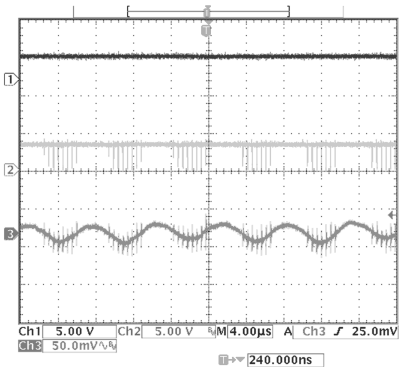
Figure 41. Switch Pins in Buck Mode Operation



V_{IN} = 3.6 V V_{OUT} = 3.3 V I_{LOAD} = 250 mA

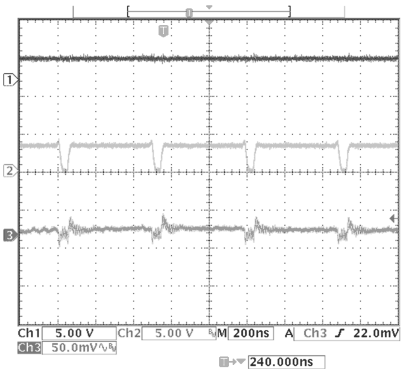
Figure 42. Switch Pin on Edge of Buck Mode Operation

Buck-Boost Characteristics (continued)



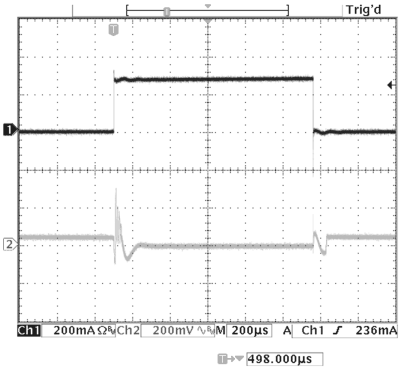
V_{IN} = 3.35 V V_{OUT} = 3.3 V I_{LOAD} = 250 mA

Figure 43. Switch Pin on Edge of Boost Mode Operation



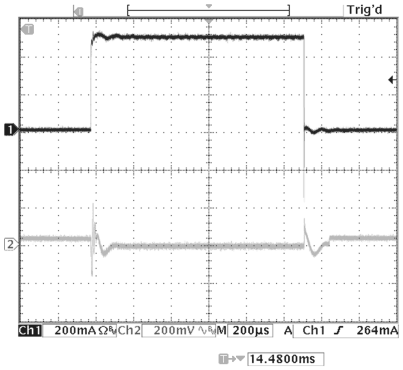
V_{IN} = 3.2 V V_{OUT} = 3.3 V I_{LOAD} = 250 mA

Figure 44. Switch Pins in Boost Mode Operationa



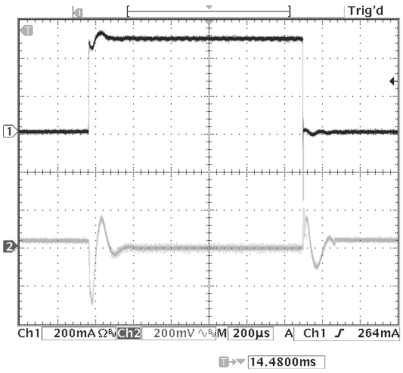
V_{IN} = 4.2 V V_{OUT} = 3.3 V I_{LOAD} = 0 to 500 mA

Figure 45. Load Transient, Buck Response



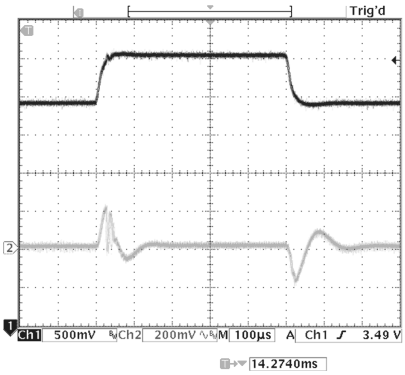
V_{IN} = 3.6 V V_{OUT} = 3.3 V I_{LOAD} = 0 to 500 mA

Figure 46. Load Transient, Edge of Buck Response



V_{IN} = 2.7 V V_{OUT} = 3.3 V I_{LOAD} = 0 to 500 mA

Figure 47. Load Transient, Boost Response



V_{IN} = 3 V to 3.6 V V_{OUT} = 3.3 V I_{LOAD} = 500 mA

Figure 48. Line Transient, Boost Response

8 Detailed Description

8.1 Overview

The LP3910 incorporates 2 low-dropout LDO voltage regulators, 2 integrated buck DC-DC converters with dynamic voltage scaling (DVS), one wide load range buck-boost DC-DC converter with programmable output voltage, a 4-channel 8-bit ADC and a dual source Li-ion or Li-polymer battery charger. The charger has the capability to charge and maintain a single cell battery by seamlessly switching between regulated wall adapter and USB power sources. The LP3910 also incorporates advanced battery management functions such as battery temperature measurement, reverse current blocking for USB, LED charger status indication, thermally regulated internal power FETs, battery-voltage monitoring, overcurrent protection, and a 10-hour safety timer.

The buck-boost DC-DC converter targets the power management of hard disk drives and maintains a typical operating voltage of 3.3 V ±5% with a battery voltage below or above this output level. The buck- boost output voltage can be selected to be as low as 1.8 V.

The 4-channel ADC measures the battery voltage and charge current, which can be used for fuel gauging. Two undedicated channels can be used to measure other analog parameters such as discharge current, battery temperature, keyboard resistor scanning and more. The various device parameters are programmable through a 400-kHz I^2C-compatible interface.

8.1.1 Two Buck Converters

The LP3910 incorporates two high efficiency synchronous switching buck regulators, Buck1 and Buck2 that deliver a constant voltage from a wall adapter or a single Li-ion battery to the portable system processors, memory and I/O. Using a voltage mode architecture with synchronous rectification, both bucks have the ability to deliver up to 600 mA. Buck1 can output voltages from 0.8 V to 2 V while Buck2 can output voltages from 1.8 V to 3.3 V. Additional features include soft-start, undervoltage lockout, current-overload protection, and thermal-overload protection.

8.1.2 Buck-Boost Converter

The synchronous buck-boost magnetic DC-DC converter supplies power to a hard drive that has a typical 3.3-V operating voltage. This voltage is lower than the maximum battery (4.2 V typically for Li-polymer cells) and higher than the minimum battery (typically 2.8 V). Therefore, in order to provide 3.3 V, regardless of the battery voltage, the buck-boost converter either steps down the battery voltage or steps up the battery voltage. The buck-boost automatically switches between PWM and PFM modes depending on the load and automatically switches between buck and boost modes depending on the battery voltage. The buck-boost converter uses an input voltage from 2.7 V to 5.7 V and generates an output voltage between 1.8 V and 3.3 V for up to 1-A loads.

8.1.3 LDO Regulators

LDO1 is a regulator that can respond to fast transients and is slated for digital loads and high bandwidth analog loads. LDO2 is a linear regulator with a similar architecture but has a slower transient response time with a lower noise performance to supply analog loads. Both regulators can supply up to 150-mA loads and have output voltages that are register programmable through the I^2C interface. The LDO1 output voltage is programmable from 1.2 V to 3.3 V, and the LDO2 output voltage is programmable in steps of 100 mV from 1.3 V to 3.3 V.

8.1.4 Battery Charger

The LP3910 can safely charge and maintain a single-cell Li-ion or Li-polymer battery operating off a regulated 6-V automotive adapter, an AC wall adapter, or USB power (VBUS). Input power source selection of USB/adapter is seamless. If present, the charger uses the adapter power regardless of the presence of USB power. The connection of either power source is detected by LP3910. The charger module is a linear charger with constant current pre-qualification, constant current (CC) full-rate charging and constant voltage (CV) charging. CC and CV regulation is performed using an internal power FET Q2 with reverse current blocking. The power FET Q1 acts as a switch with programmable current limit for USB operation.

Overview (continued)

8.1.5 ADC

The LP3910 is equipped with an 8-bit dual-slope integrating analog-to-digital converter (ADC). Dual-slope converters provide effective filtering of > 500-kHz and < 125-kHz noise components on the input voltage and do not require a sample-and-hold stage. The ADC core digitizes the input voltage ranging from V_{REF} to 2 × V_{REF}, where V_{REF} is the voltage measured on the VREFH pin.

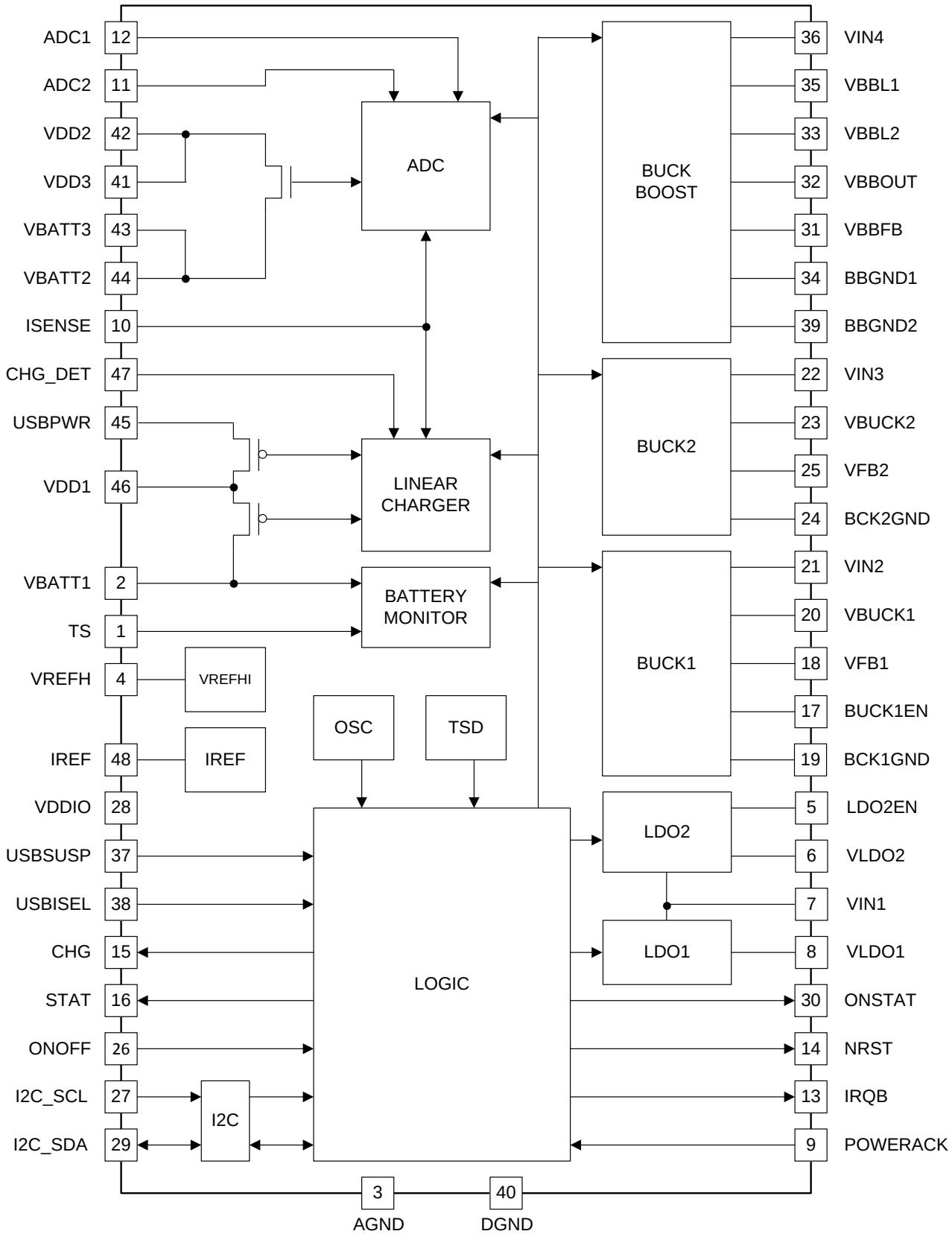
8.1.6 Supply Specification

Table 4 lists the output characteristics of various regulators.

Table 4. Supply Specification

SUPPLY	LOAD	V_{OUT} (V)			I_{MAX} MAXIMUM OUTPUT CURRENT (mA)
		DEFAULT (V)	RANGE (V)	RESOLUTION (mV)	
LDO1	various	Factory-programmed default	1.2 to 3.3	100	150
LDO2	analog		1.3 to 3.3	100	150
Buck1	CPU, DSP		0.8 to 2	50	600
Buck2	I/O, logic, memory		1.8 to 3.3	100	600
Buck-Boost	HD		1.8 to 3.3	50	1000

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Buck1, Buck2: Synchronous Step-Down Magnetic DC-DC Converters

The LP3910 incorporates two high-efficiency synchronous switching buck regulators, Buck1 and Buck2, that deliver a constant voltage from a wall adapter or a single Li-ion battery to the portable system processors, memory and I/O. Using a voltage mode architecture with synchronous rectification, both bucks have the ability to deliver up to 600 mA depending on the input voltage and output voltage (voltage headroom), and the inductor chosen (maximum current capability).

There are three modes of operation depending on the current required: PWM, PFM, and shutdown. PWM mode handles current loads of approximately 70 mA or higher, delivering voltage precision of ±3% with 90% efficiency or better. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_Q = 15 µA typical) and a longer battery life. The Standby operating mode turns off the device, offering the lowest current consumption. PWM or PFM mode is selected automatically or PWM mode can be forced through the setting of the buck control register.

Both Buck1 and Buck2 can operate up to a 100% duty cycle (PMOS switch always on). Additional features include soft-start, undervoltage lockout, current overload protection, and thermal overload protection.

8.3.1.1 Buck1, Buck2 Operation

Buck1 is recommended to be used as the processor core supply and has I^2C selectable output voltages ranging from 0.8 V to 2 V (typical). Buck2 is recommended for I/O power, Memory power and logic power. Its voltage range can be programmed using the I^2C interface from 1.8 V to 3.3 V (typical). The default output voltage for each buck converter is factory programmable (see *Application and Implementation*).

The system designer can also determine the output voltage of either Buck1 or Buck2 through an external feedback resistor ladder by clearing the output voltage selection field in the Buck1 or Buck2 control registers.

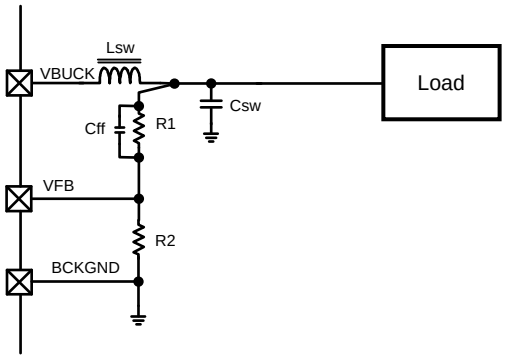


Figure 49. External Control Of Buck Output Voltage Through Feedback Resistor Ladder

8.3.1.2 Circuit Operation Description

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground (BCKGND pin) and a feedback path. During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $V_{IN} – V_{OUT} / L$.

by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $–V_{OUT} / L$.

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

Feature Description (continued)

8.3.1.3 PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed-forward voltage inversely proportional to the input voltage is introduced.

8.3.1.4 Internal Synchronous Rectification

While in PWM mode, the buck uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

8.3.1.5 Current Limiting

A current limit feature allows the buck to protect itself and external components during overload conditions PWM mode implements cycle-by-cycle current limiting using an internal comparator that trips at 1000 mA (typical).

8.3.1.6 PFM Operation

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The device automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

The inductor current becomes discontinuous or the peak PMOS switch current drops below the I_{MODE} level:

$$\left(\text{Typically } I_{MODE} < 66\ \text{mA} + \frac{V_{IN}}{160\Omega}\right) \tag{1}$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the high PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the high PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is:

$$I_{PFM} = 66\ \text{mA} + \frac{V_{IN}}{80\Omega} \tag{2}$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the *high* PFM comparator threshold (see Figure 50), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this sleep mode is less than 30 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the *low* PFM threshold, the cycle repeats to restore the output voltage to approximately 1.6% above the nominal PWM output voltage.

If the load current increases during PFM mode (see Figure 50) causing the output voltage to fall below the 'low2' PFM threshold, the device automatically transitions into fixed-frequency PWM mode.

Feature Description (continued)

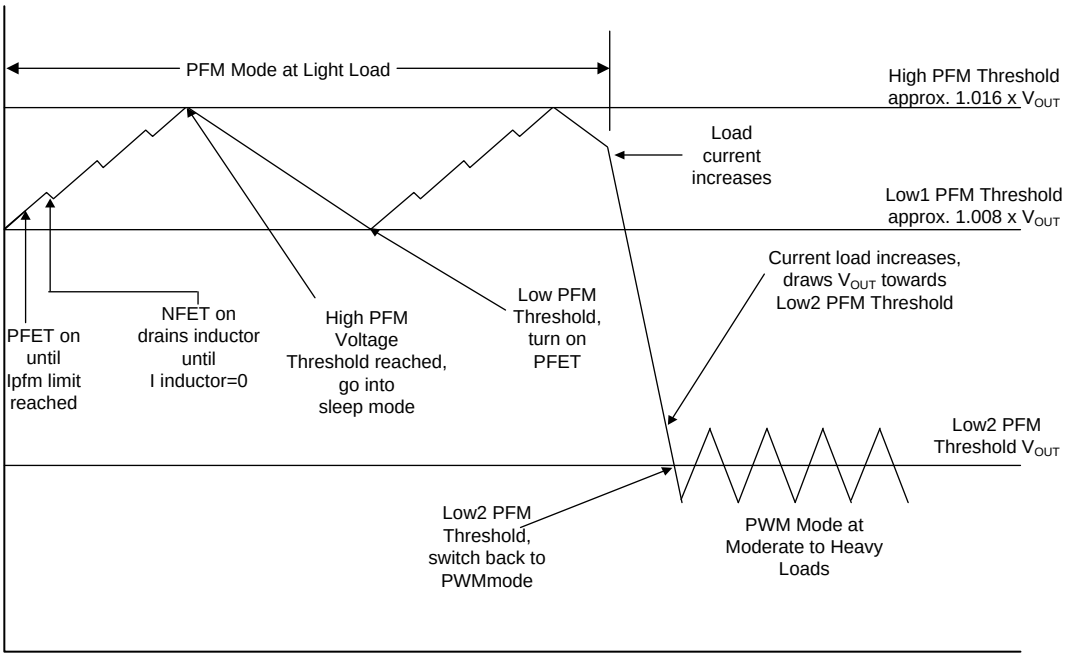


Figure 50. Operation in PFM Mode and Transfer to PWM Mode

8.3.2 Buck-Boost: Synchronous Buck-Boost Magnetic DC-DC Converter

The LP3910 is equipped with a synchronous buck-boost magnetic DC-DC converter to supply power to the hard drive that has a typical 3.3-V operating voltage. This voltage is lower than the maximum battery (4.2 V typically for Li-polymer cells) and higher than the minimum battery (typically 2.8 V). Therefore, in order to provide 3.3 V, regardless of the battery voltage, the Buck-Boost converter either steps down the battery voltage or steps up the battery voltage. The Buck-Boost automatically switches between PWM and PFM modes depending on the load and automatically switches between buck and boost modes, depending on the battery voltage.

By setting bit D6 of the Buck-Boost control register, the Buck-Boost is forced to operate using PWM modulation regardless of the load. By default this bit is cleared.

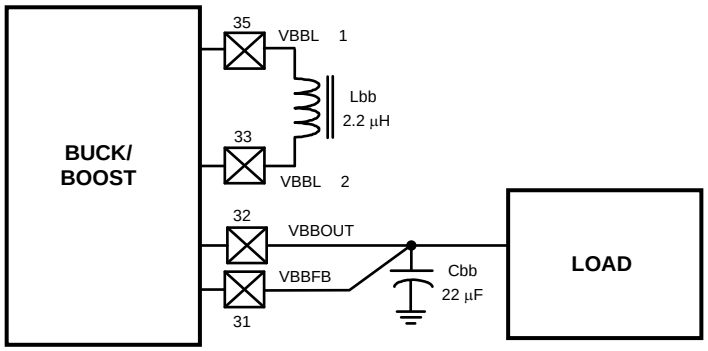


Figure 51. Schematic Section for Buck-Boost Operation

8.3.3 Linear Low Dropout Regulators (LDOs)

LDO1 is a regulator that can respond to fast transients and is slated for digital loads and high bandwidth analog loads. LDO2 is a linear regulator with a similar architecture but has a slower transient response time with a lower noise performance to supply analog loads. The output voltages of both LDOs are register programmable through the I^2C interface. The default output voltages are factory programmed during final test.

Feature Description (continued)

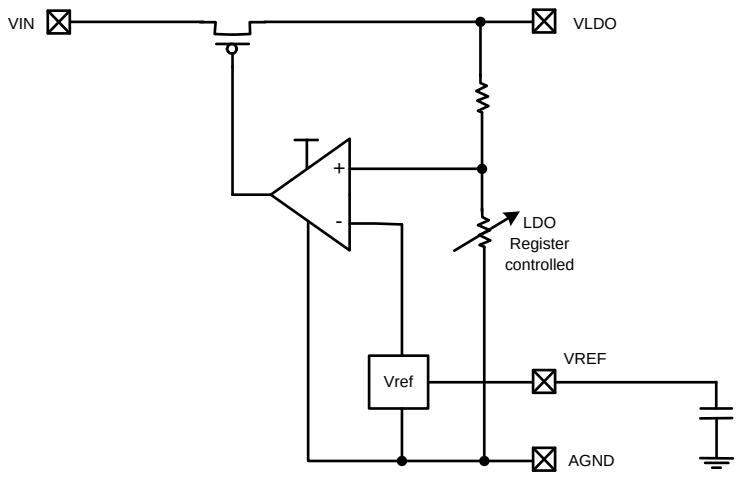


Figure 52. LDO Architecture Diagram

8.3.3.1 No-Load Stability

The LDOs remain stable and in regulation with no external load. This is an important consideration in some circuits, for example, CMOS RAM keep-alive applications.

8.3.4 Li-Ion Linear Charger

8.3.4.1 Charger Architecture

The LP3910 can safely charge and maintain a single cell Li-ion or Li-polymer battery operating from a regulated 6-V car adapter, AC wall adapter, or USB power (VBUS). Input power source selection of USB/adapter is seamless. If present, the charger uses the adapter power regardless of the presence of USB power. The connection of either power source is detected by the LP3910 device.

Feature Description (continued)

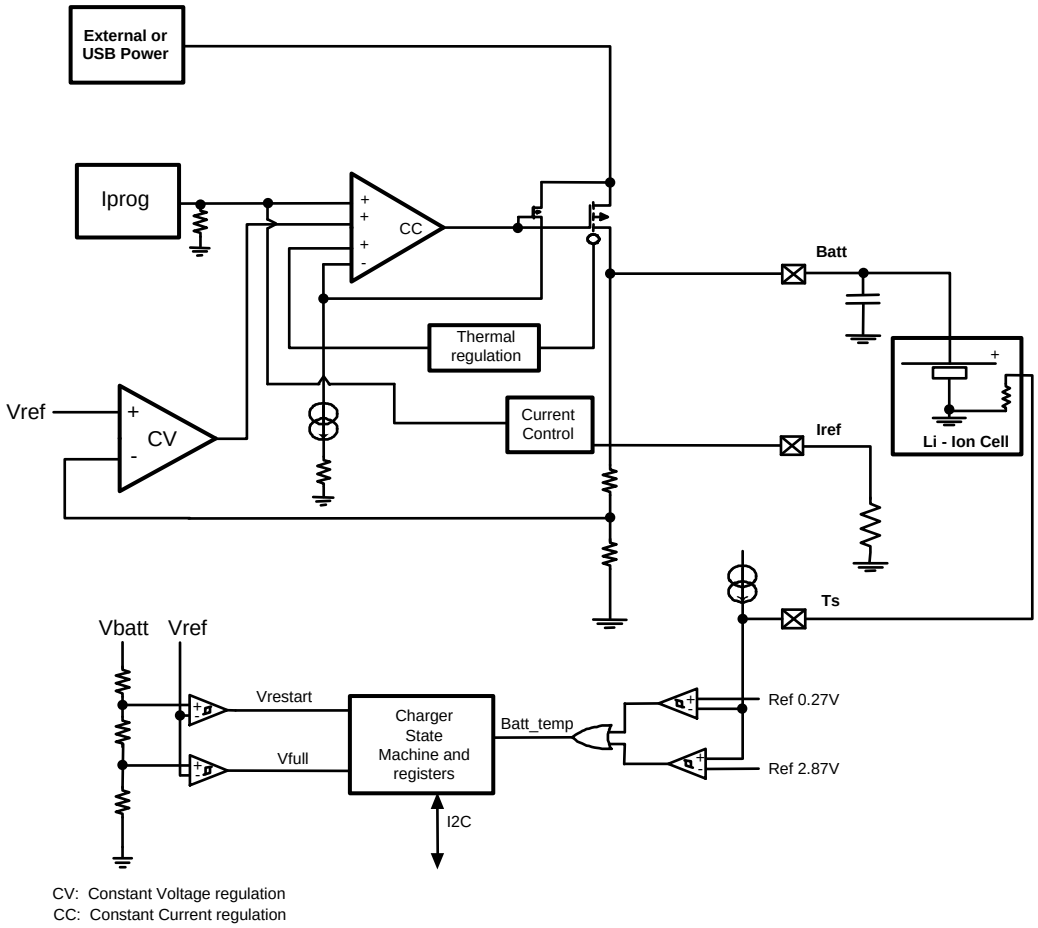


Figure 53. Charger Architecture

The charger module is a linear charger with constant current pre-qualification, CC full-rate charging and CV charging. CC and CV regulation is performed using an internal Power FET Q2 with reverse current blocking. The termination voltage is controlled to within ±0.35% at room temperature.

The power FET Q1 acts as a switch with programmable current limit for USB operation.

Feature Description (continued)

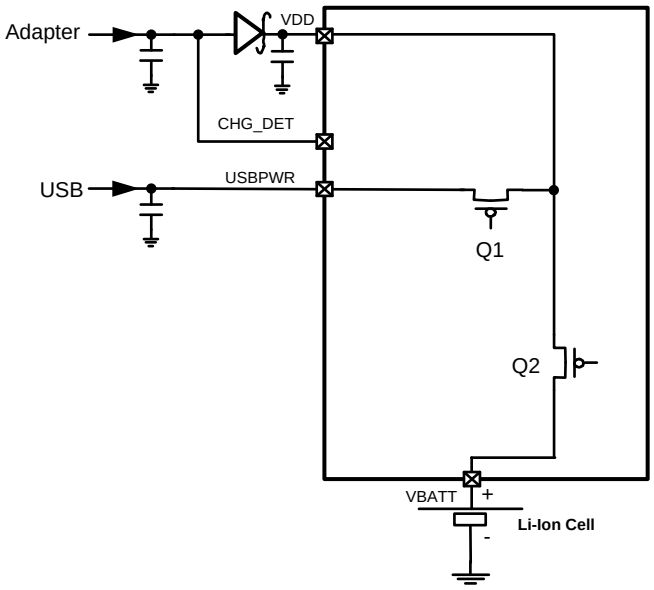


Figure 54. Switches for USB Charging Path

8.3.4.2 Charge Status Indication

Two LEDs connected to the LP3910 are used to indicate the status of the charging. The CHG pin is connected to a red LED that is enabled when an external power source is connected and the battery is charging. The second STAT pin is connected to a green LED. When the battery charging transitions from CC to CV mode, then the green LED is blinking with a 50% duty cycle and a period of 1 second. When the battery is fully charged, then the green LED is always on.

Both LEDs are off when there is no external power connected.

Table 5. Truth Table for the LED Status Indicators

CONDITION	RED LED	GREEN LED
No Charger or USB	OFF	OFF
Charger off	ON	OFF
Pre-Qualification	ON	OFF
Constant Current CC	ON	OFF
Constant Voltage CV	ON	50% duty cycle
EOC / Top-OFF charging	ON	ON
Charge cycle complete	ON	ON
ERROR (Battery Temperature, Thermal shutdown)	50% duty cycle	OFF
Safety Timer Expired	50% duty cycle	OFF

50% duty cycle indicates the LED is pulsed on and off for equal times at a frequency of 1 Hz.

The RED pin and GREEN pin are connected to a regulated driver to ensure that the brightness is independent from the external power. The LEDs need to be connected between the CHG and STAT pins and GND.

8.3.4.3 Thermal Charger Power FET Regulation

The internal power FET Q2 in the linear charger module is thermally regulated to the junction temperature of 115°C to ensure optimal charging of the battery. The charge current is limited by the charge current selected in the charger control register but is also thermally limited to prevent the junction from overheating during high charge currents at high ambient temperatures as the package power dissipation is limited.

Thermal regulation ensures maximum charge current and superior charge rate without exceeding the power dissipation limits of LP3910 device.

8.3.4.4 Battery Charger Operating Modes

8.3.4.4.1 Pre-Qualification Mode

Lithium batteries cannot be subjected to a high current when the battery voltage is under a certain threshold, otherwise the longevity of the battery would be compromised. Below this threshold of $V_{FULLRATE}$, which typically measures 2.85 V, the charger circuit supplies a pre-qualification charge current. If the wall adapter is charging the battery, the charger circuit supplies a constant current of 10% of the programmed charge current. If the USB is charging the battery, the charger circuit supplies a constant 50-mA charge current. When the battery voltage reaches V_{FULL_RATE}, the charger transitions from pre-qualification to full-rate charging. In pre-qualification mode, the STAT2, STAT1, and STAT0 bits in the charger supervisory register are respectively low, low, high.

8.3.4.4.2 Full-Rate Charging Mode

The full-rate charge cycle is initiated following the successful completion of the pre-qualification mode. During full-rate charging, the battery voltage steadily increases while charged with a CC. The three charger status bits STAT2, STAT1, and STAT0 are respectively low, high, and low. The full-rate charge current is selected using the charge control register, which defaults to 100 mA.

Charging Li-ion batteries at a rate of 1C is recommended (where *C* is the capacity of the battery). As an example, it is recommended to charge a battery with a capacity of 800 mA at 800 mA, or 1C. Charging at a higher rate may compromise the quality and lifetime of the battery.

8.3.4.4.3 Constant-Voltage (CV) Charging Mode

The battery voltage increases rapidly as a result of full-rate charging and once it reaches the programmable termination voltage of either 4.1 V, 4.2 V or 4.38 V, the charger moves to constant-voltage charge mode. During this mode, the charge current gradually decreases while the battery remains at the termination voltage. The termination voltage can be selected to be either 4.1 V, 4.2 V or 4.38 V by programming bits D6 and D7 in the Charger Control register to accommodate different battery chemistries. In CV charging mode, the Charge Control Status bits STAT2, STAT1 and STAT0 are respectively logic 0, logic 1, and logic 1.

8.3.4.4.4 Top-Off Charging Mode

When the charge current reduces to the EOC threshold (programmable to 5% or 10% of programmed full rate charge current), constant voltage charging continues for an additional 21 minute TOP-OFF time period. In TOP-OFF charging mode, the Charge Control Status bits STAT2, STAT1 and STAT0 are respectively logic 1, logic 1 and logic 1. At the end of the TOP-OFF period, the charger transitions to Charge Cycle Complete.

8.3.4.4.5 Charge Cycle Complete

During charge cycle complete, the charger is automatically disabled, regardless of the state of the charge enable bit. In charge cycle complete, the STAT2, STAT1 and STAT0 bits are respectively logic 1, logic 0, and logic 1. When the battery voltage drops below the $V_{RESTART}$ threshold, charging resumes in full-rate charging mode.

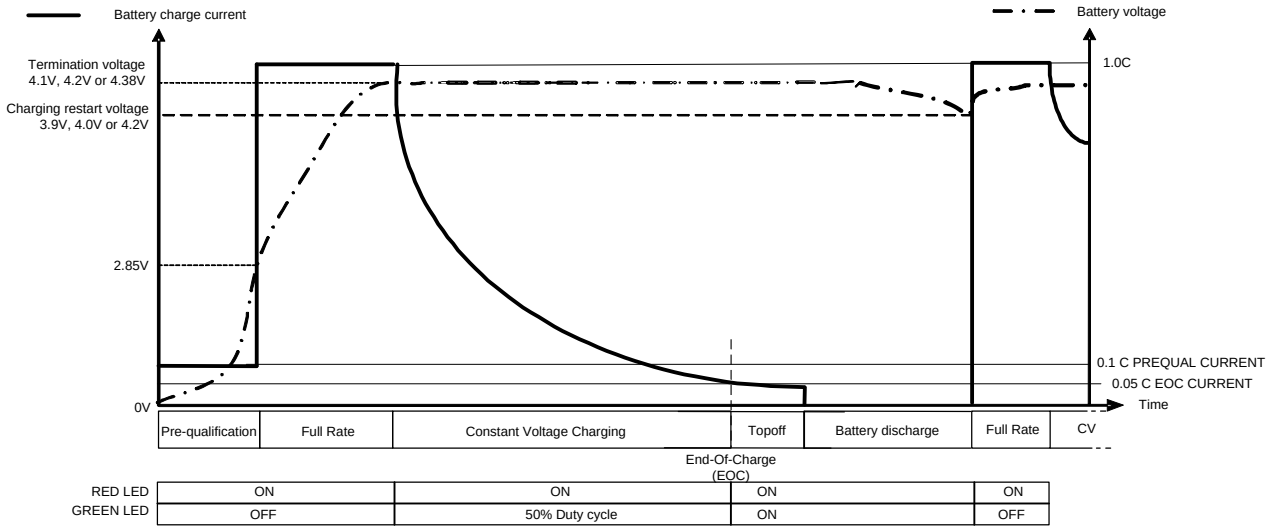


Figure 55. Charge Cycle Complete

8.3.4.5 Battery Temperature Monitoring (TS Pin)

The LP3910 is equipped with a battery thermistor terminal to continuously monitor the battery temperature by measuring the voltage between the T_S pin and GND. With the T_S pin connected to the battery thermistor, charging is allowed only if the battery temperature is within the acceptable temperature range set by a pair of internal comparators inside the LP3910. The temperature window is 0°C to 45°C or 0°C to 50°C, depending on the setting of D2 of the charger supervisory (CHSPV) register. There is 3°C of temperature hysteresis associated with each temperature threshold. The default temperature range is 0°C to 50°C and can be changed to 0°C to 45°C by setting bit D3 in the CHSPV register. If the battery temperature is out of range, STAT2, STAT1, and STAT0 bits in the CHSPV register are set to logic1, logic0, logic0, and charging is suspended.

The TS pin is only active during charging and draws no current from the battery when no external power source is present.

If the TS pin is not used in the application, it must be connected to GND through a 100-kΩ pulldown resistor.

When the TS pin is left floating (battery removal), the charger is disabled as the TS voltage exceeds the lower temperature limit.

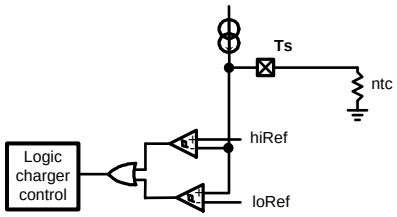


Figure 56. Battery Temperature Monitor with TS Pin

8.3.4.6 Disabling Charger

Charging can be safely interrupted by clearing the Charge enable bit D1 in the Charge Control Register and can subsequently resume upon setting this bit. When the charger is disabled, STAT2, STAT1, and STAT0 bits in the CHSPV register are set to logic 0.

8.3.4.7 Safety Timer

In order to prevent endless charging, which could degrade the battery quality and life time, the LP3910 contains a safety timer that limits charging regardless whether the battery has reached its full capacity or not. In prequalification the safety timer is 1 hour. In full rate or constant voltage charging the safety timer is a maximum of 10 hours minus the time in prequalification.

When the timer times out of uninterrupted charging, an IRQ is generated to alert system processor. The status of the timer can also be polled by reading the IRQ register if the system doesn't support hardware interrupts.

The safety timer resets and starts counting from zero upon the following events:

1. Power ON (through connecting valid power to either USBPWR or CHGN_IN pins).
2. Interchanging USBPWR and CHG_IN sources.
3. The voltage of a charged battery drops below the restart value, and the charger is enabled.
4. Disabling and re-enabling of the charger by toggling bit D1 of the Charge Control Register.
5. Emerging from thermal shutdown.
6. Emerging from a battery temperature out-of-range, and the charger is enabled.
7. Emerging from USB suspend mode when charging with USB power.

8.3.4.8 Charging Maintenance

When a fully charged battery is being loaded by the system while the external power is present and while bit D1 in the charge control register is set to a 1 (charge enable) then the charging restarts when the battery voltage drops below the charging restart threshold. The value of the threshold depends on the termination voltage according to the following table:

Table 6. Charging Thresholds

V_{TERM}	CHARGING RESTART VOLTAGE
4.1 V	3.9 V
4.2 V	4 V
4.38 V	4.2 V

8.3.5 ADC

The LP3910 is equipped with an 8-bit dual-slope integrating an ADC. Dual-slope converters provide effective filtering of > 500-kHz and < 125-kHz noise components on the input voltage, and does not require a sample and hold stage. The ADC core digitizes the input voltage ranging from V_{REF} to $2V_{REF}$, where V_{REF} is the voltage measured on the VREFH pin. After an initial 2-ms warm-up for the first activation of the ADC enable bit, the dual-slope converter integrates the input signal during the first phase for approximately 2 ms, followed by a second phase that integrates V_{REF} for 0 ms to 2 ms depending on the level of the input signal. As a result the total conversion time varies from 2 ms to 4 ms.

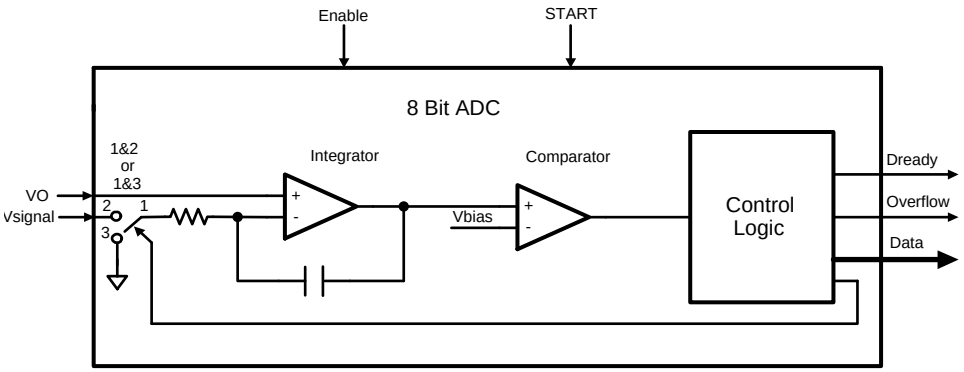


Figure 57. Simplified ADC Block Diagram

The ADC multiplexes 4 different sources:

1. The battery voltage
2. The battery charge current
3. External source ADC1
4. External source ADC2

The voltage ranges for the first two sources are scaled to match the input voltage interval of the ADC: [V_{REFH}, $2V_{REFH}$]. This is accomplished by using two internal scalars.

8.3.5.1 Battery Voltage Measurement

The battery voltage scalar transforms the battery voltage ranging from 2.6 V to 3.5 V to the reference voltage interval: [V_{REFH}, $2*V_{REFH}$]. A wider voltage range (2.6 V to 4.4 V) can be selected through I^2C by setting the voltage range bit D7 in register 0xA to 0'b1.

8.3.5.2 Battery Charge Current Measurement

The battery charge current is indirectly measured by measuring the voltage across the ISENSE resistor, R_{SENSE}. A fixed portion of the battery charge current is mirrored over the R_{SENSE} as in Equation 3:

$$V_{ISENSE} = K \times I_{CHARGE} \times R_{SENSE} \quad (3)$$

where K is a ratio between the I_{SENSE} current and the charge current.

The battery charge current scalar transforms the voltage across the external ISENSE resistor to the [V_{REFH}, 2 × V_{REFH}] input voltage interval of the ADC.

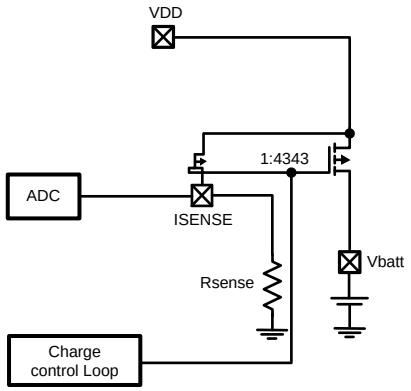


Figure 58. Battery Charge Scalar

8.3.5.3 External General-Purpose Sources

Two additional ADC sources are available on the ADC1 and ADC2 pins of the LP3910. These two external ADC sources are not internally scaled and have an input voltage range of [V_{REFH}, 2 × V_{REFH}]. The system designer can use these two sources for general-purpose applications such as resistive keyboard matrix scanning, temperature measurements, battery load current, battery ID resistor measurement, and others.

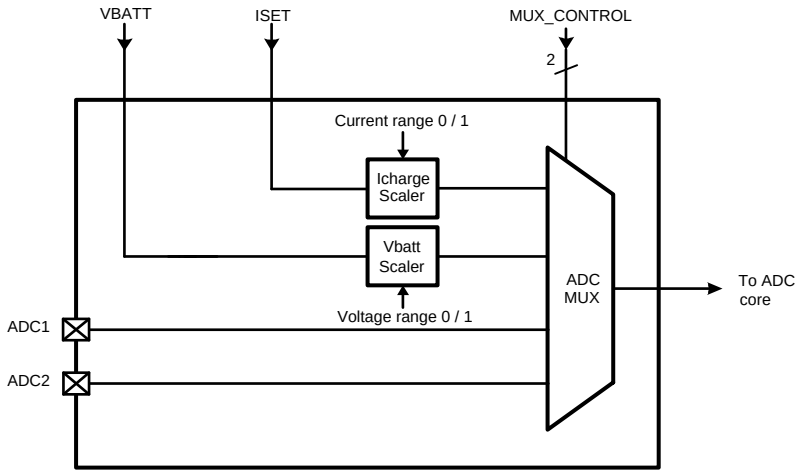


Figure 59. ADC Analog Front-End Block Diagram

The source selection and the access to the conversion results are established through the I^2C linked control registers: ADCC and ADCD.

The ADC is by default disabled to minimize current consumption and must be enabled by setting D2 in the ADCC register. Writing a logic 1 to bit D3 in the ADC initiates a conversion. It is advised to select the correct ADC source before a conversion is started. The ADC sets bit D4 in the ADCC register upon the completion of a conversion, which is typically 4 ms after the start of the conversion. At the same time an interrupt request is generated. (See IRQ Register (0d)H Interrupt Request Register).

To save power, disable the ADC by setting bit 2 of D2 to 0. To make repetitive starts, set bit D3 to 0 then to 1 for register 0Ah to initiate start of conversion. The interrupt driven protocol between LP3910 and the system processor is the most efficient way to acquire data from successive measurements as shown in Figure 60:

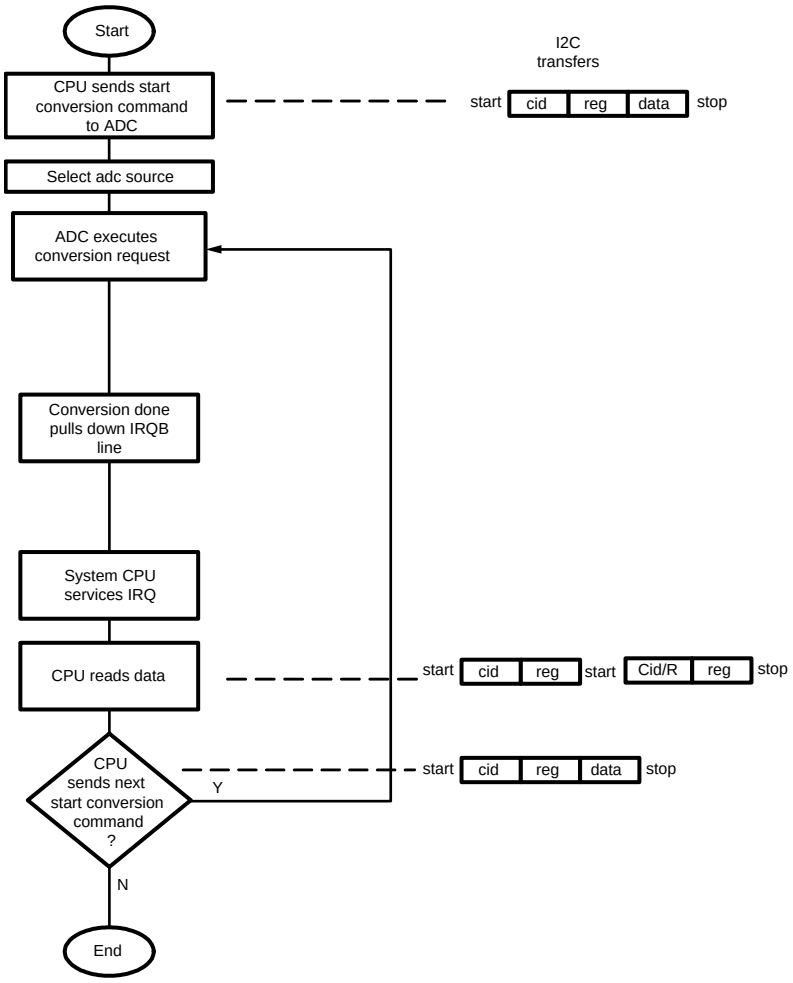


Figure 60. Data Measurement and Acquisition Sequence

8.3.6 Interrupt Request Output

The LP3910 has the ability to interrupt the system processor through the open drain IRQB pin, which transitions to an active logic low level upon the following 8 events:

- USB Power detected
- USB disconnected
- CHG_IN Power detected
- CHG_IN disconnected
- Battery low alarm
- Thermal alarm
- ADC conversion completed
- Charger safety timer time-out

The events form the interrupt sources that correspond to a certain bit location in the interrupt request (IRQ) register. All interrupt sources can be masked by the interrupt mask register (IMR). Masking the interrupt prevents the interrupt event from asserting the IRQB pin, yet the event is still captured in the IRQ register, which allows the processor to poll the interrupt sources.

After an active low IRQB has been detected by the system processor, the latter services the interrupt and accesses the IRQ register to determine which source was responsible for the interrupt request. Reading the IRQ register automatically clears the register to enable the capture of the next interrupt events.

As new interrupts can occur while the I^2C read cycle is clearing the IRQ register, a buffer register called interrupt pending register (IPR), not accessible through the I^2C-compatible interface holds the next interrupts. De-asserting the IRQB output is immediately followed by a new transition of IRQB to logic low when an interrupt is pending.

The Interrupts are not hardware prioritized. It is up to the firmware to determine the priority in case more than one interrupt request is set.

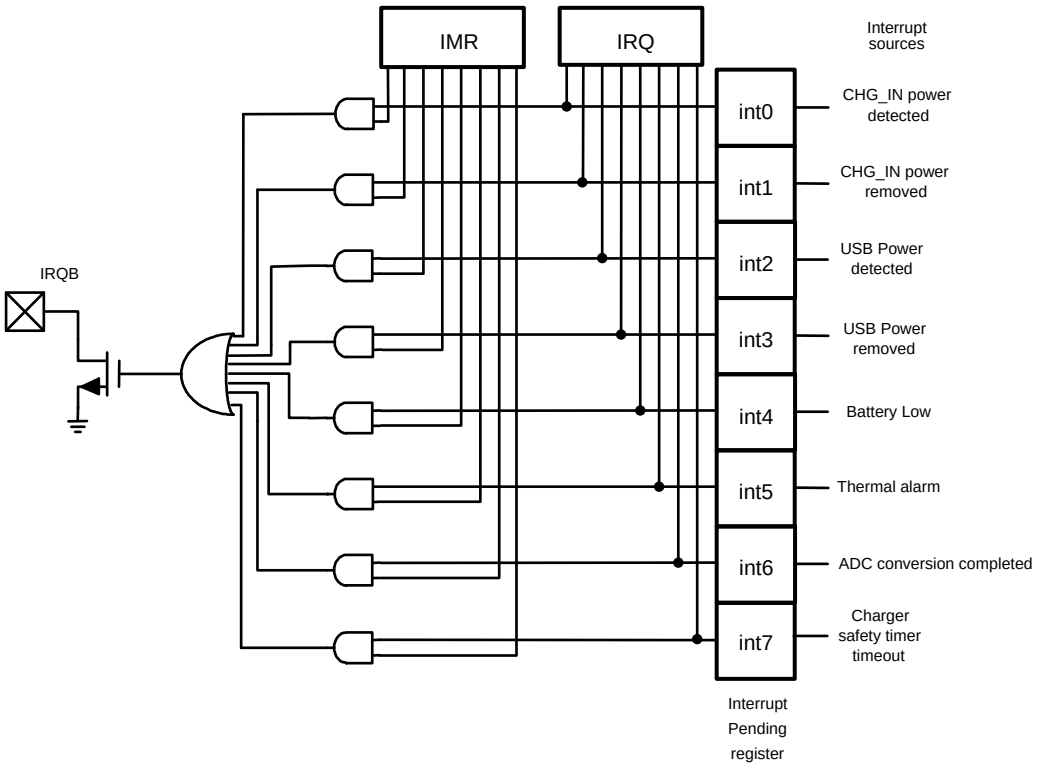


Figure 61. Interrupt Request Setting

8.3.6.1 Interrupts and Standby Mode

Interrupts are captured in standby mode and can be serviced when the system processor is enabled when the LP3910 is in an active state.

8.3.6.2 Interrupt Sources

- CHG_IN Power Detected and CHG_IN Disconnect (INT0 and INT1): An interrupt (INT0) is generated when CHG_IN power is connected to the LP3910. Another interrupt (INT1) is generated upon CHG_IN power removal.
- USB Power Detected and USB Disconnect (INT2 and INT3): An interrupt (INT2) is generated when USB power is connected to the LP3910. Another interrupt (INT3) is generated upon disconnecting the USB power.
- Battery Low (INT4): When the battery voltage drops below the battery low threshold IRQ, an interrupt is generated. This allows the processor to perform some routine tasks prior to going to standby mode.
- Thermal Alarm (INT5): If the junction temperature of the LP3910 exceeds 115°C, an interrupt is generated.
- ADC Conversion Done (INT6): The ADC generates an interrupt request upon the completion of a data conversion.
- Charger Timer Interrupt (INT7): A charger timeout occurs 10 hours after it started (see *Li-Ion Linear Charger*) and subsequently requests an interrupt.

8.3.7 Power-On-Reset

The LP3910 is equipped with an internal power-on-reset (POR) circuit that resets the logic when $V_{DD} < V_{POR}$. This ensures that the logic is properly initialized when V_{DD} rises above the minimum operating voltage of the logic and the internal oscillator that clocks the sequential logic in the control section.

8.3.8 Thermal Shutdown and Thermal Alarm

An internal temperature sensor monitors the junction temperature of the LP3910. This sensor forcibly invokes standby mode in the unusual case of the junction temperature of the silicon exceeding the normal operating level due to excessive loads on all power regulators, the Li-ion charger, or due to an abnormally high ambient temperature. The thermal shutdown threshold is 160°C.

The thermal shutdown is preceded by a thermal alarm that generates an interrupt request if unmasked. The temperature threshold for triggering the alarm is 115°C.

8.3.9 NRST Pin

The NRST pin is an open-drain output and is active low during standby, power-off and charger standby modes. The NRST timing is determined by a factory programmable counter.

8.3.10 Operation Without I²C Interface

Operation of the LP3910 without the I²C interface is possible if the system can operate with default values for the DC-DC converters and the charge (see Table 3). The I²C-less system must use the POWERACK pin to power cycle the LP3910.

8.3.11 I²C Master Power Concern

The processor that contains the I²C master must be powered by BUCK1 or LDO2 as these converters require no I²C access to enable/disable them. If the I²C master were to be powered by a DC-DC converter that is enable/disabled through a control register, then a corrupted application software execution could by accident disable the power to the I²C master, which in this case has no means to recover. It is possible that the regulator connected to V_{DDIO} may accidentally disable, in which case the processor should recognize that communication has been broken, then power down the system to allow for a clean restart.

8.3.12 System Operation When the Load Current Exceeds the USB or Adapter Current Limit

In the event that the system requires current that exceeds the current limit of either the USB or the adapter source, then the battery can provide the extra power provided that it has been charged. It is clear that a long sustained overload eventually discharges the battery such that its extra power is no longer be sufficient to properly operate the system. This is the case when the system is for instance operated from a USB host with a 100-mA current limit.

8.3.13 Power Routing

The LP3910 power can originate from three different sources: Adapter power, USB power, or battery power. The objective of the power routing is to be able to:

- Operate the portable system from external power regardless of the battery voltage.
- Operate the portable system from USBPWR when the battery exceeds the full-rate qualification threshold voltage ($V_{FULLRATE}$).
- Concurrently charging and operating the system when external power is present
- Seamless selection of Adapter or USB power as the primary external power source

Power Routing supports 4 modes:

1. A regulated external adapter power is present and concurrently supplies the system power and the battery charger.
2. USB power is present and supplies the system and the battery.
3. USB power is present but the system demand exceeds the USB current limit, so that the battery provides the additional power to operate the system.
4. The battery is the sole supply source to the system when no external power source is present

The current flows in the different modes are realized through internal FETS and an external Schottky as shown in Figure 62:

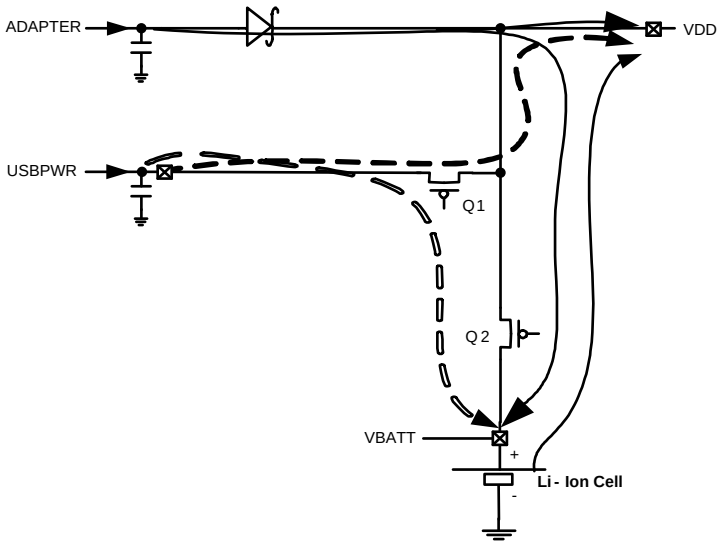


Figure 62. Charging and Sourcing Current Paths

The current provided by the external adapter power or USB power, when inserted, first supplies the system load; the remainder is used for charging.

The different paths are configured through two internal power FETs, Q1 and Q2, and an external Schottky diode. Q1 is a power FET that is only active during USB charging. Q2 functions either as a linear power FET during charging or as a low R_{DSON} switch when no external power is present, and the battery discharges to supply power to the system.

Table 7. Power Routing Options

POWER ROUTE	Q1	Q2
Regulated adapter supply & battery charging	OFF	Regulated
USB supply & battery charging	ON	Regulated
No external supply and battery discharging	OFF	ON

The power routing function allocates power to the system through the VDD pin and to the battery. VDD1, VDD2, VDD3, VIN1, VIN2, VIN3, and VIN4 must be connected together externally. VBATT1, VBATT2, and VBATT3 must be connected together externally.

8.3.14 Battery Monitor

The battery voltage is monitored and invokes the power-off mode when the battery low threshold is breached for more than 5 ms (typical). The battery-low threshold DEFAULT is factory programmed. The battery low threshold range is 2.5 V to 3.5 V with steps of 50 mV. The battery-low threshold in the table below refers to a decreasing battery voltage. The threshold when the battery voltage is transitioning out of the $V_{BATTLOW}$ is 50 mV (typical) higher than the values listed in the table below due to a built-in hysteresis of 50 mV (typical).

The battery low IRQ is triggered 200 mV above the battery low alarm threshold that powers down the device. This gives the user time for a controlled shutdown.

8.3.15 External Power and Battery Detection

When a wall adapter is detected, regardless of the battery voltage, the LP3910 moves to the active mode and the power-up sequencer is started. Similar to the ONOFF pin, there is a 32-ms deglitch time to ensure a clean wall adapter detection and the system processor must set the PACK bit (D4) in the PON register or the POWERACK pin within 128 ms (maximum) of the start of the power-up sequencer.

When USB PWR is detected, and the battery is above the low-battery-alarm threshold, the LP3910 moves to the active mode, and the power-up sequencer is started. As with the ONOFF pin, there is a 32-ms deglitch time to ensure a clean USB detection, and the system processor must set the PACK bit (D4) in the PON register or the POWERACK pin within 128 ms (maximum) of the start of the power-up sequencer. If the battery is below the low-battery-alarm threshold, the system remains powered down until the USBPWR charges the battery up to the low-battery-alarm threshold, at which point the power-up sequencer is started.

The four LSB bits of the PON register indicate which PON source moves the LP3910 device out of standby and into active mode:

- Battery insert
- ONOFF push button
- CHG_IN detect (connection of power adapter)
- USB power (plug-in of powered USB cable)

These bits are cleared upon powering off.

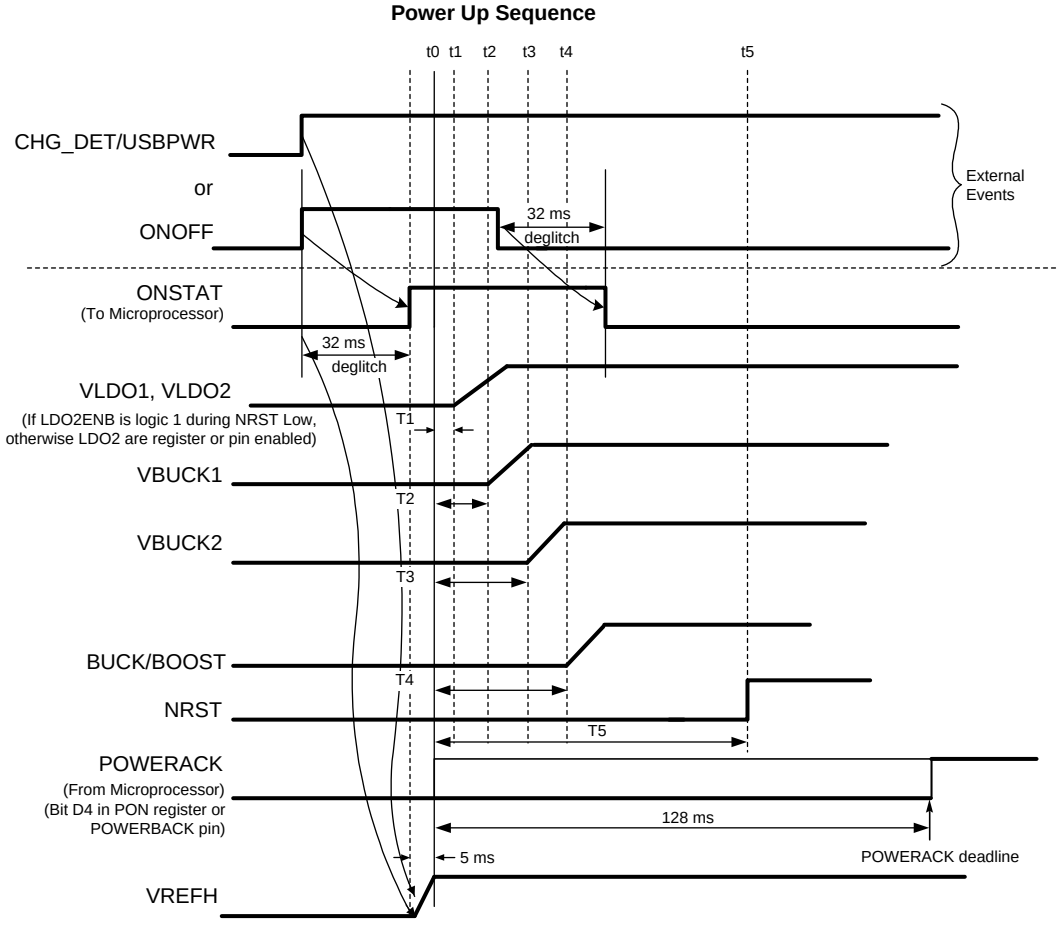


Figure 63. Power-Up Sequence

8.3.16 USB Suspend Mode

The LP3910 USB current consumption can be disabled during suspend mode through a dedicated pin (USBSUSP). Applying a logic 1 to this pin disables the USB current path, and current is reduced to input leakage current less than 30 µA on the USBPWR pin.

8.3.17 Setting the USB Current Limit

The USB current that is available from the USB on the VBUS wire is limited by default to 100 mA. More current (up to 800 mA) can be negotiated through a session request protocol between host and peripheral. The USB current limit must be signaled to the LP3910 by means of the USBISEL pin or the I_{LIMIT} register as indicated below:

- If the USB current limit is 100 mA then the USB controller of the peripheral system must set the USBISEL logic 0 or by setting the I_{LIMIT} register bits [D1, D0] to 2'b00.
- If the USB current limit is 500 mA, the USB controller must apply logic 1 to the USBISEL pin or change the I_{LIMIT} register accordingly. Under this condition, the LP3910 allows charging with a charge current that is determined by the charge control register, not exceeding 500 mA.

The LP3910 prevents (through internal circuitry) the charge current from exceeding the USB current limit, even if the current setting in the Charge Control Register exceeds 500 mA.

The controller can also select a USB current limit of 800 mA through I^2C that exceeds current USB spec values.

8.3.18 Control Registers

The LP3910 contains 14 user-programmable registers that configure the functionality of the individual modules inside the device. Registers are programmed through an I^2C interface and have default values that are invoked during an internal reset. Some of the default values can be tailored to the specific needs of the system designer.

8.4 Device Functional Modes

The LP3910 can be in 3 different operating modes as shown in Figure 64:

Device Functional Modes (continued)

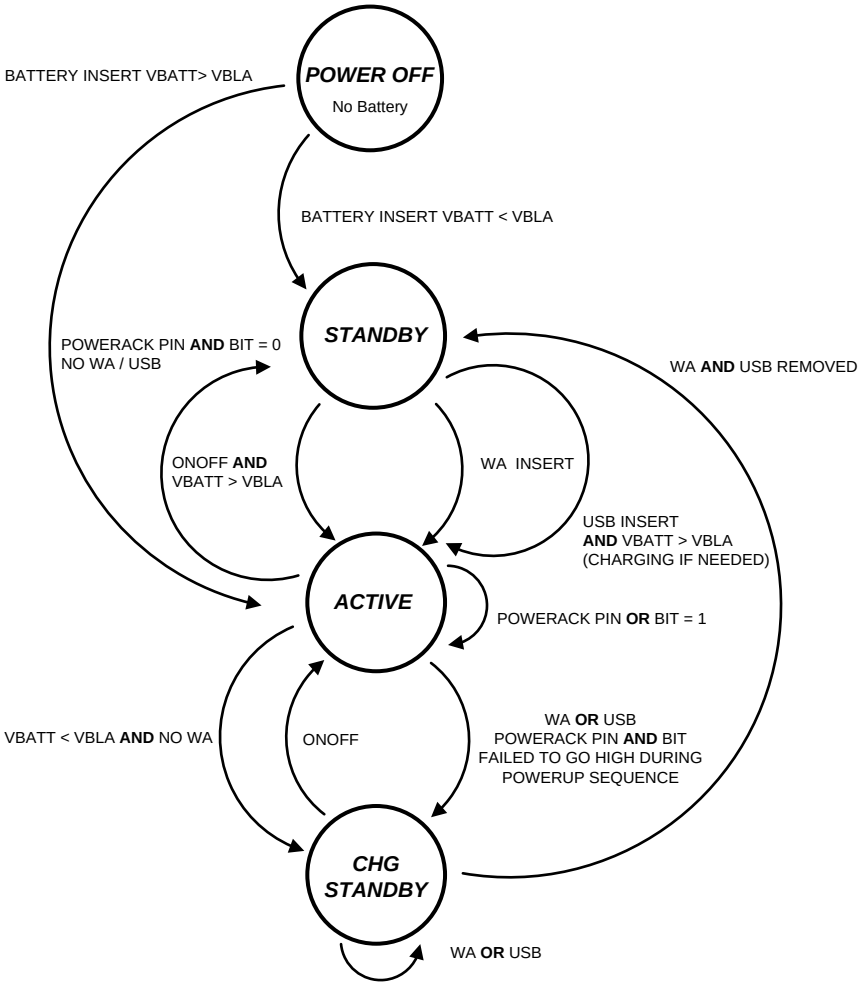


Figure 64. Operating Mode State Diagram

8.4.1 State Machine Definitions

V_{BLA} Battery low alarm threshold

V_{BATT} Battery voltage

WA Wall Adapter

USB Universal Serial Bus Adapter

ONOFF On off pin event

POWERACK Acknowledgment from the Host Processor

Device Functional Modes (continued)

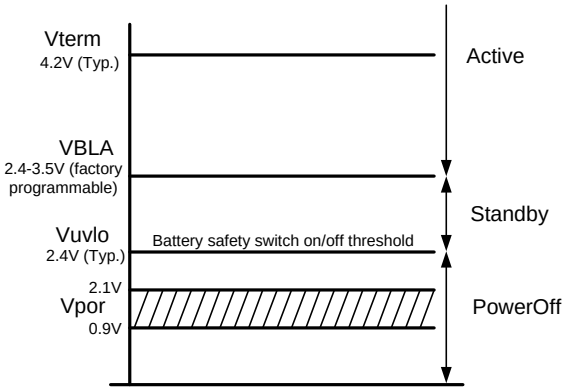


Figure 65. Voltage Threshold Levels

Table 8. Power State Table

	POWER OFF	STANDBY	ACTIVE	CHARGER STANDBY
LDO1,2	Off	Off	On	Off
Buck1,2	Off	Off	On	Off
Buck-Boost	Off	Off	On	Off
Charger	Off	Off	On if Charger / USB Present	On if Charger / USB Present
ADC	Off	Off	On	Off
NRST	Low	Low	High	Low
I^2C interface	Off	Off	On	On
Internal system oscillator	Off	Off	On	On
Battery monitor	Off	On	On	On
Current consumption	<1 µA	10 µA (typical)	See *Specifications*	See *Specifications*

8.4.1.1 Power-Off Mode

In power-off mode the main battery, the battery charger supply, and the USB supply are below their minimum on levels. All internal circuits are disabled as the supply voltage is below the level to activate them. The LP3910 is in power-off mode when the battery voltage is below the battery V_{UVLO} (2.4 V, typical) except when a valid external supply is detected.

8.4.1.2 Standby Mode

When the LP3910 is in standby mode, the chip is waiting for a valid power-on event to transition to active mode. There are 3 valid wake-up signals. First is the ONOFF pin. Second is wall adapter insertion. Third is the USB insertion. V_{BATT} must be greater than the battery V_{UVLO} in order to stay in standby mode; otherwise, the chip transitions to power-off mode. Standby mode is skipped when advancing from power-off mode when a battery is inserted that is above the battery low alarm threshold.

If the battery is below the battery low alarm threshold, power-off mode transitions to standby mode. However, hot insertion of the battery with the adapter connected is NOT permitted. In standby mode, the current consumption is reduced to I_Q (10 µA, typical).

8.4.1.3 Active Mode

All LP3910 circuits are fully operational in active mode.

8.4.2 Mode Sequencing

8.4.2.1 Power-On, Power-Off Sequencing

Each DC-DC converter (Buck1, Buck2, Buck-Boost, LDO1, LDO2) and the NRST pin of the LP3910 has its own delay after which it is enabled following a power-on event or disabled following a power-off event. Following the deglitching of the power-on event, the system bandgaps are enabled. Following this is a 5 ms delay that internal circuitry requires to cleanly power up. The programmable delays are measured from this time point. Following the deglitching of a power-down event (up to 5 ms if POWERACK pin is used), the power-down sequencer starts. Each delay ranges from 0 ms to 63 ms in steps of 1 ms and is factory programmed to the desired values submitted by the system designer. As shown in Figure 66, the power-on or power-off sequencing is designed around a 6-bit up or down timer that is clocked at 1 kHz. A power-on or power-off event triggers the timer, which counts up from 0 during a power-on sequence and counts down from 5'b11111 during a power-down cycle. The timer output is connected to 5 comparators with factory-programmed timeout values that correspond to the on and off delays for each DC-DC converter and the NRST pin. Once the timer has incremented beyond the comparator timeout value during a power-on cycle, the output of the comparator enables the corresponding DC-DC converter or raises the NRST pin to a logic high level. Subsequently, once the timer has decremented below the comparator timeout value during a power-down cycle, the output of the comparator disables the corresponding DC-DC converter or activates the NRST pin to a logic low level.

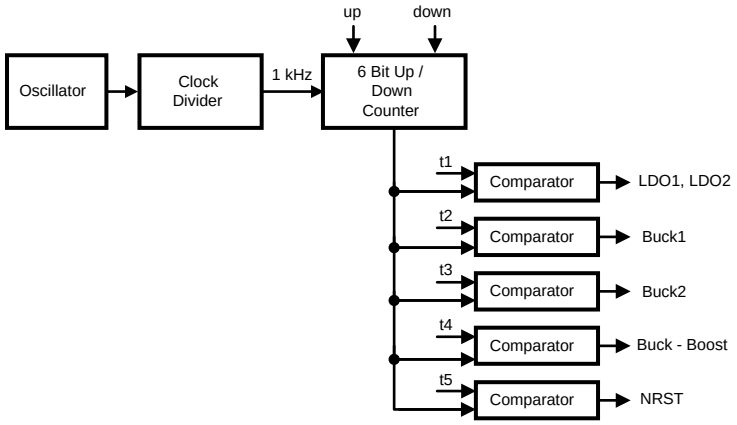


Figure 66. Power Sequencer Block Diagram

8.4.2.2 Power-On Timing

Each timeout T1 thru to T5 are factory programmed from 0 ms to 63 ms. The power-on defaults are shown in Table 9.

Table 9. Power-On Timing Defaults

SYMBOL	DESCRIPTION	TIME (STANDARD OPTIONS)	TIME (AP OPTION)	UNIT
T1	Delay for LDO1 and LDO2	5	6	ms
T2	Delay to Buck1	15	3	ms
T3	Delay for Buck2	20	1	ms
T4	Delay for Buck-Boost	25	0	ms
T5	Delay for NRST	60	10	ms

8.4.2.3 Power-Off Timing

The timing delays during a power-off sequence are equal to 63 ms minus the timing delay during the power on sequence (see Table 10).

Table 10. Power-Off Timing Defaults

SYMBOL	DESCRIPTION	TIME (STANDARD OPTIONS)	TIME (AP option)	UNIT
T1	Delay for LDO1 and LDO2	58	10	ms
T2	Delay to Buck1	48	10	ms
T3	Delay for Buck2	43	10	ms
T4	Delay for Buck-Boost	38	10	ms
T5	Delay for NRST	3	3	ms

8.4.2.4 Transitioning From Standby to Active Mode (Power Up) Battery Power Present Only

When only battery power is present and the battery voltage $V_{BATT} > V_{BATTLOW}$, the LP3910 is waiting for one of three valid wakeup signals. The first is the ONOFF pin. The second and third wakeups are the wall adapter and USBPWR. The ONOFF pin is a factory-programmable wakeup source. It can be a rising edge, a falling edge, a level high, or a level low event. Regardless of the mode, the signal requires a 32-ms deglitch time. A deglitched version of the ONOFF pin is output on the open-drain output pin ONSTAT. ONOFF is usually connected to a push button. Asserting the ONOFF pin starts the power-on sequencer. This enables the DC-DC converters, including the Buck1 DC-DC converter that supplies power to the system processor. The system processor then must set bit D4 (PACK bit) in the power-on event register through the I^2C interface or apply a logic high to the POWERACK pin to keep the device in the Active mode. These serve as power acknowledgment, confirming the power-on request initiated by the ONOFF pin. If neither the PACK bit (D4) in the PON register or the POWERACK pin is set within 128 ms (maximum) of the start of the power-up sequencer, the LP3910 is automatically turned off, as the system has failed to acknowledge the power-on request. Connecting the battery is considered a power-on event. However, hot insertion of the battery with the adapter connected is NOT permitted.

8.4.2.5 Transitioning From Active Mode to Standby Mode

8.4.2.5.1 External Event Triggers the Transition From Active to Standby Mode

When the device is active, a subsequent re-assertion of the push button turns off the LP3910 indirectly by first flagging the system processor though the ONSTAT pin. Upon detecting the ONSTAT transition, the system processor must clear bit D4 (PACK) in the power on event register and apply a logic low to the POWERACK pin to power down the LP3910, which then transitions to Standby Mode. Clearing the PACK register bit and POWERACK pin while external supply sources are present (either USB or CHG_IN) does *not* power down the LP3910, to keep the charger active. The system can as always disable all necessary DC-DC converters, except Buck1, through the register control.

When external power is disconnected, LP3910 remains in its active state unless the battery voltage is below V_{BLA} (battery low alarm) or unless the PACK (either bit D4 in the PON register and the POWERACK pin) is cleared by the system processor.

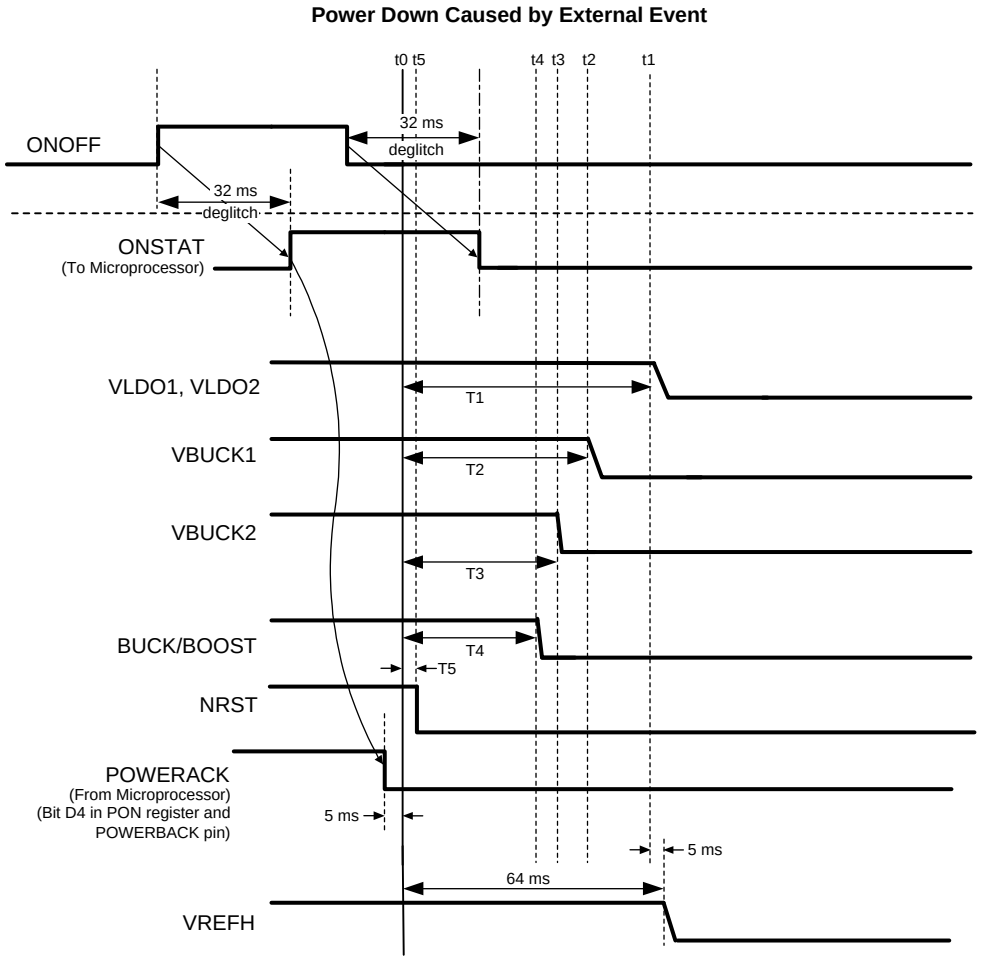


Figure 67. Power-Down Event Caused by External Event

8.4.2.5.2 Transition From Active to Standby Mode Due to Expiring POWERACK Deadline

With no external charger present when the system processor fails to acknowledge the power-on in time by setting either the PACK bit (D4) in the PON register or the POWERACK pin before the 128-ms deadline following the start of the power-up sequencer, then the NRST is immediately de-asserted and after 2 ms all power sources are disabled before transitioning to Standby Mode. This 2-ms delay allows the microprocessor to receive a clean reset before the power is de-asserted. A new power-on event is then required to transition back to active mode.

With either external charger present when the system processor fails to acknowledge the power-on in time by setting either the PACK bit (D4) in the PON register or the POWERACK pin before the 128-ms deadline following the start of the power-up sequencer, the NRST is immediately de-asserted; after 2 ms all power sources are disabled before transitioning to charger standby mode.

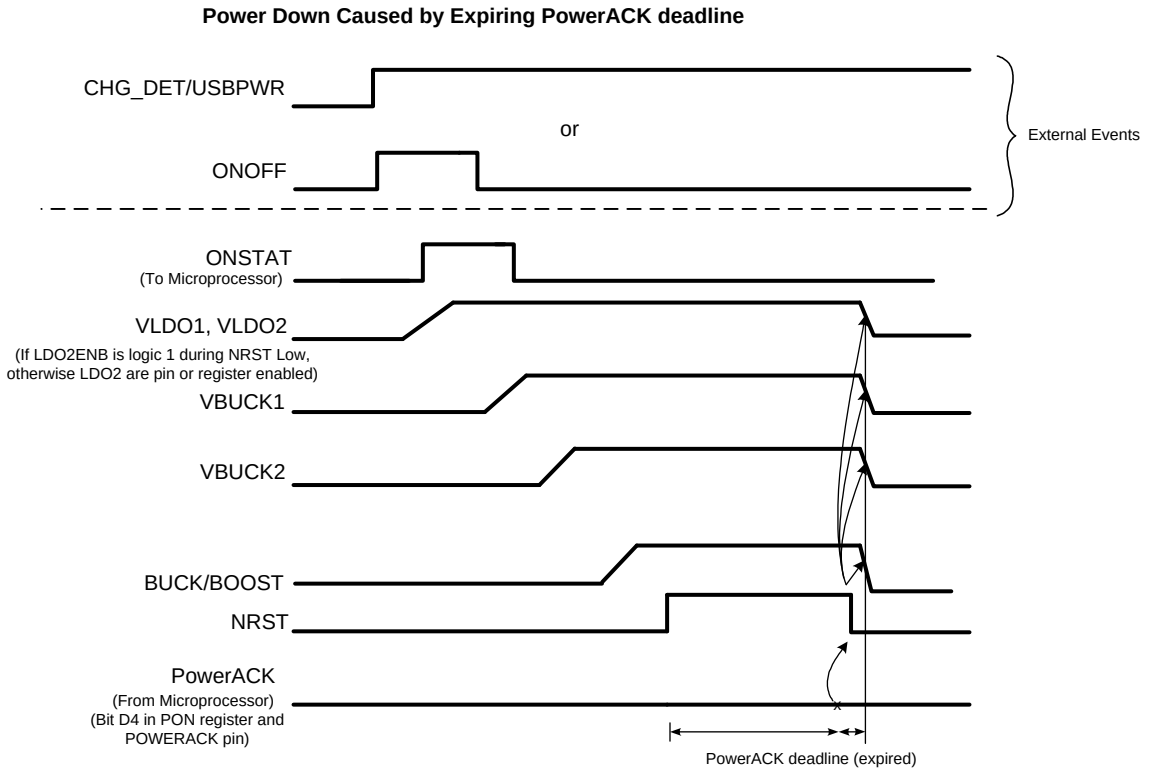


Figure 68. Power Down Caused by Expiring PowerACK Deadline

8.4.2.5.3 Transition From Charger Standby Mode to Either Active or Standby Mode

While in charger standby mode, the battery is charged using the default values of I_{PROG}, EOC, V_{TERM}, battery temperature range, and USB I_{SEL}. In charger standby mode, all the regulators and the I^2C are disabled. A new power-on event is required to transition back to active mode. Removing the charger during charger standby mode causes a transition back to standby mode.

8.5 Programming

8.5.1 I²C-Compatible Serial Interface

8.5.1.1 I²C Signals

The LP3910 features an I²C-compatible serial interface, using two dedicated pins: I²C_SCL and I²C_SDA for I²C clock and data, respectively. Both signals need a pullup resistor according to the I²C specification. The LP3910 interface is an I²C slave that is clocked by the incoming SCL clock.

Signal timing specifications are according to the I²C bus specification. The maximum bit rate is 400 kbit/s. See I²C specification from NXP for further details.

8.5.1.2 I²C Data Validity

The data on I²C_SDA line must be stable during the HIGH period of the clock signal (I²C_SCL); that is, the state of the data line can only be changed when CLK is LOW.

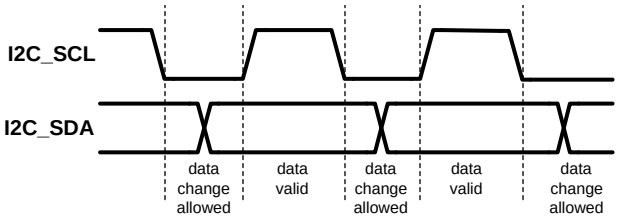


Figure 69. I²C Data Valid Diagram

8.5.1.3 I²C Start and Stop Conditions

START and STOP bits classify the beginning and the end of the I²C session. The START condition is defined the as the I²C_SDA signal transitioning from HIGH to LOW while SCL line is HIGH. The STOP condition is defined as the SDA transitioning from LOW to HIGH while I²C_SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

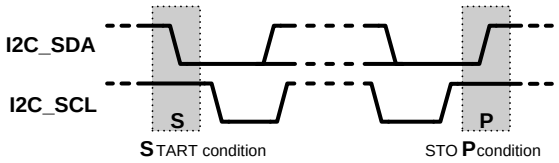


Figure 70. Start and Stop Conditions

8.5.1.4 Transferring Data

Every byte put on the I²C_SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledged related clock pulse is generated by the master. The transmitter releases the I²C_SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the I²C_SDA line during the 9th clock pulse, signifying acknowledgement. A receiver which has been addressed must generate an acknowledgement (ACK) after each byte has been received.

8.5.1.5 Register Write Cycle

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data that is written to the selected register.

LP3910 has a chip address of 60'h, which is set by a metal mask option.

Programming (continued)

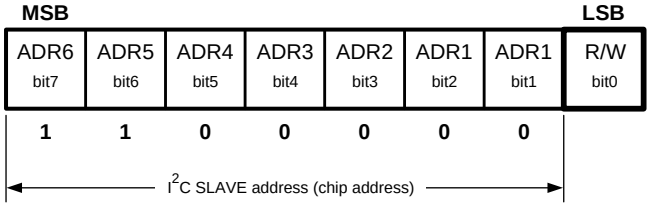
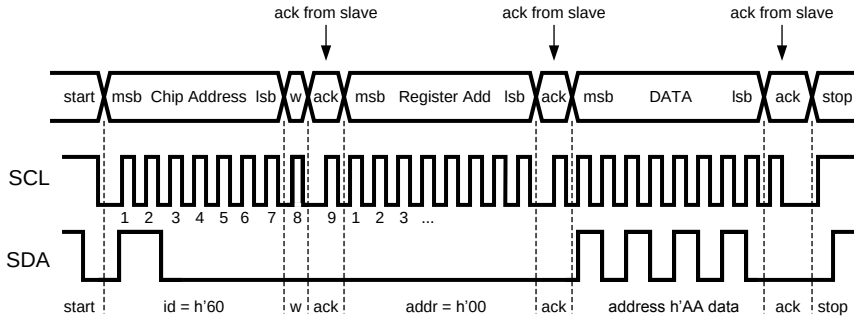


Figure 71. I²C Chip Address



w = write (I²C_SDA = 0)
r = read (I²C_SDA = 1)
ack = acknowledge (I²C_SDA pulled down by either master or slave)
rs = repeated start
id = LP3910 chip address: 60'h

Figure 72. I²C Write Cycle

8.5.1.6 Register Read Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown Figure 73.

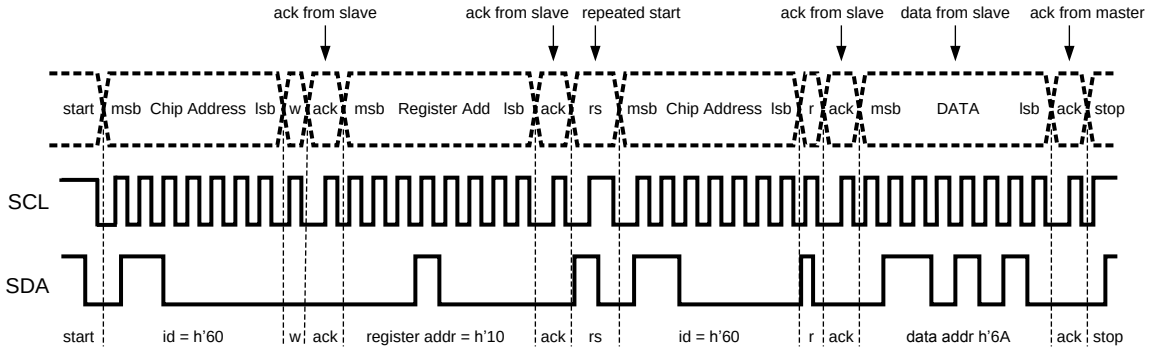


Figure 73. I²C Read Cycle

8.5.1.7 Multi-Byte I²C Command Sequence

The I²C serial interface of the LP3910 device supports random register multi-byte command sequencing: during a multi-byte write the Master sends the Start command followed by the device address, which is sent only once, followed by the 8-bit register address, then 8 bits of data, The I²C slave must then accept the next random register address followed by 8 bits of data and continue this process until the master sends a valid stop condition.

Programming (continued)

A typical multi-byte random register transfer is: Device Address, Register A Address, Ack, Register A Data, Ack Register M Address, Ack, Register M Data, Ack Register X Address, Ack, Register X Data, Ack Register Z Address, Ack, Register Z Data, Ack, Stop

NOTE

The PMIC is not required to detect the I^2C device address for each transaction. A, M, X, and Z are random numbers.

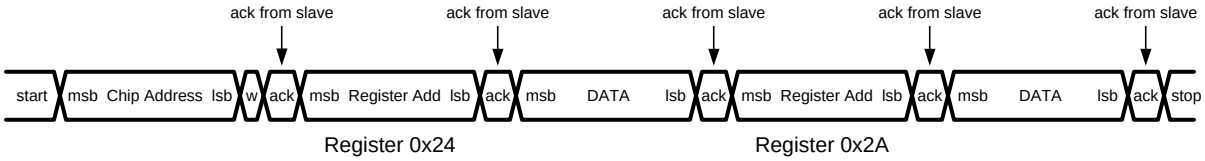


Figure 74. Example Multi-Byte Command Sequencing

8.6 Register Maps

8.6.1 LDO1 Control Register

LDO1 can be configured through its own I^2C control register. The output voltage is programmable in steps of 100 mV from 1.2 V to 3.3 V. LDO1 gets enabled during the power-on sequence. Disable/enable control is provided through bit D5 in the LDO1 control register after selecting the appropriate D4–0 settings, which determine the output voltage.

The output voltage can be altered while LDO1 is enabled. When LDO1 is disabled, it shunts the output to AGND with a R_{SHUNT} = 200 Ω (maximum).

8.6.2 BATTLOW Register (04)H Battery Low Alarm Register

	D7–5	D4–0		
Access	Read Only 0	R/W		
Data	**Reserved**	**Battery low threshold voltage (V)**		**Battery low IRQ threshold voltage (V)**
		5'h14–1F	2.50	2.70
		5'h13	2.55	2.75
		5'h12	2.60	2.80
		5'h11	2.65	2.85
		5'h10	2.70	2.90
		5'h0F	2.75	2.95
		5'h0E	2.80	3.00
		5'h0D	2.85	3.05
		5'h0C	2.90	3.10
		5'h0B	2.95	3.15
		5'h0A	3.00	3.20
		5'h09	3.05	3.25
		5'h08	3.10	3.30
		5'h07	3.15	3.35
		5'h06	3.20	3.40
		5'h05	3.25	3.45
		5'h04	3.30	3.50
		5'h03	3.35	3.55
		5'h02	3.40	3.60
		5'h01	3.45	3.65
		5'h00	3.50	3.70
Reset Standard Default "AP" Default	**n/a**	5'h0C 5'h1F	2.90 2.70	3.10 2.70

8.6.3 PON Register (00)H Power-On Event Register

	D7–5	D4	D3	D2	D1	D0
Access	Read Only 0	R/W	Read Only			
Data	**Reserved**	**PACK**	**Battery Insert**	**PON by ONOFF**	**PON by CHG_IN**	**PON by USB Power**
		0: Disable Power, go in standby, and wait for power on event.	0: default	0: default	0: default	0: default
		1: Acknowledge Power On request	1: Battery Insert caused by Battery Insertion	1: ONOFF caused Power On event	1: Power On caused by CHG_IN power detection	1: Power On caused by USB power detection
Reset	**n/a**	0	0	0	0	0

8.6.4 CHCTL Register (01)H Charger Control Register

	D7–6	D5–2	D1	D0
Access	R/W			
Data	**Termination voltage**	**I_{CC}: Full Rate Charge current**	**Charger enable**	**End of Charge Select**
	00: 4.1V (Li Ion) 01: 4.2V (Li Polymer) 10: 4.38V (Li Polymer) 11: reserved	0000: 100 mA 0001: 200 mA 0010: 300 mA 0011: 400 mA 0100: 500 mA 0101: 600 mA 0110: 700 mA 0111: 800 mA 1000: 900 mA 1001: 1000 mA	0: disabled 1: enabled	0: 5% 1: 10%
Reset	01	Factory-Programmed Default	1	1

8.6.5 CHSPV Register (02)H Charger Supervisor Register

	D7–6	D5	D4	D3	D2–0			
Access	Read only	R/W	R/W	R/W				
Data	**Reserved**	**LED Current**	**LED ENABLE** 0: Disabled 1:Enabled	**Battery temperature range**	**Charger status**			
		0: 5 mA (Standard default) 0: 1 mA (AP default)		0: 0°C–50°C	**Stat2**	**Stat1**	**Stat0**	
		1: 10 mA (Standard default) 1: 2 mA (AP default)		1: 0°C–45°C	0	0	0	Charger is off
					0	0	1	Prequalification
					0	1	0	Constant current charging
					0	1	1	Constant voltage charging
					1	0	0	Error
					1	0	1	Charge cycle complete
					1	1	0	Safety Timer Expired
					1	1	1	EOC / Top-off
Reset	n/a	1	1	0	2'b000			

8.6.6 I_{LIMIT} Register (03)H Current Limit Register

	D7–2	D1–0
Access	Read only 0	
Data	**Reserved**	**USB Current Limit**
		00: controlled by USB_{ISEL} pin [low = 100 mA, high = 500 mA] 01: 100 mA 10: 500 mA 11: 800 mA
Reset	n/a	2'b00

8.6.7 ADCC Register (0a)H ADC Control Register

	D7	D6	D5	D4	D3	D2	D1–0
Access	R/W	R/W	Read Only		R/W	R/W	
Data	V_{RANGE}	I_{RANGE}	**ADC Overflow**	**Data Ready**	**Start Conversion**	**ADC Enable**	**ADC source selection**
	0: 2.6 V – 3.5 V	0: 0 mA – 605 mA	0: no overflow	0: no data	0: default	0: Disabled	00: battery voltage
	1: 2.6 V – 4.4 V	1: 0 mA – 1100 mA	1: overflow	1: data ready	1: start conversion	1: Enabled	01: battery charge current
							10: ADC1
							11: ADC2
Reset	0	0	0	0	0	0	0

8.6.8 ADCD Register (0b)H ADC Output Data Register

Charge current 0 A to 1.1 A mirrored to 0 µA to 250 µA, ADC measures voltage drop across R_{SENSE} 4.64 kΩ.

	D7–0		
Access	Read Only 0		
Data	Battery voltage:	8'h00 = 2.6V	8'hFF = 3.5V 1 LSB = 0.9 / 256 = (3.5 mV) range 0
		8'h00= 2.6V	8'hFF = 4.4 V 1 LSB = 1.8 / 256 = (7.0 mV) range 1
	Battery charge current	8'h00 = 0	8'hFF = 0.6463 V = 605 mA range 0
		8'h00 = 0	8'hFF = 1.175V = 1100 mA range 1
	ADC1: 8'h00 = V_{REFH} = 1.225V	8'hFF = 2*V_{REFH} = 2.45 V	(1 LSB = V_{REFH}/256)
	ADC2: 8'h00 = V_{REFH} = 1.225V	8'hFF = 2*V_{REFH} = 2.45 V	(1 LSB = V_{REFH}/256)
Reset	8'h00		

8.6.9 IMR Register (0c)H Interrupt Mask Register

	D7–0
Access	r/w
Data	1: Enable INTn (n=0…7) to pull IRQB low 0: Mask Interrupt source INTn
Reset	8'h00

8.6.10 IRQ Register (0d)H Interrupt Request Register

	D7–0
Access	Read only
Data	1: Interrupt IRQn (n=0…7) requested 0: No interrupt requested
Reset	8'h00

8.6.11 LDO1 Control Register (08)H

	D7–6	D5	D4–0	
Access	Read Only 0	R/W		
Data	**Reserved**	**Operation** 0: disable 1: enable	**LDO1 Output Voltage (V)**	
			5'h00	1.2
			5'h01	1.3
			5'h02	1.4
			5'h03	1.5
			5'h04	1.6
			5'h05	1.7
			5'h06	1.8
			5'h07	1.9
			5'h08	2.0
			5'h09	2.1
			5'h0A	2.2
			5'h0B	2.3
			5'h0C	2.4
			5'h0D	2.5
			5'h0E	2.6
			5'h0F	2.7
			5'h10	2.8
			5'h11	2.9
			5'h12	3.0
			5'h13	3.1
			5'h14	3.2
			5'h15 –5'h1F	3.3
Reset	n/a	1	Factory-Programmed Default	

8.6.12 LDO2 Control Register

LDO2 can be configured through its own I^2C control register. The output voltage is programmable in steps of 100 mV from 1.3 V to 3.3 V. LDO2 is by default disabled and can be enabled by setting bit D5 in the control register after selecting the appropriate D4–0 settings, which determine the output voltage. LDO2 can also be enabled through the external LDO2EN pin, which is the default enable control. With a logic 0 programmed to bit D5 in the corresponding control register, enable/disable control is passed onto the LDO2EN pin; a logic 1 applied to this pin enables LDO2 while a logic 0 disables the LDO2. Setting D5 to 1 in the LDO2 control register enables LDO2, regardless of the state of the LDO2EN pin. If the system designer permanently connects the LDO2EN pin to GND, then D5 is simply a enable/disable control bit. If the system design permanently connects the LDO2EN pin to V_{DD}, the LDO is enabled during the power-on sequence and is always on, regardless of the state of bit D5 in the LDO2 control register. In that particular case, the LDO2 is sequenced with the same timing as LDO1 (see *Power-On, Power-Off Sequencing*).

The output voltage can be altered while LDO2 is enabled. When LDO2 is disabled, it shunts the output to AGND with a R_{SHUNT} = 200 Ω (maximum).

Table 11. LDO2 Control Register (09)H

	D7–6	D5	D4–0	
Access	Read Only 0	R/W		
Data	**Reserved**	**Operation** 0: enable/ disable determined by state of LDO2EN pin 1: enable, override LDO2EN state	**LDO1 Output Voltage (V)**	
			5'h00	1.3
			5'h01	1.4
			5'h02	1.5
			5'h03	1.6
			5'h04	1.7
			5'h05	1.8
			5'h06	1.9
			5'h07	2
			5'h08	2.1
			5'h09	2.2
			5'h0A	2.3
			5'h0B	2.4
			5'h0C	2.5
			5'h0D	2.6
			5'h0E	2.7
			5'h0F	2.8
			5'h10	2.9
			5'h11	3
			5'h12	3.1
			5'h13	3.2
			5'h14 –5'h1F	3.3
Reset	n/a	0	Factory-Programmed Default	

8.6.13 Buck1, Buck2 Control Registers and BUCK1EN Pin

Buck1 and Buck2 are configurable through I^2C accessible registers. Bit fields D4–0 control the output voltage. Bit D5 defines the Modulation mode of the buck, which by default automatically selects PWM or PFM mode depending on the load as described above in the functional description. The modulation mode can be forced to PWM mode regardless of the load by setting bit D5 to a logic 1 in the corresponding buck control register.

Bit D6 controls the enable/disable state of the buck, which is different for Buck1 and Buck2 as Buck1 has an external enable pin: BUCK1EN.

For Buck1, by default or when D6 is programmed logic 0 in the Buck1 control register, enable/disable control is passed onto the BUCK1EN pin. A logic 1 applied to this pin enables Buck1 while a logic 0 disables Buck1. Setting D6 to 1 in the Buck1 control register enables BUCK1, regardless of the state of the BUCK1EN pin. If the system designer permanently connects the BUCK1EN pin to GND, then D6 is simply a enable/disable control bit. If the system design permanently connects the enable pin to V_{DD}, then the Buck1 is enabled during the power-on sequence and is always be on, regardless of the state of bit D6 in the Buck1 control register (see *Power-On, Power-Off Sequencing*).

BUCK2 is by default enabled during the power-on sequence and can be enabled/disabled through bit D6 in the Buck2 control register.

Table 12. Buck1 Control Register (05)H

	D7	D6	D5	D4–0	
Access	Read Only 0	R/W			
Data	**Reserved**	**Operation** 0: enable/disable determined by state of BUCK1EN pin 1: enable, override BUCK1EN state	**Force PWM mode** 0: Automatic Modulation Mode 1: Force PWM mode	**BUCK1 Output Voltage (V)**	
				5'h00	Externally controlled
				5'h01	0.80
				5'h02	0.85
				5'h03	0.90
				5'h04	0.95
				5'h05	1.00
				5'h06	1.05
				5'h07	1.10
				5'h08	1.15
				5'h09	1.20
				5'h0A	1.25
				5'h0B	1.30
				5'h0C	1.35
				5'h0D	1.40
				5'h0E	1.45
				5'h0F	1.50
				5'h10	1.55
				5'h11	1.60
				5'h12	1.65
				5'h13	1.70
				5'h14	1.75
				5'h15	1.80
				5'h16	1.85
				5'h17	1.90
				5'h18	1.95
				5'h19–1F	2.00
Reset	n/a	0	0	Factory-Programmed Default	

Table 13. Buck2 Control Register (06)H

	D7	D6	D5	D4–0	
Access	Read Only 0	R/W			
Data	**Reserved**	**Operation** 0: disabled 1: enabled	**Force PWM mode** 0: Automatic Modulation Mode 1: Force PWM mode	**BUCK2 Output Voltage (V)**	
				5'h00	Externally controlled
				5'h01	1.80
				5'h02	1.90
				5'h03	2.00
				5'h04	2.10
				5'h05	2.20
				5'h06	2.30
				5'h07	2.40
				5'h08	2.50
				5'h09	2.60
				5'h0A	2.70
				5'h0B	2.80
				5'h0C	2.90
				5'h0D	3.00
				5'h0E	3.10
				5'h0F	3.20
				5'h1x	3.30
Reset	n/a	1	0	Factory-Programmed Default	

8.6.14 Buck-Boost Control Register

The buck-boost is controlled through its dedicated control register. The buck-boost is enabled through the power-on sequencing. The system processor is required to select the desired buck-boost output voltage through bits D4–0 before enabling it by setting bit D6 in the control register. The buck-boost is also disabled when b'00000 is programmed in the register field D4–0, regardless of the state of the bit D6. When the buck-boost is disabled, its output is internally tied low through a 1-MΩ resistor. If D4–0 is set to b'00000 the 1 MΩ resistor is disconnected. The default output voltage for the buck-boost is factory programmable.

Table 14. Buck–Boost Control Register (07)H

	D7	D6	D5	D4–0	
Access	Read Only 0	R/W			
Data	**Reserved**	**Force PWM** 0: Automatic modulation mode 1: Force PWM modulation	**Operation** 0: disable 1: enable	**Buck–Boost Output Voltage (V)**	
				5'h00	disabled
				5'h01	1.80
				5'h02	1.85
				5'h03	1.90
				5'h04	1.95
				5'h05	2.00
				5'h06	2.05
				5'h07	2.10
				5'h08	2.15
				5'h09	2.20
				5'h0A	2.25
				5'h0B	2.30
				5'h0C	2.35
				5'h0D	2.40
				5'h0E	2.45
				5'h0F	2.50
				5'h10	2.55
				5'h11	2.60
				5'h12	2.65
				5'h13	2.70
				5'h14	2.75
				5'h15	2.80
				5'h16	2.85
				5'h17	2.90
				5'h18	2.95
				5'h19	3.00
				5'h1A	3.05
				5'h1B	3.10
				5'h1C	3.15
				5'h1D	3.20
				5'h1E	3.25
				5'h1F	3.30
Reset	n/a	0	1	Factory-Programmed Default	

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP3910 is a programmable system power management unit optimized for HDD-based portable media players. The device is intended to connect to an AC-DC wall adapter or USB power source in addition to a lithium-Ion or lithium-polymer single-cell battery. The device can be configured over an I^2C interface, or the default configuration stored in EPROM can be used. Additional features such as current and voltage measurements with the ADC or battery thermal monitoring can also be controlled via the I^2C interface and interrupt pins.

9.2 Typical Application

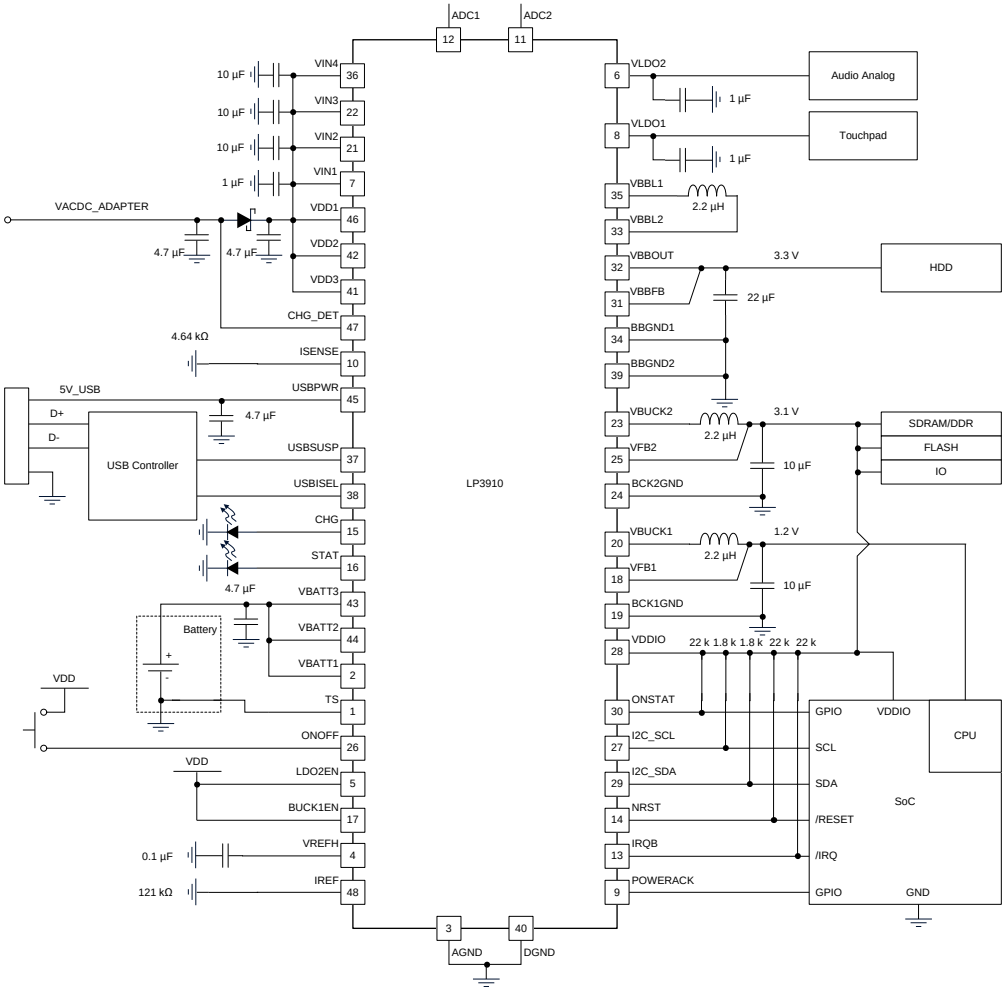


Figure 75. LP3910 Typical Application

Typical Application (continued)

9.2.1 Design Requirements

For typical PMU applications, use the parameters listed in Table 15.

Table 15. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.7 V
Maximum input voltage	5.5 V
LDO1 output voltage	2.5 V
LDO2 output voltage	3 V
Buck1 output voltage	1.6 V
Buck2 output voltage	1.8 V
Buck-Boost output voltage	3.3 V
Charge current	100 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inductors for Buck1, Buck2 and Buck-Boost

There are two main considerations when choosing an inductor; the inductor must not saturate and the inductor current ripple is small enough to achieve the desired output voltage ripple. Care must be taken when reviewing the different saturation current ratings that are specified by different manufacturers.

Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application must be requested from the manufacturer.

There are two methods to choose the inductor saturation current rating:

9.2.2.1.1 Method 1

The saturation current is greater than the sum of the maximum load current and the worst-case average-to-peak inductor current. This can be written as Equation 4:

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where} \quad I_{RIPPLE} = \frac{1}{f} * \left(\frac{V_{IN} - V_{OUT}}{2L} \right) * \left(\frac{V_{OUT}}{V_{IN}} \right) \tag{4}$$

Considered when using the Buck-Boost in boost mode, use Equation 5:

$$I_{SAT} > I_{RIPPLE} + I_{AVE}$$

$$\text{where} \quad I_{RIPPLE} = V_{IN} * \frac{\left(1 - \frac{V_{IN}}{V_{OUT}} \right)}{2Lf}$$

$$I_{AVE} > I_{OUTMAX} * \frac{V_{OUT}}{V_{IN}}$$

where

- I_{RIPPLE}: Average-to-peak inductor current
- I_{OUTMAX}: Maximum load current
- V_{IN}: Maximum input voltage in application
- L: Minimum inductor value including worst case tolerances (30% drop can be considered for Method 1)
- f: Minimum switching frequency
- V_{OUT}: Output voltage

(5)

9.2.2.1.2 Method 2

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the maximum current limit.

INDUCTOR	VALUE	DESCRIPTION	NOTES
L_{SW}1,2	2.2 µH	Buck1,2 Inductor	DCR 70 mΩ
L_{BB}	2.2 µH	Buck-Boost Inductor	DCR 70 mΩ

9.2.2.2 External Capacitors

The regulators on the LP3910 require external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.2.1 LDO Capacitor Selection

9.2.2.2.1.1 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LDO input pin and ground. (This capacitance value may be increased without limit.)

The input capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge currents when connected to a low impedance source of power (such as a battery or a very large capacitor). If a tantalum capacitor is used at the input, it should be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains approximately 1 µF over the entire operating temperature range.

9.2.2.2.1.2 Output Capacitor

The LDOs on the LP3910 are designed specifically to work with very small ceramic output capacitors. A 1-µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 mΩ to 500 mΩ, are suitable in the application circuit.

Tantalum or film capacitors may also be used at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost.

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

9.2.2.2.1.3 Capacitor Characteristics

The LDOs are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LDOs.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection must take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values also show some decrease over time due to aging. The capacitor parameters are also dependent on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 76 shows a typical graph comparing different capacitor case sizes.

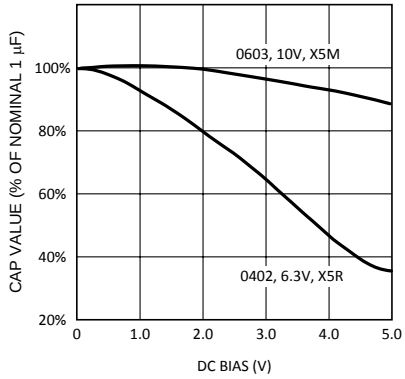


Figure 76. Typical Variation in Capacitance vs DC Bias

As shown in Figure 76, increasing the DC Bias condition can result in the capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that Figure 76 shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (for example, 0402) may not be suitable in the actual application.

Capacitance of a ceramic capacitor can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, only varies the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature changes significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases about 2:1 as the temperature goes from +25°C down to −40°C, so some guard band must be allowed.

9.2.2.2.1.4 Noise Bypass Capacitors for VREFH Pin

Connecting respectively 100 nF and 1 nF grounded bypass capacitors to the V_{REFH} pin significantly reduces noise on the LDO outputs. VREFH is a high-impedance node connected to a bandgap reference used for the LDOs. Any significant loading on this node causes a change on the regulated output voltages. For this reason, DC leakage current through these pins must be kept as low as possible for best output voltage accuracy. The types of capacitors best suited for the noise bypass capacitors are ceramic and film capacitors. High-quality ceramic capacitors with either NPI or COG dielectric typically have very low leakage. Polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current. *Residual solder flux* is another potential source of leakage, which mandates thorough cleaning of the assembled PCBs.

9.2.2.2.2 Buck1, Buck2 and Buck-Boost Capacitor Selection

9.2.2.2.2.1 Input Capacitor Selection for Buck1, Buck2 and Buck-Boost

A ceramic input capacitor of 10 µF, 6.3 V is sufficient for the magnetic DC-DC converters. Place the input capacitor as close as possible to the input of the device. A large value may be used for improved input voltage filtering. The recommended capacitor types are X7R or X5R. Y5V-type capacitors must not be used. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the DC-DC converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. Low ESR in a ceramic capacitor provides the best noise filtering of the input voltage spikes due to fast current transients. A capacitor with sufficient ripple current rating must be selected. The Input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \sqrt{\frac{V_{IN}}{V_{OUT}} \left(1 - \frac{V_{IN}}{V_{OUT}} + \frac{r^2}{12}\right)}$$

$$\text{where} \quad r = \frac{(V_{IN} - V_{OUT}) * V_{OUT})}{L * f * I_{OUTMAX} * V_{IN}} \tag{6}$$

The worse case is when $V_{IN} = 2 \times V_{OUT}$.

9.2.2.2.2.2 Output Capacitor Selection for Buck1, Buck2 and Buck-Boost

A 10-µF, 6.3-V ceramic capacitor must be used on the output of the Buck1 and Buck2 magnetic DC-DC converters. The buck-boost needs a 22-µF capacitor. The output capacitor must be mounted as close as possible to the output of the device. A large value may be used for improved input voltage filtering. The recommended capacitor types are X7R or X5R. Y5V-type capacitors should not be used. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and DC bias curves should be requested from them and analyzed as part of the capacitor selection process.

The output filter capacitor of the magnetic DC-DC converter smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESD to perform these functions.

The output voltage ripple is caused by the charging and the discharging of the output capacitor and also due to its ESR and can be calculated using Equation 7:

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4 * f * C} \tag{7}$$

Voltage peak-to-peak ripple due to ESR can be expressed by Equation 8:

$$V_{PP\text{-}ESR} = 2 \times I_{RIPPLE} \times R_{ESR} \tag{8}$$

Because the $V_{PP\text{-}C}$ and $V_{PP\text{-}ESR}$ are out of phase, the RMS value can be used to get an approximate value of the peak-to-peak ripple:

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2} \tag{9}$$

The output voltage ripple is dependent on the inductor current ripple and the ESR of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent as well as temperature dependent. The R_{ESR} must be calculated with the applicable switching frequency and ambient temperature.

Table 16. Recommended Capacitors

CAPACITOR	MINIMUM VALUE (µF)	DESCRIPTION	RECOMMENDED TYPE
C_{VDD}	4.7	Charger input capacitor	Ceramic, 6.3 V, X5R
C_{CHG_DET}	4.7	Charger input capacitor	Ceramic, 6.3 V, X5R
C_{USB}	4.7	USB power (V_{BUS}) capacitor	Ceramic, 6.3 V, X5R
C_{BATT}	4.7	Li-ion battery capacitor	Ceramic, 6.3 V, X5R
C_{LDO1}	1	LDO output capacitor	Ceramic, 6.3 V, X5R
C_{LDO2}	1	LDO output capacitor	Ceramic, 6.3 V, X5R
C_{VREFH}	0.1	Bypass capacitor for internal voltage reference	Ceramic, PolyPropylene and Polycarbonate Film
$C_{VIN2,3}$	10	Buck1, Buck2 input capacitor	Ceramic, 6.3 V, X5R
CVBUCK1,2	10	BUCK1,2 output capacitor	Ceramic, 6.3 V, X5R
C_{BB}	22	Buck-Boost output capacitor	Ceramic, 6.3 V, X5R
C_{VIN1}	1	LDO bypass capacitor	Ceramic, 6.3 V, X5R
C_{VIN4}	10	Buck and Buck-Boost bypass capacitor	Ceramic, 6.3 V, X5R

9.2.2.3 Schottky Diode on Charger Input CHG_IN

A Schottky diode is required in the external adapter path to block the reverse current from either the USB or the battery source. The most critical parameter in the selection of the right Schottky diode is the leakage current, which must be below 10 µA over the temperature range in order to prevent false detection of the presence of an external adapter. In addition the Schottky diode must have a maximum voltage rating of 10 V or higher. The current rating depends on the current limit of the adapter. The forward voltage must be limited to 500 mV at its maximum current. The recommended Schottky diode is MBRA210ET3 from ON Semiconductor, which has a reverse leakage current under 1 µA at room temperature and a forward voltage drop of 500 mV at the maximum rated current (I_F = 2 A).

9.2.2.4 Resistors

9.2.2.4.1 Battery Thermistor

The LP3910 battery thermistor bias provided by the TS pin is tailored to thermistors with the following specification:

- Negative temperature coefficient
- 100-kΩ resistance

A suitable solution is available from AVX thermistors:

AVXNB21250104 http://www.avxcorp.com/docs/Catalogs/nb21-23.pdf

9.2.2.4.2 I^2C Pullup Resistors

I^2C_SDA and I^2C_SCL pins must have pullup resistors connected to the VDDIO pin. VDDIO must be connected to a power supply that is less than or equal to V_{DD}, such as BUCK2. The values of the pullup resistors (typical approximately 1.8 kΩ) are determined by the capacitance of the bus. A resistor that is too large, combined with a given bus capacitance, results in a rise time that would violate the maximum rise time specification. A resistor that is too small results in a contention with the pulldown transistor on either slave(s) or master.

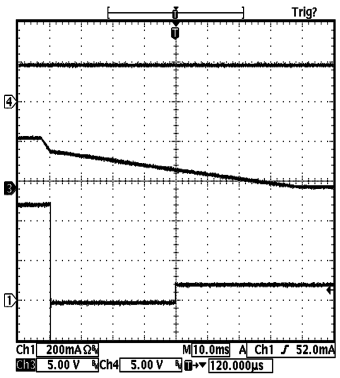
9.2.2.4.3 R_{IREF} Resistor

The current through this resistor is used as a reference current that biases many analog circuits inside the LP3910 and must have a resistance of 121 kΩ ±1%.

9.2.2.4.4 R_{ISENSE} Resistor

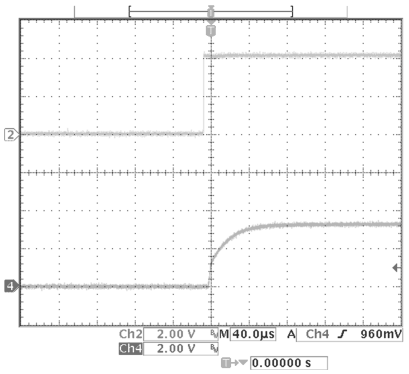
The current through this resistor is used as a reference current for the charge current. The accuracy of the ADC is dependent on the tolerance of this resistor. R_{ISENSE} must have a resistance of 4.64 kΩ ±1% tolerance.

9.2.3 Application Curves



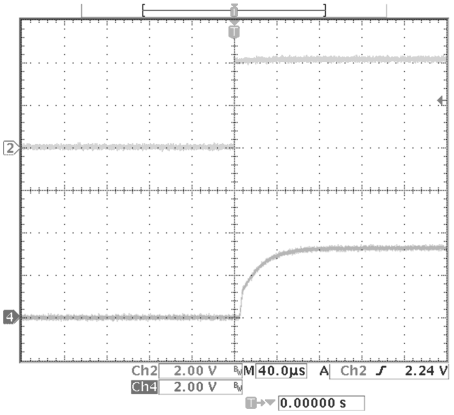
Ch1 = Charge Current (mA) Ch4 = USBPWR (V)
Ch3 = CHG_DET (V)

Figure 77. Wall Adapter Removal With USBPWR Present



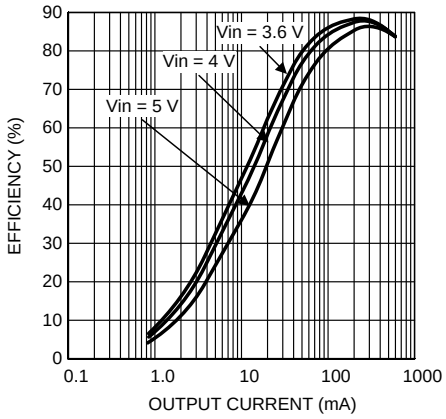
V_{IN} = 0 to 3.6 V V_{OUT} = 3.3 V Load = 1 mA

Figure 78. Enable Startup Time (LDO1)



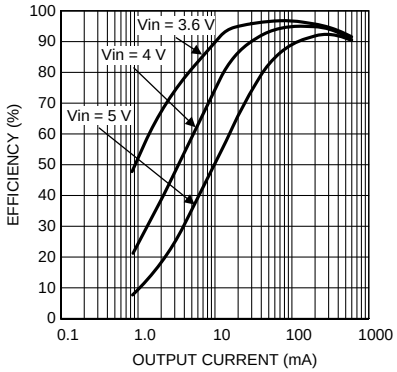
V_{IN} = 0 to 3.6 V V_{OUT} = 1.8 V Load = 1 mA

Figure 79. Enable Start-Up Time (LDO2)



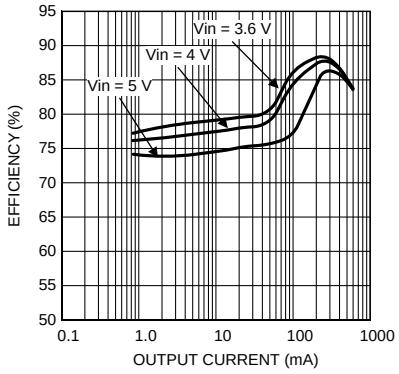
V_{OUT} = 1.8 V L = 2.2 µH Forced PWM Mode

Figure 80. Buck2 Efficiency vs Output Current



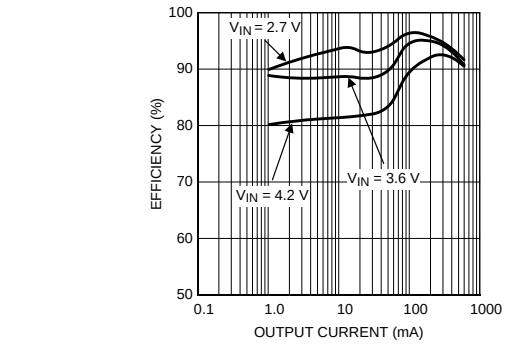
V_{OUT} = 3.3 V L = 2.2 µH Forced PWM Mode

Figure 81. Buck2 Efficiency vs Output Current



V_{OUT} = 1.8 V L = 2.2 µH PFM-to-PWM Mode

Figure 82. Buck2 Efficiency vs Output Current



V_{OUT} = 3.3 V L = 2.2 µH PFM-to-PWM Mode

Figure 83. Buck2 Efficiency vs Output Current

10 Power Supply Recommendations

The LP3910 is designed to use a standard single-cell lithium-ion or lithium-polymer battery. Battery voltage maximum operating voltage can be up to 4.5 V. The LP3910 can also use an AC-DC wall adapter as a charging source up to 6 V or a USB source of at least 4.25 V. The USB charging source must supply charging currents of 100 mA, 500 mA, or 800 mA.

11 Layout

11.1 Layout Guidelines

For good performance of the circuit, it is essential to place the input and output capacitors very close to the circuit, using wide routing for the traces to allow high currents. Sensitive components must be placed far from those components with high pulsating current, and decoupling capacitors must be placed close to circuit VIN pins. Digital and analog grounds must be routed separately and connected together in a star connection. It is good practice to minimize high current and switching current paths.

11.1.1 LDO Regulators

Place the filter capacitors very close to the input and output pins. Use large trace width for high current-carrying traces and the returns to ground.

11.1.2 Buck and Buck-Boost Regulators

Place the supply bypass, filter capacitor, and inductor close together, keeping the traces short. The traces between these components carry relatively high switching current and act as antennas. Following these rules reduces radiated noise. Arrange the components so that the switching current loops curl in the same direction.

Connect the buck ground and the ground of the capacitors together using generous component-side copper fill as a pseudo-ground plane. Connect the grounds to the general board system ground plane at a single point. Place the pseudo-ground plane below these components and then have it tied to system ground of the output capacitor outside of the current loops. This prevents the switched current from injecting noise into the system ground. These components, along with the inductor and output, must be placed on the same side of the circuit board, and their connections must be made on the same layer.

Route the noise sensitive traces such as the voltage feedback path away from the inductor. This is done by routing it on the bottom layer or by adding a grounded copper area between switching node and feedback path. Noisy traces between the power components and keep any digital lines away from this section. Keep the feedback node as small as possible so that the ground pin and ground traces shield the feedback node from the SW or buck output.

Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses.

11.2 Layout Example

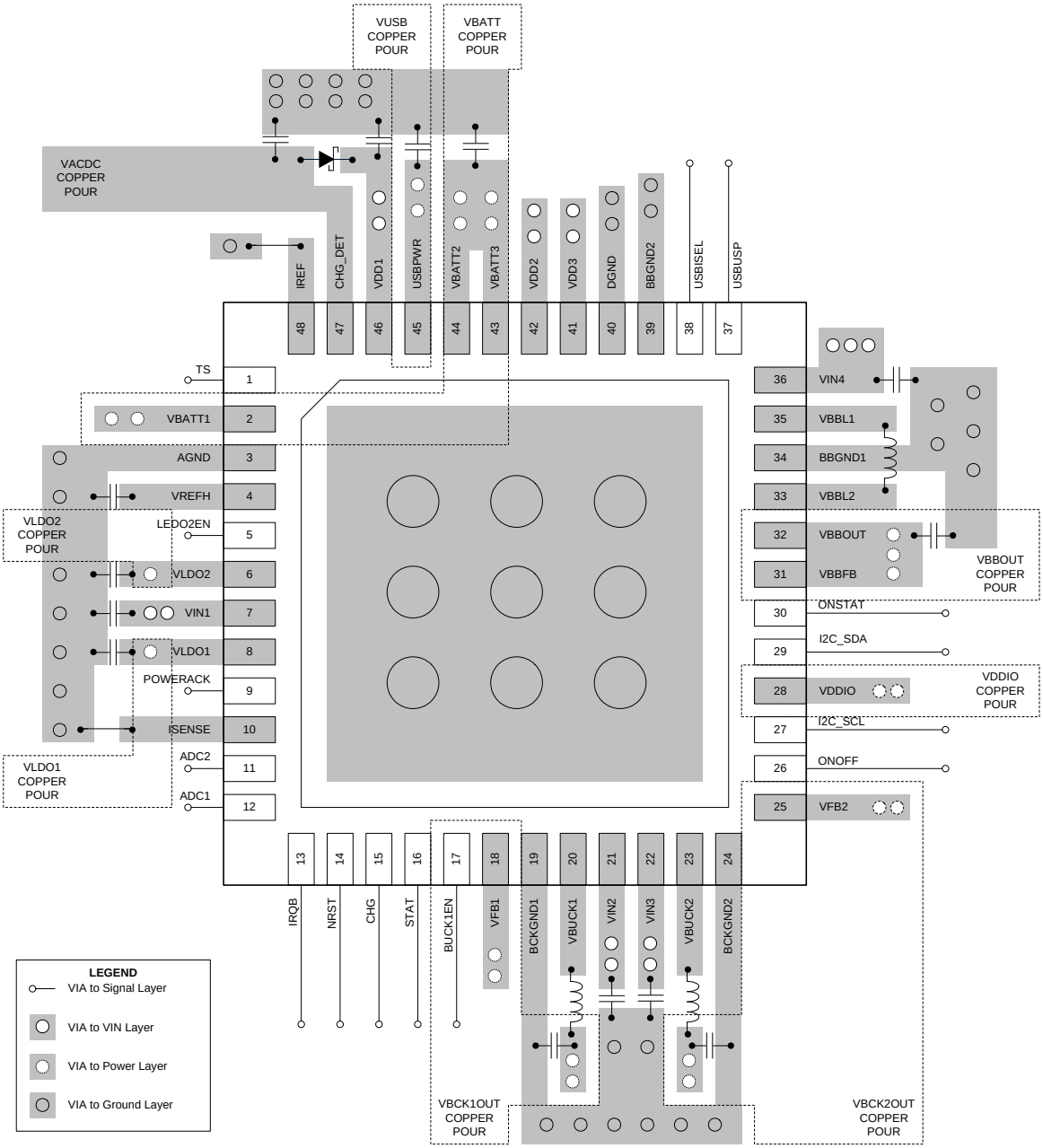


Figure 84. LP3910 Layout Example

11.3 Thermal Performance of the WQFN Package

The LP3910 is a monolithic device with integrated power FETs. For that reason, it is important to pay special attention to the thermal impedance of the WQFN package and to the PCB layout rules in order to maximize power dissipation of the WQFN package.

The WQFN package is designed for enhanced thermal performance and features an exposed die attach pad at the bottom center of the package that creates a direct path to the PCB for maximum power dissipation. Compared to the traditional leaded packages where the die attach pad is embedded inside the molding compound, the WQFN reduces one layer in the thermal path.

The thermal advantage of the WQFN package is fully realized only when the exposed die-attach pad is soldered down to a thermal land on the PCB board with thermal vias planted underneath the thermal land. Based on thermal analysis of the WQFN package, the junction-to-ambient thermal resistance ($R_{\theta JA}$) can be improved by a factor of two when the die attach pad of the WQFN package is soldered directly onto the PCB with thermal land and thermal vias, as opposed to an alternative with no direct soldering to a thermal land. Typical pitch and outer diameter for thermal vias are 1.27 mm and 0.33 mm, respectively. Typical copper via barrel plating is 1 oz., although thicker copper may be used to further improve thermal performance. The LP3910 die attach pad is connected to the substrate of the device and therefore, the thermal land and vias on the PCB board need to be connected to ground (GND pin).

For more information on board layout techniques, refer to *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401). This application note also discusses package handling, solder stencil, and the assembly process.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For additional information, see the following:

AN1187 Leadless Leadframe Package (LLP) (SNOA401)

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3910SQ-AK/NOPB	ACTIVE	WQFN	NJV	48	250	RoHS & Green	SN	Level-1-260C-UNLIM		L3910-AK	Samples
LP3910SQ-AN/NOPB	ACTIVE	WQFN	NJV	48	250	RoHS & Green	SN	Level-1-260C-UNLIM		L3910-AN	Samples
LP3910SQX-AA/NOPB	ACTIVE	WQFN	NJV	48	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L3910-AA	Samples
LP3910SQX-AN/NOPB	ACTIVE	WQFN	NJV	48	2500	RoHS & Green	SN	Level-1-260C-UNLIM		L3910-AN	Samples
LP3910SQX-AP/NOPB	ACTIVE	WQFN	NJV	48	2500	RoHS & Green	SN	Level-1-260C-UNLIM		3910-AP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

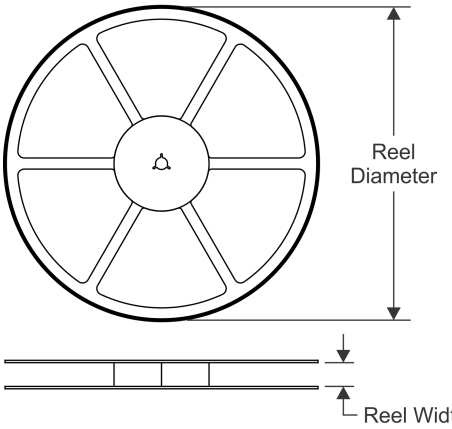
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

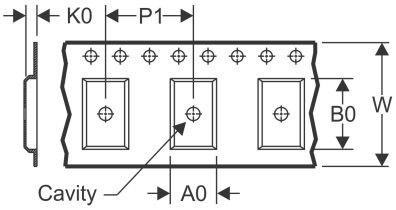
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

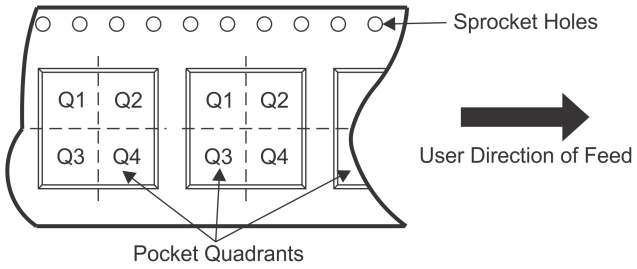


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

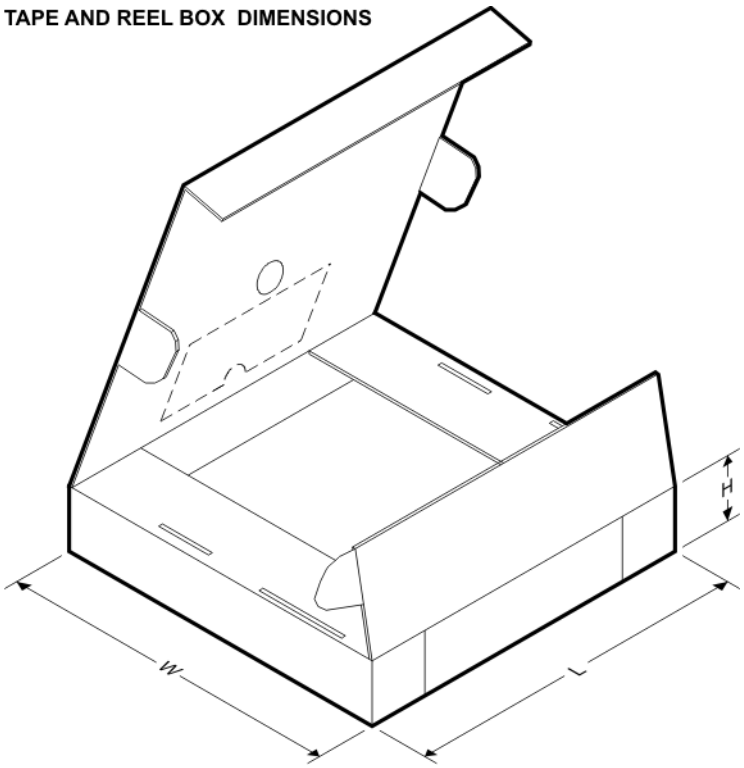
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3910SQ-AK/NOPB	WQFN	NJV	48	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LP3910SQ-AN/NOPB	WQFN	NJV	48	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LP3910SQX-AA/NOPB	WQFN	NJV	48	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LP3910SQX-AN/NOPB	WQFN	NJV	48	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LP3910SQX-AP/NOPB	WQFN	NJV	48	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3910SQ-AK/NOPB	WQFN	NJV	48	250	208.0	191.0	35.0
LP3910SQ-AN/NOPB	WQFN	NJV	48	250	208.0	191.0	35.0
LP3910SQX-AA/NOPB	WQFN	NJV	48	2500	367.0	367.0	35.0
LP3910SQX-AN/NOPB	WQFN	NJV	48	2500	367.0	367.0	35.0
LP3910SQX-AP/NOPB	WQFN	NJV	48	2500	367.0	367.0	35.0

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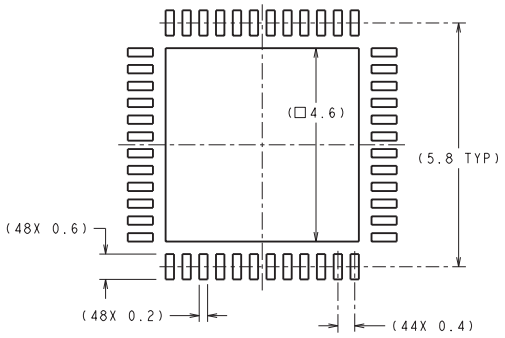
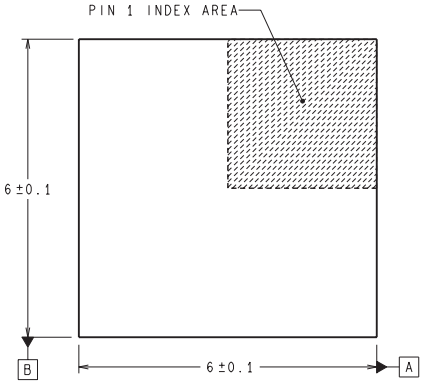
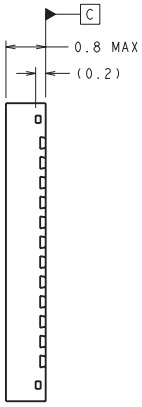
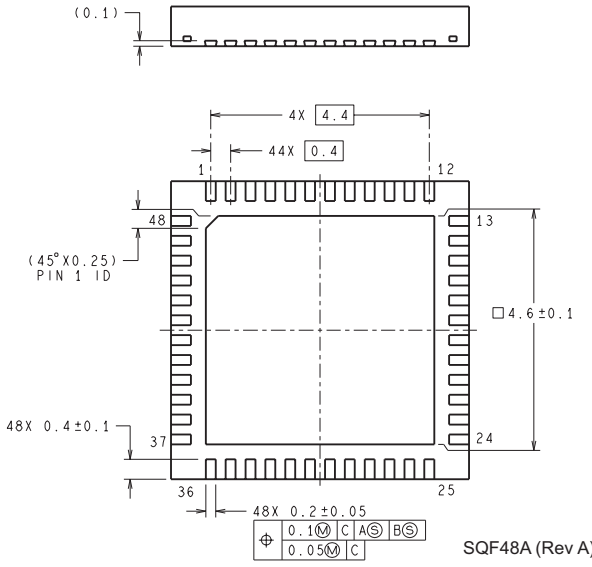


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







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