TPS22968-Q1 5.5V、4A、27mΩ 导通电阻负载开关

1 特性

- 集成双通道负载开关
- 符合汽车应用要求:
  - 器件温度 1 级（工作环境温度范围：-40°C 至 125°C）
- 输入电压范围：0.8V 至 5.5V
- VBIAS 电压范围：2.5V 至 5.5V
- 导通电阻
  - V_{IN} = 5V (V_{BIAS} = 5V) 时，R_{ON} = 29mΩ
  - V_{IN} = 3.3V (V_{BIAS} = 5V) 时，R_{ON} = 27mΩ
  - V_{IN} = 1.8V (V_{BIAS} = 5V) 时，R_{ON} = 26mΩ
- 每通道最大 4A 持续开关电流
- 低静态电流
  - V_{BIAS} = 5V 时为 58μA（双通道）
- 低控制输入阈值支持使用 1.2/1.8/2.5/3.3V 逻辑器件
- 可通过 CT 引脚(1) 配置上升时间
- 快速输出放电 (QOD)(2)
- 10 引脚晶圆级小外形无引线 (WSON) 封装，具有可湿性侧面
- 静电放电 (ESD) 性能经测试符合 JEDEC STD 标准
  - ±2kV 人体模型 (HBM) 和 ±1kV 器件充电模型 (CDM)
- 锁断性能达 100mA，符合 JESD 78 II 类规范的要求
- 通用输入输出 (GPIO) 使能 - 高电平有效

(1) 有关 CT 值与上升时间的关系，请参见 *Adjustable Rise Time*

(2) 此特性通过一个 270Ω 电阻将开关的输出放电至接地 (GND)，从而防止输出悬空。

2 应用

- 汽车电子产品
- 信息娱乐
- 仪表板
- ADAS

3 说明

TPS22968-Q1 是一款具有可配置上升时间的小型双通道负载开关。 此器件包含两个可在 0.8 至 5.5V 输入电压范围内运行的 N 通道 MOSFET，并且每通道可支持最大 4A 的持续电流。 每个开关可由一个打开/关闭输入（ON1 和 ON2）独立控制，此输入可与低压控制信号直接对接。 TPS22968-Q1 包含一个 270Ω 片上负载电阻，用于在此开关被关闭时进行快速输出放电。

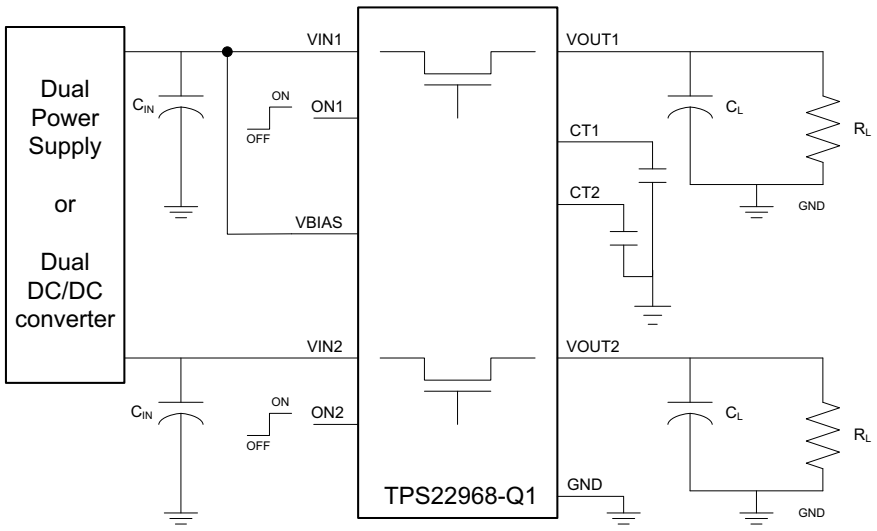
TPS22968-Q1 采用节省空间的小型封装 (DMG)，并且具有可湿性侧面和集成散热焊盘。 可湿性侧面支持目视焊接检查。 器件在自然通风环境下的额定运行温度范围为 40°C 至 125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS22968-Q1	WSON (10)	2.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



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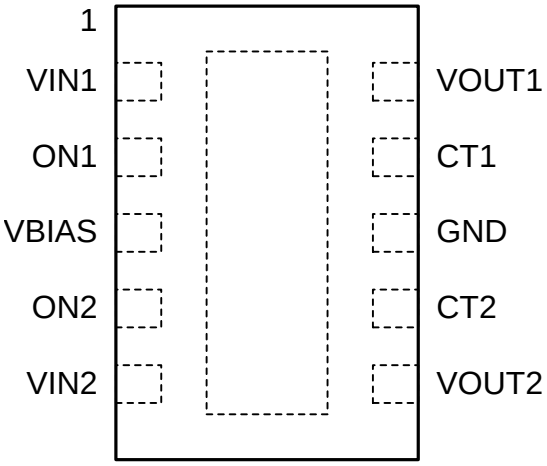
4 修订历史记录

Changes from Original (November 2014) to Revision A **Page**

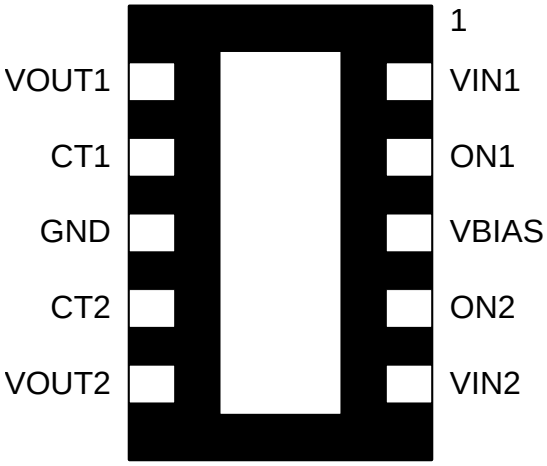
- 已将器件状态更改为量产数据 1

5 Pin Configuration and Functions

DMG Package
(Top View)



DMG Package
(Bottom View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN1	1	I	Switch 1 input. Bypass this input with a ceramic capacitor to GND.
ON1	2	I	Active-high switch 1 control input. Do not leave floating.
VBIAS	3	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 to 5.5 V. See *V_{IN} and V_{BIAS} Voltage Range*.
ON2	4	I	Active-high switch 2 control input. Do not leave floating.
VIN2	5	I	Switch 2 input. Bypass this input with a ceramic capacitor to GND.
VOUT2	6	O	Switch 2 output
CT2	7	O	Switch 2 slew rate control. Can be left floating.
GND	8	—	Ground
CT1	9	O	Switch 1 slew rate control. Can be left floating.
VOUT1	10	O	Switch 1 output
Thermal Pad	—	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See *Layout Guidelines*.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
$V_{OUT1,2}$	Output voltage	–0.3	6	V
$V_{ON1,2}$	ON voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current per channel, T_A = 50 °C		4	A
I_{PLS}	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle		6	A
T_J	Maximum junction temperature		150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage range		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
$V_{ON1,2}$	ON voltage range		0	5.5	V
$V_{OUT1,2}$	Output voltage range			V_{IN}	V
$V_{IH,\ ON1,2}$	High-level input voltage, ON1,2	V_{BIAS} = 2.5 to 5.5 V	1.2	5.5	V
$V_{IL,\ ON1,2}$	Low-level input voltage, ON1,2	V_{BIAS} = 2.5 to 5.5 V	0	0.5	V
$C_{IN1,2}$	Input capacitor		1(1)		µF
T_A	Operating free-air temperature (2)		–40	125	°C

(1) Refer to *Application Information*.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$.

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS22968-Q1 DMG (10 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.7	
ψ_{JT}	Junction-to-top characterization parameter	1.9	
ψ_{JB}	Junction-to-board characterization parameter	21.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

6.5 Electrical Characteristics (V_{BIAS} = 5 V)

V_{BIAS} = 5 V. Typical values are for T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 A, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 5 V		–40°C to 85°C		58	70	µA
				–40°C to 125°C			70	
	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 A, V_{ON2} = 0 V, $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 5.0 V		–40°C to 85°C		58	68	µA
				–40°C to 125°C			68	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to 85°C		1	2	µA
				–40°C to 125°C			2	
$I_{SD, VIN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 5 V	–40°C to 85°C		0.5	8	µA
				–40°C to 125°C			36	
			$V_{IN1,2}$ = 3.3 V	–40°C to 85°C		0.1	3	
				–40°C to 125°C			13	
			$V_{IN1,2}$ = 1.8 V	–40°C to 85°C		0.07	2	
				–40°C to 125°C			6	
			$V_{IN1,2}$ = 1.2 V	–40°C to 85°C		0.05	1	
				–40°C to 125°C			4	
			$V_{IN1,2}$ = 0.8 V	–40°C to 85°C		0.04	1	
				–40°C to 125°C			4	
$I_{ON1,2}$	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to 125°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		29	35	mΩ
				–40°C to 85°C			40	
				–40°C to 125°C			43	
			V_{IN} = 3.3 V	25°C		27	32	mΩ
				–40°C to 85°C			36	
				–40°C to 125°C			40	
			V_{IN} = 1.8 V	25°C		26	32	mΩ
				–40°C to 85°C			36	
				–40°C to 125°C			39	
			V_{IN} = 1.2 V	25°C		26	32	mΩ
				–40°C to 85°C			36	
				–40°C to 125°C			39	
			V_{IN} = 0.8 V	25°C		26	32	mΩ
				–40°C to 85°C			36	
				–40°C to 125°C			39	
R_{PD}	Output pulldown resistance	V_{IN} = 5 V, V_{ON} = 0 V, I_{OUT} = 5 mA		–40°C to 125°C		270	320	Ω

6.6 Electrical Characteristics (V_{BIAS} = 3.3 V)

V_{BIAS} = 3.3 V. Typical values are for T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 A, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 3.3 V		–40°C to 85°C		27	40	µA
				–40°C to 125°C			40	
	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 A, V_{ON2} = 0 V, $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 3.3 V		–40°C to 85°C		27	40	µA
				–40°C to 125°C			40	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to 85°C		0.5	1	µA
				–40°C to 125°C			1	
$I_{SD, VIN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 3.3 V	–40°C to 85°C		0.1	3	µA
				–40°C to 125°C			13	
			$V_{IN1,2}$ = 1.8 V	–40°C to 85°C		0.07	2	
				–40°C to 125°C			6	
			$V_{IN1,2}$ = 1.2 V	–40°C to 85°C		0.05	1	
				–40°C to 125°C			4	
			$V_{IN1,2}$ = 0.8 V	–40°C to 85°C		0.04	1	
				–40°C to 125°C			4	
$I_{ON1,2}$	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to 125°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 3.3 V	V_{IN} = 3.3 V	25°C		32	38	mΩ
				–40°C to 85°C			44	
				–40°C to 125°C			48	
			V_{IN} = 1.8 V	25°C		28	33	mΩ
				–40°C to 85°C			38	
				–40°C to 125°C			42	
			V_{IN} = 1.2 V	25°C		27	33	mΩ
				–40°C to 85°C			38	
				–40°C to 125°C			41	
			V_{IN} = 0.8 V	25°C		27	32	mΩ
				–40°C to 85°C			37	
				–40°C to 125°C			40	
R_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0 V, I_{OUT} = 5 mA		–40°C to 125°C		270	320	Ω

6.7 Electrical Characteristics (V_{BIAS} = 2.5 V)

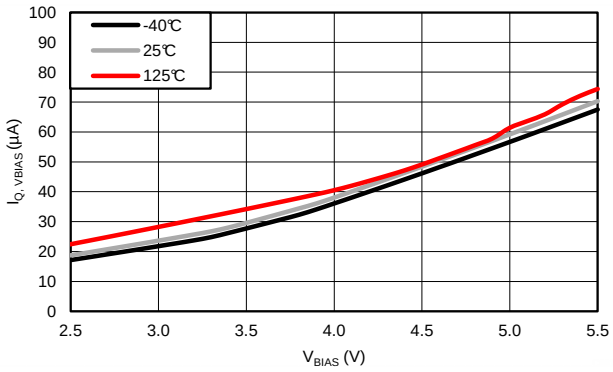
V_{BIAS} = 2.5 V. Typical values are for T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0$, $V_{IN1,2} = V_{ON1,2} = V_{BIAS}$ = 2.5 V		–40°C to 85°C		19	27	µA
				–40°C to 125°C			27	
	V_{BIAS} quiescent current (single channel)	$I_{OUT1} = I_{OUT2} = 0$, V_{ON2} = 0 V, $V_{IN1,2} = V_{ON1} = V_{BIAS}$ = 2.5 V		–40°C to 85°C		19	27	µA
				–40°C to 125°C			27	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to 85°C		0.4	1	µA
				–40°C to 125°C			1	
$I_{SD, VIN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 2.5 V	–40°C to 85°C		0.1	2	µA
				–40°C to 125°C			9	
			$V_{IN1,2}$ = 1.8 V	–40°C to 85°C		0.07	2	
				–40°C to 125°C			6	
			$V_{IN1,2}$ = 1.2 V	–40°C to 85°C		0.05	1	
				–40°C to 125°C			4	
			$V_{IN1,2}$ = 0.8 V	–40°C to 85°C		0.04	1	
				–40°C to 125°C			4	
$I_{ON1,2}$	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to 125°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		39	45	mΩ
				–40°C to 85°C			52	
				–40°C to 125°C			57	
			V_{IN} = 1.8 V	25°C		34	39	mΩ
				–40°C to 85°C			46	
				–40°C to 125°C			50	
			V_{IN} = 1.2 V	25°C		31	37	mΩ
				–40°C to 85°C			42	
				–40°C to 125°C			46	
			V_{IN} = 0.8 V	25°C		30	35	mΩ
				–40°C to 85°C			41	
				–40°C to 125°C			44	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 5 mA		–40°C to 125°C		270	320	Ω

6.8 Switching Characteristics

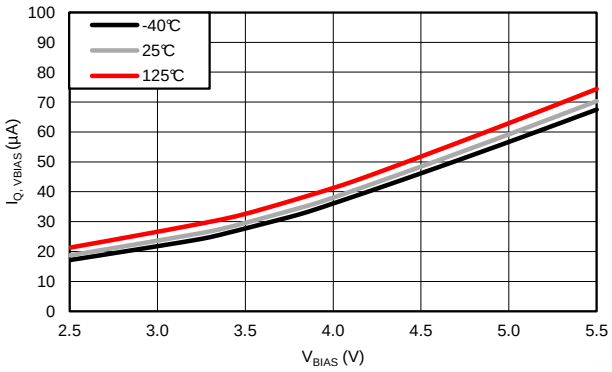
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25 °C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1150		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		4		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1400		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		469		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25 ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		514		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		31		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		271		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		382		
V_{IN} = 3.3 V, V_{ON} = 5 V, V_{BIAS} = 3.3 V, T_A = 25 ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1455		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		5		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1592		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		681		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 3.3 V, T_A = 25 ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		805		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		31		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		455		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		577		
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25 ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1800		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		6		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1830		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		909		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25 ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1140		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		28		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		664		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		798		

6.9 Typical DC Characteristics



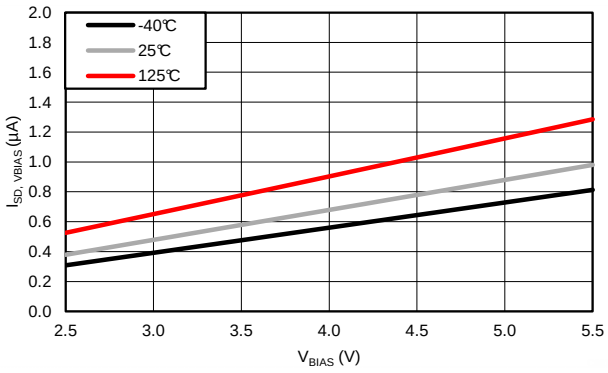
V_{ON} = 5 V V_{OUT} = Open

Figure 1. $I_{Q, VBIAS}$ vs V_{BIAS} (Single Channel)



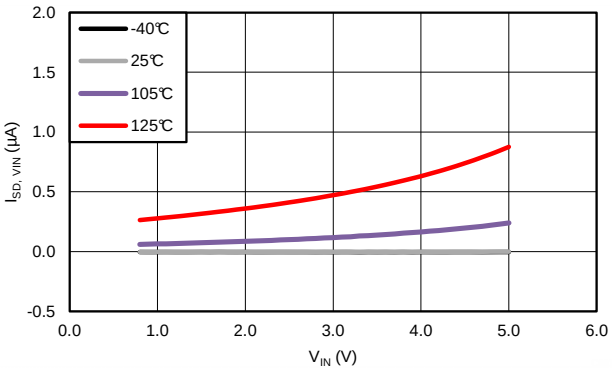
V_{ON} = 5 V V_{OUT} = Open

Figure 2. $I_{Q, VBIAS}$ vs V_{BIAS} (Dual Channel)



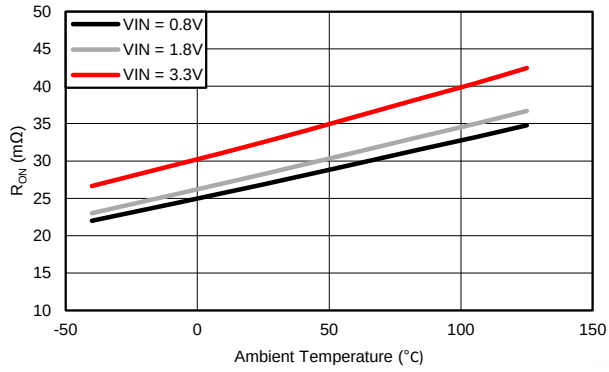
V_{ON} = 0 V V_{OUT} = 0 V

Figure 3. $I_{SD, VBIAS}$ vs V_{BIAS}



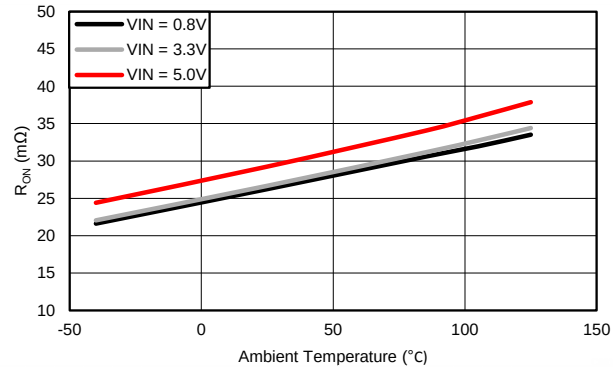
V_{BIAS} = 5 V V_{OUT} = 0 V V_{ON} = 0 V

Figure 4. $I_{SD, VIN}$ vs V_{IN} (One Channel)



I_{OUT} = –200 mA

Figure 5. R_{ON} vs Ambient Temperature, V_{BIAS} = 3.3 V



I_{OUT} = –200 mA

Figure 6. R_{ON} vs Ambient Temperature , V_{BIAS} = 5 V

Typical DC Characteristics (continued)

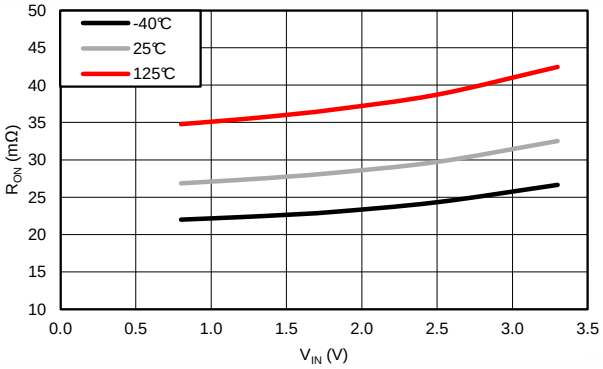


Figure 7. R_{ON} vs V_{IN}, V_{BIAS} = 3.3 V

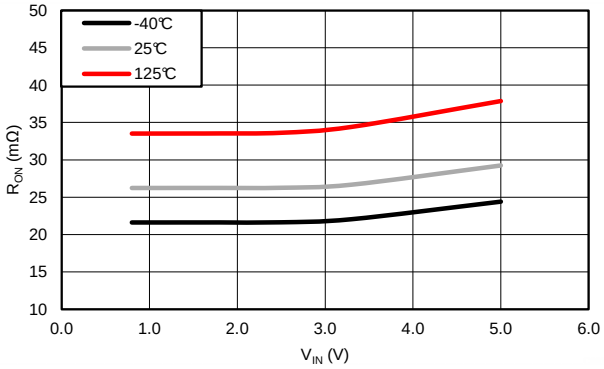


Figure 8. R_{ON} vs V_{IN}, V_{BIAS} = 5 V

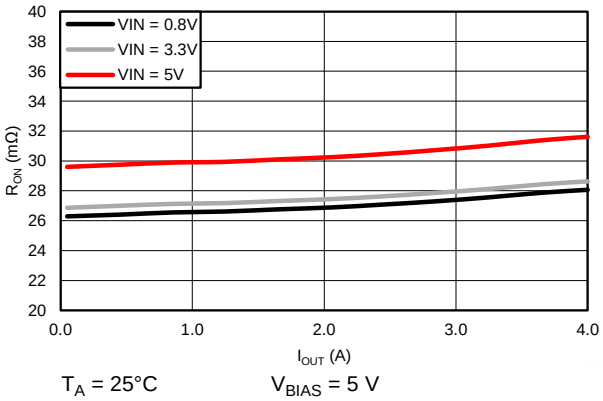


Figure 9. R_{ON} vs I_{OUT}

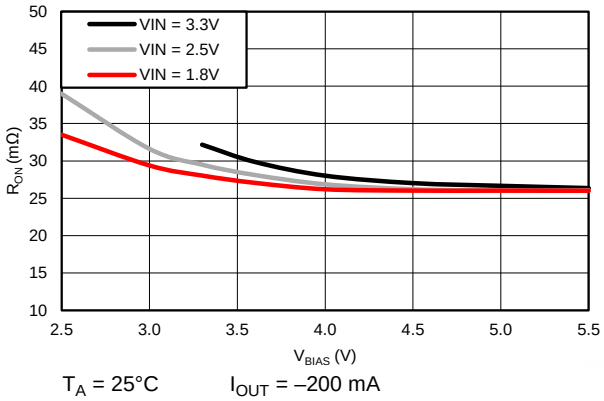


Figure 10. R_{ON} vs V_{BIAS}

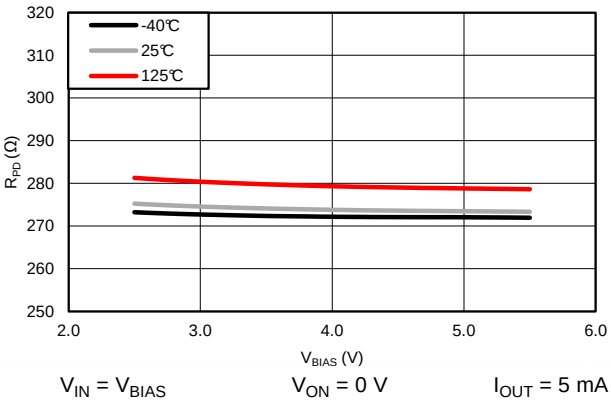


Figure 11. R_{PD} vs V_{BIAS}

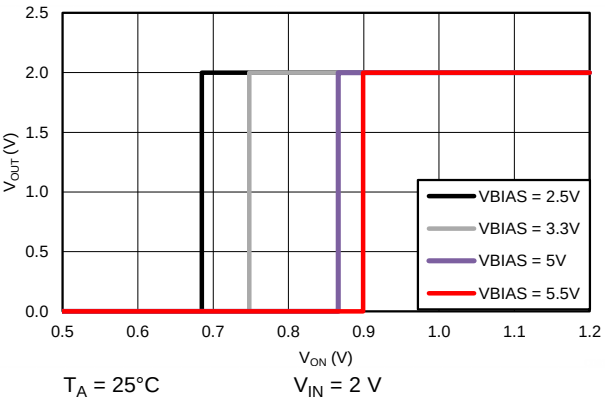


Figure 12. V_{OUT} vs V_{ON}

6.10 Typical AC Characteristics

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CT = 1 nF (unless otherwise specified)

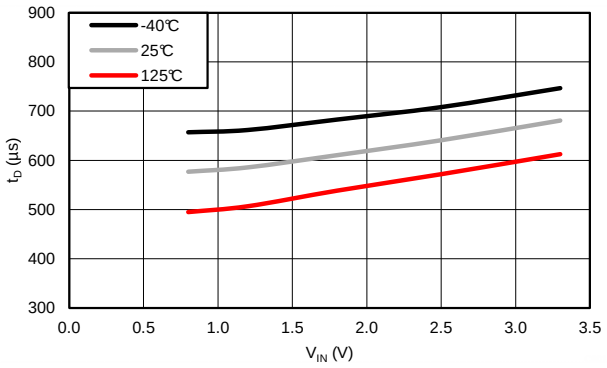


Figure 13. t_D vs V_{IN}, V_{BIAS} = 3.3 V

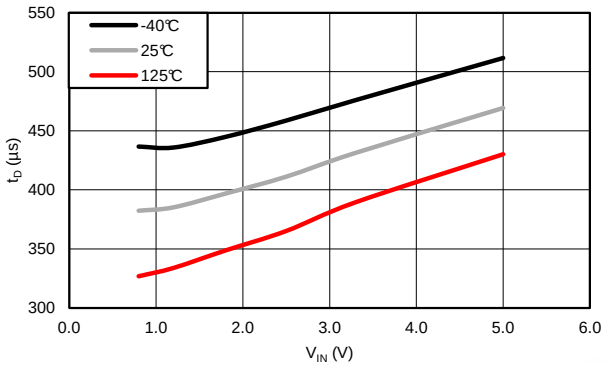


Figure 14. t_D vs V_{IN}, V_{BIAS} = 5 V

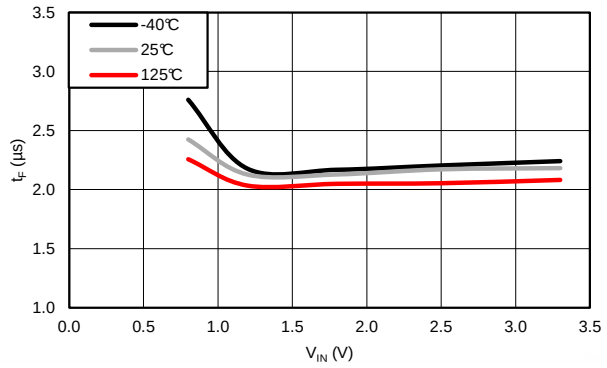


Figure 15. t_F vs V_{IN}, V_{BIAS} = 3.3 V

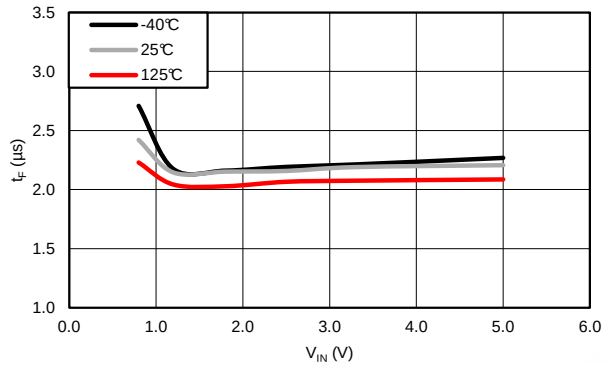


Figure 16. t_F vs V_{IN}, V_{BIAS} = 5 V

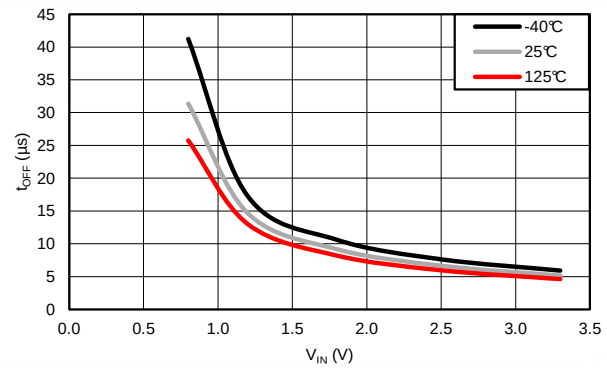


Figure 17. t_{OFF} vs V_{IN}, V_{BIAS} = 3.3 V

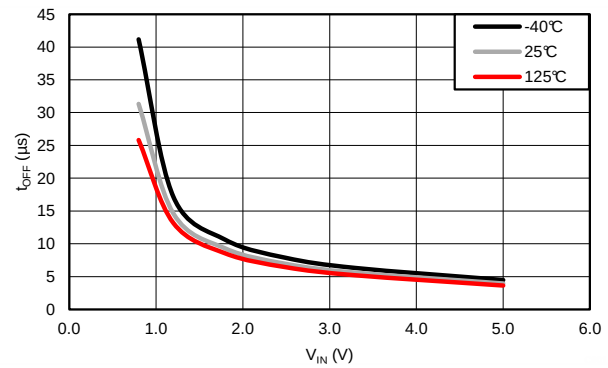


Figure 18. t_{OFF} vs V_{IN}, V_{BIAS} = 5 V

Typical AC Characteristics (continued)

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CT = 1 nF (unless otherwise specified)

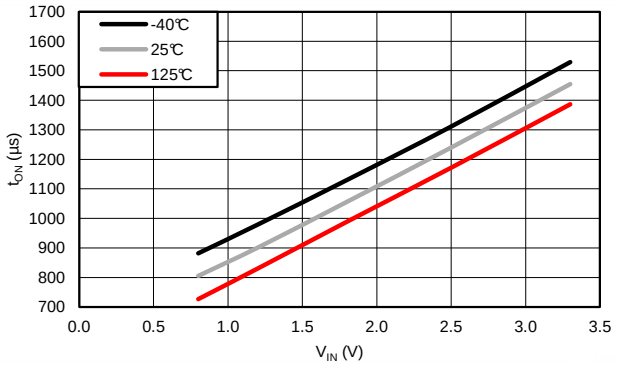


Figure 19. t_{ON} vs V_{IN}, V_{BIAS} = 3.3 V

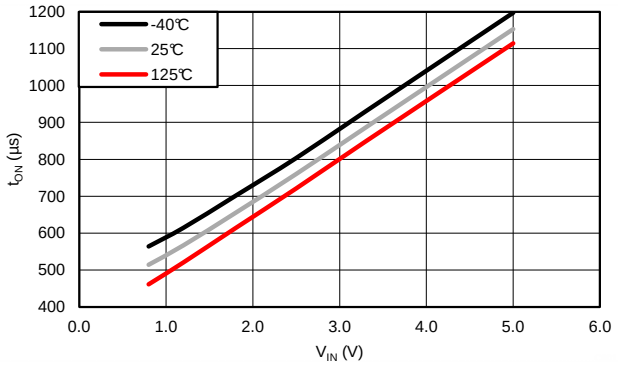


Figure 20. t_{ON} vs V_{IN}, V_{BIAS} = 5 V

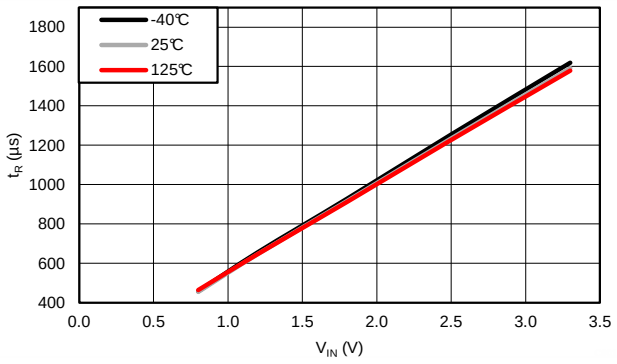


Figure 21. t_R vs V_{IN}, V_{BIAS} = 3.3 V

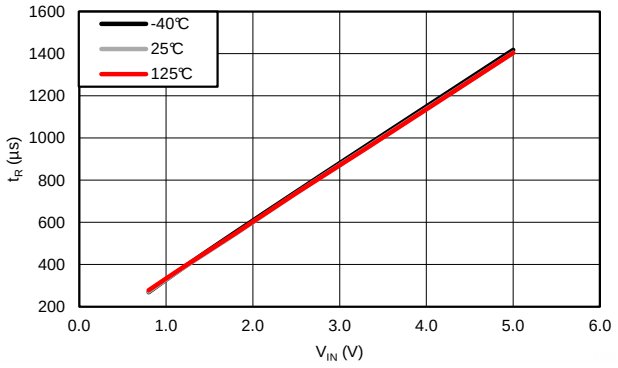


Figure 22. t_R vs V_{IN}, V_{BIAS} = 5 V

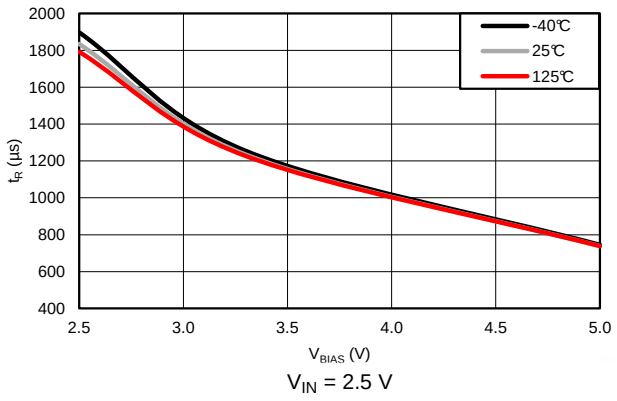


Figure 23. t_R vs V_{BIAS}

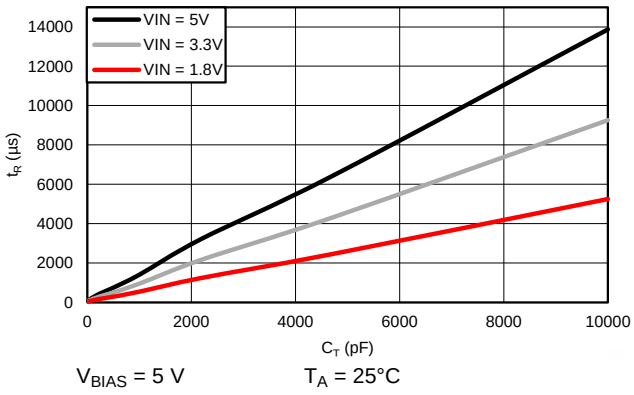


Figure 24. t_R vs CT

Typical AC Characteristics (continued)

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CT = 1 nF (unless otherwise specified)

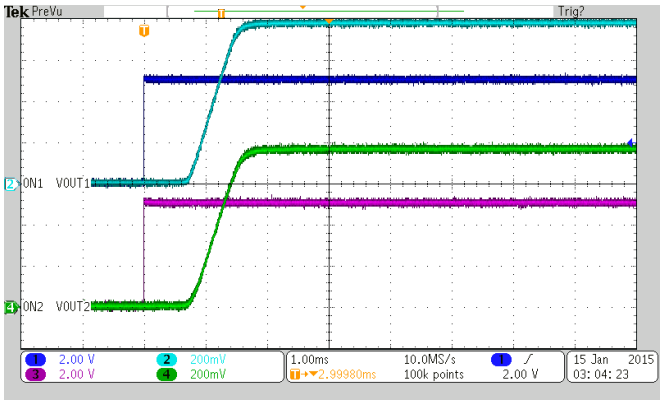


Figure 25. Turn-On Response Time (V_{IN} = 0.8 V, V_{BIAS} = 2.5 V)

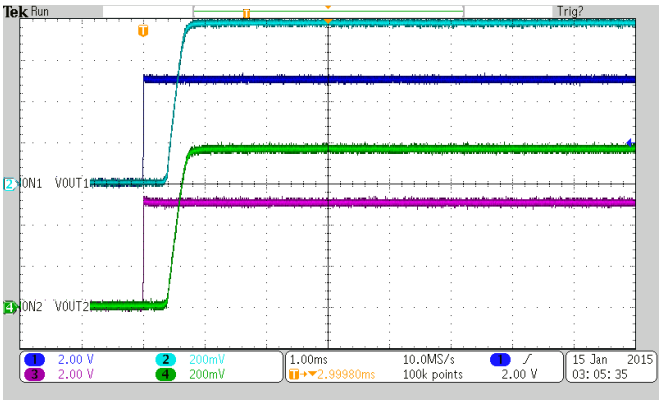


Figure 26. Turn-On Response Time (V_{IN} = 0.8 V, V_{BIAS} = 5 V)

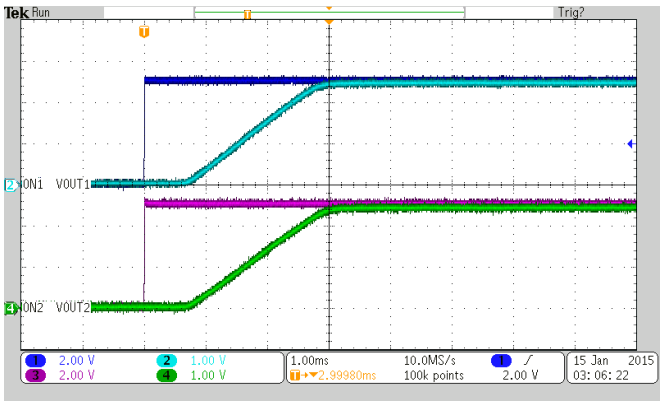


Figure 27. Turn-On Response Time (V_{IN} = 2.5 V, V_{BIAS} = 2.5 V)

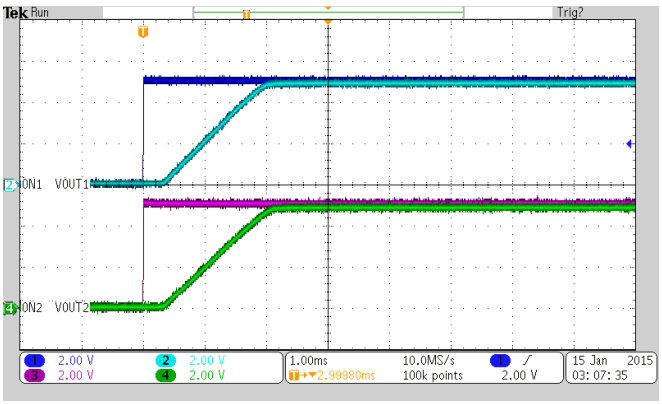


Figure 28. Turn-On Response Time (V_{IN} = 5 V, V_{BIAS} = 5 V)

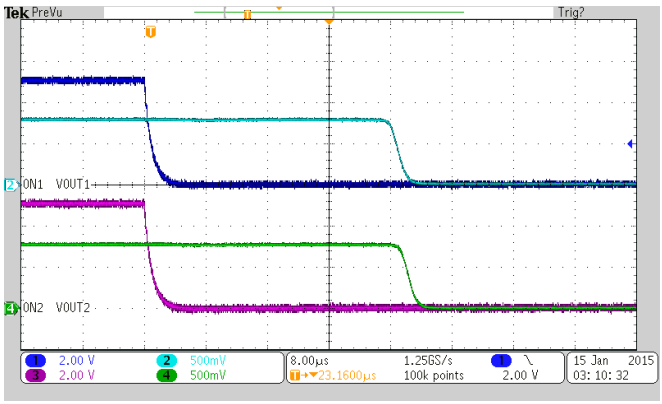


Figure 29. Turn-Off Response Time (V_{IN} = 0.8 V, V_{BIAS} = 2.5 V)

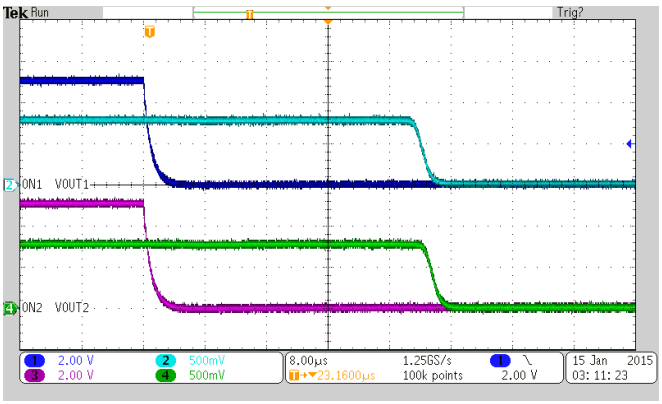


Figure 30. Turn-Off Response Time (V_{IN} = 0.8 V, V_{BIAS} = 5 V)

Typical AC Characteristics (continued)

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CT = 1 nF (unless otherwise specified)

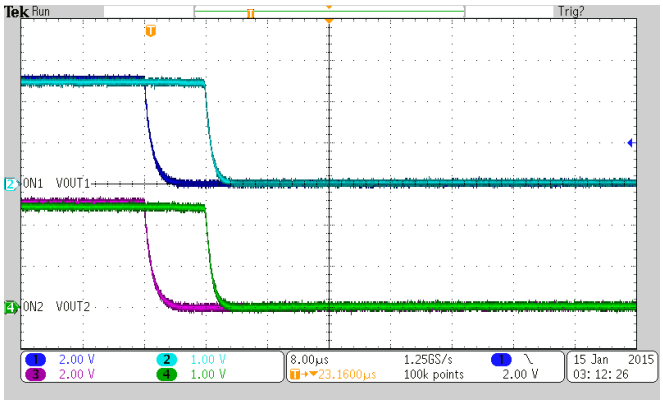


Figure 31. Turn-Off Response Time (V_{IN} = 2.5 V, V_{BIAS} = 2.5 V)

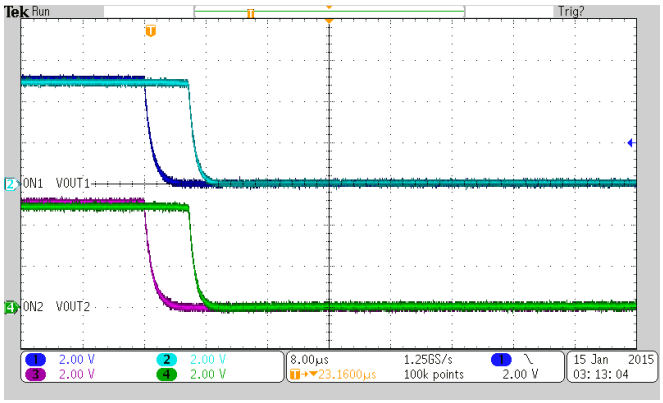
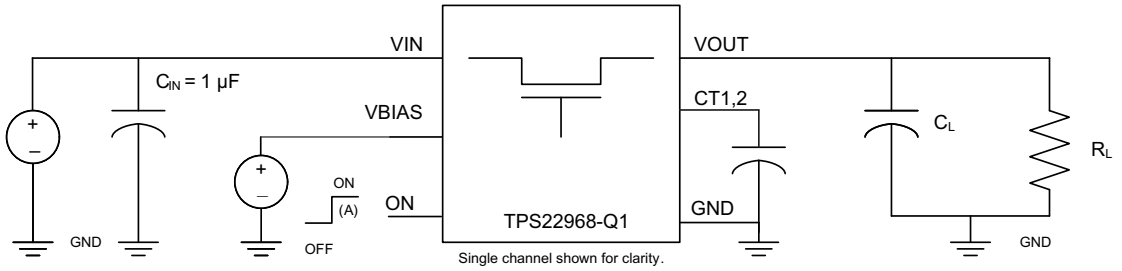
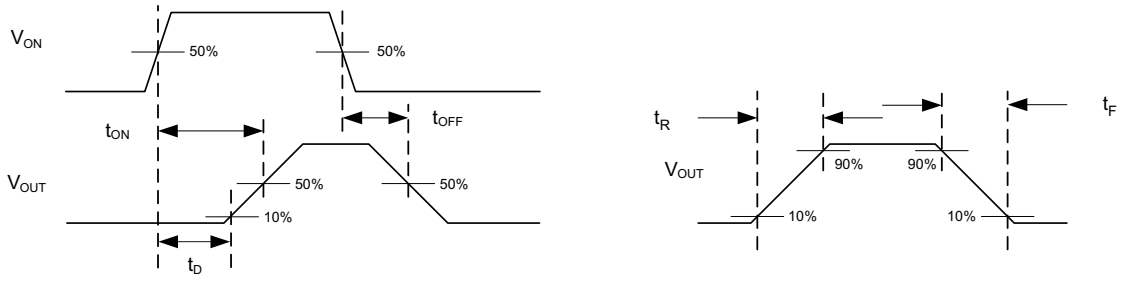


Figure 32. Turn-Off Response Time (V_{IN} = 5 V, V_{BIAS} = 5 V)

7 Parameter Measurement Information



Test Circuit



Timing Waveforms

A. Rise and fall times of the control signal is 100 ns.

Figure 33. Test Circuit and Timing Waveforms

8 Detailed Description

8.1 Overview

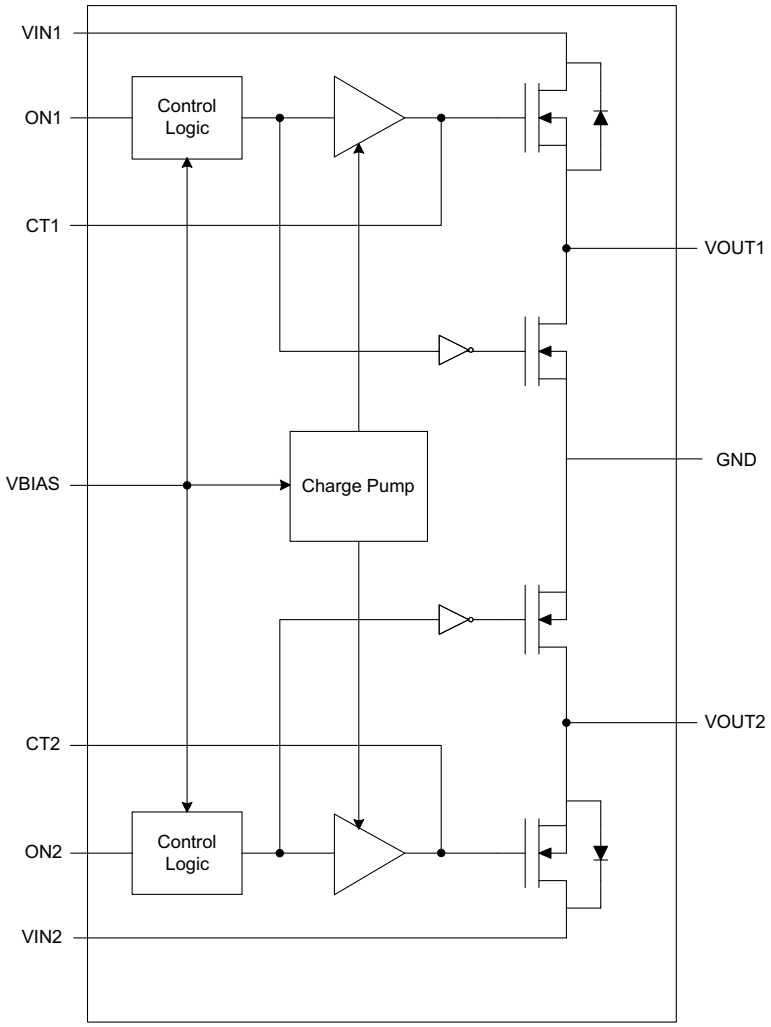
The device is a 5.5-V, 4-A, dual-channel ultra-low R_{ON} load switch with controlled turn on. The device contains two N-channel MOSFETs. Each channel can support a maximum continuous current of 4 A. Each channel is controlled by an on/off GPIO-compatible input. The ON pin must be connected and cannot be left floating. The device is designed to control the turn-on rate and therefore the inrush current. By controlling the inrush current, power supply sag can be reduced during turn-on. The slew rate for each channel is set by connecting a capacitor to GND on the CT pins.

The slew rate is proportional to the capacitor on the CT pin. Refer to *Adjustable Rise Time* to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the VBIAS pin, which supports voltages from 2.5 to 5.5 V. This circuitry includes the charge pump, QOD, and control logic. For these internal blocks to function correctly, a voltage between 2.5 and 5.5 V must be supplied to VBIAS.

When a voltage is supplied to VBIAS and the ON1, 2 pin goes low, the QOD turns on. This connects VOUT1, 2 to GND through an on-chip resistor. The typical pulldown resistance (R_{PD}) is 270 Ω.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON/OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

8.3.2 Quick Output Discharge (QOD)

The TPS22968-Q1 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 270 Ω and prevents the output from floating while the switch is disabled.

8.3.3 Adjustable Rise Time

A capacitor to GND on the CT pins sets the slew rate for each channel. The capacitor to GND on the CT pins should be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate with V_{BIAS} = 5 V is:

$$SR = 0.35 \times CT + 25 \quad (1)$$

where

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CT pin (in pF)
- The units for the constant 25 is in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device.

Table 1. Rise Time Table

CTx (pF)	Rise Time (µs)(1) (2)					
	V_{IN} = 5 V	V_{IN} = 3.3 V	V_{IN} = 2.5 V	V_{IN} = 1.8 V	V_{IN} = 1.2 V	V_{IN} = 0.8 V
0	84	63	52	43	35	27
220	418	285	223	168	122	88
470	711	479	372	276	196	139
1000	1405	952	738	545	385	271
2200	3236	2174	1684	1246	876	615
4700	6415	4306	3317	2454	1725	1217
10000	13872	9261	7150	5253	3694	2591

(1) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V
(2) Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT

8.4 Device Functional Modes

Table 2. Functional Table

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations for implementing this device in various applications. A PSPICE model for this device is also available on the product page for further aid.

9.1.1 Input Capacitor (Optional)

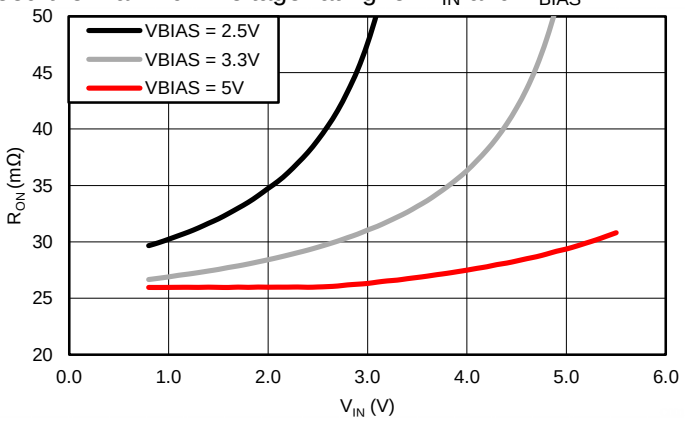
To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor must be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current applications. When switching heavy loads, TI recommends to have an input capacitor about 10× higher than the output capacitor to avoid excessive voltage drop.

9.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, TI highly recommends a C_{IN} greater than C_L. A C_L greater than C_{IN} can cause the voltage on VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. TI recommends a C_{IN} to C_L ratio of 10 to 1 for minimizing V_{IN} dip caused by inrush currents during startup.

9.1.3 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$, but it will exhibit R_{ON} greater than what is listed in the *Electrical Characteristics (V_{BIAS} = 5 V)* and *Electrical Characteristics (V_{BIAS} = 2.5 V)*. See Figure 34 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.



T_A = 25°C I_{OUT} = –200 mA

Figure 34. R_{ON} vs V_{IN}

Application Information (continued)

9.1.3.1 Parallel Configuration

To increase the current capabilities and lower the R_{ON} by approximately 50%, both channels can be placed in parallel as shown in Figure 35 (parallel configuration). With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, CT, as shown in Figure 35. With a single CT capacitor, the rise time will be half of the typical rise-time value. Refer to the Table 1 for typical timing values.

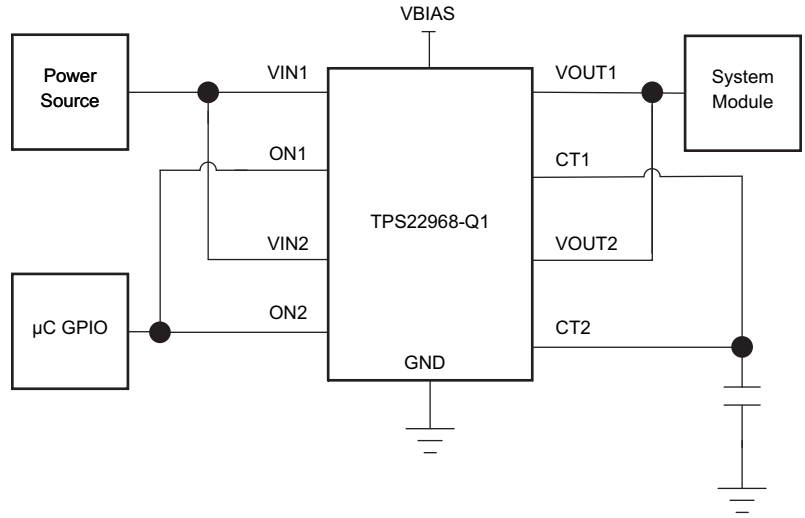


Figure 35. Parallel Configuration Schematic

9.1.3.2 Standby Power Reduction

TPS22968-Q1 can help to reduce the standby power consumption of a module. Some loads will consume a non-trivial amount of power when turned off. If the power to the load is removed by the load switch, the standby power consumption can be significantly reduced.

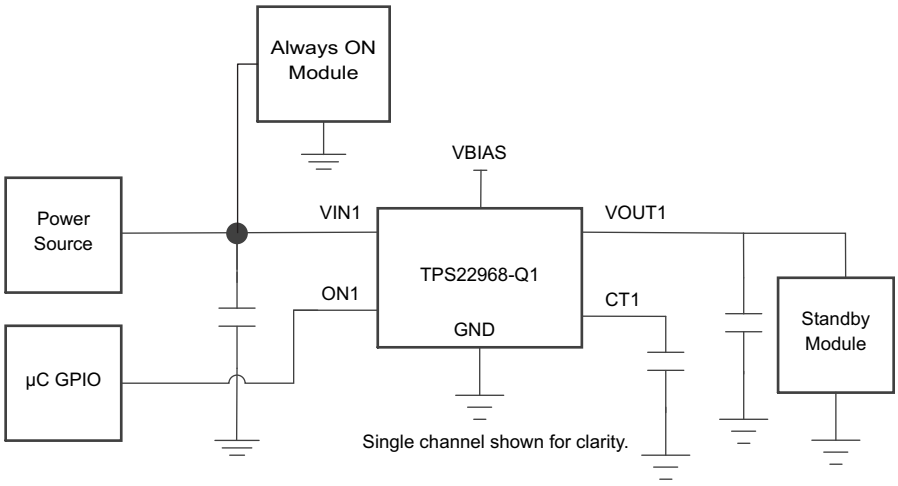
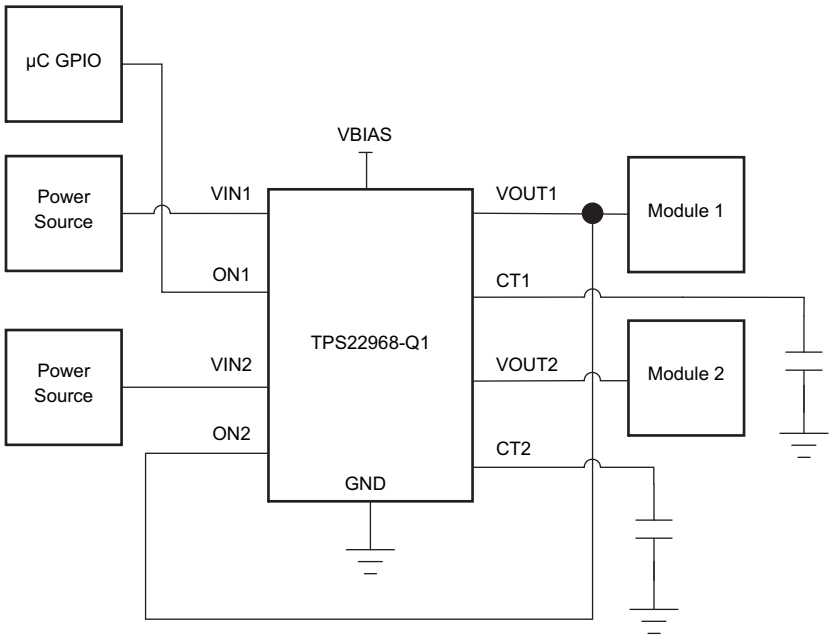


Figure 36. Standby Power Reduction Schematic

Application Information (continued)

9.1.3.3 Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a predetermined manner. TPS22968-Q1 can solve the problem of power sequencing without adding any complexity to the overall system.



A. VIN1 must be greater V_{IH}.

Figure 37. Power Sequencing Without a GPIO Input Schematic

9.1.3.4 Reverse Current Blocking

In certain applications, it may be desirable to have reverse current blocking. Reverse current blocking prevents current from flowing from the output to the input of the load switch when the device is disabled. With the following configuration, the TPS22968-Q1 can be converted into a single-channel switch with reverse current blocking. In this configuration, VIN1 or VIN2 can be used as the input and VIN2 or VIN1 is the output.

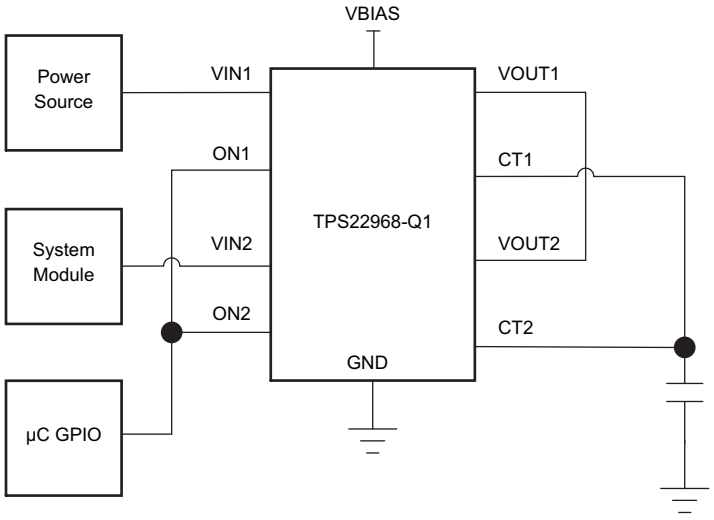


Figure 38. Reverse Current Blocking Schematic

9.2 Typical Application

This application demonstrates how the TPS22968-Q1 can be used to power a downstream load with a large capacitance. The example in Figure 39 is powering a 22-µF capacitive output load.

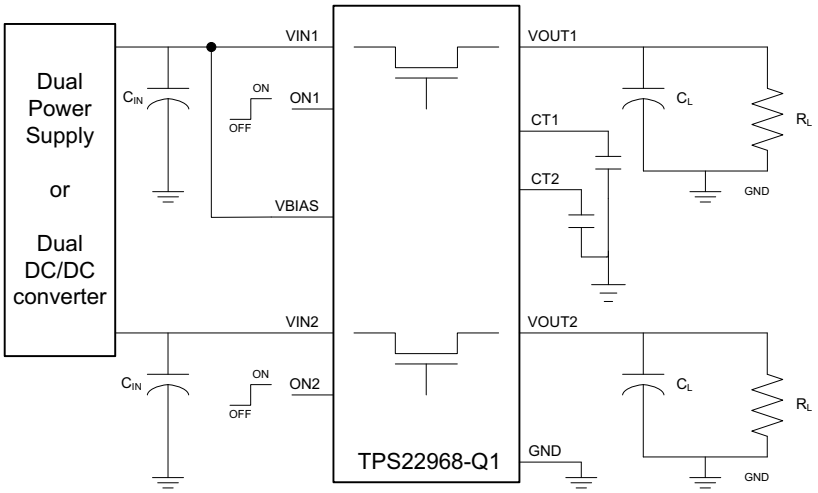


Figure 39. Typical Application Schematic for Powering a Downstream Module

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5.0 V
Output capacitance (C_L)	22 µF
Allowable inrush current on VOUT	0.400 A

9.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Output capacitance (C_L)
- Allowable inrush current on VOUT due to C_L capacitor

9.2.2.1 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 2.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- I_{INRUSH} = amount of inrush current caused by C_L
- C_L = capacitance on VOUT
- dt = V_{OUT} rise time
- dV_{OUT} = increase in V_{OUT} during the rise time (2)

Inrush current is proportional to rise time. The rise time is adjustable by use of the CT capacitor. The appropriate rise time can be calculated using the design requirements and the inrush current equation (Equation 2).

400 mA = 22 µF × 3.3 V / dt (3)

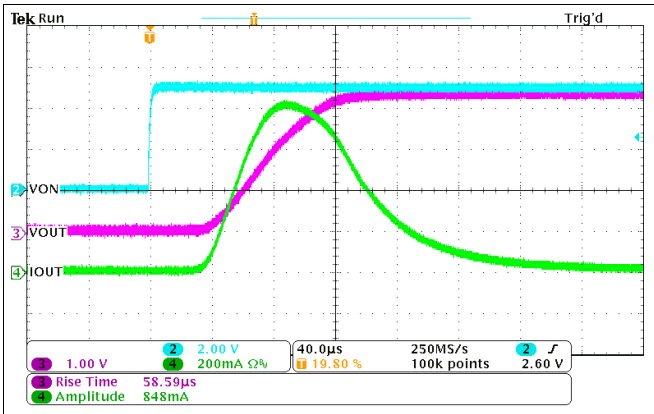
dt = 182 µs (4)

To ensure an inrush current of less than 400 mA, choose a CT capacitor value that will yield a rise time of more than 182 µs. See the oscilloscope captures in the *Application Curves* for an example of how the CT capacitor can be used to reduce inrush current. See Table 1 for correlation between rise times and CT values.

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

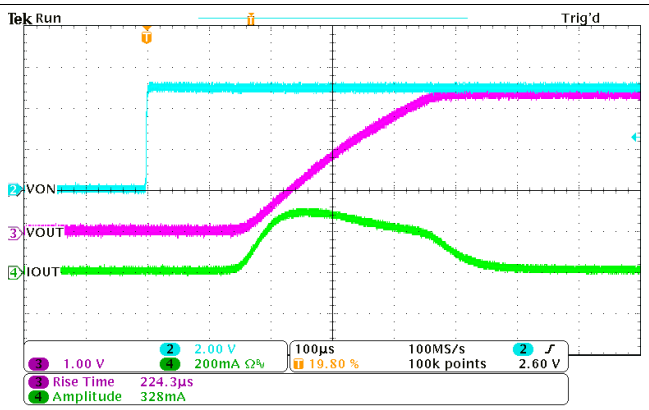
9.2.3 Application Curves

The two scope captures below show how the CT capacitor can be used to reduce inrush current.



VBIAS = 5 V VIN = 3.3 V T_A = 25°C
CT = Open C_L = 22 µF

Figure 40. Inrush Current Without CT Capacitor



VBIAS = 5 V VIN = 3.3 V T_A = 25°C
CT = 220 pF C_L = 22 µF

Figure 41. Inrush Current With CT = 220 pF

10 Power Supply Recommendations

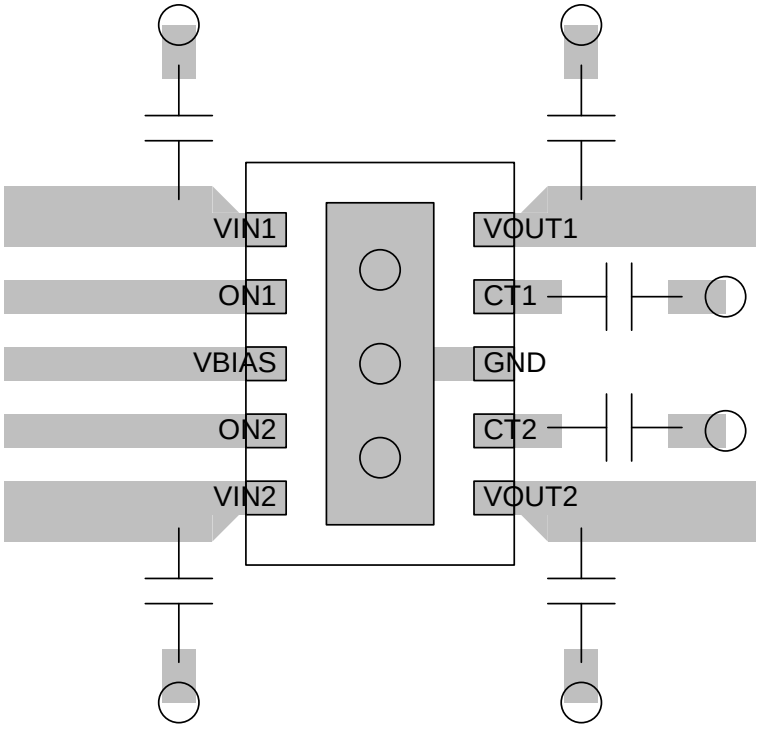
The device is designed to operate from a V_{BIAS} range of 2.5 to 5.5 V and V_{IN} range of 0.8 to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

11 Layout

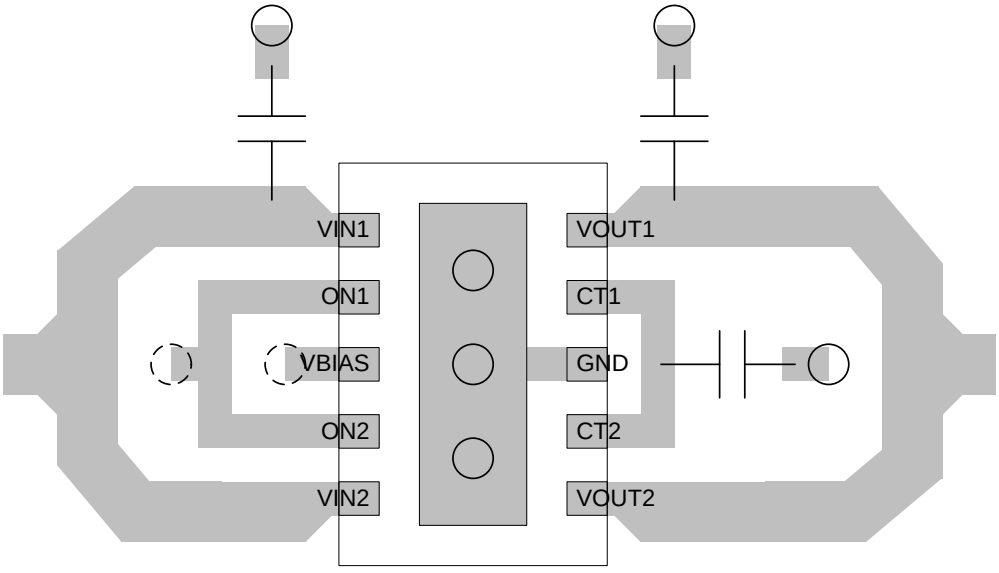
11.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- VINx pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- VOUTx pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VINx bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The VBIAS pin should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-µF ceramic with X5R or X7R dielectric.
- The CTx capacitors should be placed as close to the device pins as possible. The typical recommended CTx capacitance is a capacitor of X5R or X7R dielectric rating with a rating of 25 V or higher.

11.2 Layout Example



Dual-channel layout



Single-channel layout

Via to GND

Via to internal or bottom layer

Figure 42. Layout Schematic

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given ambient temperature, use Equation 5.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (5)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22968-Q1)
- T_A = ambient temperature of the device
- $R_{\theta JA}$ = junction to air thermal impedance. See *Thermal Information*. This parameter is highly dependent upon board layout.

Following are two examples demonstrating how to use the above information: For V_{BIAS} = 5 V, V_{IN} = 5 V, the maximum allowable ambient temperature with a 3-A load through each channel can be determined by using the following calculations.

NOTE

When calculating power dissipation in the switch, it is important to use the correct R_{ON} value. R_{ON} is dependent on the junction temperature of the device.

$$P_D = I^2 \times R \times 2 \text{ (multiplied by 2 because there are two channels)} \quad (6)$$

$$2 \times I^2 \times R = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (7)$$

$$T_A = T_{J(MAX)} - R_{\theta JA} \times 2 \times I^2 \times R \quad (8)$$

$$T_A = 150°C - 55.6°C/W \times 2 \times (3\ A)^2 \times 45\ m\Omega = 105°C \quad (9)$$

For V_{BIAS} = 5 V, V_{IN} = 5 V, the maximum continuous current for an ambient temperature of 85°C with the same current flowing through each channel can be determined by using the following calculation:

$$2 \times I^2 \times R = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (10)$$

$$I = \sqrt{\frac{T_{J(MAX)} - T_A}{2 \times R \times R_{\theta JA}}} \quad (11)$$

$$I = \sqrt{\frac{150°C - 85°C}{2 \times 45\ m\Omega \times 55.6°C/W}} = 3.6\ A \quad (12)$$

12 器件和文档支持

12.1 商标

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12.2 静电放电警告

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12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22968NQDMGRQ1	ACTIVE	WSON	DMG	10	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	11C	Samples
TPS22968NQDMGTQ1	ACTIVE	WSON	DMG	10	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	11C	Samples
TPS22968QDMGRQ1	ACTIVE	WSON	DMG	10	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SIV	Samples
TPS22968QDMGTQ1	ACTIVE	WSON	DMG	10	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SIV	Samples

(1) The marketing status values are defined as follows:
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OBSOLETE: TI has discontinued the production of the device.

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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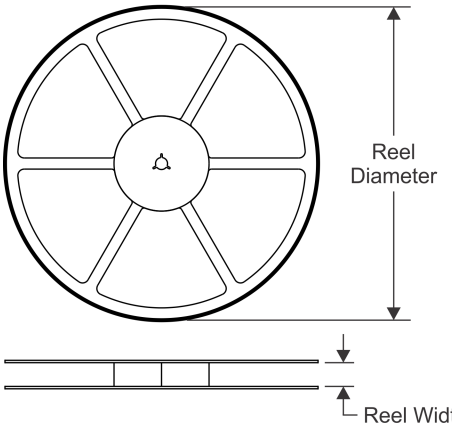
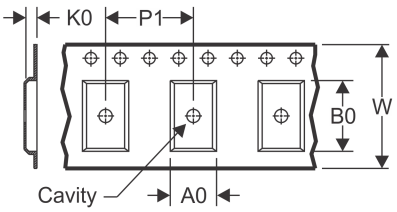
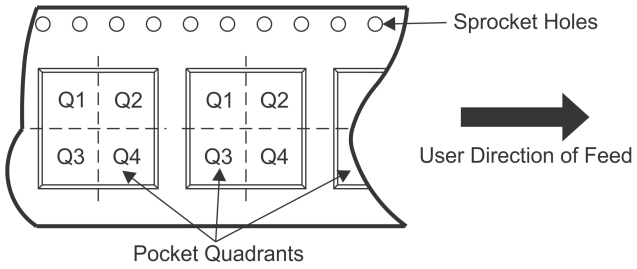


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

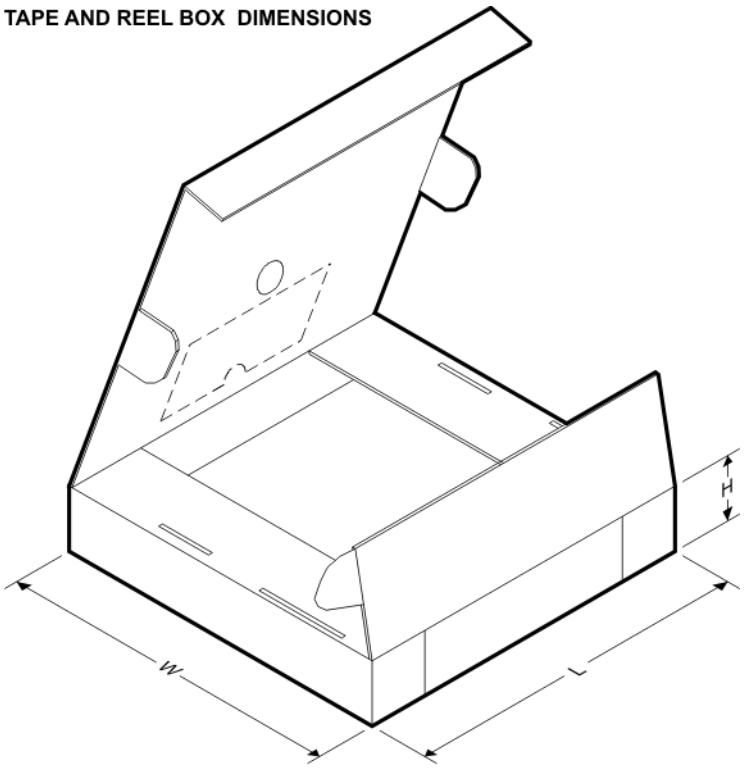
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22968NQDMGRQ1	WSON	DMG	10	3000	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS22968NQDMGTQ1	WSON	DMG	10	250	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS22968QDMGRQ1	WSON	DMG	10	3000	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS22968QDMGTQ1	WSON	DMG	10	250	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

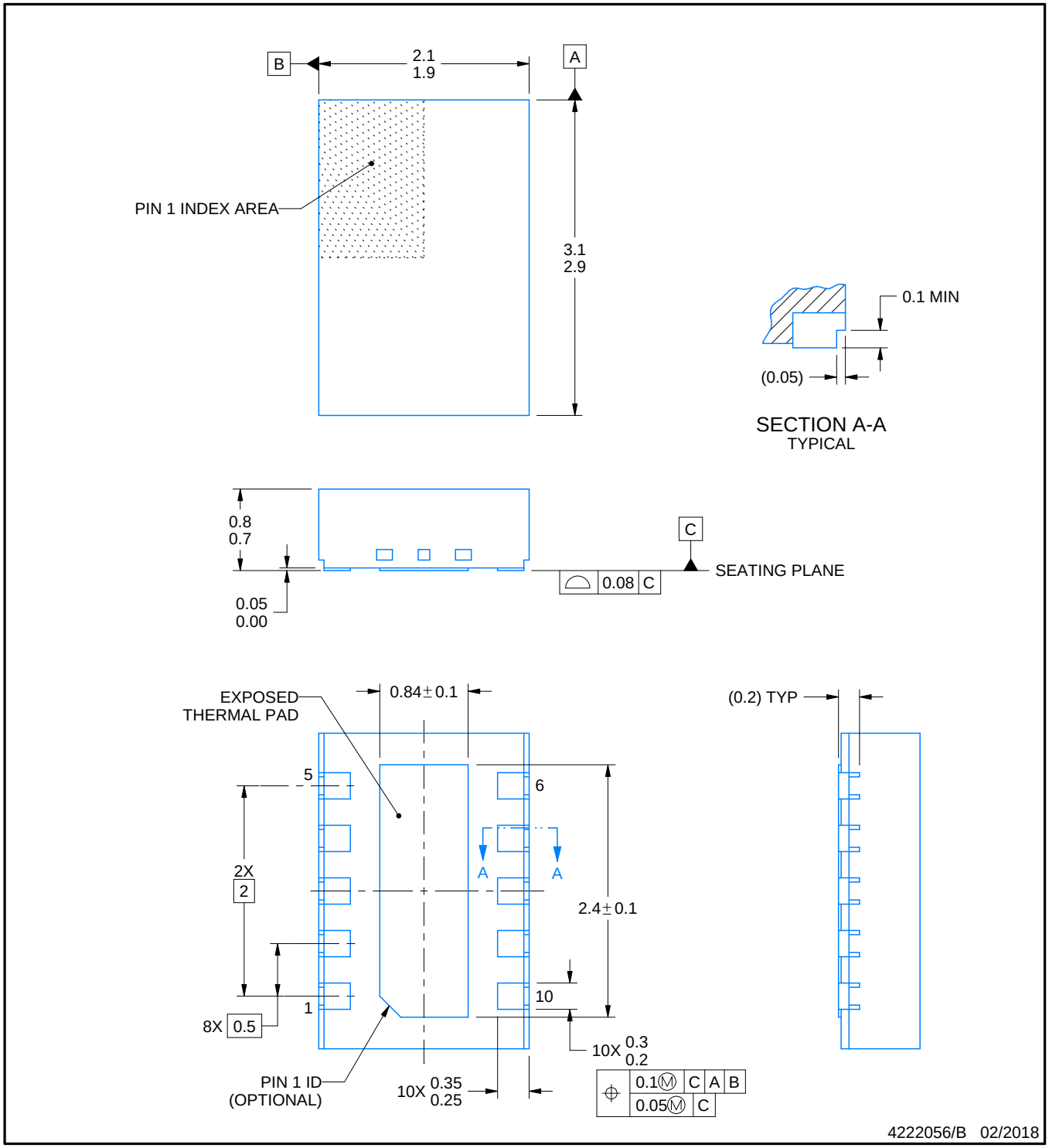
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22968NQDMGRQ1	WSON	DMG	10	3000	213.0	191.0	35.0
TPS22968NQDMGTQ1	WSON	DMG	10	250	213.0	191.0	35.0
TPS22968QDMGRQ1	WSON	DMG	10	3000	213.0	191.0	35.0
TPS22968QDMGTQ1	WSON	DMG	10	250	213.0	191.0	35.0

PACKAGE OUTLINE

DMG0010A

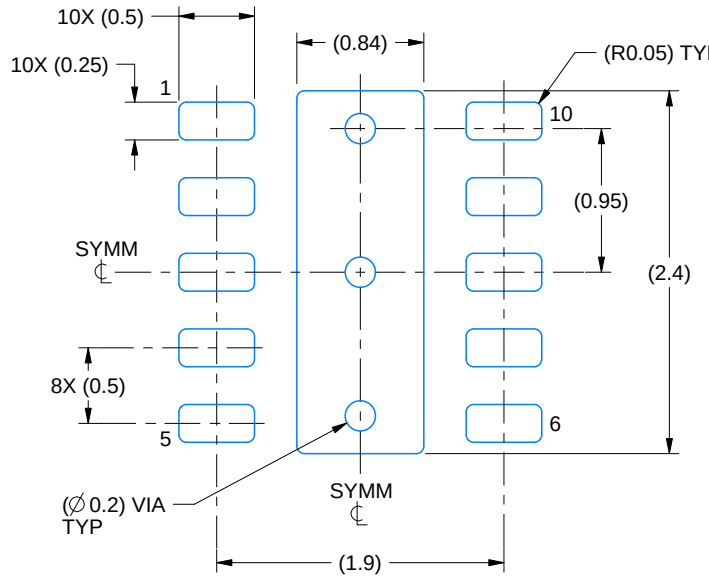
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

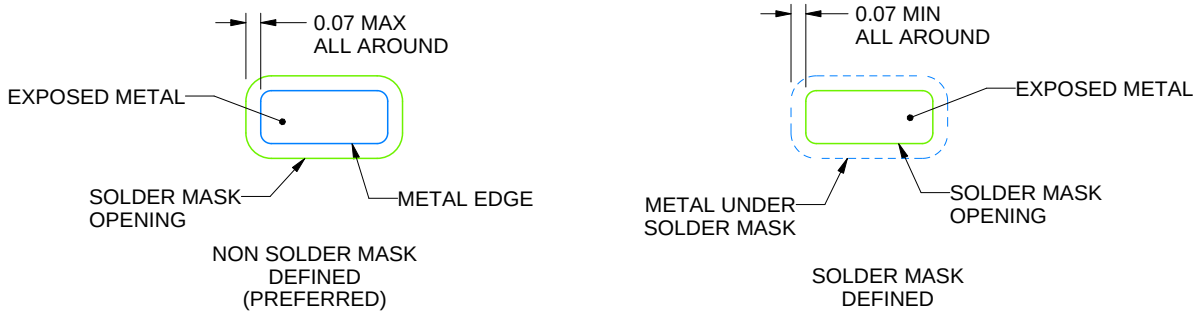


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

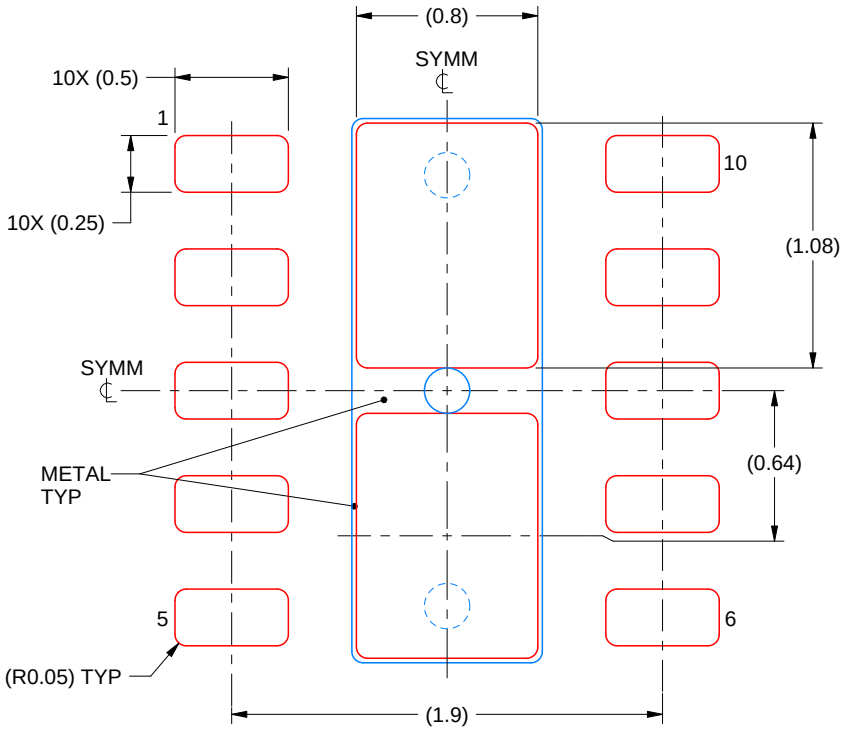


SOLDER MASK DETAILS

4222056/B 02/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
86% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4222056/B 02/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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