OPA2673 具有主动脱机控制的双路高输出电流运算放大器

1 特性

- 宽带运行：340 MHz (G = 4V/V)
- 单位增益稳定：600MHz (G = 1V/V)
- 高输出电流：700 mA
- 发生 TDMA 事件时采用主动脱机模式
- 可调功耗模式：
  - 满偏置模式：16.5 mA/通道
  - 75% 偏置模式：12.5 mA/通道
  - 50% 偏置模式：8.5 mA/通道
  - 离线模式：2.4 mA/通道
- 双极电源电压范围：±3.5 V 至 ±6.5 V
- 单电源电压范围：5.75 V 至 13 V
- 高压摆率：3500 V/µs
- 过热保护电路
- 输出电流限制 (±1A)

2 应用

- 电源线调制解调器
- 匹配的 I/Q 通道放大器
- 宽带视频线路驱动器
- ARB 线路驱动器
- 高容性负载驱动器
- 超声波压电式驱动器

3 说明

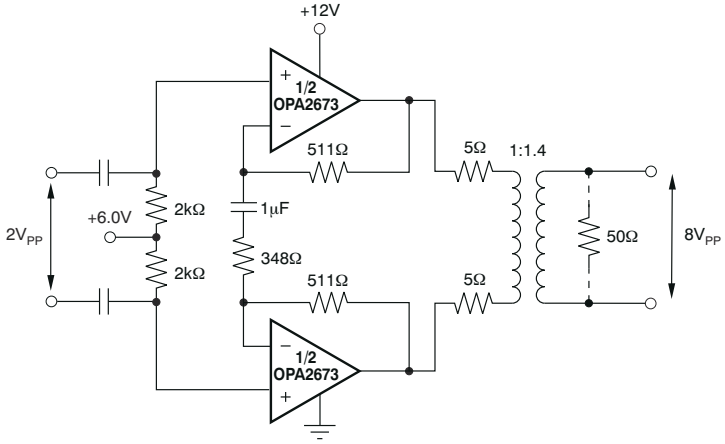
OPA2673 提供电力线调制解调器驱动器和测试测量应用所需的高输出电流和低失真。OPA2673 由 5.75V 至 13V 的电源电压供电运行，消耗 16.5mA/通道的低静态电流以提供非常高的 700mA 输出电流。OPA2673 可以通过 460mA 有保障的最小输出电流驱动（在 25°C 下）支持苛刻的电力线调制解调器要求。

包括电源控制功能，以尽可能减少系统功耗。两条逻辑控制线允许四种静态功率设置：全功率、75% 偏置功率、50% 偏置功率和具有主动离线控制的离线模式，即使输出引脚上存在大信号，也能呈现高阻抗。OPA2673 的两个通道可以作为单独的运算放大器独立使用，也可以配置为差分输入到差分输出的高电流线路驱动器。

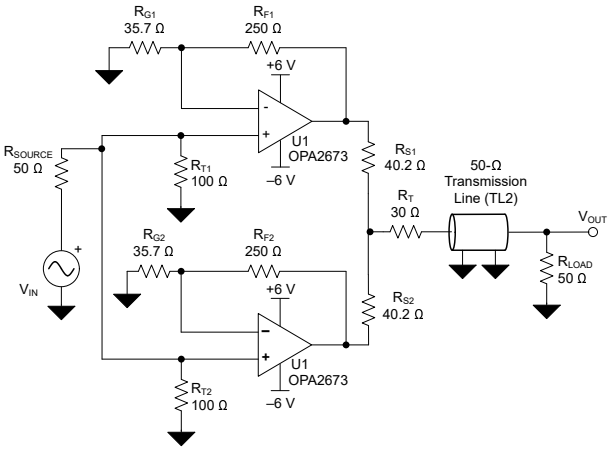
器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA2673	VQFN (16)	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



单电源 PLC 线路驱动器



50 Ω 传输线路驱动器

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (April 2010) to Revision G (December 2021) **Page**

- 添加了*器件信息* 表、*引脚功能* 表、*ESD 等级* 表、*建议运行条件* 表、*热性能信息* 表、*概述* 部分、*功能方框图* 部分、*特性说明* 部分、*器件功能模式* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 更新了整个文档的表、图和交叉参考的编号格式 1
- Changed the title of the *Related Products* section to *Device Family Comparison Table* 4
- Deleted *Package/Ordering Information* table 4
- Changed the title of the *Pin Configuration* section to *Pin Configuration and Functions* 5
- Changed QFN to VQFN throughout the document 5
- Changed all input pin current limit from ±30 mA to ±10 mA 6
- Added new thermal metric table 7
- Changed SSBW across temperaure at G = 4 V/V from 260 MHz to 300 MHz 7
- Changed SSBW across temperaure at G = 8 V/V from 260 MHz to 300 MHz 7
- Added new specifications for LSBW at gain of 9 V/V and 8 V/V 7
- Changed LSBW at G = 4 V/V from 300 MHz to 144 MHz 7
- Changed Slew Rate specification from 3000 V/µs to 3500 V/µs 7
- Changed HD2 from -68 dBc to -70 dBc 7
- Changed HD3 from -72 dBc to -73 dBc 7
- Changed noninverting input current noise from 5.2 pA/ √ Hz to 3 pA/ √ Hz 7
- Changed inverting input current noise from 35 pA/ √ Hz to 25 pA/ √ Hz 7
- Changed crosstalk from -92 dBc to -85 dBc 7
- Changed typical noninverting input resistance from 1.5 MΩ to 3 MΩ 7
- Changed minimum inverting input resistance from 16Ω to 10Ω 7
- Changed typical short circuit current limit from ±800 mA to ±1000 mA 7
- Changed typical closed-loop output impedance from 10 mΩ to 0.4 mΩ 7

- Changed maximum quiescent current at full bias from 38 mA to 42 mA.....7
- Changed maximum quiescent current across temperature at full bias from 42 mA to 46 mA 7
- Added +PSRR specification.....7
- Added AC performance data at 75% Bias.....9
- Changed HD3 spec at 75% bias from -66 dBc to -72 dBc.....9
- Changed maximum quiescent current at 75% bias from 29 mA to 31 mA.....9
- Added AC performance data at 50% Bias.....10
- Changed HD3 spec at 50% bias from -60 dBc to -70 dBc.....10
- Quiescent current at 75% and 50% bias condition at room temperature and across temperature increased by 2mA.....10
- Changed maximum quiescent current at full bias from 19 mA to 21 mA.....10

Changes from Revision E (April 2010) to Revision F (May 2010) **Page**

- Added *minimum operating voltage* (single supply) parameter.....6

Changes from Revision D (January 2010) to Revision E (April 2010) **Page**

- Revised *Absolute Maximum Ratings* table; deleted lead temperature specification, changed storage temperature range from -40°C to -65°C.....6

5 Device Family Comparison Table

SINGLES	DUALS	TRIPLES	NOTES
OPA691	OPA2691	OPA3691	Single +12 V capable
—	THS6042	—	±15 V capable
—	OPA2677	—	Single +12 V capable
—	OPA2674	—	Single +12 V capable, output current limit

6 Pin Configuration and Functions

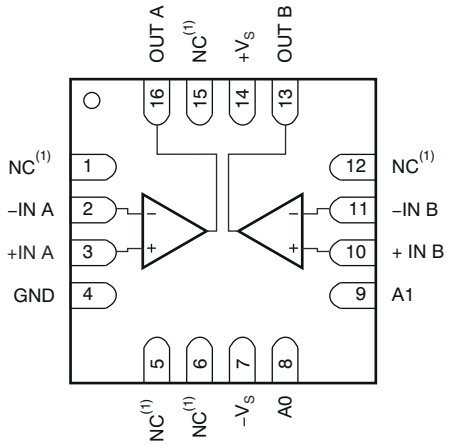


图 6-1. RGV Package, 16-Pin VQFN (Top View)

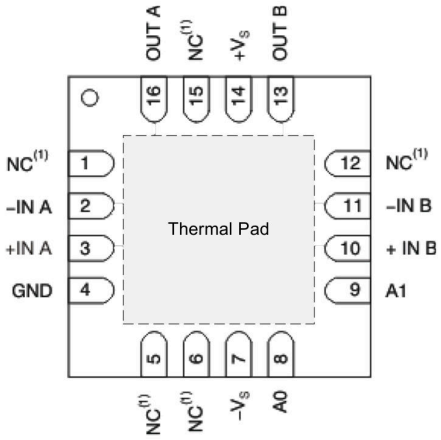


图 6-2. RGV Package, 16-Pin VQFN (Bottom View)

表 6-1. Pin Functions

PIN		TYPE(2)	DESCRIPTION
NAME	NO.		
A0	8	I	Bias Mode Control
A1	9	I	Bias Mode Control
GND	4	P	Ground
–IN A	2	I	Amplifier A inverting input
+IN A	3	I	Amplifier A noninverting input
–IN B	11	I	Amplifier B inverting input
+IN B	10	I	Amplifier B noninverting input
NC(1)	1, 5, 6, 12, 15	—	Do not connect.
OUT A	16	O	Amplifier A output
OUT B	13	O	Amplifier B output
$-V_S$	7	P	Negative power-supply connection
$+V_S$	14	P	Positive power-supply connection
Thermal Pad		—	Electrically connected to die substrate and V_{S-}. Connect to V_{S-} on the PCB for best performance.

(1) There is no internal connection. Typically GND is the recommended connection to a heat spreading plane.
(2) I = input, O = output, P = power, GND = ground, NC = no connect.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_S = (V_{S+}) - (V_{S-})$(2)		13	V
	Bias control pin voltage, referenced to GND	0	V_{S-} + 5	
	All pins except V_{S+}, V_{S-} and Bias control pins	V_{S-}	V_{S+}	
	GND Pin	V_{S-}	V_{S+}	
	Output pin: Offline mode		±4.5	
	Inverting input pin: Offline mode		±1.1	
	Differential input voltage (each amplifier)		±2	
Current	All input pins, current limit		±10	mA
	Continuous power dissipation	See Thermal Information		
Temperature	Continuous operating junction temperature(3)		139	°C
	Maximum junction, T_J (under any condition)(3)		150	
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Refer to Breakdown Test.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature can result in reduced reliability and/or lifetime of the device. OPA2673 has thermal protection that shuts down the device at approximately 180°C junction temperature and recovery at approximately 160°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, Dual Supply	±3.5		±6.5	V
V_S	Supply voltage, Single Supply	5.75		13	
GND	GND pin voltage	V_{S-}		V_{S+} – 2.5	
T_A	Ambient operating air temperature	–40	25	85	°C
	Thermal Shutdown(1)		180		

(1) OPA2673 has thermal protection that shuts down the device at approximately 180°C junction temperature and recovery at approximately 160°C.

7.4 Thermal Information

THERMAL METRIC[1]		OPA2673A RGV (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	18	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: Full Bias and Offline Mode V_S = ±6 V

At T_A = +25°C, A0 = A1 = 0 (full power), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE[1]						
SSBW	Small-signal bandwidth	G = 1 V/V, R_F = 511 Ω, V_O = 0.5 V_{PP}		600		MHz
		G = 2 V/V, R_F = 475 Ω, V_O = 0.5 V_{PP}		450		
		G = 4 V/V, R_F = 402 Ω, V_O = 0.5 V_{PP}	270	340		
		G = 4 V/V, T_A = –40°C to 85°C		300		
		G = 8 V/V, R_F = 250 Ω, V_O = 0.5 V_{PP}	270	340		
		G = 8 V/V, T_A = –40°C to 85°C		300		
	Peaking at G = 1V/V	G = 1V/V, R_F = 511 Ω		1.5		dB
	Peaking at G = 4V/V	G = 4V/V, R_F = 402 Ω		0.1		dB
LSBW	Large-signal bandwidth	G = 9 V/V, R_F = 250 Ω, V_O = 9 V_{PP}		230		MHz
	Large-signal bandwidth	G = 8 V/V, R_F = 250 Ω, V_O = 5 V_{PP}		330		
	Large-signal bandwidth	G = 4 V/V, V_O = 5 V_{PP}		144		
	±0.1-dB bandwidth flatness			70		
SR	Slew rate (20% to 80%)	V_O = 5-V step		3500		V/µs
		T_A = –40°C to 85°C	2300			
	Rise and fall time (10% to 90%)	V_O = 2-V Step		1.2		ns
HD	2nd-order harmonic distortion	V_O = 2 V_{PP}, 20 MHz, R_L = 50 Ω		–70		dBc
	3rd-order harmonic distortion			–73		
HD	2nd-order harmonic distortion	V_O = 2 V_{PP}, 20 MHz, R_L = 50 Ω, T_A = –40°C to 85°C	–63			
	3rd-order harmonic distortion		–61			
e_n	Input voltage noise	f ≥ 1 MHz, input-referred		2.4	2.62	nV/√Hz
i_{n+}	Noninverting input current noise			3	4.6	pA/√Hz
i_{n-}	Inverting input current noise			25	30	
e_n	Input voltage noise	f ≥ 1 MHz, input-referred, T_A = –40°C to 85°C			4.2	nV/√Hz
i_{n+}	Noninverting input current noise				8.3	pA/√Hz
i_{n-}	Inverting input current noise				35	
	Channel-to-channel crosstalk	f ≥ 1 MHz, input-referred		–85		dBc

7.5 Electrical Characteristics: Full Bias and Offline Mode V_S = ±6 V (continued)

At T_A = +25°C, A0 = A1 = 0 (full power), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
Z_{OL}	Open-loop transimpedance gain		60	90		kΩ
		T_A= –40°C to 85°C	55			
	Input offset voltage (each amplifier)			±2	±7	mV
		T_A = –40°C to 85°C			±9	
	Input offset voltage mismatching	Amplifier A to B		±0.5	±2.2	
		T_A = –40°C to 85°C			±2.5	
	Input offset voltage drift	T_A = –40°C to 85°C			±30	µV/°C
	Noninverting input bias current			±5	±25	µA
		T_A = –40°C to 85°C			±28	
	Inverting input bias current			±6	±48	
		T_A = –40°C to 85°C			±55	
	Noninverting input bias current matching			±0.5	±5	µA
		T_A = –40°C to 85°C			±7	
	Inverting input bias current matching			±6	±25	
		T_A = –40°C to 85°C			±30	
	Noninverting input bias current drift	T_A = –40°C to 85°C			±47	nA/°C
	Inverting input bias current drift				±110	
INPUT CHARACTERISTICS						
CMIR	Common-mode input range		±3.5	±3.6		V
		T_A= –40°C to 85°C	±3.2			
CMRR	Common-mode rejection ratio		50	56		dB
		T_A = –40°C to 85°C	47			
	Noninverting input resistance			3 || 1.5		MΩ || pF
	Inverting input resistance		10	24	40	Ω
	Shutdown Isolation,Offline Mode	Input to Output Isolation at 1 MHz		85		dB
OUTPUT CHARACTERISTICS						
V_O	Output voltage swing(2)	No Load	±4.8	±4.9		V
		No Load, T_A = –40°C to 85℃	±4.7			
V_O	Output voltage swing(2)	R_L = 100 Ω	±4.75	±4.9		V
		R_L = 100 Ω, T_A = –40°C to 85℃	±4.65			
		R_L = 25 Ω	±4.5	±4.7		
		R_L = 25 Ω, T_A = –40°C to 85℃	±4.4			
I_O	Output current (sourcing and sinking) (2)	R_L = 4 Ω	±460	±700		mA
		R_L = 4 Ω, T_A = –40°C to 85℃	±425			
	Short-circuit output current	Sourcing and Sinking		±1000		mA
Z_{OUT}	Closed-Loop output impedance	f = 100 kHz		0.4		mΩ
Z_O	Open-Loop Output impedance	f = 100 kHz, Offline Mode		25 || 4.5		kΩ || pF

7.5 Electrical Characteristics: Full Bias and Offline Mode V_S = ±6 V (continued)

At T_A = +25°C, A0 = A1 = 0 (full power), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current, Total both channels	Full bias (A0 = 0, A1 = 0)		33	42	mA
		Full bias, T_A = –40°C to 85°C			46	
		Offline Mode (A0 = 1, A1 = 1)		5.5	7.2	
		Offline Mode, T_A = –40°C to 85°C			9	
+PSRR	Positive power-supply rejection ratio	T_A = –40°C to 85℃	57	60		dB
–PSRR	Negative power-supply rejection ratio		47	55		
BIAS CONTROL						
	Bias control pin logic threshold	Logic 1, with respect to GND	2			V
		Logic 0, with respect to GND			0.8	
	Bias control pin current	A0, A1 = 0.5 V(3) , T_A = –40°C to 85°C			30	μA
		A0, A1 = 3.3 V, T_A = –40°C to 85°C			150	

(1) Min/Max limits for AC performance set by design
(2) See Output Headroom vs Output Current for output voltage vs output current characteristics.
(3) Current flows into the pins.

7.6 Electrical Characteristics: 75% Bias Mode V_S = ±6 V

At T_A = +25°C, A0 = 1, A1 = 0 (75% Bias), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	G = 4 V/V, R_F = 402 Ω, V_O = 0.5 V_{PP}		310		MHz
LSBW	Large-signal bandwidth	V_O = 4 V_{PP}		160		
SR	Slew rate (20% to 80%)	V_O = 5-V step		3000		V/μs
HD2	2nd-order harmonic distortion	V_O = 2 V_{PP}, 20 MHz ,R_L = 50 Ω		-69		dBc
HD3	3rd-order harmonic distortion			-72		
e_n	input voltage noise	f ≥ 1 MHz, input-referred		2.6		nV/√Hz
	Input offset voltage (each amplifier)			±2	±7	mV
		T_A = –40°C to 85°C			±9	
I_O	Output current (sourcing and sinking)	R_L = 4 Ω	±350	±500		mA
		R_L = 4 Ω, T_A = –40°C to 85℃	±300			
	Short-circuit output current	Sourcing and Sinking		±1000		
POWER SUPPLY						
I_Q	Quiescent current, Total both channels			25	31	mA
		T_A = –40°C to 85°C			34	

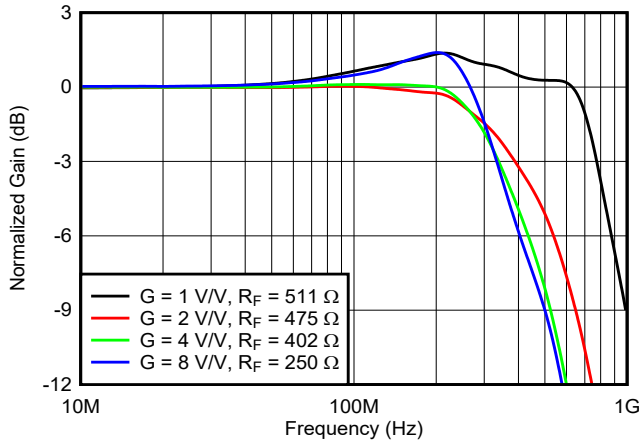
7.7 Electrical Characteristics: 50% Bias Mode V_S = ±6 V

At T_A = +25°C, A0 = 0 , A1 = 1 (50% Bias), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	G = 4 V/V, R_F = 402 Ω, V_O = 0.5 V_{PP}		260		MHz
LSBW	Large-signal bandwidth	V_O = 4 V_{PP}		140		
SR	Slew rate (20% to 80%)	V_O = 5-V step		2700		V/µs
HD2	2nd-order harmonic distortion	V_O = 2 V_{PP}, 20 MHz, R_L = 50 Ω		-66		dBc
HD3	3rd-order harmonic distortion			-70		
e_n	input voltage noise	f ≥ 1 MHz, input-referred		3.2		nV/√Hz
	Input offset voltage (each amplifier)			±2	±7	mV
		T_A = –40°C to 85°C			±9	
I_O	Output current (sourcing and sinking)	R_L = 4 Ω	±120	±180		mA
		R_L = 4 Ω, T_A = –40°C to 85℃	±110			
	Short-circuit output current	Sourcing and Sinking		±1000		
POWER SUPPLY						
I_Q	Quiescent current, Total both channels			17	21	mA
		T_A = –40°C to 85°C			23	

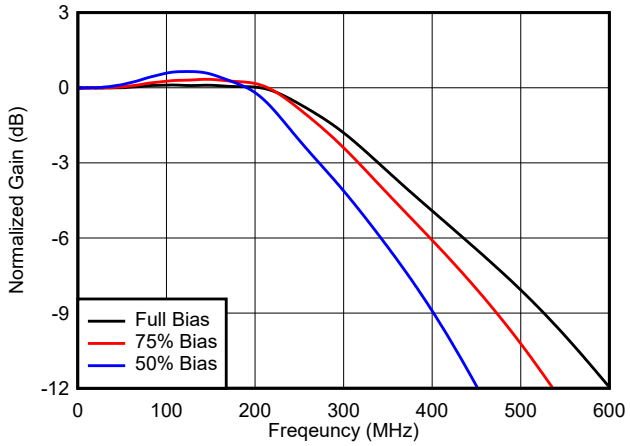
7.8 Typical Characteristics: V_S = ±6 V, Full Bias

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.



V_O = 500 mV_{PP}

图 7-1. Small-Signal Frequency Response



V_O = 500 mV_{PP}

图 7-2. Small-Signal Frequency Response Over Power Settings

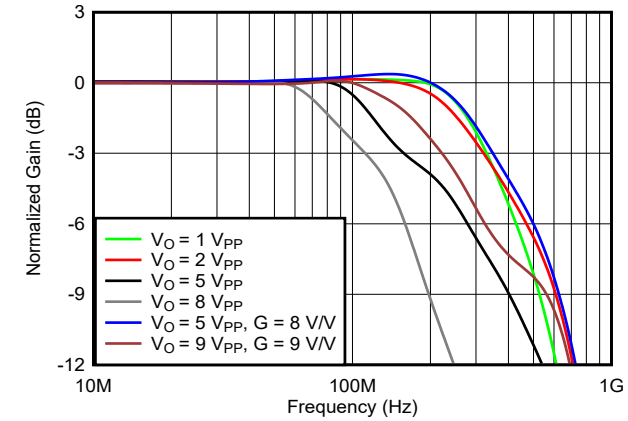
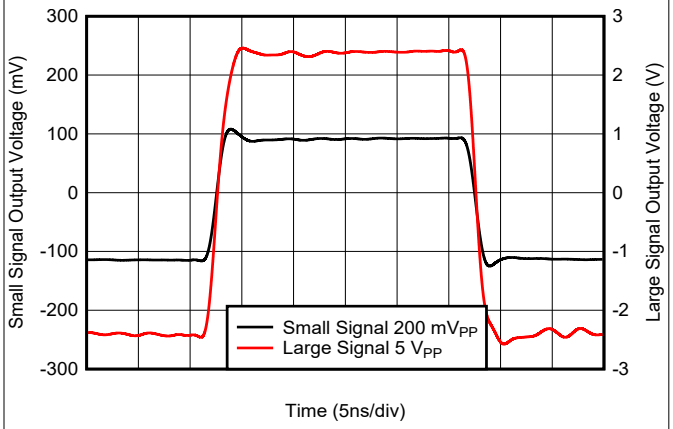
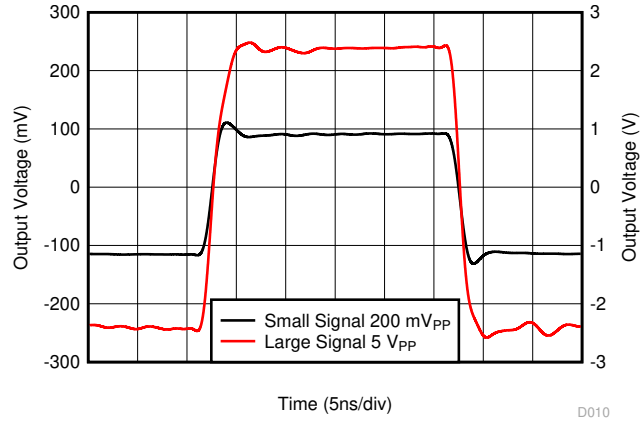


图 7-3. Large-Signal Frequency Response



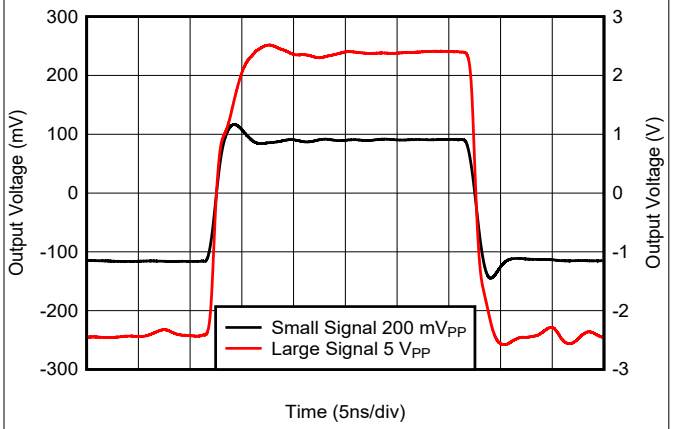
Full Bias Mode

图 7-4. Small-Signal and Large-Signal Pulse Responses



75% Bias Mode

图 7-5. Small-Signal and Large-Signal Pulse Responses



50% Bias Mode

图 7-6. Small-Signal and Large-Signal Pulse Responses

7.8 Typical Characteristics: V_S = ±6 V, Full Bias (continued)

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.

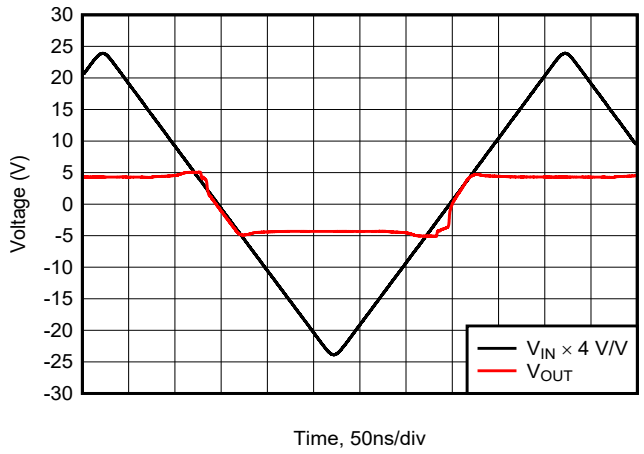


图 7-7. Overdrive Recovery

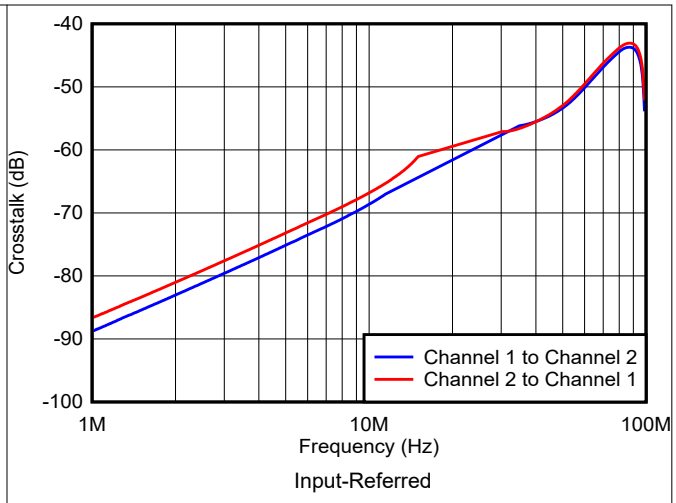


图 7-8. Channel-to-Channel Crosstalk

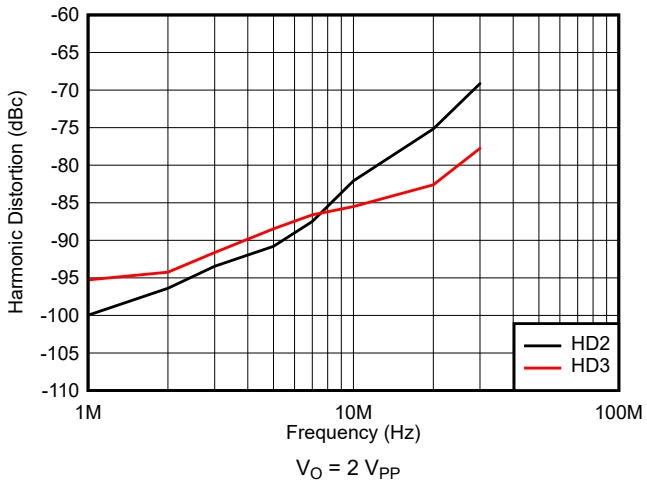


图 7-9. Harmonic Distortion vs Frequency

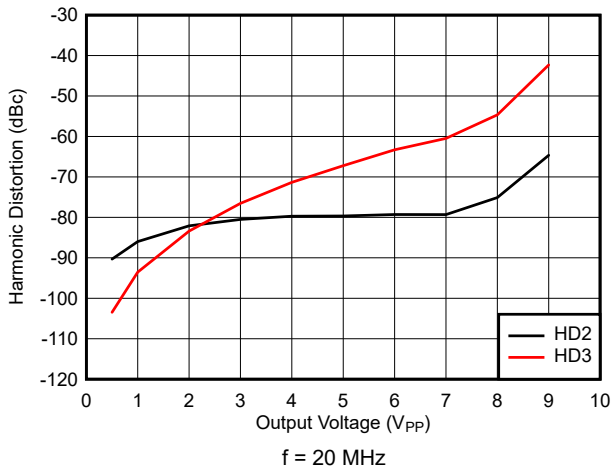


图 7-10. Harmonic Distortion vs Output Voltage

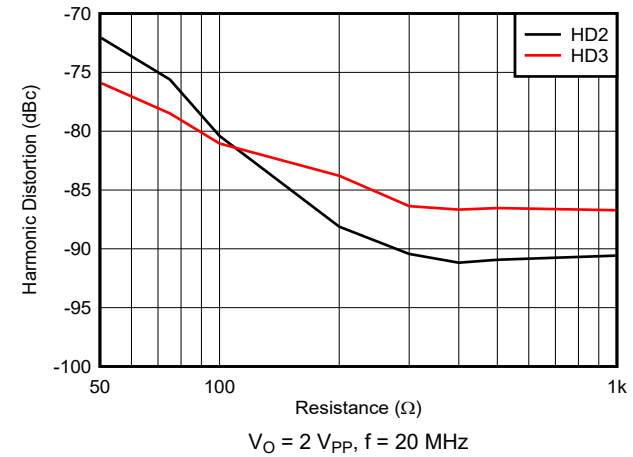


图 7-11. Harmonic Distortion vs Load Resistance

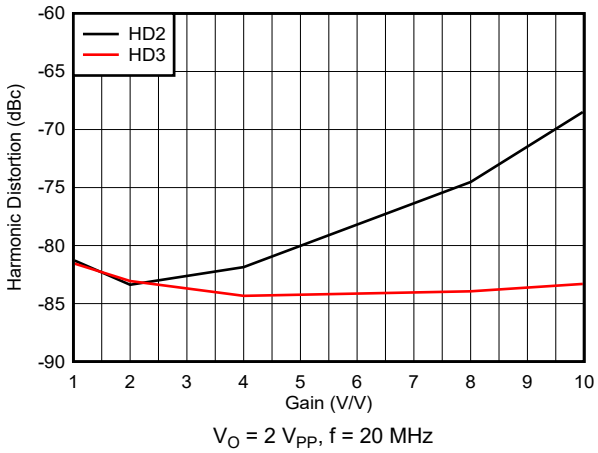


图 7-12. Harmonic Distortion vs Noninverting Gain

7.8 Typical Characteristics: V_S = ±6 V, Full Bias (continued)

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.

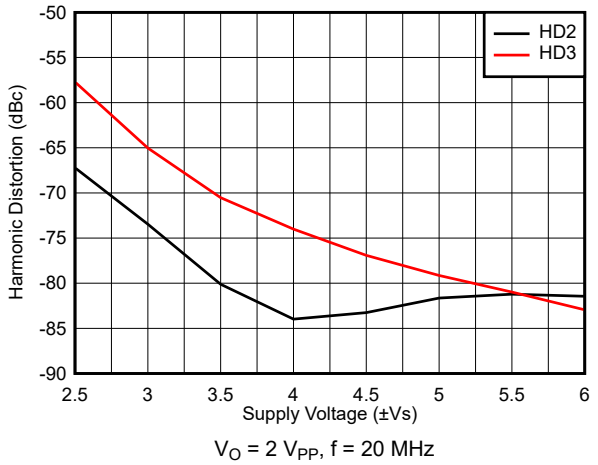


图 7-13. Harmonic Distortion vs Supply Voltage

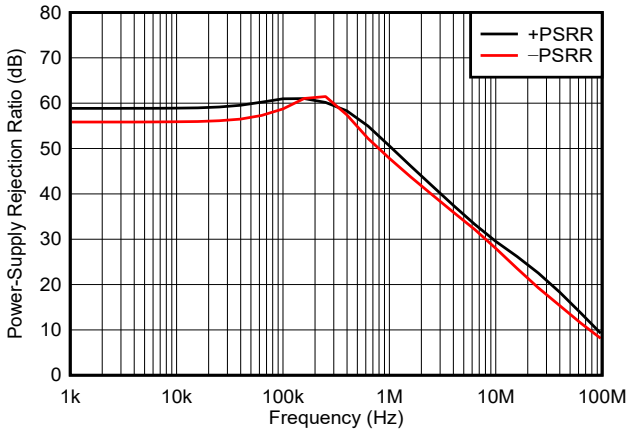


图 7-14. CMRR and PSRR vs Frequency

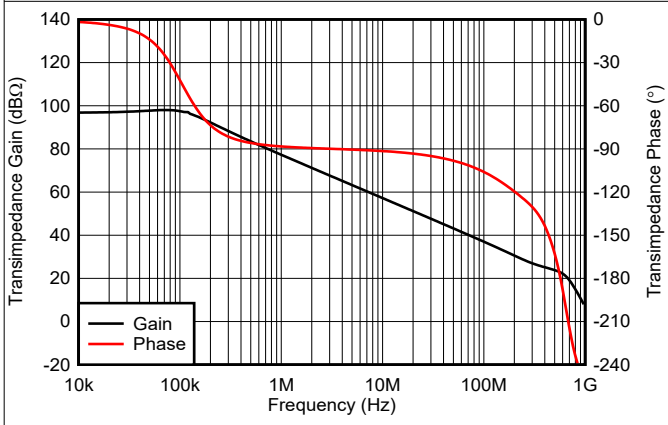


图 7-15. Open-Loop Transimpedance Gain and Phase

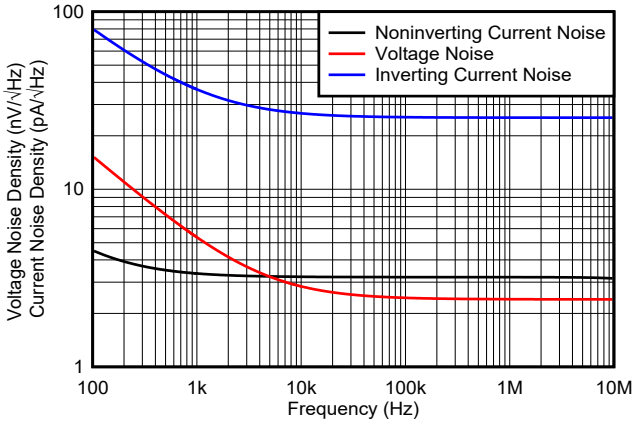


图 7-16. Input Voltage and Current Noise Density

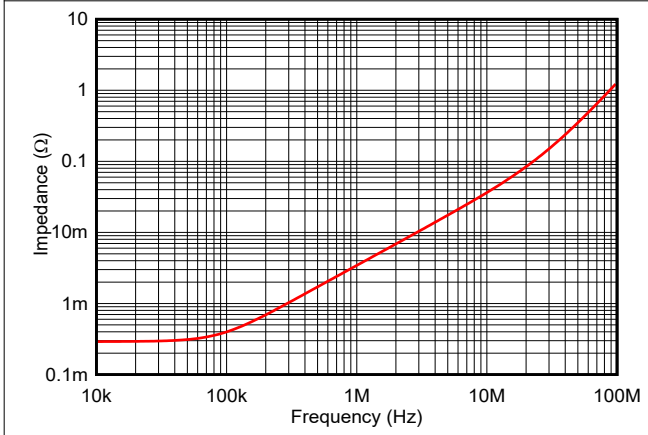


图 7-17. Closed-Loop Output Impedance vs Frequency

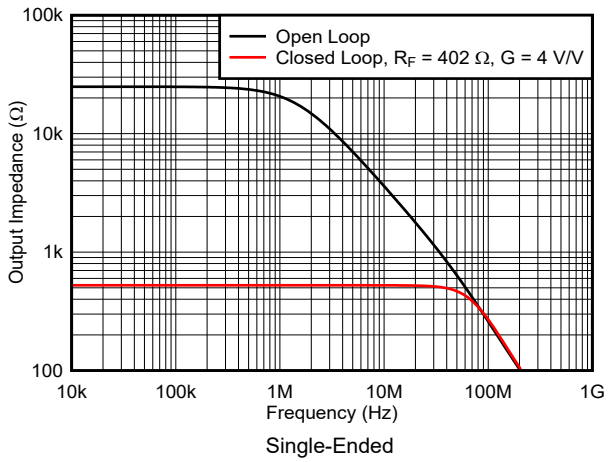


图 7-18. Active Off-Line Impedance vs Frequency

7.8 Typical Characteristics: V_S = ±6 V, Full Bias (continued)

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.

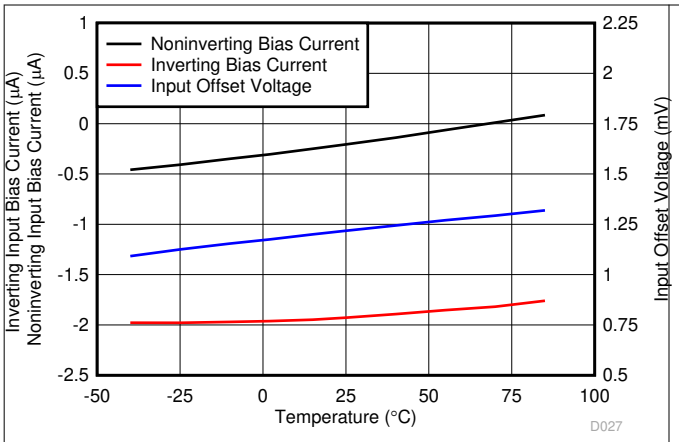


图 7-19. Typical DC Drift Over Temperature

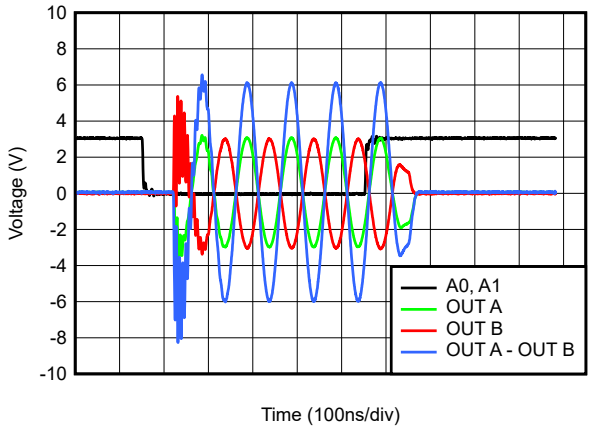


图 7-20. Full Bias Mode to Offline Mode Transition Time

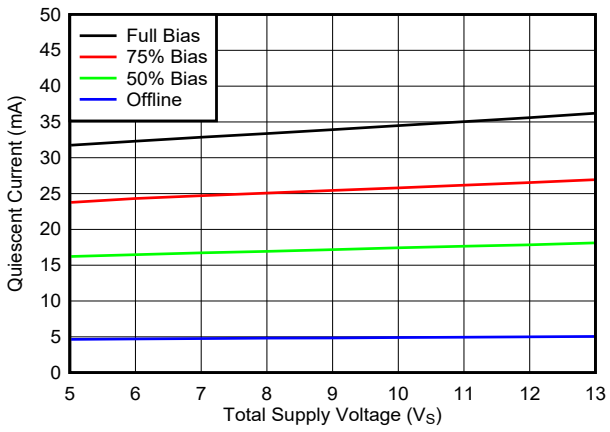


图 7-21. Supply Current vs Supply Voltage

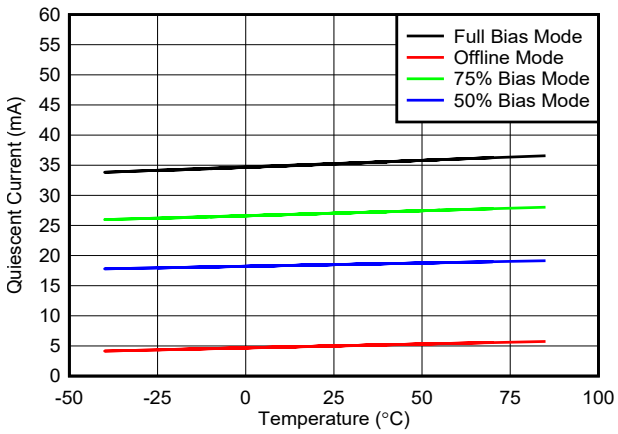
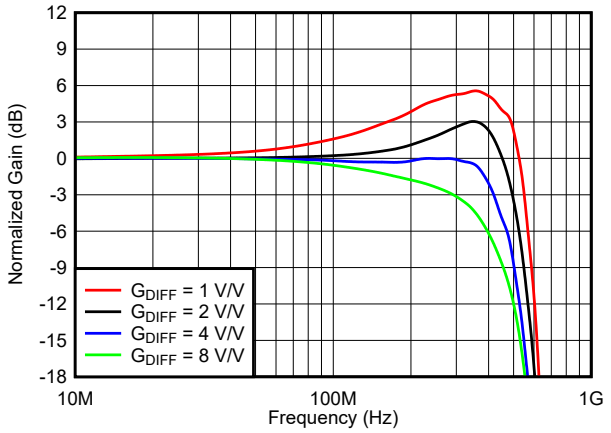


图 7-22. Supply Current vs Temperature

7.9 Typical Characteristics: V_S = ±6 V Differential, Full Bias

At T_A = +25°C, R_F = 511 Ω, R_L = 100 Ω Differential, G_{DIFF} = +4 V/V, and G_{CM} = +1 V/V, unless otherwise specified.



V_O = 500 mV_{PP}

图 7-23. Small-Signal Frequency Response

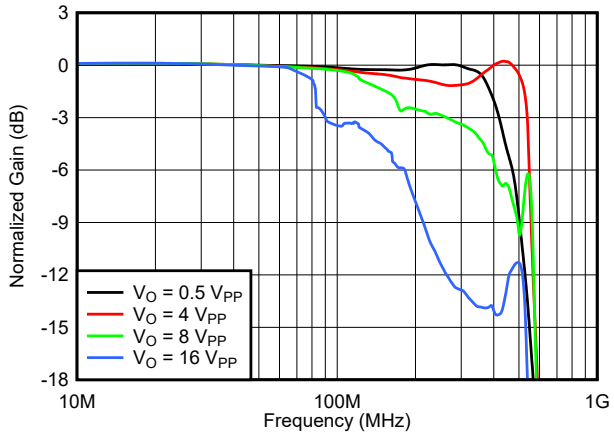


图 7-24. Large-Signal Frequency Response

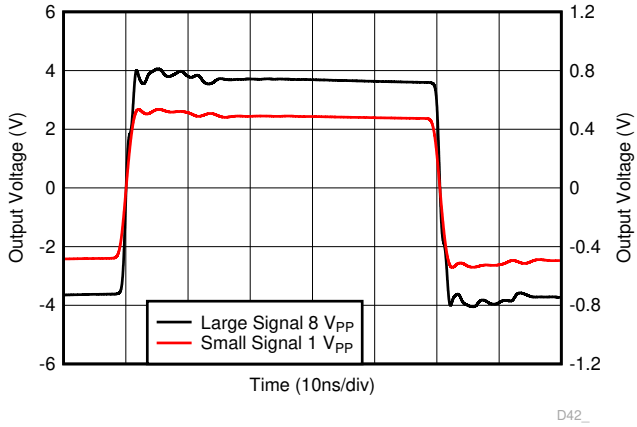
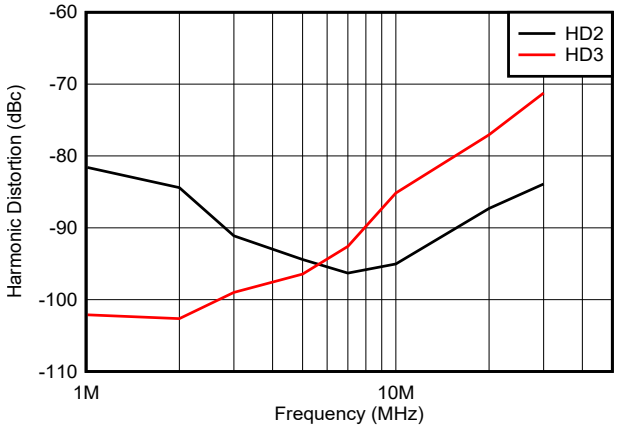
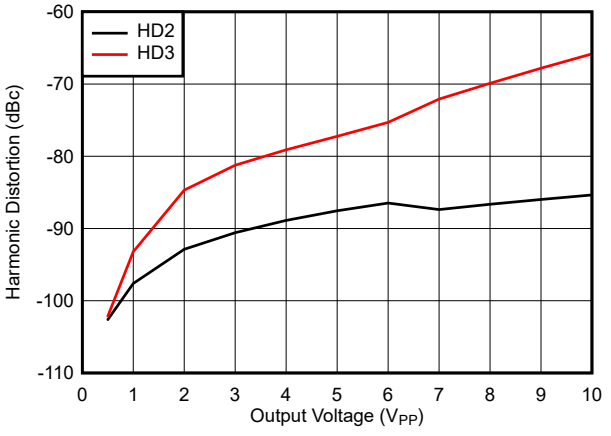


图 7-25. Small-Signal and Large-Signal Pulse Responses



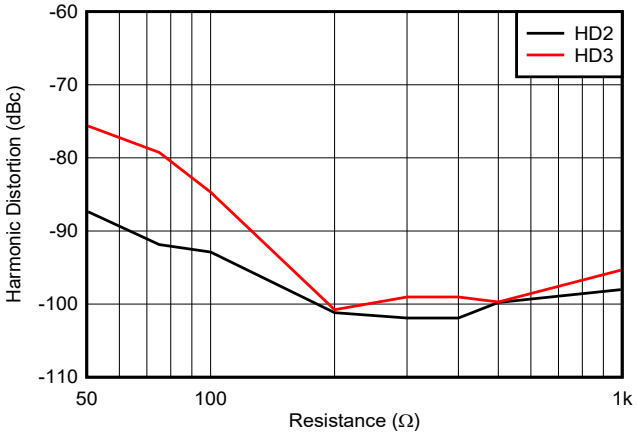
V_O = 2 V_{PP}

图 7-26. Harmonic Distortion vs Frequency



f = 20 MHz

图 7-27. Harmonic Distortion vs Output Voltage

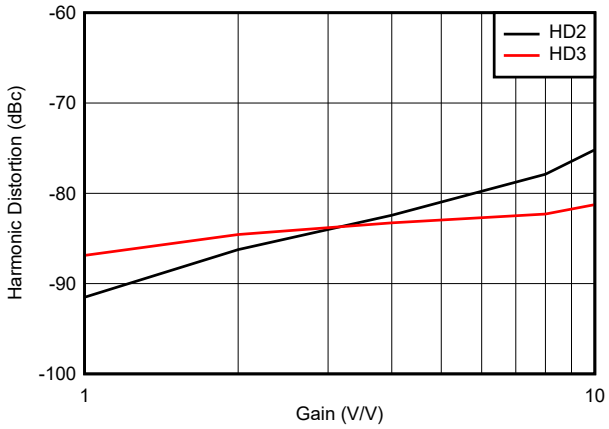


V_O = 2 V_{PP}, f = 20 MHz

图 7-28. Harmonic Distortion vs Load Resistance

7.9 Typical Characteristics: V_S = ±6 V Differential, Full Bias (continued)

At T_A = +25°C, R_F = 511 Ω, R_L = 100 Ω Differential, G_{DIFF} = +4 V/V, and G_{CM} = +1 V/V, unless otherwise specified.

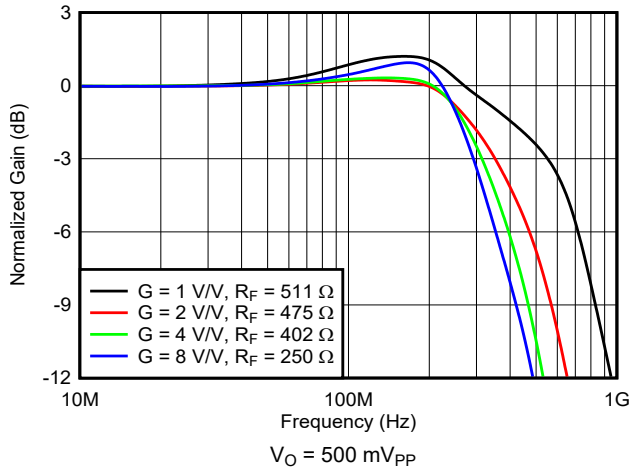


V_O = 2 V_{PP}, f = 20 MHz

图 7-29. Harmonic Distortion vs Noninverting Gain

7.10 Typical Characteristics: V_S = ±6 V, 75% Bias

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.



V_O = 500 mV_{PP}

图 7-30. Small-Signal Frequency Response

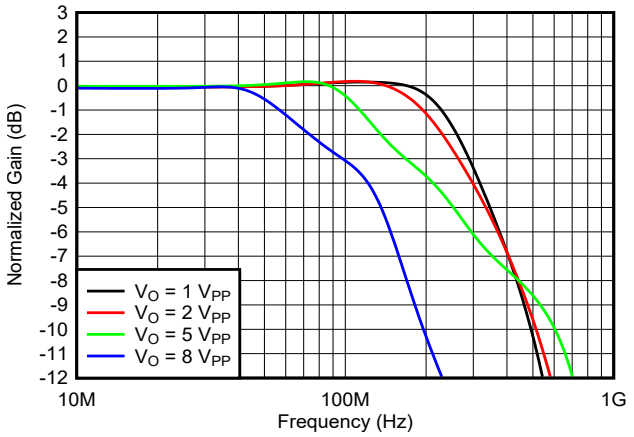
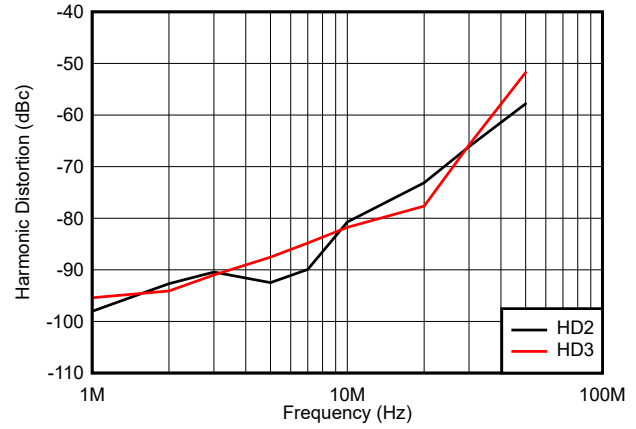
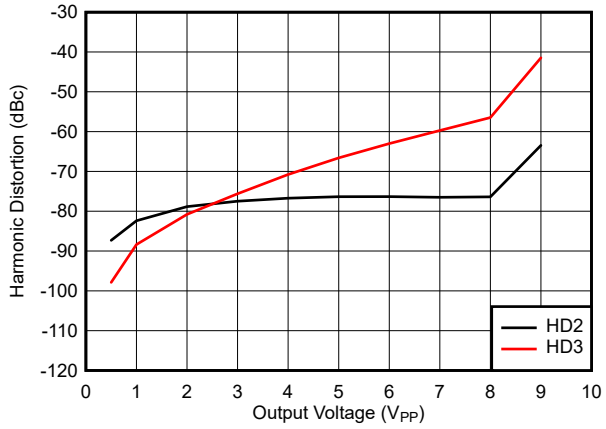


图 7-31. Large-Signal Frequency Response



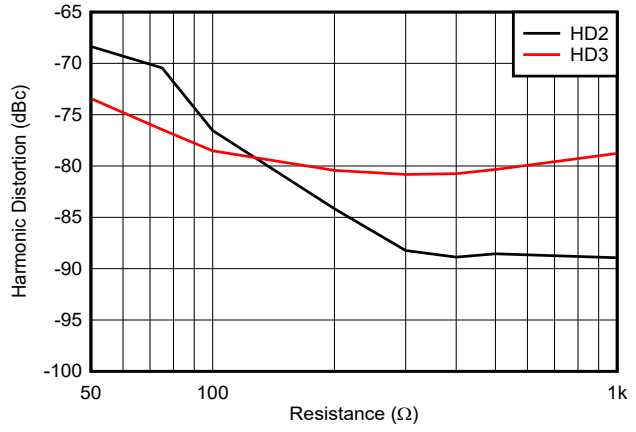
V_O = 2 V_{PP}

图 7-32. Harmonic Distortion vs Frequency



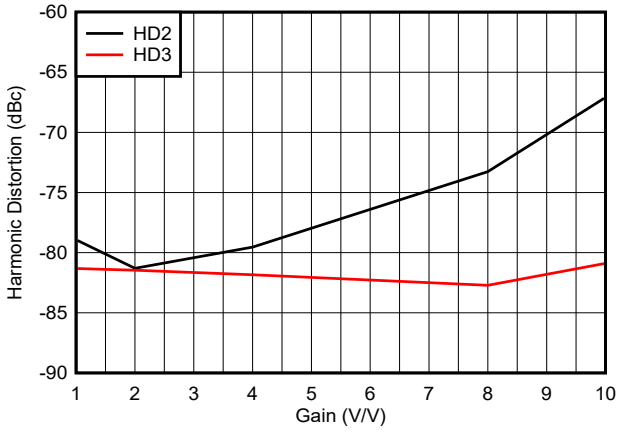
f = 20 MHz

图 7-33. Harmonic Distortion vs Output Voltage



V_O = 2 V_{PP}, f = 20 MHz

图 7-34. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 20 MHz

图 7-35. Harmonic Distortion vs Noninverting Gain

7.11 Typical Characteristics: V_S = ±6 V, 50% Bias

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.

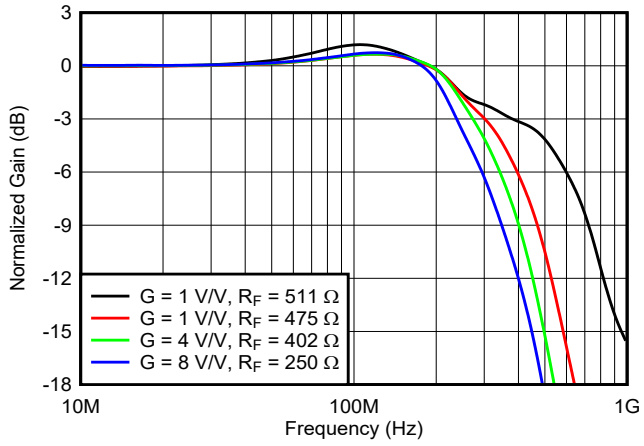


图 7-36. Small-Signal Frequency Response

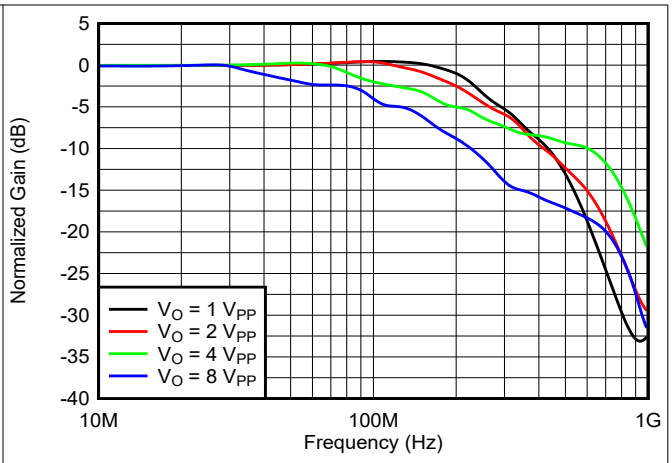
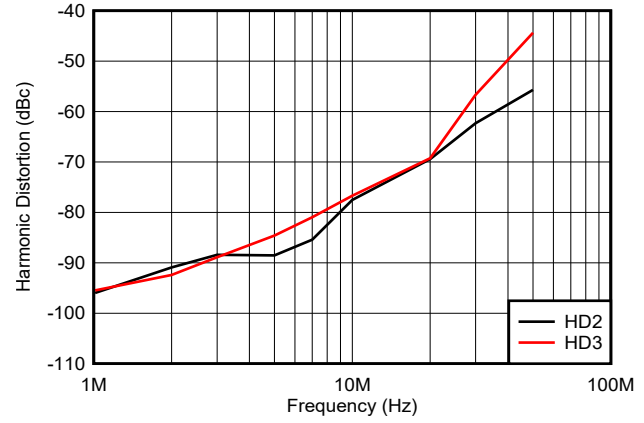
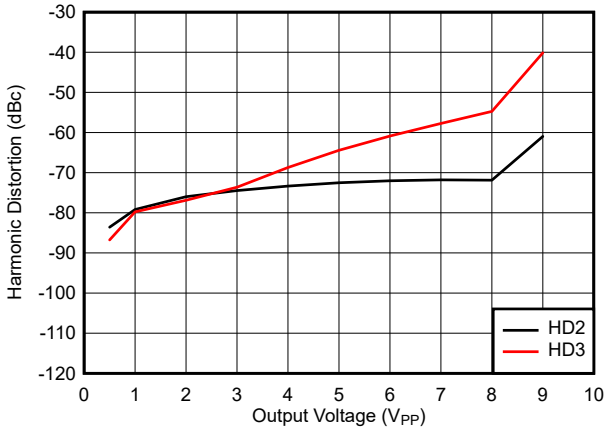


图 7-37. Large-Signal Frequency Response



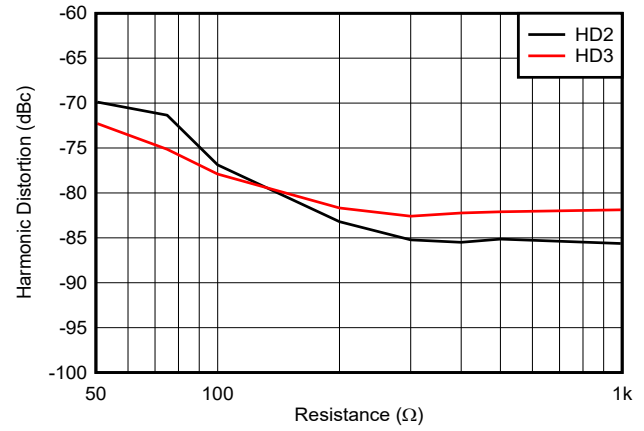
V_O = 2 V_{PP}

图 7-38. Harmonic Distortion vs Frequency



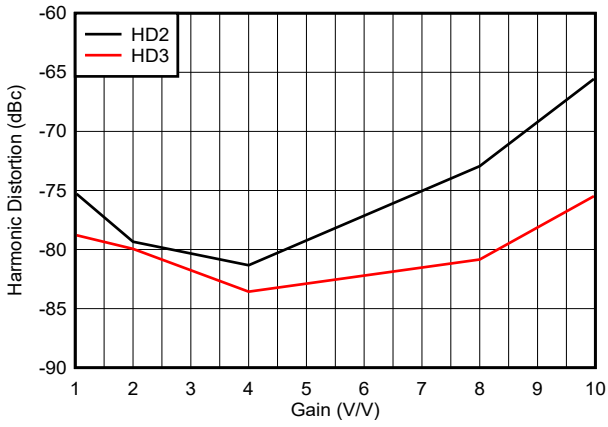
f = 20 MHz

图 7-39. Harmonic Distortion vs Output Voltage



V_O = 2 V_{PP}, f = 20 MHz

图 7-40. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 20 MHz

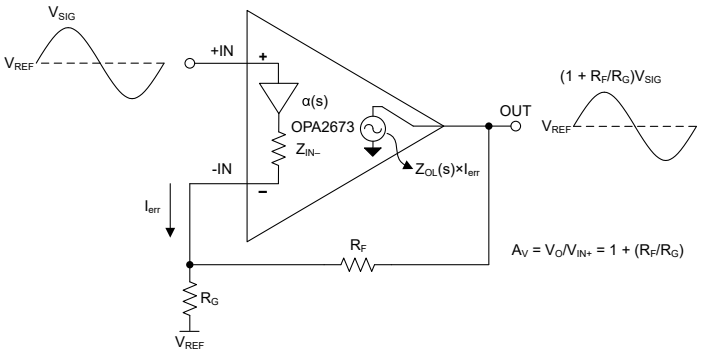
图 7-41. Harmonic Distortion vs Noninverting Gain

8 Detailed Description

8.1 Overview

The OPA2673 is a high-speed, high-current output, current-feedback amplifier (CFA) designed to operate over a wide supply range of ±3.5 V to ±6.5 V for applications requiring large-drive currents along with wide-bandwidth. The OPA2673 features an offline-mode that enables the amplifier to operate in a high-output impedance condition ensuring no loading to the network when connected in a bus-topology. 图 3-1 shows how the two channels of the OPA2673 can be used as two independent amplifiers or can be connected in a differential-input to differential-output configuration.

8.2 Functional Block Diagram



8.3 Feature Description

The OPA2673 gives exceptional ac performance with a highly linear, high-power output stage. Requiring 16-mA/ch quiescent current, the OPA2673 swings to within 1.1 V of either supply rail and delivers in excess of 460 mA at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable dual (±6 V) supply operation. The OPA2673 delivers greater than 450 MHz bandwidth driving a 2 V_{PP} output into 100 Ω on a single +12 V supply.

The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that ac performance (bandwidth and distortion) is relatively independent of signal gain. 图 8-1 shows the dc-coupled, gain of +4 V/V, dual power-supply circuit configuration used as the test circuit for the ±6 V *Electrical Characteristics* and *Typical Characteristics*. Voltage swings reported in the *Electrical Characteristics* are taken directly at the input and output pins. For measuring the ac performance, the output of the OPA2673 is terminated with a matched 50 Ω loading. Thus, the total effective load seen by the OPA2673 is 100 Ω || 402 Ω = 80 Ω.

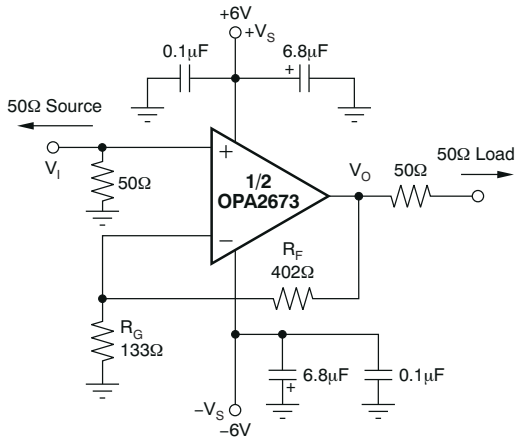


图 8-1. DC-Coupled, G = +4 V/V, Bipolar Supply

8.3.1 Operating Suggestions

8.3.1.1 Setting Resistor Values to Optimize Bandwidth

A current-feedback op amp such as the OPA2673 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values, which are shown in the *Typical Characteristics*; the small-signal bandwidth decreases only slightly with increasing gain. These characteristic curves also show that the feedback resistor is changed for each gain setting. The absolute values of R_F on the inverting side of the circuit for a current-feedback op-amp can be treated as frequency response compensation element, whereas the ratios of R_F and R_G set the signal gain.

图 8-2 shows the small-signal frequency response analysis circuit for the OPA2673.

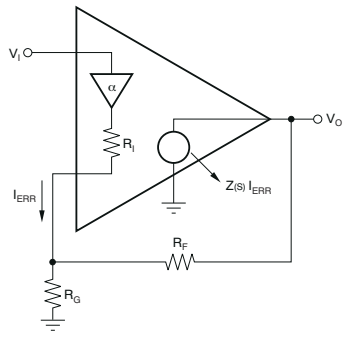


图 8-2. Current-Feedback Transfer Function Analysis Circuit

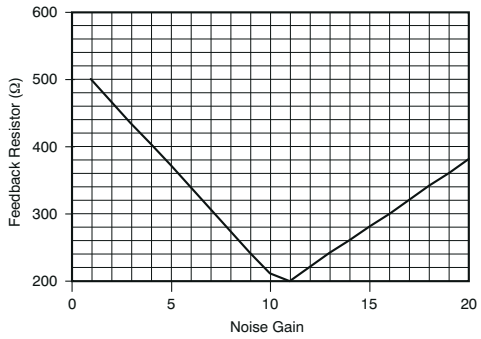


图 8-3. Feedback Resistor Versus Noise Gain

The key elements of this current-feedback op amp model are:

α = buffer gain from the noninverting input to the inverting input

R_I = buffer output impedance

I_{ERR} = feedback error current signal

Z(s) = frequency-dependent open-loop transimpedance gain from I_{ERR} to V_O

$$NG = \text{Noise Gain} = 1 + \frac{R_F}{R_G} \tag{1}$$

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency-dependent transimpedance gain. The *Typical Characteristics* show this open-loop transimpedance response, which is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Refer to the training videos shown in *TI Precision Labs* for further understanding on the CFA operating theory.

The values for R_F versus gain shown in 图 8-3 are approximately equal to the values used to generate the *Typical Characteristics* and give a good starting point for designs where bandwidth optimization is desired.

8.3.1.2 Output Current and Voltage

The OPA2673 provides output voltage and current capabilities that are unsurpassed in a low-cost dual monolithic op amp. Under no-load conditions at +25°C, the output voltage typically swings closer than 1.1 V to either supply rail; the tested (+25°C) swing limit is within 1.2 V of either rail. The OPA2673 is capable of delivering around 700 mA of source and sink current at room temperature. 图 8-4 and 图 8-5 shows the relation between current output of the OPA2673 at different temperatures and maximum voltage swing at that current output under loaded conditions.

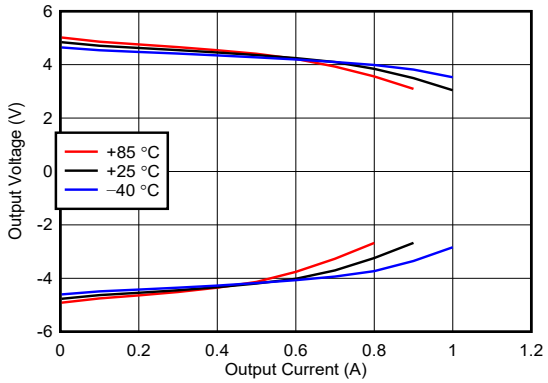


图 8-4. Output Headroom vs Output Current

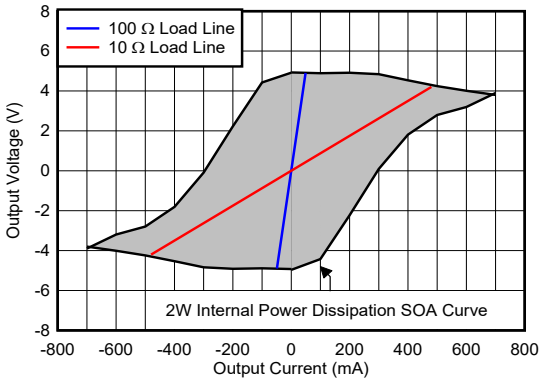


图 8-5. Output Voltage and Current Limitations

For the specifications described previously, consider voltage and current limits separately. In many applications, it is the voltage times the current (or V-I product) that is more relevant to circuit operation. See 图 8-5.

图 8-5 shows the zero-voltage output current limit and the zero-current output voltage limit on the X- and Y-axes, respectively. The four quadrants give a more detailed view of the OPA2673 output drive capabilities, noting that the graph is bounded by a safe operating area of 2W maximum internal power dissipation (in this case, for one channel only). Superimposing resistor load lines onto the plot shows that the OPA2673 can drive ±4 V into 10 Ω or ±4.5 V into 25 Ω without exceeding the output capabilities or the 2-W dissipation limit. A 100 Ω load line (the standard test circuit load) shows the full ±4.8 V output swing capability, as stated in the *Electrical Characteristics* table.

8.3.1.3 Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. The capacitive load is often the input of an analog-to-digital converter (ADC), including additional external capacitance that may be recommended to improve the ADC linearity. A high-speed, high open-loop gain amplifier such as the OPA2673 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested.

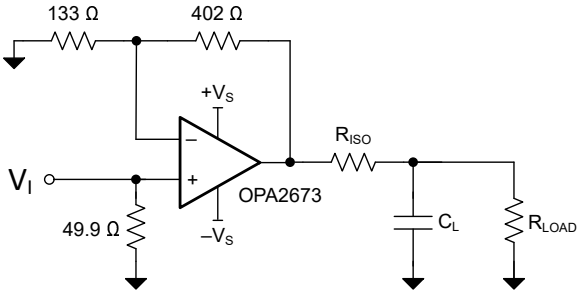


图 8-6. Driving a Large Capacitive Load Using an Output Series Isolation Resistor

When the primary considerations are frequency response flatness, pulse response fidelity, and distortion, the simplest and most effective solution is to isolate the capacitive load (C_L) from the feedback loop by inserting a series isolation resistor (R_{ISO}) between the amplifier output and the capacitive load as shown in 图 8-6. This approach does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. 图 8-7 and 图 8-8 shows the *Recommended R_{ISO} vs C_L* and the resulting frequency response with the optimized R_{ISO} value.

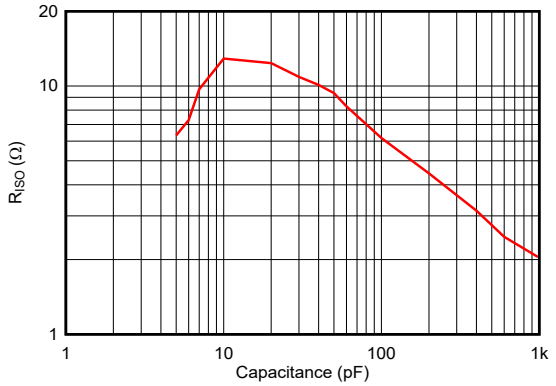


图 8-7. Recommended R_{ISO} vs Capacitive Load

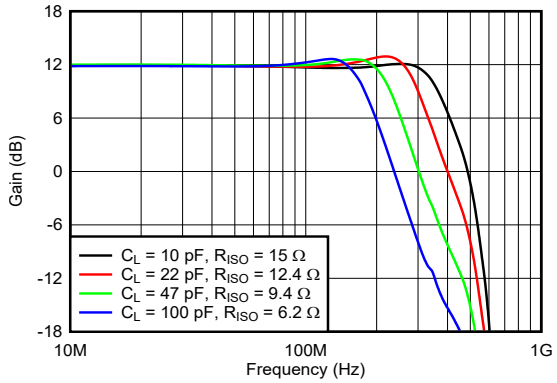


图 8-8. Frequency Response vs Capacitive Load

8.3.1.4 Line Driver Headroom Model

The first step in a driver design is to compute the peak-to-peak output voltage from the target specifications. This calculation is done using the following equations:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1mW) \times R_L} \quad (2)$$

With P_L power and V_{RMS} voltage at the load, and R_L load impedance, this calculation gives:

$$V_{RMS} = \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (3)$$

$$V_P = \text{CrestFactor} \times V_{RMS} = CF \times V_{RMS} \quad (4)$$

With V_P peak voltage at the load and the crest factor, CF:

$$V_{LPP} = 2 \times CF \times V_{RMS} \quad (5)$$

with V_{LPP}: peak-to-peak voltage at the load.

Consolidating 方程式 2 through 方程式 5 allows the required peak-to-peak voltage at the load function of the crest factor, the load impedance, and the power in the load to be expressed. Thus:

$$V_{LPP} = 2 \times CF \times \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (6)$$

This V_{LPP} is usually computed for a nominal line impedance and may be taken as a fixed design target.

The next step for the driver is to compute the individual amplifier output voltage and currents as a function of V_{PP} on the line and transformer turns ratio. As the turns ratio changes, the minimum allowed supply voltage also changes. The peak current in the amplifier is given by:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4R_M} \quad (7)$$

With V_{LPP} defined in 方程式 6 and R_M defined in 方程式 8.

$$R_M = \frac{Z_{LINE}}{2n^2} \quad (8)$$

The peak current is computed in 图 8-9 by noting that the total load is $4R_M$ and that the peak current is half of the peak-to-peak calculated using V_{LPP}.

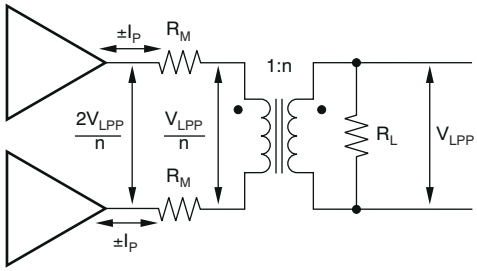


图 8-9. Driver Peak Output Model

With the required output voltage and current versus turns ratio set, an output stage headroom model allows the required supply voltage versus turns ratio to be developed.

The headroom model (see 图 8-10) can be described with the following set of equations:

First, as available output voltage for each amplifier:

$$V_{OPP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \quad (9)$$

Or, second, as required single-supply voltage:

$$V_{CC} = V_{OPP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \quad (10)$$

The minimum supply voltage for a set of power and load requirements is given by 方程式 10. Where V_1, V_2, R_1, and R_2 are internal to the OPA2673, and values of the same are provided below.

表 8-1 gives V_1, V_2, R_1, and R_2 for +12-V operation of the OPA2673.

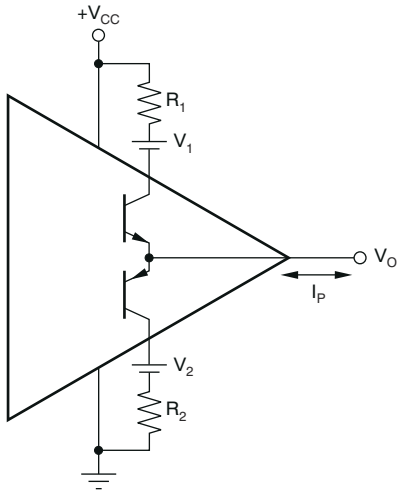


图 8-10. Line Driver Headroom Model

表 8-1. Line Driver Headroom Model Values

V_1	R_1	V_2	R_2
0.9 V	2 Ω	0.9 V	2 Ω

8.3.1.5 Noise Performance

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2673 offers an excellent balance between voltage and current noise terms to achieve low output noise. The low input voltage noise is achieved at the price of higher noninverting input current noise (3 pA/√Hz). As long as the ac source impedance from the noninverting node is less than 100 Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. 图 8-11 shows the op amp noise analysis model with all noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. 方程式 11 shows the general form for the output noise voltage using the terms given in 图 8-11.

$$E_O = \sqrt{\left[E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right] \times NG + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (11)$$

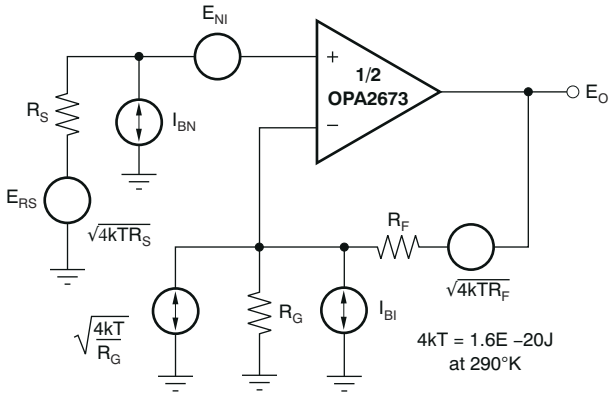


图 8-11. Op Amp Noise Analysis Model

Dividing this expression by the noise gain [NG = (1 + R_F / R_G)] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in 方程式 12.

$$E_I = \sqrt{E_{NI}^2 + (I_{BN} \times R_S)^2 + 4kTR_S + \frac{(I_{BI} \times R_F)^2}{NG^2} + \frac{4kTR_F}{NG}} \quad (12)$$

Evaluating these two equations for the OPA2673 circuit and component values of 图 8-1 gives a total output spot noise voltage of 15.6 nV/√Hz and a total equivalent input spot noise voltage of 3.9 nV/√Hz. This total input-referred spot noise voltage is higher than the 2.4 nV/√Hz specification for the op amp voltage noise alone. This result is due to the noise added to the output by the inverting current noise times the feedback resistor 402 Ω in this case. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input-referred voltage noise given by 方程式 12 approaches only the 2.4 nV/√Hz of the op amp. For example, going to a gain of +8 V/V using R_F = 250 Ω gives a total input-referred noise of 2.9 nV/√Hz.

8.4 Device Functional Modes

OPA2673 has four different functional modes set by the A0 and A1 pins. 表 8-2 shows the truth table for the device mode pin configuration and the associated description of each mode.

表 8-2. A0 and A1 Logic Table

A0	A1	FUNCTION	DESCRIPTION
0	0	Full-bias mode (100%)	Both amplifiers are on with the lowest distortion possible
1	0	Mid-bias mode (75%)	Both amplifiers are on with power savings and a reduction in distortion performance
0	1	Low-bias mode (50%)	Both amplifiers are on with enhanced power savings and a reduction of overall performance
1	1	Offline mode	Both amplifiers are off and the output is high impedance

OPA2673 can be switched between the full-bias and offline mode using just one control bit by tying the A0 and A1 together. If switching between the mid-bias or low-bias modes and the offline mode is required for the application, then either the A0 or A1 pin can be connected to ground and the control pin can be connected to the non-grounded BIAS pin.

The OUT pin of OPA2673 enters high output impedance in offline mode. However, due to the presence of the feedback resistance R_F as shown in 图 8-12, the impedance seen by the load looking into the OPA2673 is (high impedance || R_F), making the net impedance as seen from the load equal to R_F. The maximum voltage allowed to be incident on the OUT pin and the Inverting Input pin during offline mode is mentioned in the *Absolute Maximum Ratings* table. The voltage appearing on the Inverting Input pin is a resistor divided value of the voltage on the OUT pin as shown in 图 8-12. Care should be taken to ensure both the absolute maximum limits mentioned for the OUT and Inverting pins are satisfied.

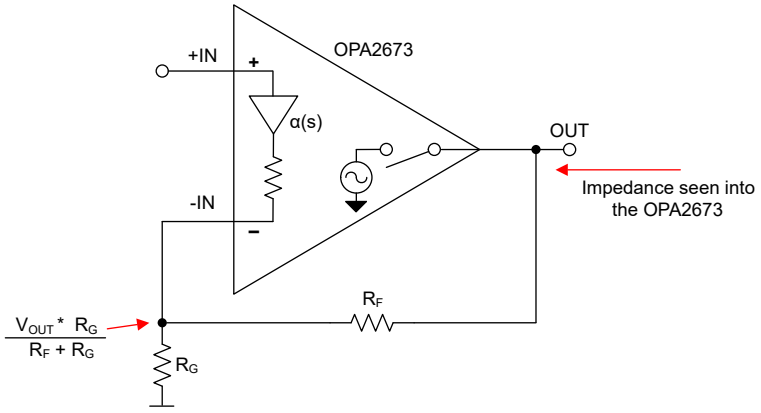


图 8-12. OPA2673 Offline Mode

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 High-Speed Active Filters

9.1.1.1 Design Requirements

Wideband current-feedback op amps make ideal elements for implementing high-speed active filters where the amplifier is used as a fixed gain block inside a passive RC circuit network. The relatively constant bandwidth versus gain provides low interaction between the actual filter poles and the required gain for the amplifier. shows an example single-supply buffered filter application. In this case, one of the OPA2673 channels is used to set up the dc operating point and provide impedance isolation from the signal source into the second-stage filter. That stage is set up to implement a 20 MHz, maximally flat Butterworth frequency response and provide an ac gain of +4 V/V.

9.1.1.2 Detailed Design Procedure

The 51 Ω input matching resistor is optional in this case. The input signal is ac-coupled to the 5 V dc reference voltage developed through the resistor divider from the +10 V power supply. This first stage acts as a gain of +1 V/V voltage buffer for the signal where the 600-Ω feedback resistor is required for stability. This first stage easily drives the low input resistors required at the input of this high-frequency filter. The second stage is set for a dc gain of +1 V/V, carrying the 5-V operating point through to the output pin, and an ac gain of +4 V/V. The feedback resistor has been adjusted to optimize bandwidth for the amplifier itself. As the single-supply frequency response plots show, the OPA2673 in this configuration gives greater than 400 MHz small-signal bandwidth. The capacitor values were chosen as low as possible but adequate to override the parasitic input capacitance of the amplifier. The resistor values were slightly adjusted to give the desired filter frequency response while accounting for the approximate 1 ns propagation delay through each channel of the OPA2673.

9.1.1.3 Application Curves

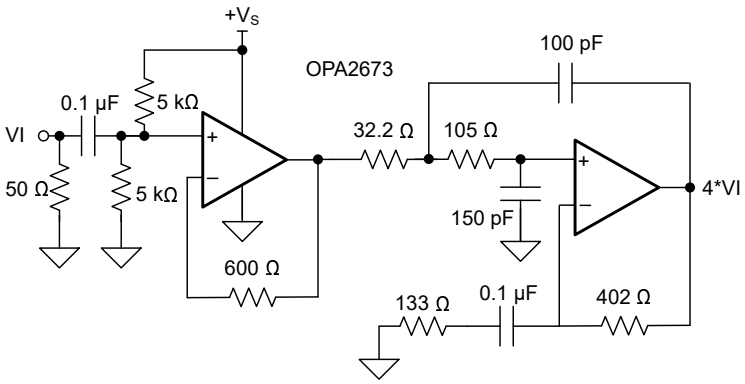


图 9-1. Buffered Single-Supply Active Filter

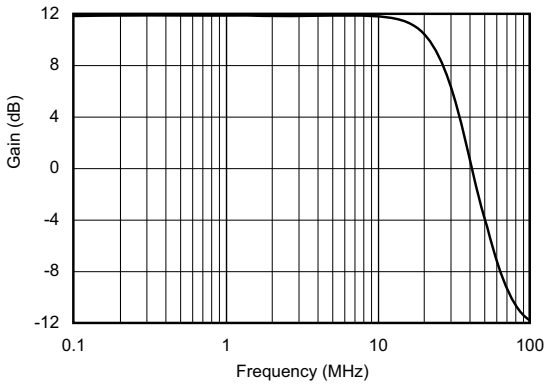


图 9-2. Buffered Single-Supply Active Filter: Gain vs Frequency

9.1.2 PLC Line Driver

9.1.2.1 Design Requirements

The main design requirements for an ac-coupled wideband current-feedback operation are to choose power supplies that satisfy the output voltage requirement, and also to use a feedback resistor value that allows for the proper bandwidth while maintaining stability. Use the design requirements shown in 表 9-1 to design a broadband PLC application circuit.

表 9-1. Design Requirements

DESIGN PARAMETER	VALUE
Power supply	12 V, single-supply
Differential gain G_{DIFF}	8 V/V
Output Voltage	18 V_{PP}
Large-Signal Bandwidth	220 MHz

9.1.2.2 Detailed Design Procedure

The closed-loop gain equation for a differential line driver configuration such as shown below is given as G_{DIFF} = 1 + 2 × (R_F / R_G), where R_F = R_{F1} = R_{F2}. The OPA2673 is a current-feedback amplifier and thus the bandwidth of the closed-loop configuration is set by the value of the R_F resistor. This advantage of the current-feedback architecture allows for flexibility in setting the differential gain by choosing the value of the R_G resistor without reducing the bandwidth as is the case with voltage-feedback amplifiers. The OPA2673 is designed to provide optimal bandwidth performance with R_{F1} = R_{F2} = 350 Ω. To configure the device in a gain of 8 V/V, the R_G resistor is chosen to be 100 Ω.

9.1.2.3 Application Curves

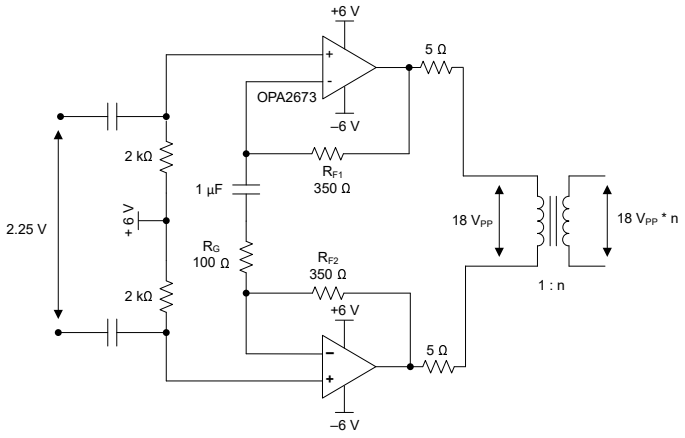


图 9-3. Typical Schematic for PLC Applications

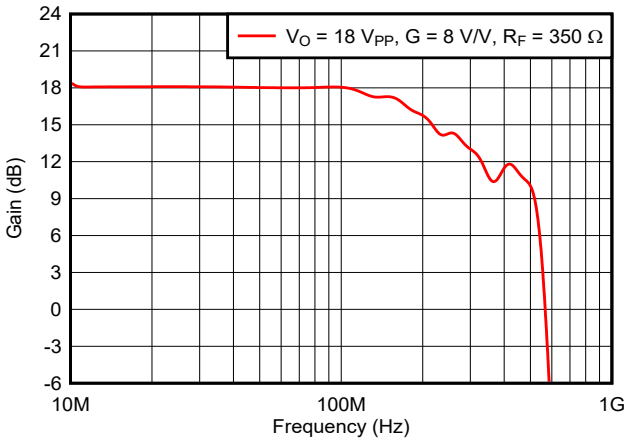


图 9-4. Large-Signal Frequency Response

10 Power Supply Recommendations

10.1 Thermal Analysis

As a result of the high output power capability of the OPA2673, heat-sinking or forced airflow may be required under extreme operating conditions. The maximum desired junction temperature sets the maximum allowed internal power dissipation, described below. The maximum junction temperature allowed should not exceed +150°C.

Operating junction temperature (T_J) is given by

$$T_J = T_A + P_D \times \theta_{JA} \quad (13)$$

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, however, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition,

$$P_{DL} = V_S^2 / (4 \times R_L), \quad (14)$$

where R_L includes feedback network loading.

This is the power dissipated at the output stage of OPA2673 that determines the internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2673 VQFN-16 in the circuit of 图 8-1 operating at the maximum specified ambient temperature of +85°C with both outputs driving a grounded 20 Ω load to +2.5 V.

$P_D = 12\ V \times 33\ mA + 2 \times [5^2 / (4 \times [20\ \Omega\ //\ 535\ \Omega])] = 1.05\ W$

Maximum $T_J = +85°C + (1.05 \times 45°C/W) = 132.2°C$

The output V-I plot in *Output Current and Voltage* includes a boundary for 2-W maximum internal power dissipation under these conditions.

10.2 Input and ESD Protection

The OPA2673 is built using a high-speed complementary bipolar process. The internal junction breakdown voltages are shown in the *Absolute Maximum Ratings* table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in 图 10-1.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 10 mA continuous current. Where higher currents are possible (for example, in systems with ±15 V supply parts driving into the OPA2673), current-limiting series resistors should be added into the two inputs.

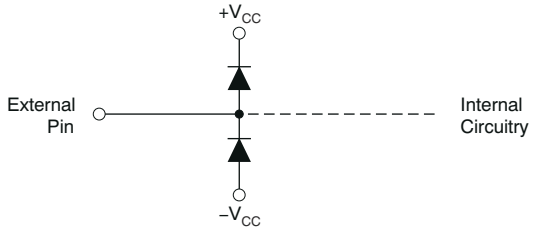


图 10-1. ESD Steering Diodes

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA2673 requires careful attention to board layout parasitic and external component types.

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25 in, or 6.35 0 mm) from the power-supply pins to high-frequency 0.1 µF decoupling capacitors. The power-supply connections (on pins 7 and 14 for a VQFN package) should always be decoupled with low-ESR capacitors. The ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor connected across the two power supplies (for bipolar operation) improves second-harmonic distortion performance.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA2673. Resistors should be of a very low reactance type. Surface-mount resistors, metal film and carbon composition based axially-leaded resistors can provide good high-frequency performance. Keep the leads and PCB trace length as short as possible. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins.

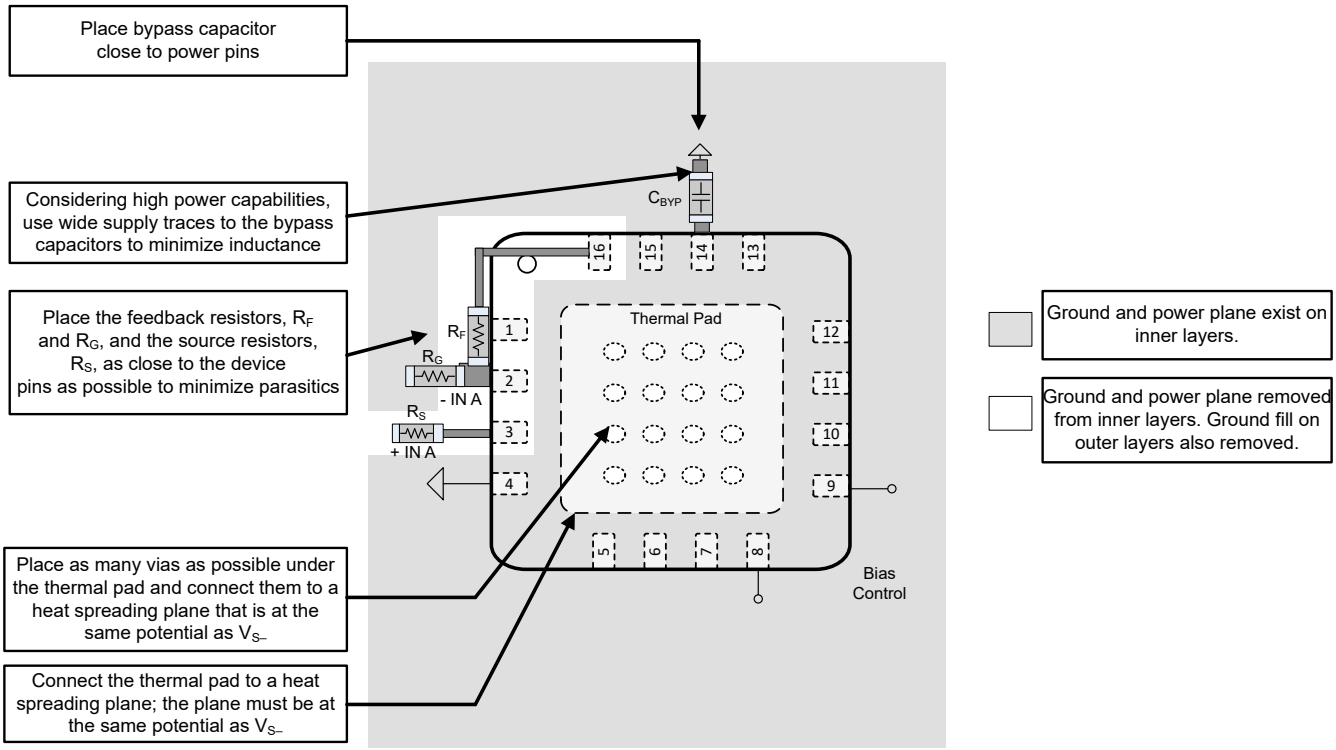
d) The frequency response is primarily determined by the feedback resistor value as described previously. Increasing the value reduces the bandwidth, whereas decreasing it gives a more peaked frequency response. The 402 Ω feedback resistor used in the *Typical Characteristics* at a gain of +4 V/V on ±6 V supplies is a good starting point for design. Note that a current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability. A 511 Ω feedback resistor, rather than a direct short, is recommended for the unity-gain follower application.

e) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils, or 1.27 mm to 2.54 mm) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of 图 8-6. Low parasitic capacitive loads (< 5 pF) may not need an R_{ISO} because the OPA2673 is nominally compensated to operate with a 2 pF parasitic load.

If a long trace is required, and the 6 dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).

The high output voltage and current capability of the OPA2673 allows multiple destination devices to be handled as separate transmission lines, each with respective series and shunt terminations. If the 6 dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only.

11.2 Layout Example



Layout Recommendations have been shown for Channel A only, follow similar precautions for Channel B.

图 11-1. Layout Recommendations

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2673IRGVR	ACTIVE	VQFN	RGV	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2673	Samples
OPA2673IRGVT	ACTIVE	VQFN	RGV	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2673	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

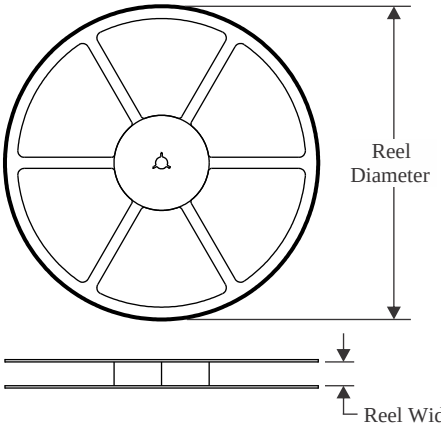
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

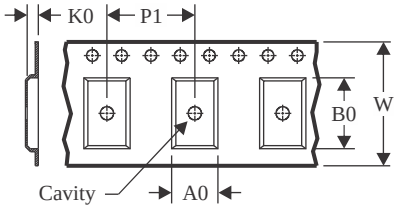
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

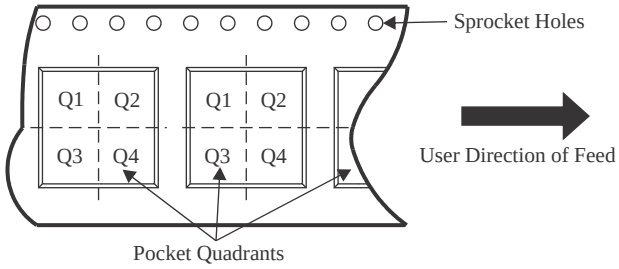


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

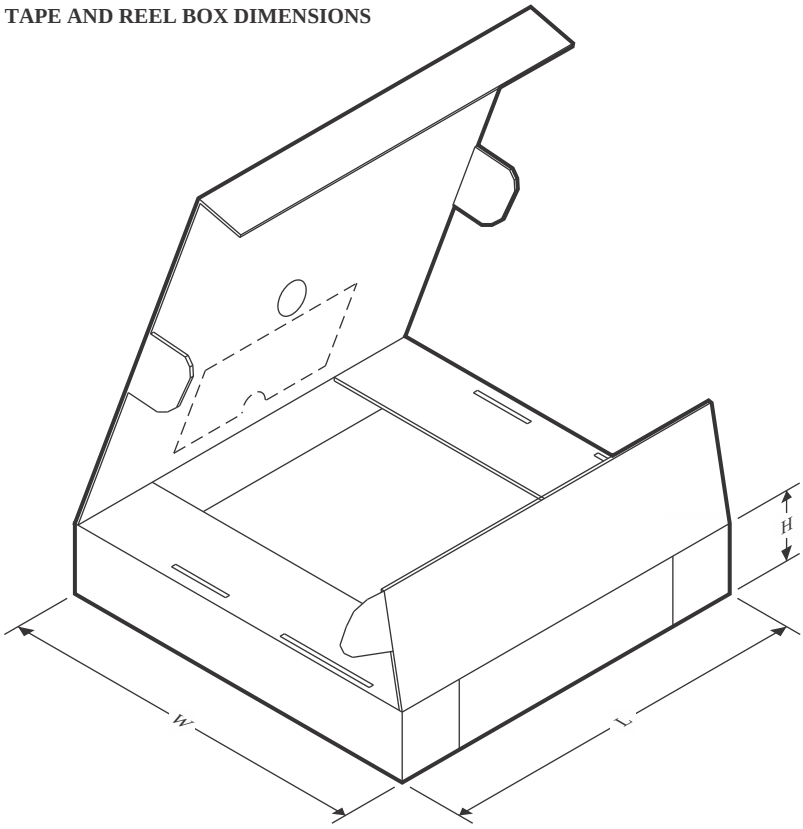
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2673IRGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2673IRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2673IRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2673IRGVR	VQFN	RGV	16	2500	367.0	367.0	35.0
OPA2673IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0
OPA2673IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0

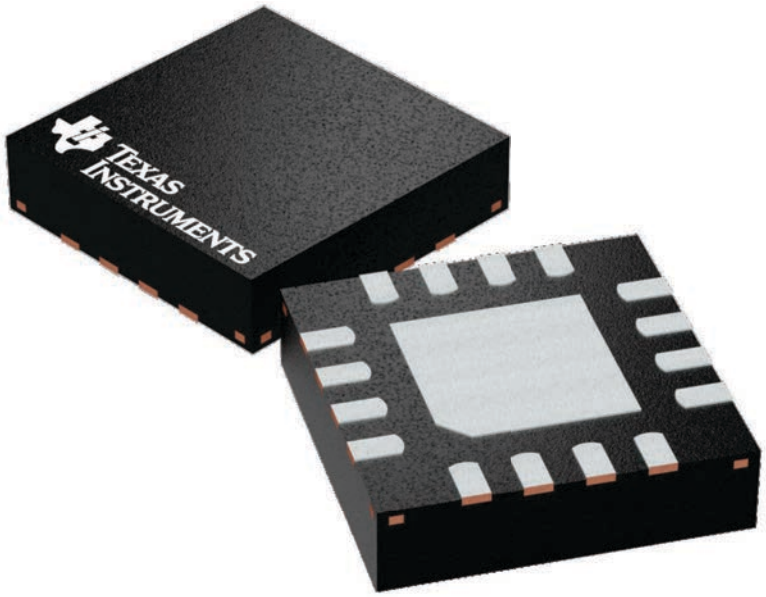
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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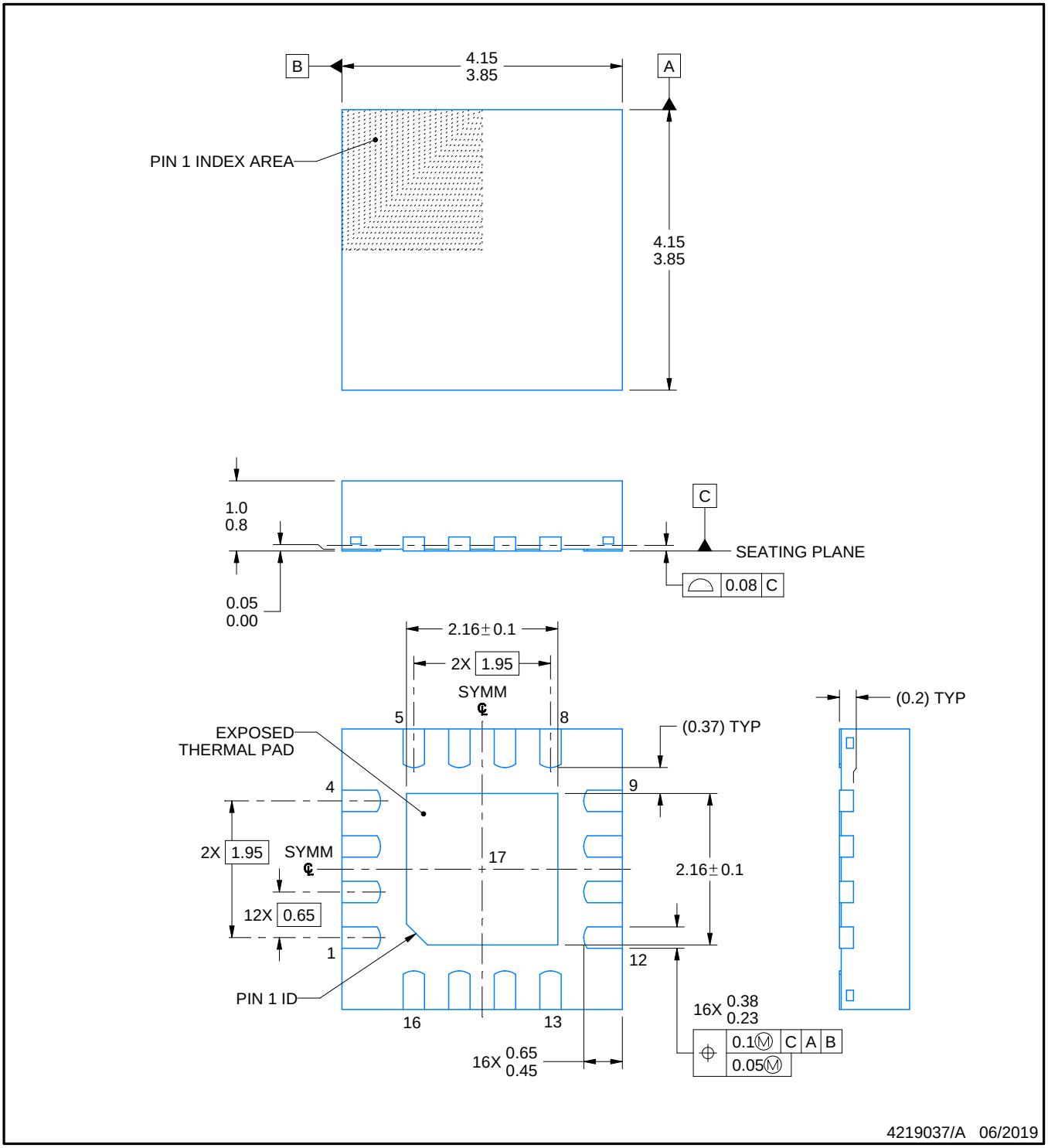
RGV0016A

PACKAGE OUTLINE

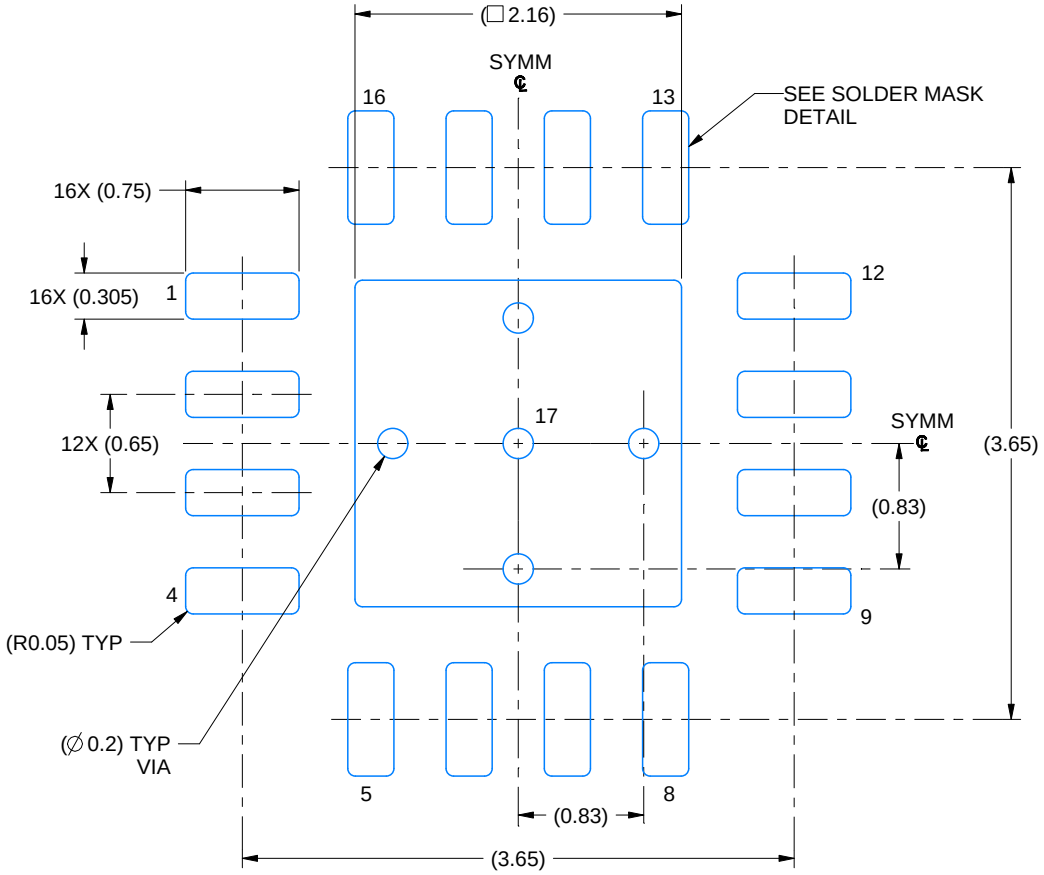
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

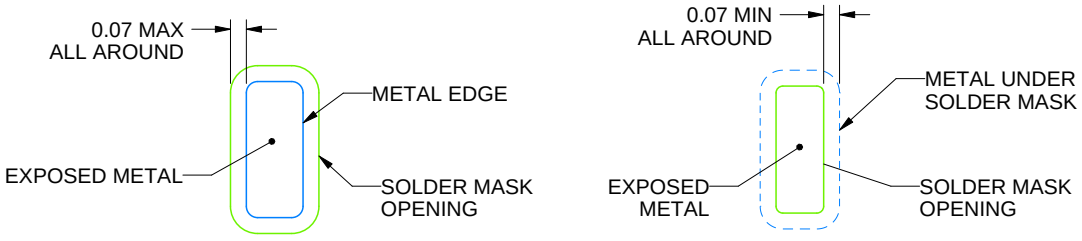


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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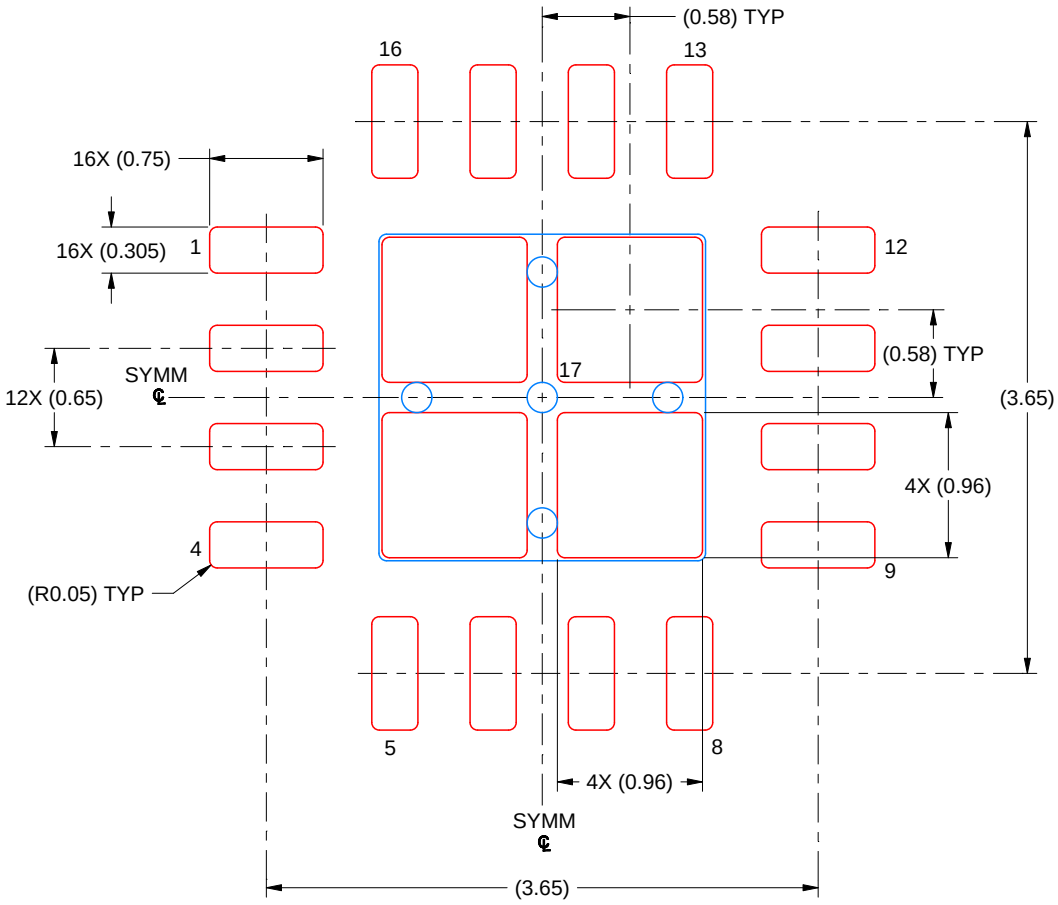
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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