TPS65981 USB Type-C® 和 USB PD 控制器、电源开关和高速多路复用器

1 特性

- 该器件由 USB-IF 进行了 PD2.0 认证
  - 截至 2020 年 6 月，PD2.0 认证对于新设计不再适用
  - 所有需要认证的新设计应使用符合 PD3.0 的器件
  - 有关 PD2.0 与 PD3.0 的文章
- 完全可配置的 USB PD 控制器
  - 通过 GPIO 控制外部直流/直流电源
    - 例如：TPS65981EVM
  - 端口数据多路复用器
    - USB 2.0 HS 数据和低速端点
    - 用于交替模式的边带使用数据
  - 用于为各种应用轻松配置 TPS65981 的 GUI 工具
  - 支持 DisplayPort 交替模式
  - 支持工业温度范围
  - 有关更详尽的选择指南和入门信息，请参阅 www.ti.com/usb-c 和 E2E 指南
- 完全管理的集成电源路径：
  - 集成 5V、3A、55mΩ 电源开关
  - 集成 5V-20V、3A、95mΩ 双向负载开关
  - 适用于外部 5V-20V、5A 双向开关（背靠背 NFET）的栅极控制和电流检测
  - UL2367 认证编号：E169910-20150728
- 集成强大的电源路径保护
  - 集成式反向电流保护、欠压保护、过压保护和压摆率可控制高压双向电源路径
  - 集成了欠压和过压保护以及限流功能，可为 5V/3A 拉电流电源路径提供浪涌电流保护
- USB Type-C® 功率传输 (PD) 控制器
  - 8 个可配置 GPIO
  - 支持 BC1.2 充电
  - 符合 USB PD 2.0 标准
  - 符合 USB Type-C 规范
  - 线缆连接和方向检测
  - 集成式 VCONN 开关
  - 物理层和策略引擎
  - 3.3V LDO 输出，在电池电量耗尽时提供支持
  - 通过 3.3V 或 VBUS 源供电
  - 1 个 I2C 主要端口
  - 1 个 I2C 次级端口

2 应用

- 汽车信息娱乐系统售后
- 其他个人电子产品和工业应用
- 医疗设备
- 耐用 PC 和笔记本电脑
- 集线站
- 平板监视器

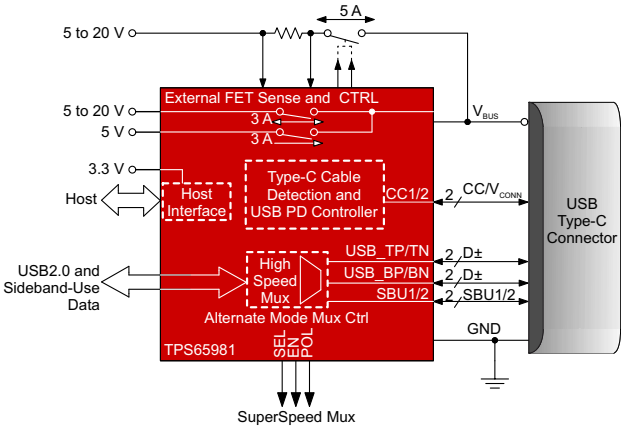
3 说明

TPS65981 是一款高度集成的独立式 USB Type-C 和电力传输 (PD) 控制器，针对笔记本电脑应用进行了优化。TPS65981 集成了全面管理的电源路径与强大的保护功能，可提供完整的 USB-C PD 解决方案。TPS65981 集成了一个高速多路复用器，该多路复用器取决于 CC 引脚提供的 USB Type-C 电缆方向。多路复用器会传递用于交替模式的边带使用数据。TPS65981 具有用于可靠制造的 QFN 封装（具有 0.5mm 间距并与 2 层 PCB 兼容），并具有扩展的（工业）温度范围。TPS65981 通过了 USB PD 2.0 认证，不可再通过 USB IF 进行认证。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS65981	VQFN (56)	8.00mm x 8.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版图表

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (August 2016) to Revision C (August 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 更新了*特性* 列表	1
• 将提到 SPI 的旧术语实例全局更改为控制器和外设	1
• 更新了*应用* 列表	1
• 更新了*描述* 部分	1

Changes from Revision A (April 2016) to Revision B (August 2016)	Page
• 将器件状态从*产品预发布* 更改为*量产数据*	1

5 说明（续）

端口电源开关在 5V 电压下可为传统 USB 电源和 Type-C USB 电源提供高达 3A 的下行电流。当 USB PD 电源用作供电器件（主机）、受电器件（设备）或供电-受电器件时，附加的双向开关路径可在最高 20V 的电压下为其提供高达 3A 的电流。

此外，TPS65981 器件也可用作上行数据端口 (UFP)、下行数据端口 (DFP) 或者双角色数据端口。端口数据多路复用器可实现端口与顶部或底部 D+/D– 信号对之间的 USB 2.0 HS 数据传输，并且具有一个 USB 2.0 低速端点。此外，还可以将边带使用 (SBU) 信号对用于辅助或交替模式的通信（例如 DisplayPort）。

电源管理电路使用系统内部的 3.3V 电压供电，同时使用 VBUS 启动并针对电池电量耗尽或无电池情况进行供电协商。

6 Pin Configuration and Functions

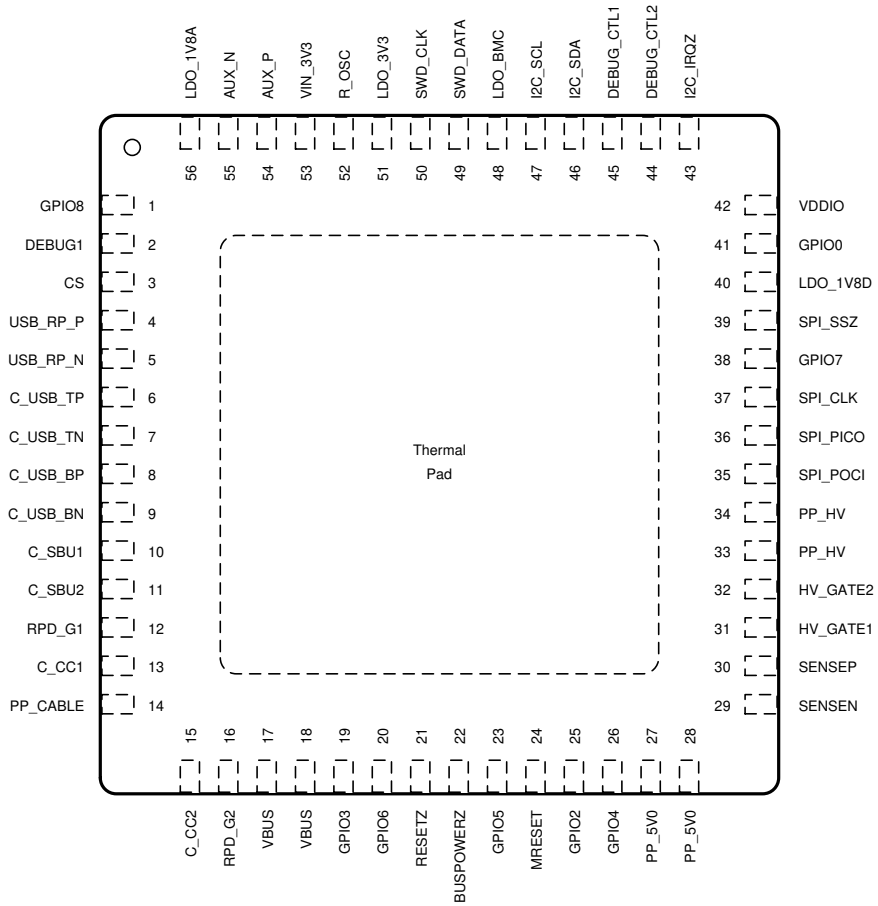


图 6-1. RTQ Package 56-Pin VQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN		CATEGORY	I/O TYPE	POR STATE	DESCRIPTION
NAME	NO.				
AUX_N	55	Port Multiplexer	Analog I/O	Hi-Z	System-side DisplayPort connection to the port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
AUX_P	54	Port Multiplexer	Analog I/O	Hi-Z	System-side DisplayPort connection to the port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
BUSPOWERZ	22	Digital Core I/O and Control	Analog Input	Input (Hi-Z)	General-purpose digital I/O 10. Sampled by ADC at boot. Tie pin to LDO_3V3 through a 100-kΩ resistor to disable PP_HV and PP_EXT power paths during dead-battery or no-battery boot conditions. Refer to the *BUSPOWERZ* table for more details.
C_CC1	13	Type-C Port	Analog I/O	Hi-Z	Output to Type-C CC or VCONN pin. Filter noise with capacitance CC_CC1 to GND.
C_CC2	15	Type-C Port	Analog I/O	Hi-Z	Output to Type-C CC or VCONN pin. Filter noise with capacitance CC_CC2 to GND.
C_SBU1	10	Type-C Port	Analog I/O	Hi-Z	Port side-sideband use connection of port multiplexer.
C_SBU2	11	Type-C Port	Analog I/O	Hi-Z	Port side-sideband use connection of port multiplexer.
C_USB_BN	9	Type-C Port	Analog I/O	Hi-Z	Port-side bottom USB D – connection to the port multiplexer.
C_USB_BP	8	Type-C Port	Analog I/O	Hi-Z	Port-side bottom USB D+ connection to the port multiplexer.
C_USB_TN	7	Type-C Port	Analog I/O	Hi-Z	Port-side top USB D – connection to the port multiplexer.
C_USB_TP	6	Type-C Port	Analog I/O	Hi-Z	Port-side top USB D+ connection to the port multiplexer.

表 6-1. Pin Functions (continued)

PIN		CATEGORY	I/O TYPE	POR STATE	DESCRIPTION
NAME	NO.				
DEBUG_CTL1	45	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 16. At power-up, pin state is sensed to determine bit 4 of the I2C address.
DEBUG_CTL2	44	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 17. At power-up, pin state is sensed to determine bit 5 of the I^2C address.
DEBUG1	2	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 15. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO0	41	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 0. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO2	25	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 2. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO3	19	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 3. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO4	26	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 4. Configured as a hot-plug detect (HPD) transistor, HPD receiver, or both when DisplayPort mode is supported. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO5	23	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 5. Can be configured as a HPD receiver when DisplayPort mode is supported. Must be tied high or low through a 1-kΩ pull-up or pull-down resistor when used as a configuration input. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO6	20	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 6. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO7	38	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 7. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO8	1	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 8. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
HV_GATE1	31	External HV FET Control and Sense	Analog Output	Short to SENSEP	External NFET gate control for high voltage power path. Float pin when unused.
HV_GATE2	32	External HV FET Control and Sense	Analog Output	Short to VBUS	External NFET gate control for high voltage power path. Float pin when unused.
I2C_IRQZ	43	Digital Core I/O and Control	Digital Output	Hi-Z	I^2C port interrupt. Active low. Implement externally as an open-drain with a pull-up resistance. Float pin when unused.
I2C_SCL	47	Digital Core I/O and Control	Digital I/O	Digital Input	I^2C port serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistor when used or unused.
I2C_SDA	46	Digital Core I/O and Control	Digital I/O	Digital Input	I^2C port serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistor when used or unused.
LDO_1V8A	56	Low Current	Power	N/A	Output of the 1.8-V LDO for core analog circuits. Bypass with capacitance CLDO_1V8A to GND.
LDO_1V8D	40	Low Current	Power	N/A	Output of the 1.8-V LDO for core digital circuits. Bypass with capacitance CLDO_1V8D to GND.
LDO_3V3	51	Low Current	Power	N/A	Output of the VBUS to 3.3-V LDO or connected to VIN_3V3 by a switch. Main internal supply rail. Used to power external flash memory. Bypass with capacitance CLDO_3V3 to GND.
LDO_BMC	48	Low Current	Power	N/A	Output of the USB-PD BMC transceiver output level LDO. Bypass with capacitance CLDO_BMC to GND.
MRESET	24	Digital Core I/O and Control	Digital I/O	Hi-Z	General-purpose digital I/O 11. Forces RESETZ to assert. By default, this pin asserts RESETZ when pulled high. The pin can be programmed to assert RESETZ when pulled low. Ground pin with a 1-MΩ resistor when unused in the application.
PP_5V0	27 28	High Current	Power	N/A	5-V supply for VBUS. Bypass with capacitance CPP_5V0 to GND. Tie pin to GND when unused

表 6-1. Pin Functions (continued)

PIN		CATEGORY	I/O TYPE	POR STATE	DESCRIPTION
NAME	NO.				
PP_CABLE	14	High Current	Power	N/A	5-V supply for C_CC pins. Bypass with capacitance CPP_CABLE to GND when not tied to PP_5V0. Tie pin to PP_5V0 when unused.
PP_HV	33	High Current	Power	N/A	HV supply for VBUS. Bypass with capacitance CPP_HV to GND. Tie pin to GND when unused
	34				
R_OSC	52	Digital Core I/O and Control	Analog I/O	Hi-Z	External resistance setting for oscillator accuracy. Connect R_OSC to GND through resistance RR_OSC.
RESETZ	21	Digital Core I/O and Control	Digital I/O	Push-Pull Output (Low)	General-purpose digital I/O 9. Active low reset output when VIN_3V3 is low (driven low on start-up). Float pin when unused.
RPD_G1	12	Type-C Port	Analog I/O	Hi-Z	Tie pin to C_CC1 when configured to receive power in dead-battery or no-power condition. Tie pin to GND otherwise.
RPD_G2	16	Type-C Port	Analog I/O	Hi-Z	Tie pin to C_CC2 when configured to receive power in dead-battery or no-power condition. Tie pin to GND otherwise.
SENSEN	29	External HV FET Control and Sense	Analog Input	Analog Input	Positive sense for external high voltage power path current sense resistance. Short pin to VBUS when unused.
SENSEP	30	External HV FET Control and Sense	Analog Input	Analog Input	Positive sense for external high voltage power path current sense resistance. Short pin to VBUS when unused.
SPI_CLK	37	Digital Core I/O and Control	Digital Output	Digital Input	SPI serial clock. Connect pin directly to SPI Flash IC. Refer to the *Boot Code* section for more details on the SPI Flash.
SPI_POCI	35	Digital Core I/O and Control	Digital Input	Digital Input	SPI serial controller input from peripheral. Tie pin to LDO_3V3 through a 3.3-kΩ resistor.
SPI_PICO	36	Digital Core I/O and Control	Digital Output	Digital Input	SPI serial controller output to peripheral. Connect pin directly to SPI flash IC.
SPI_CSZ	39	Digital Core I/O and Control	Digital Output	Digital Input	SPI chip select. Tie pin to LDO_3V3 through a 3.3-kΩ resistor.
SS	3	External HV FET Control and Sense	Analog Output	Driven Low	Soft Start. Tie pin to capacitance CSS to ground.
SWD_CLK	50	Port Multiplexer	Digital Input	Resistive Pull High	SWD serial clock. Float pin when unused.
SWD_DATA	49	Port Multiplexer	Digital I/O	Resistive Pull High	SWD serial data. Float pin when unused.
USB_RP_N	5	Port Multiplexer	Analog I/O	Hi-Z	System-side USB2.0 high-speed connection to the port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
USB_RP_P	4	Port Multiplexer	Analog I/O	Hi-Z	System-side USB2.0 high-speed connection to the port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
VBUS	17	High Current	Power	N/A	5-V output from PP_5V0. Input or output from PP_HV up to 20 V. Bypass with capacitance CVBUS to GND.
	18				
VDDIO	42	Low Current	Power	N/A	VDD for I/O. Some I/Os are reconfigurable to be powered from VDDIO instead of LDO_3V3. When VDDIO is not used, tie pin to LDO_3V3. When not tied to LDO_3V3 and used as a supply input, bypass with capacitance CVDDIO to GND.
VIN_3V3	53	Low Current	Power	N/A	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.
GND (Thermal Pad)		Ground	Ground	Hi-Z	Ground. Connect directly to ground plane in accordance with the guidelines listed in the *Layout Guidelines* section to achieve the measured values in the *Thermal Information* table.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage(2)	PP_CABLE, PP_5V0	–0.3	6	V
		VIN_3V3	–0.3	3.6	
		SENSEP, SENSEN(3)	–0.3	24	
		VDDIO	–0.3	LDO_3V3 + 0.3	
V_{IO}	Output voltage(2)	LDO_1V8A, LDO_1V8D, LDO_BMC, SS	–0.3	2	V
		LDO_3V3	–0.3	3.45	
		RESETZ, I2C _IRQ1Z, SPI_PICO, SPI_CLK, SPI_CSZ, SWD_CLK	–0.3	LDO_3V3 + 0.3	
		HV_GATE1, HV_GATE2	–0.3	30	
		HV_GATE1 (relative to SENSEP)	–0.3	6	
		HV_GATE2 (relative to VBUS)	–0.3	6	
V_{IO}	I/O voltage(2)	PP_HV, VBUS (2)	–0.3	24	V
		I2C_SDA1, I2C_SCL1, SWD_DATA, SPI_POCI, USB_RP_P, USB_RP_N, AUX_N, AUX_P, DEBUG1, DEBUG_CTL1, DEBUG_CTL2, GPIOn, MRESET, BUSPOWERZ, GPIO0-8	–0.3	LDO_3V3 + 0.3	
		R_OSC	–0.3	2	
		C_USB_TP, C_USB_TN, C_USB_BP, C_USB_BN, C_SBU2, C_SBU1 (Switches Open)	–2	6	
		C_USB_TP, C_USB_TN, C_USB_BP, C_USB_BN, C_SBU2, C_SBU1 (Switches Closed)	–0.3	6	
		C_CC1, C_CC2, RPD_G1, RPD_G2	–0.3	6	
T_J	Operating junction temperature		–40	125	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(3) The 24 V maximum is based on keeping HV_GATE1/2 at or below 30 V. Fast voltage transitions (<100 ns) can occur up to 30 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage(1)	VIN_3V3	2.85	3.45	V
		PP_5V0	4.75	5.5	
		PP_CABLE	2.95	5.5	
		PP_HV	4.5	22	
		VDDIO	1.7	3.45	
V_{IO}	I/O voltage(1)	VBUS	4	22	V
		C_USB_PT, C_USB_NT, C_USB_PB, C_USB_NB, C_SBU1, C_SBU2	–2	5.5	
		C_CC1, C_CC2	0	5.5	
T_A	Ambient operating temperature		–40	105	°C
T_B	Operating board temperature		–40	120	°C
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

7.4 Thermal Information

THERMAL METRIC(1)		TPS65981 RTQ (VQFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Supply Requirements and Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL						
VIN_3V3	Input 3.3-V supply		2.85	3.3	3.45	V
PP_CABLE	Input voltage to power C_CC pins. This input is also available to power core circuitry		2.95	5	5.5	V
VBUS	Bidirection DC bus voltage. Output from the TPS65981 or input to the TPS65981		4	5	22	V
PP_5V0	5-V supply input to power VBUS. This supply does not power the TPS65981		4.75	5	5.5	V
VDDIO(1)	Optional supply for I/O cells		1.7		3.45	V
INTERNAL						
VLDO_3V3	DC 3.3 V generated internally by either a switch from VIN_3V3, an LDO from PP_CABLE, or an LDO from VBUS		2.7	3.3	3.45	V
VDO_LDO3V3	Dropout voltage of LDO_3V3 from PP_CABLE	I_{LOAD} = 50 mA			250	mV
	Dropout voltage of LDO_3V3 from VBUS		250	500	750	mV
VLDO_1V8D	DC 1.8 V generated for internal digital circuitry		1.7	1.8	1.9	V
VLDO_1V8A	DC 1.8 V generated for internal analog circuitry		1.7	1.8	1.9	V
VLDO_BMC	DC voltage generated on LDO_BMC. Setting for USB-PD		1.05	1.125	1.2	V
ILDO_3V3	DC current supplied by the 3.3-V LDOs. This includes internal core power and external load on LDO_3V3				70	mA
ILDO_3V3EX	External DC current supplied by LDO_3V3				30	mA
ILDO_1V8D	DC current supplied by LDO_1V8D. This is intended for internal loads only but small external loads may be added.				50	mA
ILDO_1V8DEX	External DC current supplied by LDO_1V8D.				5	mA
ILDO_1V8A	DC current supplied by LDO_1V8A. This is intended for internal loads only but small external loads may be added.				20	mA
ILDO_1V8AEX	External DC current supplied by LDO_1V8A.				5	mA
ILDO_BMC	DC current supplied by LDO_BMC. This is intended for internal loads only				5	mA
ILDO_BMCEX	External DC current supplied by LDO_BMC				0	mA
VFWD_DROP	Forward voltage drop across VIN_3V3 to LDO_3V3 switch	I_{LOAD} = 50 mA	25	60	90	mV
RIN_3V3	Input switch resistance from VIN_3V3 to LDO_3V3	$V_{VIN\_3V3} - V_{LDO\_3V3}$ > 50 mV	0.5	1.1	1.75	Ω

(1) I/O buffers are not fail-safe to LDO_3V3. Therefore, VDDIO may power-up before LDO_3V3. When VDDIO powers up before LDO_3V3, the I/Os shall not be driven high. When VDDIO is low and LDO_3V3 is high, the I/Os may be driven high.

7.6 Power Supervisor Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV_LDO3V3	Undervoltage threshold for LDO_3V3. Locks out 1.8-V LDOs	LDO_3V3 rising	2.2	2.325	2.45	V
UVH_LDO3V3	Undervoltage hysteresis for LDO_3V3	LDO_3V3 falling	20	80	150	mV
UV_VBUS_LDO	Undervoltage threshold for VBUS to enable LDO	VBUS rising	3.35	3.75	3.95	V
UVH_VBUS_LDO	Undervoltage hysteresis for VBUS to enable LDO	VBUS falling	20	80	150	mV
UV_PCBL	Undervoltage threshold for PP_CABLE	PP_CABLE rising	2.5	2.625	2.75	V
UVH_PCBL	Undervoltage hysteresis for PP_PCABLE	PP_CABLE falling	20	50	80	mV
UV_5V0	Undervoltage threshold for PP_5V0	PP_5V0 rising	3.5	3.725	3.95	V
UVH_5V0	Undervoltage hysteresis for PP_P5V0	PP_5V0 falling	20	80	150	mV
OV_VBUS	Overvoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS rising	5		24	V
OVLSB_VBUS	Overvoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS rising		328		mV
OVH_VBUS	Overvoltage hysteresis for VBUS	VBUS falling, % of OV_VBUS	0.9%	1.3%	1.7%	
UV_VBUS	Undervoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS falling	2.5		18.21	V
UVLSB_VBUS	Undervoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS falling		249		mV
UVH_VBUS	Undervoltage hysteresis for VBUS	VBUS rising, % of UV_VBUS	0.9%	1.3%	1.7%	
UVR_RST3V3	Configurable under-voltage threshold for VRSTZ_3V3 rising. De-asserts RESETZ	VIN_3V3 and VRSTZ_3V3 rising (default setting)	2.613	2.75	2.888	V
UVRH_RST3V3	Under-voltage hysteresis for VRST_3V3 falling. Asserts RESETZ	VIN_3V3 and VRSTZ_3V3 falling		30	50	mV
TUVRASSERT	Delay from falling or MRESET assertion to RESETZ asserting low				75	µs
TUVRDELAY	Configurable delay from to RESETZ de-assertion		0		161.3	ms

7.7 Power Consumption Characteristics

Recommended operating conditions; T_A = 25°C (Room temperature) unless otherwise noted[4]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IVIN_3V3	Sleep[1]	VIN_3V3 = VDDIO = 3.45 V, VBUS = 0, PPCABLE = 0; 100-kHz oscillator running		62		µA
	Idle [2]	VIN_3V3 = VDDIO = 3.45 V, VBUS=0, PPCABLE = 0; 100-kHz oscillator running, 48-MHz oscillator running		2.5		mA
	Active[3]	VIN_3V3 = VDDIO = 3.45 V, VBUS = 0, PPCABLE = 0; 100-kHz oscillator running, 48-MHz oscillator running		6.0		mA

(1) Sleep is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active.
(2) Idle is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active, and the digital core is clocked at 4 MHz.
(3) Active is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active, all core functionality active, and the digital core is clocked at 12 MHz.
(4) Application code can result in other power consumption measurements by adjusting enabled circuitry and clock rates. Application code also provisions the wake=up mechanisms (for example, I^2C activity and GPIO activity).

7.8 Cable Detection Characteristics

Recommended operating conditions; T_A = -40 to 105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IH_CC_USB	Source current through each C_CC pin when in a disconnected state and configured as a DFP advertising Default USB current to a peripheral device		73.6	80	86.4	µA
IH_CC_1P5	Source current through each C_CC pin when in a disconnected state when configured as a DFP advertising 1.5 A to a UFP		169	180	191	µA
IH_CC_3P0	Source current through each C_CC pin when in a disconnected state and configured as a DFP advertising 3 A to a UFP.	VIN_3V3 ⩾ 3.135 V	303	330	356	µA
VD_CCH_USB	Voltage threshold for detecting a DFP attach when configured as a UFP and the DFP is advertising Default USB current source capability		0.15	0.2	0.25	V
VD_CCH_1P5	Voltage threshold for detecting a DFP advertising 1.5-A source capability when configured as a UFP		0.61	0.66	0.7	V
VD_CCH_3P0	Voltage threshold for detecting a DFP advertising 3 A source capability when configured as a UFP		1.169	1.23	1.29	V
VH_CCD_USB	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising default USB current source capability.	IH_CC = IH_CC_USB	1.473	1.55	1.627	V
VH_CCD_1P5	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising 1.5-A source capability	IH_CC = IH_CC_1P5	1.473	1.55	1.627	V
VH_CCD_3P0	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising 3-A source capability.	IH_CC = IH_CC_3P0 VIN_3V3 ⩾ 3.135 V	2.423	2.55	2.67	V
VH_CCA_USB	Voltage threshold for detecting an active cable attach when configured as a DFP and advertising default USB current capability.		0.15	0.2	0.25	V
VH_CCA_1P5	Voltage threshold for detecting active cables attach when configured as a DFP and advertising 1.5-A capability.		0.35	0.4	0.45	V
VH_CCA_3P0	Voltage threshold for detecting active cables attach when configured as a DFP and advertising 3-A capability.		0.76	0.8	0.84	V
RD_CC	Pull-down resistance through each C_CC pin when in a disconnect state and configured as a UFP. LDO_3V3 powered.	V = 1 V, 1.5 V	4.85	5.1	5.35	kΩ
RD_CC_OPEN	Pull-down resistance through each C_CC pin when in a disconnect state and configured as a UFP. LDO_3V3 powered.	V = 0 V to LDO_3V3	500			kΩ
RD_DB	Pull-down resistance through each C_CC pin when in a disconnect state and configured as a UFP when configured for dead battery (RPD_Gn tied to C_CCn). LDO_3V3 unpowered	V = 1.5 V, 2 V RPD_Gn tied to C_CCn	4.08	5.1	6.12	kΩ
RD_DB_OPEN	Pull-down resistance through each C_CC pin when in a disconnect state and configured as a UFP when not configured for dead battery (RPD_Gn tied to GND). LDO_3V3 unpowered	V = 1.5 V, 2 V RPD_Gn tied to GND	500			kΩ
VTH_DB	Threshold voltage of the pull-down FET in series with RD during dead battery	I_CC = 80 µA	0.5	0.9	1.2	V
R_RPD	Resistance between RPD_Gn and the gate of the pull-down FET		25	50	85	MΩ

7.9 USB-PD Baseband Signal Requirements and Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
PD_BITRATE	PD data-bit rate		270	300	330	Kbps
UI(1)	Unit interval (1/PD_BITRATE)		3.03	3.33	3.7	µs
CCBLPLUG(2)	Capacitance for a cable plug (each plug on a cable can have up to this value)				25	pF
ZCABLE	Cable characteristic impedance		32		65	Ω
CRECEIVER(3)	Receiver capacitance. Capacitance looking into C_CCn pin when in receiver mode.		70		120	pF
TRANSMITTER						
ZDRIVER	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750 kHz) while the source is driving the C_CCn line.		33		75	Ω
TRISE	Rise time. 10% to 90% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300			ns
TFALL	Fall time. 90% to 10% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300			ns
RECEIVER						
VRXTR	Rx receive rising input threshold		605	630	655	mV
VRXTF	Rx receive falling input threshold		450	470	490	mV
NCOUNT(4)	Number of transitions for signal detection (number to count to detect non-idle bus).		3			
TTRANWIN(4)	Time window for detecting non-idle bus.		12		20	µs
ZBMCRX	Receiver input impedance	Does not include pull-up or pull-down resistance from cable detect. Transmitter is Hi-Z.	10			MΩ
TRXFILTER(5)	Rx bandwidth limiting filter. Time constant of a single pole filter to limit broadband noise ingression		100			ns

(1) UI denotes the time to transmit an un-encoded data bit not the shortest high or low times on the wire after encoding with BMC. A single data bit cell has duration of 1 UI, but a data bit cell with value 1 will contain a centrally place 01 or 10 transition in addition to the transition at the start of the cell.
(2) The capacitance of the bulk cable is not included in the CCBLPLUG definition. It is modeled as a transmission line.
(3) CRECEIVER includes only the internal capacitance on a C_CCn pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications. TI recommends to add capacitance to bring the total pin capacitance to 300 pF for improved TX behavior.
(4) BMC packet collision is avoided by the detection of signal transitions at the receiver. Detection is active when a minimum of NCOUNT transitions occur at the receiver within a time window of TTRANWIN. After waiting TTRANWIN without detecting NCOUNT transitions, the bus is declared idle.
(5) Broadband noise ingression is because of coupling in the cable interconnect.

7.10 USB-PD TX Driver Voltage Adjustment Parameter

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VTXP0	TX transmit peak voltage		1.615	1.7	1.785	V
VTXP1			1.52	1.6	1.68	V
VTXP2			1.425	1.5	1.575	V
VTXP3			1.33	1.4	1.47	V
VTXP4			1.235	1.3	1.365	V
VTXP5			1.188	1.25	1.312	V
VTXP6			1.14	1.2	1.26	V
VTXP7			1.116	1.175	1.233	V
VTXP8			1.092	1.15	1.208	V
VTXP9			1.068	1.125	1.181	V
VTXP10			1.045	1.1	1.155	V
VTXP11			1.021	1.075	1.128	V
VTXP12			0.998	1.05	1.102	V
VTXP13			0.974	1.025	1.076	V
VTXP14			0.95	1	1.05	V
VTXP15			0.903	0.95	0.997	V

(1) VTXP voltage settings are determined by application code and the setting used must meet the needs of the application and adhere to the USB-PD Specifications.

7.11 Port Power Switch Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted. The maximum capacitance on VBUS, when configured as a source, must not exceed 12 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RPPCC	PP_CABLE to C_CCn power switch resistance				312	mΩ
RPP5V	PP_5V0 to VBUS power switch resistance			55	75	mΩ
RPPHV	PP_HV to VBUS power switch resistance			95	135	mΩ
IHVACT	Active quiescent current from PP_HV pin	EN_HV = 1			1	mA
IHVSD	Shutdown quiescent current from PP_HV pin	EN_HV = 0			100	µA
IHVEXTACT	Active quiescent current from SENSEP pin,	Configured as source; EN_HV = 1			1	mA
	Active quiescent current from VBUS pin	Configured as sink; EN_HV = 1			3.5	mA
IHVEXTSD	Shutdown quiescent current from SENSEP pin	EN_HV = 0			40	µA
IPP5VACT	Active quiescent current from PP_5V0				1	mA
IPP5VSD	Shutdown quiescent current from PP_5V0				100	µA

7.11 Port Power Switch Characteristics (continued)

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted. The maximum capacitance on VBUS, when configured as a source, must not exceed 12 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ILIMHV[4]	PP_HV current limit, setting 0		1.007	1.118	1.330	A
	PP_HV current limit, setting 1		1.258	1.398	1.638	A
	PP_HV current limit, setting 2		1.51	1.678	1.945	A
	PP_HV current limit, setting 3		1.761	1.957	2.153	A
	PP_HV current limit, setting 5		2.013	2.237	2.46	A
	PP_HV current limit, setting 6		2.265	2.516	2.768	A
	PP_HV current limit, setting 7		2.516	2.796	3.076	A
	PP_HV current limit, setting 8		2.768	3.076	3.383	A
	PP_HV current limit, setting 9		3.02	3.355	3.691	A
	PP_HV current limit, setting 10		3.271	3.635	3.998	A
	PP_HV current limit, setting 11		3.523	3.914	4.306	A
	PP_HV current limit, setting 12		3.775	4.194	4.613	A
	PP_HV current limit, setting 13		4.026	4.474	4.921	A
	PP_HV current limit, setting 14		4.278	4.753	5.228	A
	PP_HV current limit, setting 15		4.529	5.033	5.536	A
	PP_HV current limit, setting 16		5.033	5.592	6.151	A
ILIMHVEXT[3] [4]	PP_EXT current limit, setting 0		0.986	1.12	1.254	A
	PP_EXT current limit, setting 1		1.231	1.399	1.567	A
	PP_EXT current limit, setting 2		1.477	1.678	1.879	A
	PP_EXT current limit, setting 3		1.761	1.957	2.153	A
	PP_EXT current limit, setting 4		2.012	2.236	2.46	A
	PP_EXT current limit, setting 5		2.263	2.515	2.767	A
	PP_EXT current limit, setting 6		2.514	2.794	3.074	A
	PP_EXT current limit, setting 7		2.765	3.073	3.381	A
	PP_EXT current limit, setting 8		3.016	3.352	3.688	A
	PP_EXT current limit, setting 9		3.267	3.631	3.995	A
	PP_EXT current limit, setting 10		3.519	3.91	4.301	A
	PP_EXT current limit, setting 11		3.77	4.189	4.608	A
	PP_EXT current limit, setting 12		4.021	4.468	4.915	A
	PP_EXT current limit, setting 13		4.272	4.747	5.222	A
	PP_EXT current limit, setting 14		4.523	5.026	5.529	A
	PP_EXT current limit, setting 15		5.025	5.584	6.143	A
ILIMPP5V[4]	PP_5V0 current limit, setting 0		1.006	1.118	1.330	A
	PP_5V0 current limit, setting 1		1.132	1.258	1.484	A
	PP_5V0 current limit, setting 2		1.258	1.398	1.638	A
	PP_5V0 current limit, setting 3		1.384	1.538	1.691	A
	PP_5V0 current limit, setting 4		1.51	1.677	1.845	A
	PP_5V0 current limit, setting 5		1.636	1.817	1.999	A
	PP_5V0 current limit, setting 6		1.761	1.957	2.153	A
	PP_5V0 current limit, setting 7		1.887	2.097	2.307	A
	PP_5V0 current limit, setting 8		2.013	2.237	2.46	A
	PP_5V0 current limit, setting 9		2.139	2.376	2.614	A
	PP_5V0 current limit, setting 10		2.265	2.516	2.768	A
	PP_5V0 current limit, setting 11		2.39	2.656	2.922	A
	PP_5V0 current limit, setting 12		2.516	2.796	3.075	A
	PP_5V0 current limit, setting 13		2.642	2.936	3.229	A
	PP_5V0 current limit, setting 14		2.768	3.075	3.383	A
	PP_5V0 current limit, setting 15		3.019	3.355	3.69	A

7.11 Port Power Switch Characteristics (continued)

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted. The maximum capacitance on VBUS, when configured as a source, must not exceed 12 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ILIMPPCC	PP_CABLE current limit (highest setting)		0.6	0.75	0.9	A
	PP_CABLE current limit (lowest setting)		0.35	0.45	0.55	A
IHV_ACC(1)	PP_HV current sense accuracy	I = 100 mA, Reverse current blocking disabled	3.25	5	6.75	A/V
		I = 200 mA	4	5	6	A/V
		I = 500 mA	4.4	5	5.6	A/V
		I ≥ 1 A	4.5	5	5.5	A/V
IHVEXT_ACC	PP_EXT current sense accuracy (excluding RSENSE accuracy)	I = 100 mA, RSENSE = 10 mΩ, Reverse current blocking disabled	3.5	5	6.5	A/V
		I = 200 mA, RSENSE = 10 mΩ	4	5	6	A/V
		I = 500 mA, RSENSE = 10 mΩ	4.4	5	5.6	A/V
		I ≥ 1 A, RSENSE = 10 mΩ	4.5	5	5.5	A/V
IPP5V_ACC(1)	PP_5V0 current sense accuracy	I = 100 mA, Reverse current blocking disabled	1.95	3	4.05	A/V
		I = 200 mA	2.4	3	3.6	A/V
		I = 500 mA	2.64	3	3.36	A/V
		I ≥ 1 A	2.7	3	3.3	A/V
IPPCBL_ACC	PP_CABLE current sense accuracy	I = 100 mA		1		A/V
		I = 200 mA		1		A/V
		I = 500 mA		1		A/V
IGATEEXT(2)	External gate-drive current on HV_GATE1 and HV_GATE2		4	5	6	µA
VGSEXT	VGS voltage driving external FETs		4.5		7.5	V
TON_HV	PP_HV path turn on time from enable to VBUS = 95% of PP_HV voltage	Configured as a source or as a sink with soft start disabled. PP_HV = 20 V, CVBUS = 10 µF, ILOAD = 100 mA			8	ms
TON_5V	PP_5V0 path turn on time from enable to VBUS = 95% of PP_5V0 voltage	Configured as a source or as a sink with soft start disabled. PP_5V0 = 5 V, CVBUS = 10 µF, ILOAD = 100 mA			2.5	ms
TON_CC	PP_CABLE path turn on time from enable to C_CCn = 95% of the PP_CABLE voltage	PP_CABLE = 5 V, C_CCn = 500 nF, ILOAD = 100 mA			2	ms
ISS	Soft-start charging current		5.5	7	8.5	µA
RSS_DIS	Soft-start discharge resistance		0.6	1	1.4	kΩ
VTHSS	Soft-start complete threshold		1.35	1.5	1.65	V
TSSDONE	Soft-start complete time	CSS = 220 nF	31.9	46.2	60.5	ms
VREVPHV	Reverse current blocking voltage threshold for PP_HV switch		2	6	10	mV
VREVPEXT	Reverse current blocking voltage Threshold for PP_EXT external switches		2	6	10	mV
VREV5V0	Reverse current blocking voltage threshold for PP_5V0 switches		2	6	10	mV
VHVDISPD	Voltage threshold above VIN at which the pull-down RHVDISPD on VBUS will disable during a transition from PHV to 5V0		45	200	250	mV
VSAFE0V	Voltage that is a safe 0 V per USB-PD Specifications		0		0.8	V
TSAFE0V	Voltage transition time to VSAFE0V				650	ms
VSO_HV	Voltage on PP_HV or PP_HVEXT above which the PP_HV or PP_EXT to PP_5V0 transition on VBUS will meet transition requirements		9.9			V
SRPOS	Maximum slew rate for positive voltage transitions				0.03	V/µs

7.11 Port Power Switch Characteristics (continued)

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted. The maximum capacitance on VBUS, when configured as a source, must not exceed 12 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SRNEG	Maximum slew rate for negative voltage transitions		–0.03			V/µs
TSTABLE	EN to stable time for both positive and negative voltage transitions				275	ms
VSRCVALID	Supply output tolerance beyond VSRCNEW during time TSTABLE		–0.5		0.5	V
VSRCNEW	Supply output tolerance		–5		5	%

(1) The current sense in the ADC does not accurately read below the current VREV5V0/RPP5V or VREVHV/RPPHV because of the reverse blocking behavior. When reverse blocking is disabled, the values given for accuracy are valid.
(2) Limit the resistance from the HV_GATE1/2 pins to the external FET gate pins to < 1 Ω to provide adequate response time to short circuit events.
(3) Specified for a 10-mΩ RSENSE resistor and 10-mΩ RSENSE application code setting. The values scale with a different RSENSE resistance and application code setting.
(4) The settings are selected automatically by application code for the current limit required in the application.

7.12 Port Data Multiplexer Switching Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWD MULTIPLEXER PATH(1)						
SWD_RON_U	On resistance of SWD_DATA/CLK to C_USB_TP/TN/BP/BN	V_i = 3.3 V, I_O = 20 mA		35	55	Ω
		V_i = 1 V, I_O = 20 mA		30	46	
SWD_ROND_U	On resistance difference between P and N paths of SWD_DATA/CLK to C_USB_ TP/TN/BP/BN	V_i = 1 V to 3.3 V, I_O = 20 mA	–2.5		2.5	Ω
SWD_RON_S	On resistance of SWD_DATA/CLK to C_SBU1/2	V_i = 3.3 V, I_O = 20 mA		26	42	Ω
		V_i = = 1 V, I_O = 20 mA		24	37	
SWD_ROND_S	On resistance difference between P and N paths of SWD_DATA/CLK to C_SBU1/2	V_i = 1 V to 3.3 V, I_O = 20 mA	–1.5		1.5	Ω
SWD_TON	Switch-on time from enable of SWD path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			10	
SWD_TOFF	Switch-off time from disable of SWD path	Time from disable bit at charge-pump steady state			500	ns
SWD_BW	3-dB bandwidth of SWD path	C_L = 10 pF	200			MHz
DEBUG1 MULTIPLEXER PATH						
DB1_RON_U	On resistance DEBUG1 to C_USB_TP/BP	V_i = 3.3 V, I_O = 20 mA		14	26	Ω
		V_i = 1 V, I_O = 20 mA		10	17	
DB1_RON_S	On resistance of DEBUG1 to C_SBU1	V_i = 3.3 V, I_O = 20 mA		9.5	17	Ω
		V_i = 1 V, I_O = 20 mA		6.5	12	
DB1_TON	Switch-on time from enable of DEBUG path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			10	
DB1_TOFF	Switch-off time from disable of DEBUG path	Time from disable bit at charge-pump steady state			500	ns
DB1_BW	3-dB bandwidth of DEBUG path	C_L = 10 pF	200			MHz
AUX MULTIPLEXER PATH(1)						
AUX_RON	On resistance of AUX_P/N to C_SBU1/2	V_i = 3.3 V, I_O = 20 mA		3.5	7	Ω
		V_i = 1 V, I_O = 20 mA		2.5	5	
AUX_ROND	On resistance difference between P and N paths of AUX_P/N to C_SBU1/2	V_i = 1 V to 3.3 V, I_O = 20 mA	–0.25		0.25	Ω

7.12 Port Data Multiplexer Switching Characteristics (continued)

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUX_TON	Switch-on time from enable of AUX_P/N to C_SBU1/2	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			15	
AUX_TOFF	Switch-off time from disable of AUX_P/N to C_SBU1/2	Time from disable bit at charge-pump steady state			500	ns
AUX_BW	3-dB bandwidth of AUX_P/N to C_SBU1/2 path	C_L = 10 pF	200			MHz
USB_RP MULTIPLEXER PATH(1) (2)						
USB_RON	On resistance of USB_RP to C_USB_TP/TN/BP/BN	V_I = 3 V, I_O = 20 mA		4.5	10	Ω
		V_I = 400 mV, I_O = 20 mA		3	7	
USB_ROND	On resistance difference between P and N paths of USB_RP to C_USB_TP/TN/BP/BN	V_I = 0.4 V to 3 V, I_O = 20 mA	–0.15		0.15	Ω
USB_TON	Switch-on time from enable of USB USB_RP path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			15	
USB_TOFF	Switch-off time from disable of USB_RP path	Time from disable bit at charge-pump steady state			500	ns
USB_BW	3-dB bandwidth of USB_RP path	C_L = 10 pF	850			MHz
USB_ISO	Off isolation of USB_RP path	R_L = 50 Ω, V_I = 800 mV, f = 240 MHz			–19	dB
USB_XTLK	Channel to channel crosstalk of USB_RP path	R_L = 50 Ω, f = 240 MHz			–26	dB
C_SBU1/2 OUTPUT						
R_SBU_OPEN	Resistance of the open C_SBU1/2 paths	V_I = 0 V to LDO_3V3	1			MΩ
R_USB_OPEN	Resistance of the open C_USB_T/B/P/N paths	V_I = 0 V to LDO_3V3	1			MΩ

(1) All RON specified maximums are the maximum of either of the switches in a pair. All ROND specified maximums are the maximum difference between the two switches in a pair. ROND does not add to RON.
(2) See *Port Data Multiplexer USB Endpoint Requirements and Characteristics* for the USB_EP specifications.

7.13 Port Data Multiplexer Clamp Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCLMP_IND	Clamp voltage triggering indicator to digital core		3.8	3.95	4.1	V
ICLMP_IND	Clamp current at VCLMP_IND		10		250	µA
TCLMP_PRT(1)	Time from clamp current crossing ICLMP_IND to interrupt signal assertion	I ≥ ICLMP_IND rising	0		4	µs
ICLMP	USB_EP and USB_RP port clamp current	V = LDO_3V3			250	nA
		V = VCLMP_IND + 500 mV	3.5		15	mA

(1) The TCLMP_PRT time includes the time through the digital synchronizers. When the clock speed is reduced, the signal assertion time may be longer.

7.14 Port Data Multiplexer SBU Detection Requirements

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH_PORT	Port-switch detect input-high voltage	LDO_3V3 = 3.3 V	2.			v
VIL_PORT	Port-switch detect input-low voltage	LDO_3V3 = 3.3 V			0.8	V

7.15 Port Data Multiplexer Signal Monitoring Pullup and Pulldown Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RPU05	500-Ω pull-up and pull-down resistance	LDO_3V3 = 3.3 V	350	500	650	Ω
RTPU5	5-kΩ pull-up and pull-down resistance	LDO_3V3 = 3.3 V	3.5	5	6.5	kΩ
RPU100	100-kΩ pull-up and pull-down resistance	LDO_3V3 = 3.3 V	70	100	130	kΩ

7.16 Port Data Multiplexer USB Endpoint Requirements and Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTER(1)						
T_RISE_EP	Rising transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_FALL_EP	Falling transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_RRM_EP	Rise and fall time matching	Low-speed (1.5 Mbps) data rate only	–20%		25%	
V_XOVER_EP	Output crossover voltage		1.3		2	V
RS_EP	Source resistance of driver including 2nd-stage port-data multiplexer			34		Ω
DIFFERENTIAL RECEIVER (1)						
VOS_DIFF_EP	Input offset		–100		100	mV
VIN_CM_EP	Common-mode range		0.8		2.5	V
RPU_EP	D– bias resistance	Receiving	1.425		1.575	kΩ
SINGLE ENDED RECEIVER(1)						
VTH_SE_EP	Single ended threshold	Signal rising and falling	0.8		2	V
VHYS_SE_EP	Single ended threshold hysteresis	Signal falling		200		mV

(1) The USB Endpoint PHY is functional across the entire VIN_3V3 operating range, but parameter values are only verified by design for VIN_3V3 ⩾ 3.135 V

7.17 Port Data Multiplexer BC1.2 Detection Requirements and Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA CONTACT DETECT						
IDP_SRC	DCD source current	LDO_3V3 = 3.3 V	7	10	13	µA
RDM_DWN	DCD pull-down resistance		14.25	20	24.8	kΩ
VLGC_HI	Threshold for no connection	VC_USB_TP/BP ⩾ VLGC_HILDO_3V3 = 3.3 V LDO_3V3 = 3.3 V	2			V
VLGC_LO	Threshold for connection	VC_USB_TP/BP ⩽ VLGC_LO LDO_3V3 = 3.3 V			0.8	V
PRIMARY AND SECONDARY DETECT						
VDX_SRC	Source voltage		0.55	0.6	0.65	V
VDX_RSRC	Total series resistance because of port data multiplexer	VDX_SRC = 0.65 V			65	Ω
VDX_ILIM	VDX_SRC current limit		250		400	µA
IDX_SNK	Sink current	VC_USB_TN/BN ⩾ 250 mV	25	75	125	µA

7.18 Analog-to-Digital Converter (ADC) Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RES_ADC	ADC current			10		bits

7.18 Analog-to-Digital Converter (ADC) Characteristics (continued)

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_ADC	ADC clock frequency		1.477	1.5	1.523	MHz
T_ENA	ADC enable time		42.14	43	43.86	µs
T_SAMPLEA	ADC input sample time		10.5	10.67	10.9	µs
T_CONVERTA	ADC conversion time		7.88	8	8.12	µs
T_INTA	ADC interrupt time		1.31	1.33	1.45	µs
LSB	Least significant bit		1.152	1.17	1.188	mV
DNL	Differential non-linearity		–0.65		0.65	LSB
INL	Integral non-linearity		–1.2		1.2	LSB
GAIN_ERR	Gain error (divider)		–1.5%		1.5%	
	Gain error (no divider)		–1		1	
VOS_ERR	Buffer offset error		–10		10	mV
THERM_ACC	Thermal sense accuracy		–8		8	°C
THERM_GAIN	Thermal slope			3.095		mV/°C
THERM_V0	Zero degree voltage			0.823		V

7.19 Input-Output (I/O) Requirements and Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
SPI_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SPI_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SPI_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SPI_ILKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SPI_VOH	SPI output-high voltage	I_O = –8 mA, LDO_3V3=3.3 V	2.9			V
		I_O = –15 mA, LDO_3V3=3.3 V	2.5			
SPI_VOL	SPI output-low voltage	I_O = 10 mA			0.4	V
		I_O = 20 mA			0.8	
SWDIO						
SWDIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SWDIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SWDIO_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SWDIO_ILKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SWDIO_VOH	Output high voltage	I_O = –8 mA, LDO_3V3 = 3.3 V	2.9			V
		I_O = –15 mA, LDO_3V3 = 3.3 V	2.5			
SWDIO_VOL	Output low voltage	I_O = 10 mA			0.4	V
		I_O = 20 mA			0.8	
SWDIO_RPU	Pull-up resistance		2.8	4	5.2	kΩ
SWDIO_TOS	SWDIO output skew to falling edge SWDCLK		–5		5	ns
SWDIO_TIS	Input setup time required between SWDIO and rising edge of SWCLK		6			ns
SWDIO_TIH	Input hold time required between SWDIO and rising edge of SWCLK		1			ns
SWDCLK						
SWDCL_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SWDCL_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V

7.19 Input-Output (I/O) Requirements and Characteristics (continued)

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWDCL_THI	SWDIOCLK HIGH period		0.05		500	µs
SWDCL_TLO	SWDIOCLK LOW period		0.05		500	µs
SWDCL_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SWDCL_RPU	Pull-up resistance		2.8	4	5.2	kΩ
GPIO (GPIO0, GPIO2-8, DEBUG1, DEBUG_CTL1/2, MRESET, RESETZ, BUSPOWERZ)						
GPIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
		VDDDIO = 1.8 V	1.25			
GPIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
		VDDIO = 1.8 V			0.63	
GPIO_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
		VDDIO = 1.8 V	0.09			
GPIO_ILKG	I/O leakage current	Pin is Hi-Z; V_{IN} = 0 V to VDD (VDDIO or LDO_3V3)	–1		1	µA
GPIO_RPU	Pull-up resistance (GPIO0, GPIO2-8, DEBUG1, MRESET, RESETZ, BUSPOWERZ)	Pull-up enabled	50	100	150	kΩ
	Pull-up resistance (DEBUG_CTL1/2)		2.5	5	7.5	
GPIO_RPD	Pull-down resistance (GPIO0, GPIO2-8, DEBUG1, MRESET, RESETZ, BUSPOWERZ)(1)	Pull-down enabled	50	100	150	kΩ
GPIO_DG	Digital input path de-glitch			20		ns
GPIO_VOH	GPIO output-high voltage	I_O = –2 mA, LDO_3V3 = 3.3 V	2.9			V
		I_O = –2 mA, VDDIO = 1.8 V	1.35			
GPIO_VOL	GPIO output-low voltage	I_O = 2 mA, LDO_3V3 = 3.3 V			0.4	V
		I_O = 2 mA, VDDIO = 1.8 V			0.45	
I2C_IRQZ						
OD_VOL	Low-level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SBU						
SBU_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SBU_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SBU_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V

(1) DEBUG_CTL1/2 do not have an internal pull-down resistance path.

7.20 I²C Slave Requirements and Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA AND SCL COMMON CHARACTERISTICS						
ILEAK	Input leakage current	Voltage on Pin = LDO_3V3	-3		3	µA
VOL	SDA output low voltage	IOL = 3 mA, LDO_3V3 = 3.3 V			0.4	V
		IOL = 3 mA, VDDIO = 1.8 V			0.36	
IOL	SDA max output low current	VOL = 0.4 V	3			mA
		VOL = 0.6 V	6			
VIL	Input low signal	LDO_3V3 = 3.3 V			0.99	V
		VDDIO = 1.8 V			0.54	
VIH	Input high signal	LDO_3V3 = 3.3 V	2.31			V
		VDDIO = 1.8 V	1.26			
VHYS	Input Hysteresis	LDO_3V3 = 3.3 V	0.17			V
		VDDIO = 1.8 V	0.09			
TSP	I²C pulse width suppressed				50	ns

7.20 I²C Slave Requirements and Characteristics (continued)

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CI	Pin Capacitance				10	pF
SDA AND SCL STANDARD MODE CHARACTERISTICS						
FSCL	I²C clock frequency		0		100	kHz
THIGH	I²C clock high time		4			µs
TLOW	I²C clock low time		4.7			µs
TSUDAT	I²C serial data setup time		250			ns
THDDAT	I²C serial data hold time		0			ns
TVDDAT	I²C valid data time	SCL low to SDA output valid			3.4	µs
TVDACK	I²C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			3.4	µs
TOCF	I²C output fall time	10-pF to 400-pF bus			250	ns
TBUF	I²C bus free time between stop and start		4.7			µs
TSTS	I²C start or repeated start-condition setup time		4.7			µs
TSTH	I²C start or repeated start-condition hold time		4			µs
TSPS	I²C stop condition setup time		4			µs
SDA AND SCL FAST MODE CHARACTERISTICS						
FSCL	I²C clock frequency		0		400	kHz
THIGH	I²C clock high time		0.6			µs
TLOW	I²C clock low time		1.3			µs
TSUDAT	I²C serial data setup time		100			ns
THDDAT	I²C serial data hold time		0			ns
TVDDAT	I²C valid data time	SCL low to SDA output valid			0.9	µs
TVDACK	I²C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			0.9	µs
TOCF	I²C output fall time	10-pF to 400-pF bus, VDD = 3.3 V	12		250	ns
		10-pF to 400-pF bus, VDD = 1.8 V	6.5		250	
TBUF	I²C bus free time between stop and start		1.3			µs
TSTS	I²C start or repeated start-condition setup time		0.6			µs
TSTH	I²C start or repeated start-condition hold time		0.6			µs
TSPS	I²C stop condition setup time		0.6			µs

7.21 SPI Controller Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSPI	Frequency of SPI_CLK		11.82	12	12.18	MHz
TPER	Period of SPI_CLK (1/F_SPI)		82.1	83.33	84.6	ns
TWHI	SPI_CLK high width		30			ns
TWLO	SPI_CLK low width		30			ns
TDACT	SPI_SZZ falling to SPI_CLK rising delay time		30		50	ns
TDINACT	SPI_CLK falling to SPI_CSZ rising delay time		160		180	ns
TDPICO	SPI_CLK falling to SPI_PICO Valid delay time		–5		5	ns
TSUPOCI	SPI_POCI valid to SPI_CLK falling setup time		21			ns
THDMSIO	SPI_CLK falling to SPI_POCI invalid hold time		0			ns
TRSPI	SPI_CSZ/CLK/PICO rise time	10% to 90%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSPI	SPI_CSZ/CLK/PICO fall time	90% to 10%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

7.22 BUSPOWERZ Configuration Requirements

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBPZ_EXT	BUSPOWERZ Voltage for receiving VBUS Power through the PP_EXT path				0.8	V
VBPZ_HV	BUSPOWERZ Voltage for receiving VBUS Power through the PP_HV path		0.8		2.4	V
VBPZ_DIS	BUSPOWERZ Voltage for disabling system power from VBUS		2.4			V

7.23 Single-Wire Debugger (SWD) Timing Requirements

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

			MIN	NOM	MAX	UNIT
FSWD	Frequency of SWD_CLK				10	MHz
TPER	Period of SWD_CLK (1/FSWD)		100			ns
TWHI	SWD_CLK high width		35			ns
TWLO	SWD_CLK low width		35			ns
TDOUT	SWD_CLK rising to SWD_DATA valid delay time		2		25	ns
TSUIN	SWD_DATA valid to SWD_CLK rising setup time		9			ns
THDIN	SWD_DATA hold time from SWD_CLK rising		3			ns
TRSWD	SWD output rise time	10% to 90%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSWD	SWD output fall time	90% to 10%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

7.24 Thermal Shutdown Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD_MAIN	Thermal shutdown temperature of the main thermal shutdown	Temperature rising	145	160	175	°C
TSDH_MAIN	Thermal shutdown hysteresis of the main thermal shutdown	Temperature falling		20		°C
TSD_PWR	Thermal shutdown temperature of the power path block	Temperature rising	135	150	165	°C
TSDH_PWR	Thermal shutdown hysteresis of the power path block	Temperature falling		37		°C
TSD_DG	Programmable thermal shutdown detection de-glitch time				0.1	ms

7.25 HPD Timing Requirements and Characteristics

Recommended operating conditions; T_A = -40 to 105°C unless otherwise noted

			MIN	NOM	MAX	UNIT
DP SOURCE SIDE (HPD TX)						
T_IRQ_MIN	HPD IRQ minimum assert time		675	750	825	µs
T_3MS_MIN	HPD assert 3-ms minimum time		3	3.33	3.67	ms
DP SINK SIDE (HPD RX)						
T_HPD_HDB	HPD high de-bounce time	HPD_HDB_SEL = 0	300	375	450	µs
		HPD_HDB_SEL = 1	100	111	122	ms
T_HPD_LDB	HPD low de-bounce time		300	375	450	µs
T_HPD_IRQ	HPD IRQ limit time		1.35	1.5	1.65	ms

7.26 Oscillator Requirements and Characteristics

Recommended operating conditions; T_A = –40°C to +105°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FOSC_48M	48-MHz oscillator		47.28	48	48.72	MHz
FOSC_100K	100-kHz oscillator		95	100	105	kHz
RR_OSC	External oscillator set resistance (0.2%)		14.985	15	15.015	kΩ

7.27 Typical Characteristics

(T_A = –40°C to +105°C)

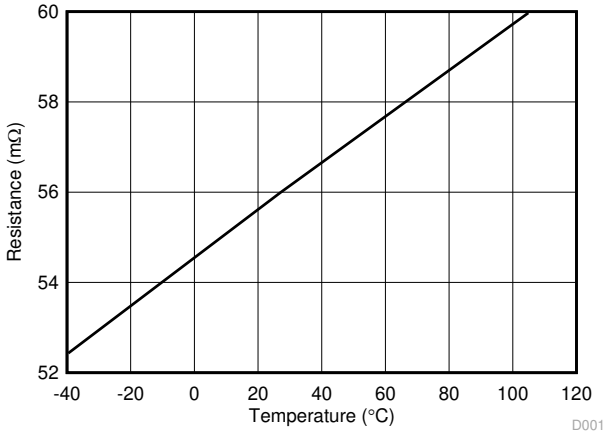


图 7-1. PP_5V0 Switch On-Resistance vs Temperature

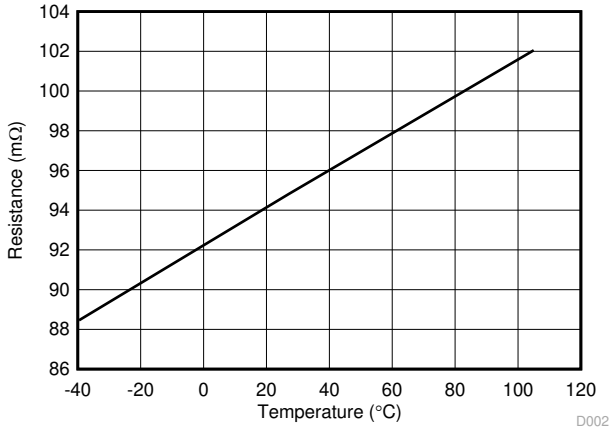


图 7-2. PP_HV Switch On-Resistance vs Temperature

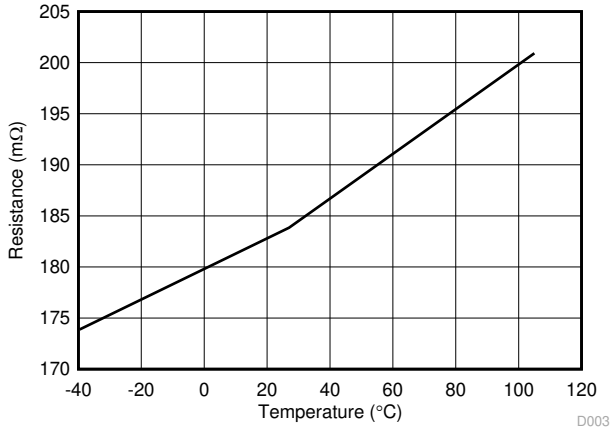


图 7-3. PP_CABLE Switch On-Resistance vs Temperature

8 Parameter Measurement Information

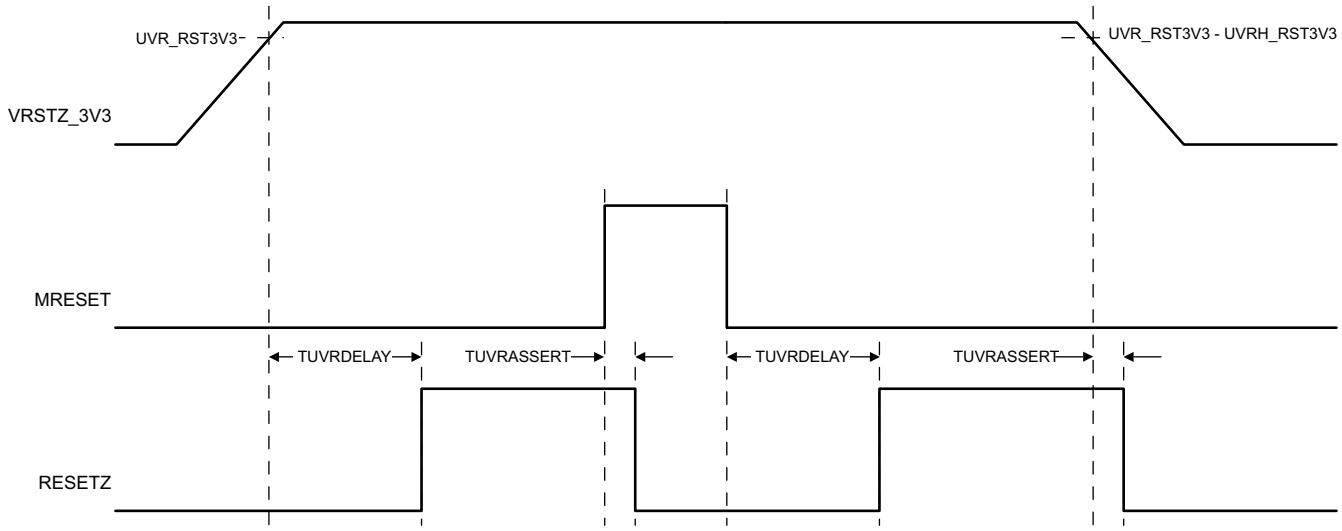


图 8-1. RESETZ Assertion Timing

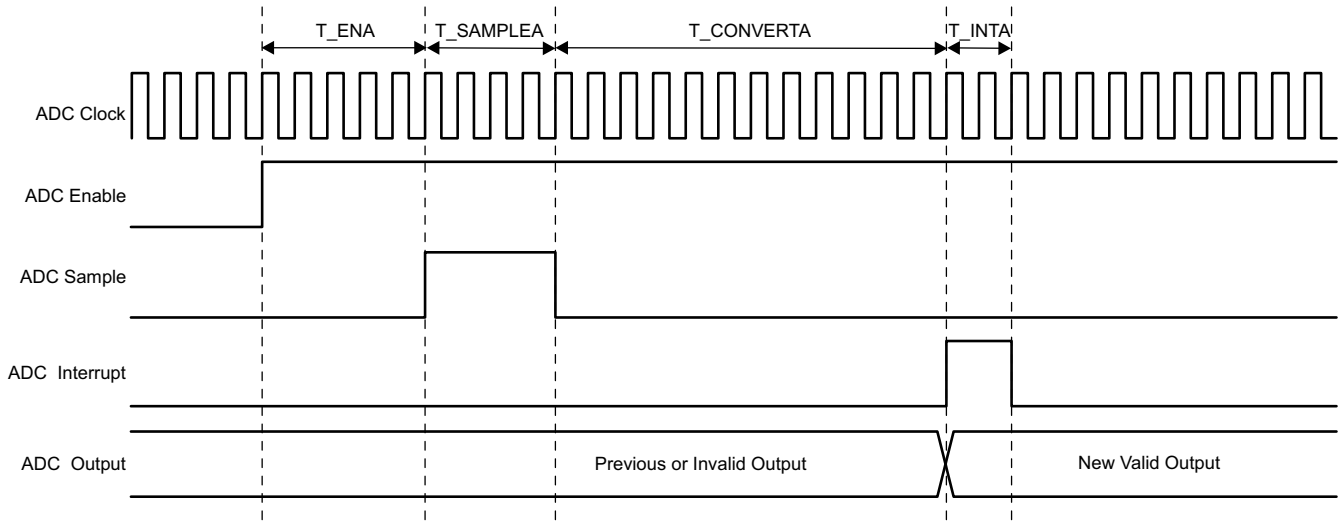


图 8-2. ADC Enable and Conversion Timing

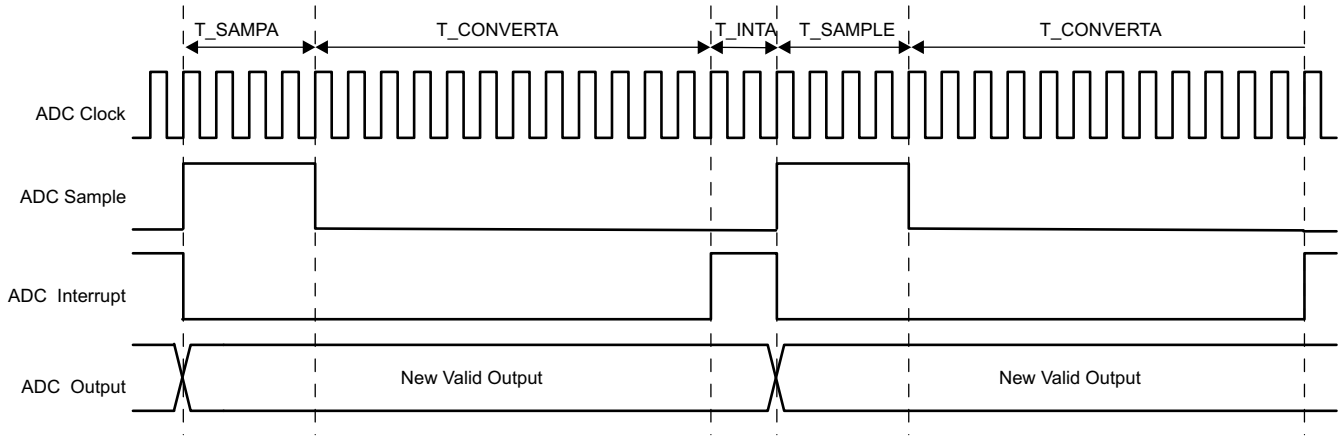


图 8-3. ADC Repeated Conversion Timing

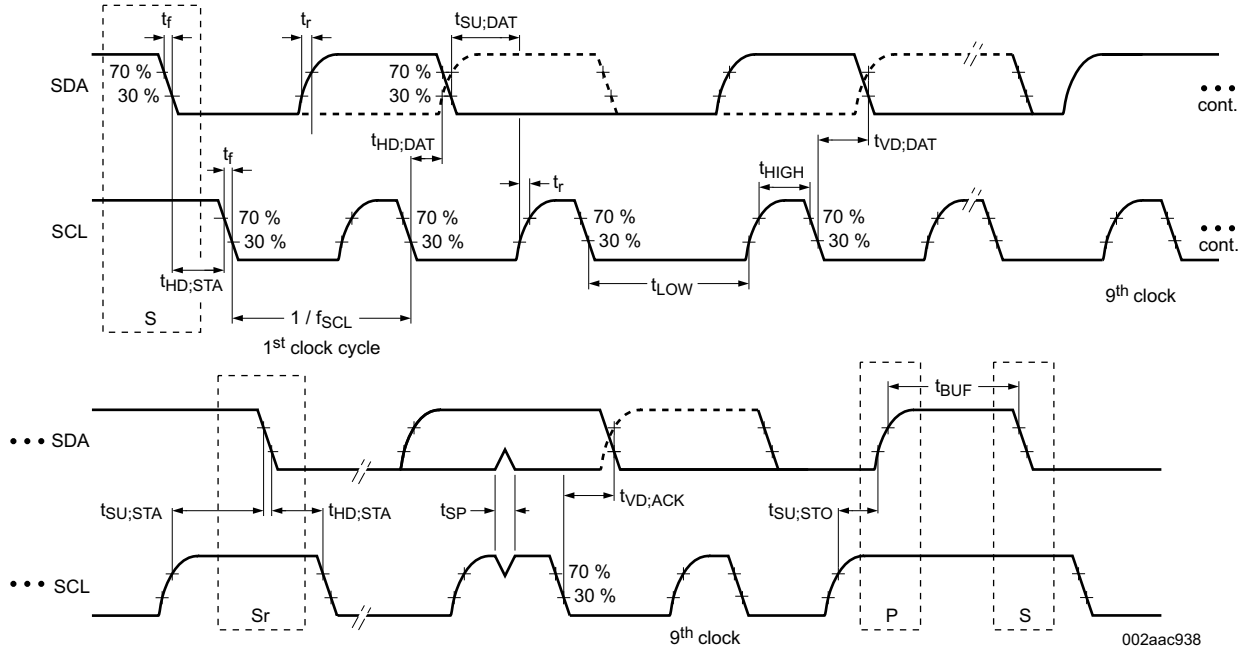


图 8-4. I²C Slave Interface Timing

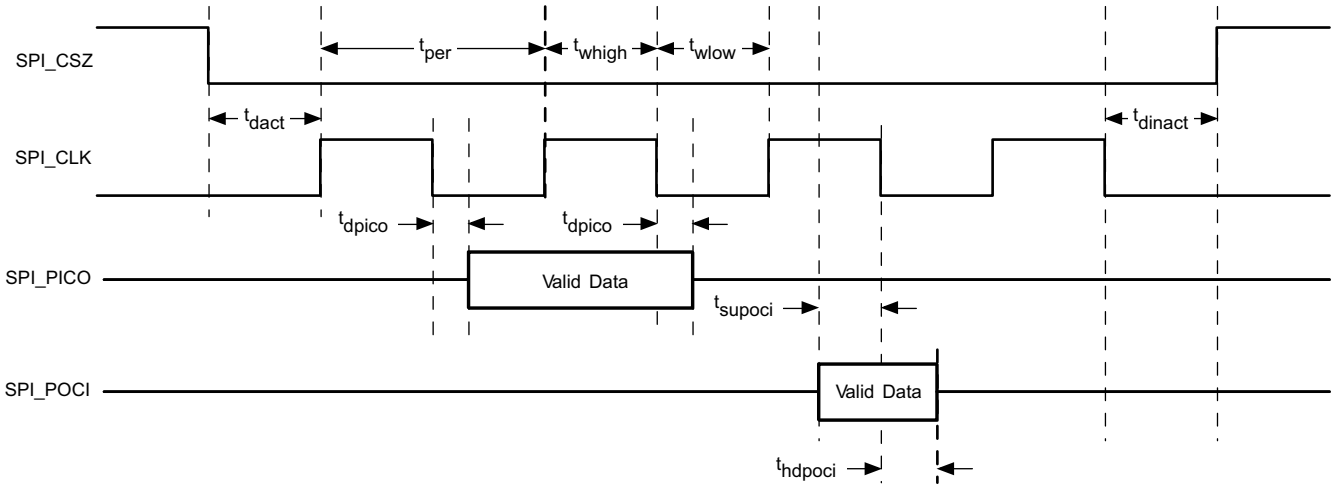


图 8-5. SPI Controller Timing

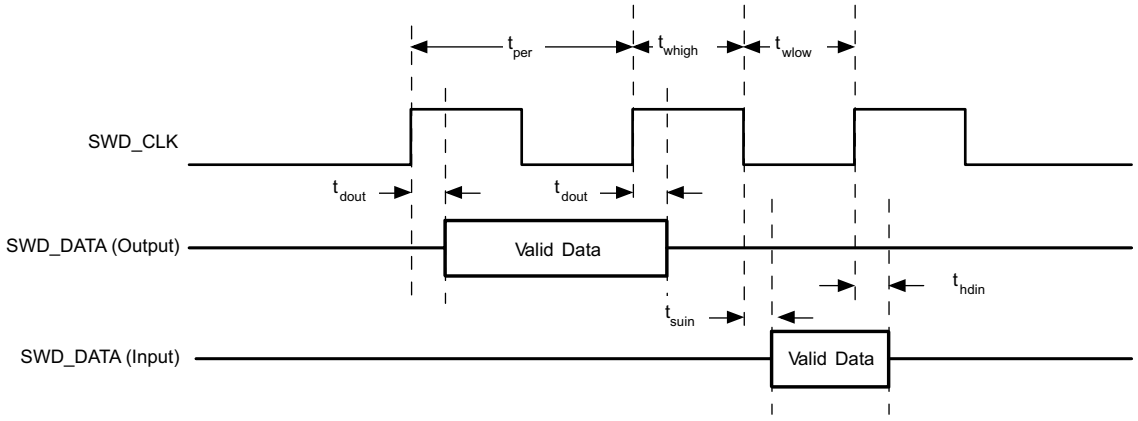


图 8-6. SWD Timing

9 Detailed Description

9.1 Overview

The TPS65981 is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for a USB Type-C and PD plug or receptacle. The TPS65981 communicates with the cable and another USB Type-C and PD device at the opposite end of the cable, enables integrated port power switches, controls an external high current port power switch, and multiplexes high-speed data to the port for USB2.0 and supported Alternate Mode sideband information. The TPS65981 also controls an attached super-speed multiplexer to simultaneously support USB3.0/3.1 data rates and DisplayPort video.

The TPS65981 is divided into six main sections: the USB-PD controller, the cable plug and orientation detection circuitry, the port power switches, the port data multiplexer, the power management circuitry, and the digital core.

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the C_CC1 pin or the C_CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of the features and more detailed circuitry, refer to the *USB-PD Physical Layer* section.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of the features and more detailed circuitry, refer to the *Cable Plug and Orientation Detection* section.

The port power switches provide power to the system port through the VBUS pin and also through the C_CC1 or C_CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of the features and more detailed circuitry, refer to the *Port Power Switches* section.

The port data multiplexer connects various input pairs to the system port through the C_USB_TP, C_USB_TN, C_USB_BP, C_USB_BN, C_SBU1 and C_SBU2 pins. For a high-level block diagram of the port data multiplexer, a description of the features and more detailed circuitry, refer to the *USB Type-C Port Data Multiplexer* section.

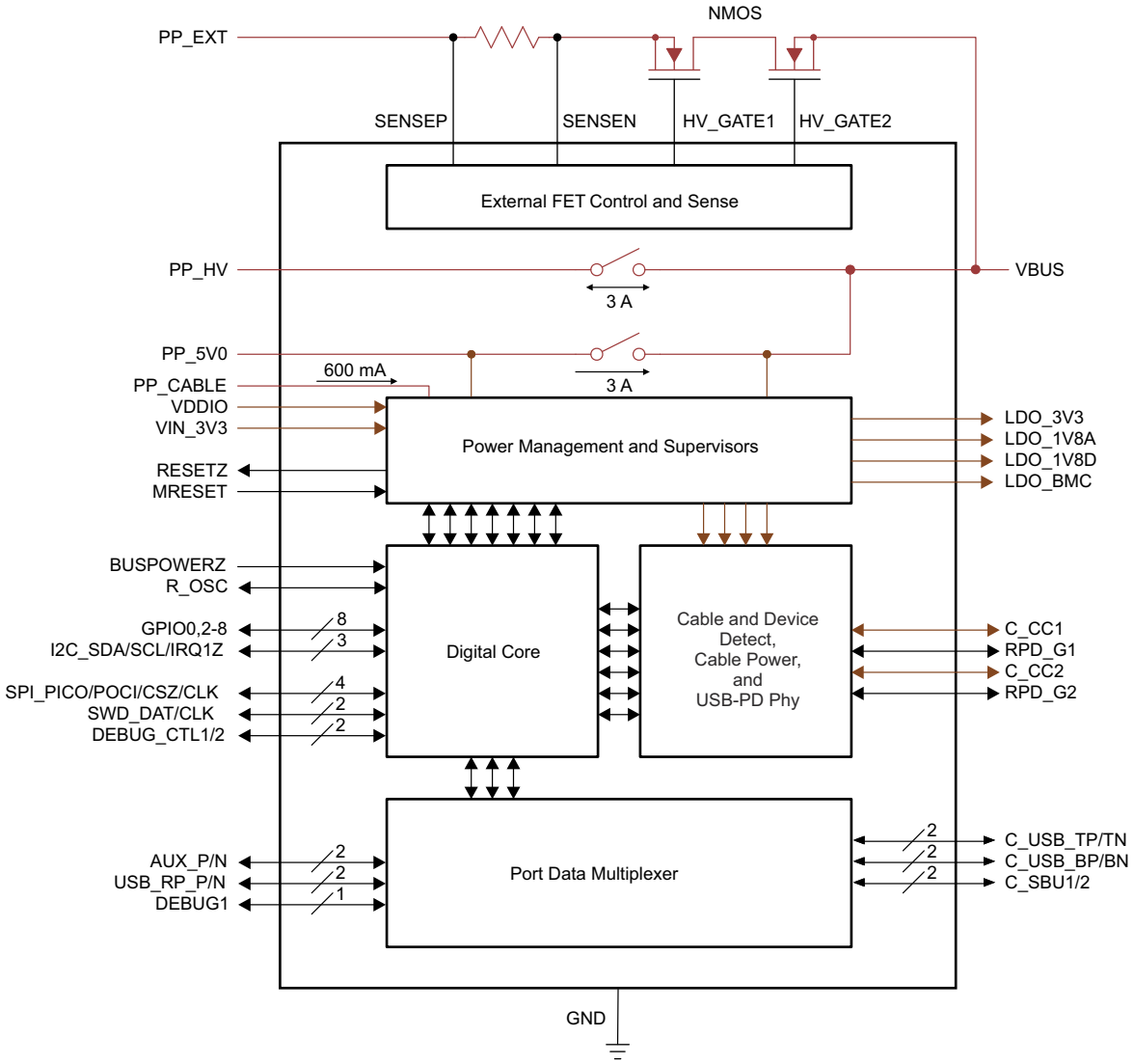
The power management circuitry receives and provides power to the TPS65981 internal circuitry and to the LDO_3V3 output. For a high-level block diagram of the power management circuitry, a description of the features and more detailed circuitry, refer to the *Power Management* section.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other TPS65981 functionality. A small portion of the digital core contains non-volatile memory, called boot code, which is capable of initializing the TPS65981 and loading a larger, configurable portion of application code into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of the features and more detailed circuitry, refer to the *Digital Core* section.

The digital core of the TPS65981 also interprets and uses information provided by the analog-to-digital converter ADC (see the *ADC* section), is configurable to read the status of general purpose inputs and trigger events accordingly, and controls general outputs which are configurable as push-pull or open-drain types with integrated pull-up or pull-down resistors and can operate tied to a 1.8-V or 3.3-V rail. The TPS65981 is an I^2C slave to be controlled by a host processor (see the *I^2C Slave Interface* section), an SPI controller to write to and read from an external flash memory (see the *SPI Controller Interface* section), and is programmed by a single-wire debugger (SWD) connection (see the *Single-Wire Debugger Interface* section).

The TPS65981 also integrates a thermal shutdown mechanism (see *Thermal Shutdown* section) and runs off of accurate clocks provided by the integrated oscillators (see the *Oscillators* section).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 USB-PD Physical Layer

图 9-1 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

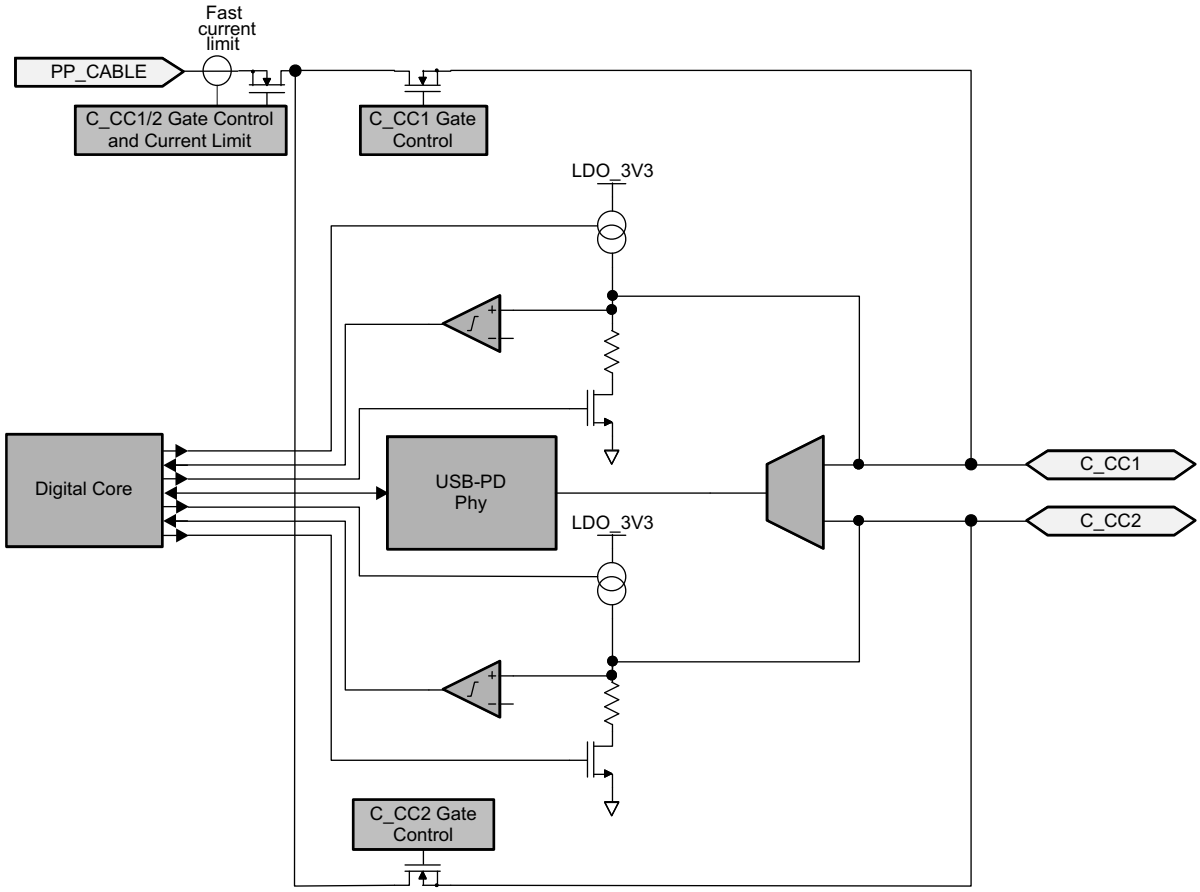


图 9-1. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (C_CC1 or C_CC2) that is DC biased because of the DFP (or UFP) cable attach mechanism discussed in the *Cable Plug and Orientation Detection* section.

9.3.1.1 USB-PD Encoding and Signaling

图 9-2 illustrates the high-level block diagram of the baseband USB-PD transmitter. 图 9-3 illustrates the high-level block diagram of the baseband USB-PD receiver.

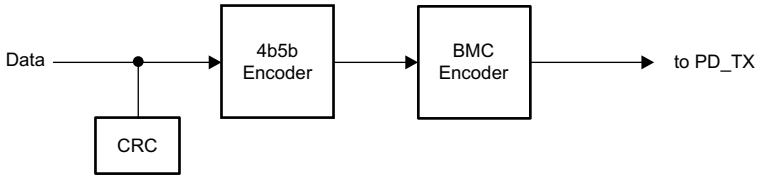


图 9-2. USB-PD Baseband Transmitter Block Diagram

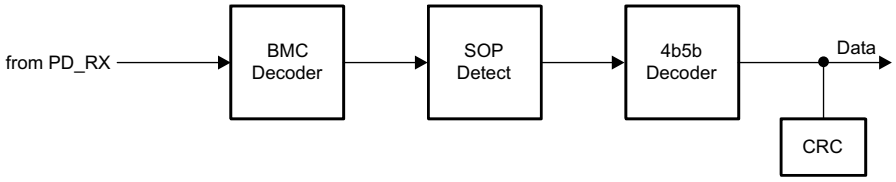


图 9-3. USB-PD Baseband Receiver Block Diagram

The USB-PD baseband signal is driven on the C_CCn pins with a tri-state driver. The tri-state driver is slew rate limited to reduce the high frequency components imparted on the cable and to avoid interference with frequencies used for communication.

9.3.1.2 USB-PD Bi-Phase Marked Coding

The USBP-PD physical layer implemented in the TPS65981 is compliant to the USB-PD Specifications. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). 图 9-4 illustrates Biphase Mark Coding.

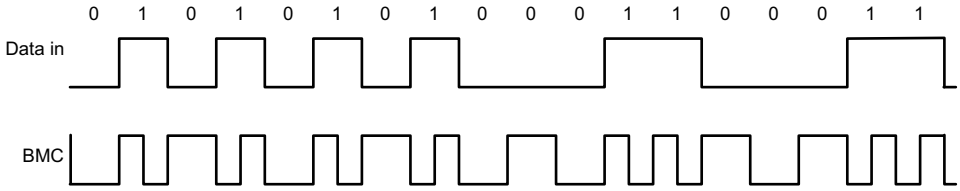


图 9-4. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the C_CC1 or C_CC2 pins with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter will start by transmitting a low level. The receiver at the other end will tolerate the loss of the first edge. The transmitter will terminate the final bit by an edge to ensure the receiver clocks the final bit of EOP.

9.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Because a BMC coded as 1 contains a signal edge at the beginning and middle of the UI, and the BMC coded as 0 contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude because of the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that will have minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the USB-PD Specifications for more details.

9.3.1.4 USB-PD BMC Transmitter

The TPS65981 transmits and receives USB-PD data over one of the C_CCn pins. The C_CCn pin is also used to determine the cable orientation (see the *Cable Plug and Orientation Detection* section) and maintain cable/device attach detection. Thus, a DC bias will exist on the C_CCn. The transmitter driver will overdrive the C_CCn DC bias while transmitting, but will return to a Hi-Z state allowing the DC voltage to return to the C_CCn pin when not transmitting. 图 9-5 shows the USB-PD BMC TX/Rx driver block diagram.

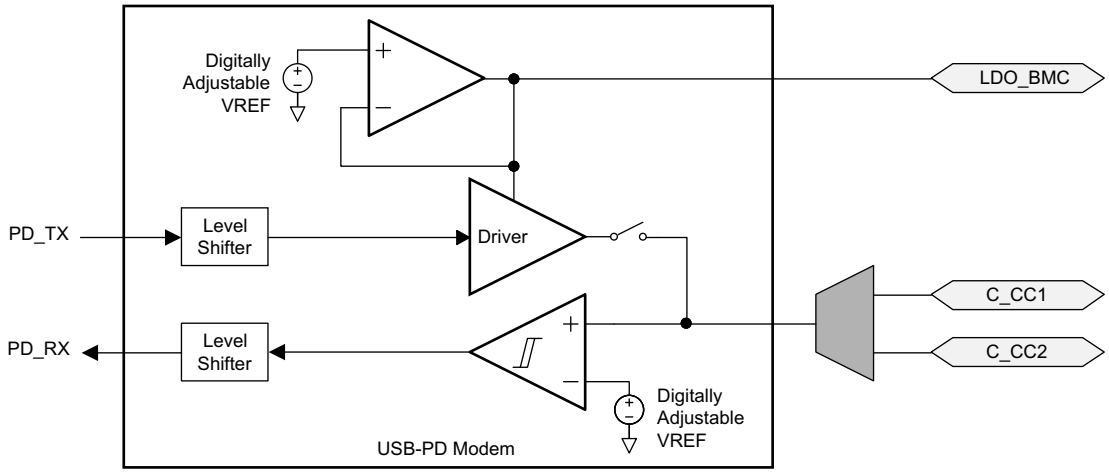


图 9-5. USB-PD BMC TX/Rx Block Diagram

图 9-6 shows the transmission of the BMC data on top of the DC bias. Note, The DC bias can be anywhere between the minimum threshold for detecting a UFP attach (VD_CCH_USB) and the maximum threshold for detecting a UFP attach to a DFP (VD_CCH_3P0) defined in the *Cable Plug and Orientation Detection* section. This means that the DC bias can be below VOH of the transmitter driver or above VOH.

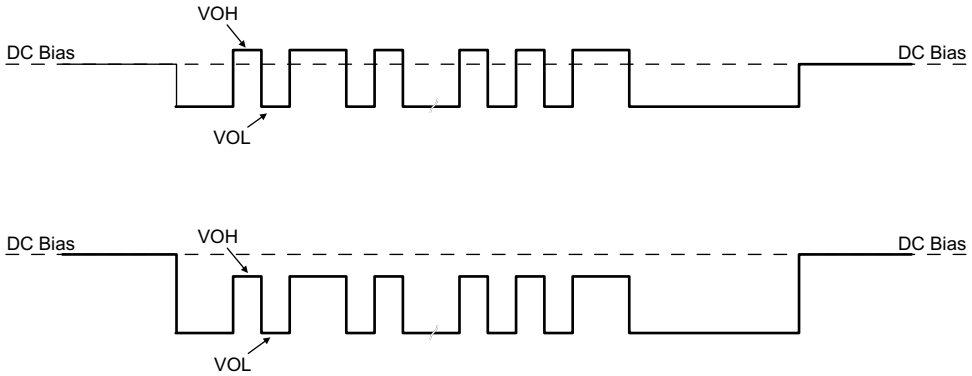


图 9-6. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the C_CCn lines. The signal peak VTXP is adjustable by application code and sets the VOH/VOL for the BMC data that is transmitted, and is defined in *USB-PD TX Driver Voltage Adjustment Parameter*. Keep in mind that the settings in a final system must meet the TX masks defined in the USB-PD Specifications.

When driving the line, the transmitter driver has an output impedance of ZDRIVER. ZDRIVER is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. ZDRIVER impacts the noise ingression in the cable.

图 9-7 shows the simplified circuit determining ZDRIVER. It is specified such that noise at the receiver is bounded.

ZDRVER is defined by 方程式 1.

$$ZDRIVER = \frac{R_{DRIVER}}{1 + s \times R_{DRIVER} \times C_{DRIVER}} \quad (1)$$

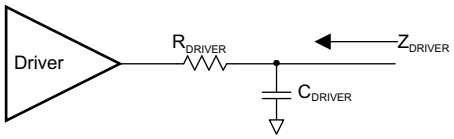


图 9-7. ZDRIVER Circuit

9.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS65981 receives a signal that falls within the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask. The values for VRXTR and VRXTF are listed in *USB-PD Baseband Signal Requirements and Characteristics*.

图 9-8 shows an example of a multi-drop USB-PD connection. This connection has the typical UFP (device) to DFP (host) connection, but also includes cable USB-PD TX/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (ZBMCRX). The USB-PD Specification also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

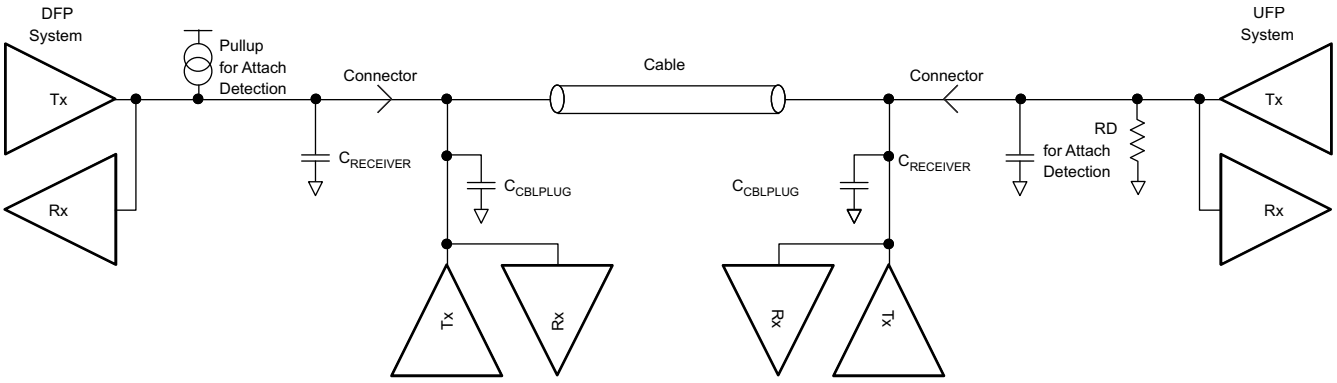


图 9-8. Example USB-PD Multi-Drop Configuration

9.3.2 Cable Plug and Orientation Detection

图 9-9 shows the plug and orientation detection block at each C_CC pin (C_CC1 and C_CC2). Each pin has identical detection circuitry.

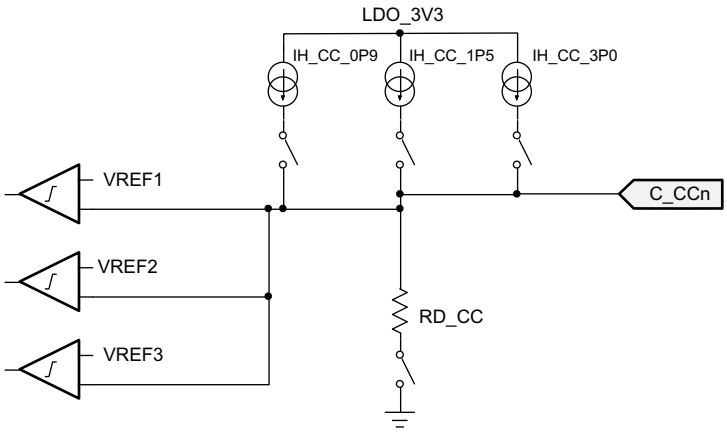


图 9-9. Plug and Orientation Detection Block

9.3.2.1 Configured as a DFP

When configured as a DFP, the TPS65981 detects when a cable or a UFP is attached using the C_CC1 and C_CC2 pins. When in a disconnected state, the TPS65981 monitors the voltages on these pins to determine what, if anything, is connected. See the USB Type-C Specification for more information.

表 9-1 shows the high-level detection results. Refer to the USB Type-C Specification for more information.

表 9-1. Cable Detect States for a DFP

C_CC1	C_CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both C_CC pins for attach. Power is not applied to VBUS or VCONN until a UFP connect is detected.
Rd	Open	UFP attached	Monitor C_CC1 for detach. Power is applied to VBUS but not to VCONN (C_CC2).
Open	Rd	UFP attached	Monitor C_CC2 for detach. Power is applied to VBUS but not to VCONN (C_CC1).
Ra	Open	Powered Cable/No UFP attached	Monitor C_CC2 for a UFP attach and C_CC1 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Open	Ra	Powered Cable/No UFP attached	Monitor C_CC1 for a UFP attach and C_CC2 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Ra	Rd	Powered Cable/UFP Attached	Provide power on VBUS and VCONN (C_CC1) then monitor C_CC2 for a UFP detach. C_CC1 is not monitored for a detach.
Rd	Ra	Powered Cable/UFP attached	Provide power on VBUS and VCONN (C_CC2) then monitor C_CC1 for a UFP detach. C_CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either C_CC pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either C_CC pin for detach.

When the TPS65981 is configured as a DFP, a current IH_CC is driven out each C_CCn pin and each pin is monitored for different states. When a UFP is attached to the pin, a pull-down resistance of Rd to GND will exist. The current IH_CC is then forced across the resistance Rd generating a voltage at the C_CCn pin.

When configured as a DFP advertising Default USB current sourcing capability, the TPS65981 applies IH_CC_USB to each C_CCn pin. When a UFP with a pull-down resistance R_D is attached, the voltage on the C_CCn pin will pull below VH_CCD_USB. The TPS65981 can also be configured as a DFP to advertise default (500 mA), 1.5-A and 3-A sourcing capabilities.

When the C_CCn pin is connected to an active cable VCONN (power to the active cable), the pull-down resistance will be different (Ra). In this case, the voltage on the C_CCn pin will pull below VH_CCA_USB/1P5/3P0 and the system will recognize the active cable.

The VH_CCD_USB/1P5/3P0 thresholds are monitored to detect a disconnection from each of these cases respectively. When a connection has been recognized and the voltage on the C_CCn pin rises above the VH_CCD_USB/1P5/3P0 threshold, the system will register a disconnection.

9.3.2.2 Configured as a UFP

When the TPS65981 is configured as a UFP, the TPS65981 presents a pull-down resistance R_{D_CC} on each C_CCn pin and waits for a DFP to attach and pull-up the voltage on the pin. The DFP will pull-up the C_CC pin by applying either a resistance or a current. The UFP detects an attachment by the presence of VBUS. The UFP determines the advertised current from the DFP by the pull-up applied to the C_CCn pin.

9.3.2.3 Dead-Battery or No-Battery Support

Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source will provide a voltage on VBUS. The TPS65981 is hardware-configurable to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd when the port is acting as a source. 图 9-10 shows the RPD_Gn pin used to configure the behavior of the C_CCn pins, and elaborates on the basic cable plug and orientation detection block shown in 图 9-9. RPD_G1 and RPD_G2 configure C_CC1 and C_CC2 respectively. A resistance R_RPD is connected to the gate of the pull-down FET on each C_CCn pin. This resistance must be pin-strapped externally to configure the C_CCn pin to behave in one of two ways: present an Rd pull-down resistance or present a Hi-Z when the TPS65981 is unpowered. During normal operation, RD will be RD_CC; however, while dead-battery or no-battery conditions exist, the resistance is un-trimmed and will be RD_DB. When RD_DB is presented during dead-battery or no-battery, application code will switch to RD_CC.

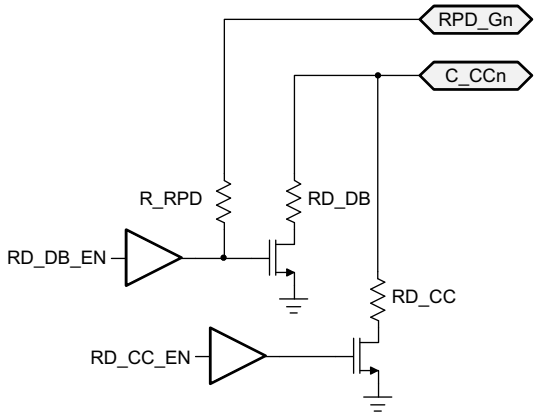


图 9-10. C_CCn and RPD_Gn pins

When C_CC1 is shorted to RPD_G1 and C_CC2 is shorted to RPD_G2 in an application of the TPS65981, booting from dead-battery or no-battery conditions will be supported. In this case, the gate driver for the pull-down FET is Hi-Z at the output. When an external connection pulls up on C_CCn (the case when connected to a DFP advertising with a pull-up resistance Rp or pull-up current), the connection through R_RPD will pull up on the FET gate turning on the pull-down through RD_DB. In this condition, the C_CCn pin will act as a clamp VTH_DB in series with the resistance RD_DB.

When RPD_G1 and RPD_G2 are shorted to GND in an application and not electrically connected to C_C1 and C_CC2, booting from dead-battery or no-battery conditions is not possible. In this case, the TPS65981 will present a Hi-Z on the C_CC1 and C_CC2 pins and a USB Type-C source will never provide a voltage on VBUS.

9.3.3 Port Power Switches

图 9-11 shows the TPS65981 port power path including all internal and external paths. The port power path provides to VBUS from PP_5V0, provides power to or from VBUS from or to PP_HV, provides power to or from an external port power node (shown and refered to as PP_EXT) from or to VBUS, and provides power from PP_CABLE to C_CC1 or C_CC2. The PP_CABLE to C_CCn switches shown in 图 9-11 are the same as in 图 9-1, but are now shown without the analog USB Type-C cable plug and orientation detection circuitry.

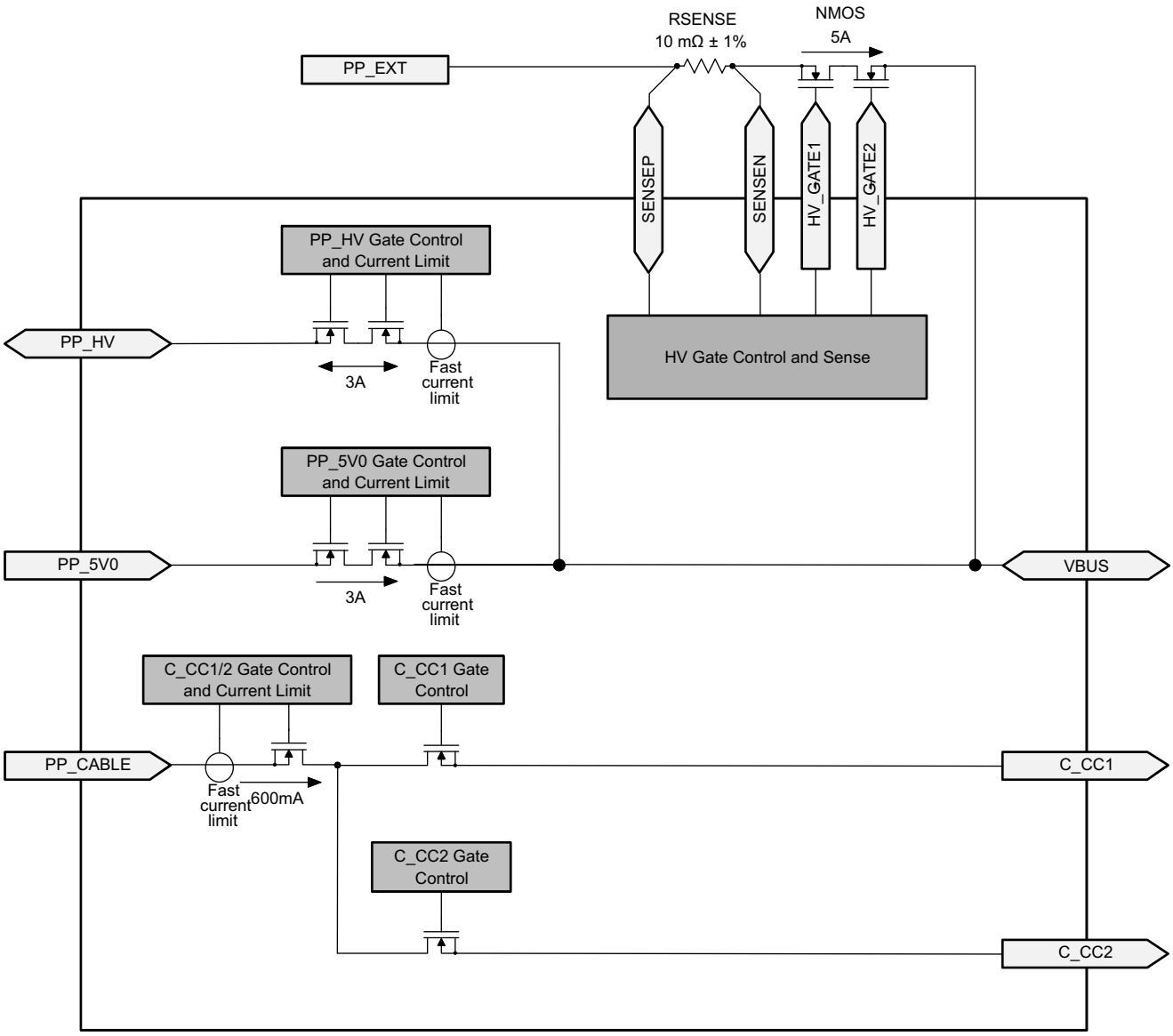


图 9-11. Port Power Paths

9.3.3.1 5-V Power Delivery

The TPS65981 provides port power to VBUS from PP_5V0 when a low voltage output is needed. The switch path provides 5 V at up to 3 A to from PP_5V0 to VBUS. 图 9-11 shows a simplified circuit for the switch from PP_5V0 to VBUS.

9.3.3.2 5V Power Switch as a Source

The PP_5V0 path is unidirectional, sourcing power from PP_5V0 to VBUS only. When the switch is on, the protection circuitry limits reverse current from VBUS to PP_5V0. 图 9-12 shows the I-V characteristics of the reverse current protection feature. 图 9-12 and the reverse current limit can be approximated using 方程式 2.

$$IREV5V0 = VREV5V0/RPP5V \quad (2)$$

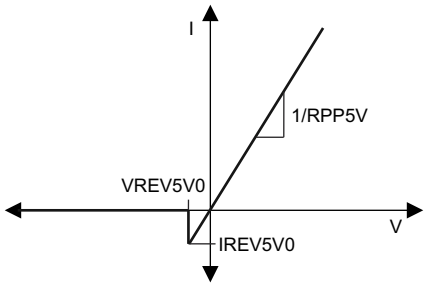


图 9-12. 5V Switch I-V Curve

9.3.3.3 PP_5V0 Current Sense

The current from PP_5V0 to VBUS is sensed through the switch and is available to be read digitally through the ADC.

9.3.3.4 PP_5V0 Current Limit

The current through PP_5V0 to VBUS is limited to ILIMPP5V and is controlled automatically by the digital core. When the current exceeds ILIMPP5V, the current-limit circuit activates. Depending on the severity of the over-current condition, the transient response will react in one of two ways: 图 9-13 and 图 9-14 show the approximate response time and clamping characteristics of the circuit for a hard short while 图 9-15 shows the shows the approximate response time and clamping characteristics for a soft short with a load of 2 Ω.

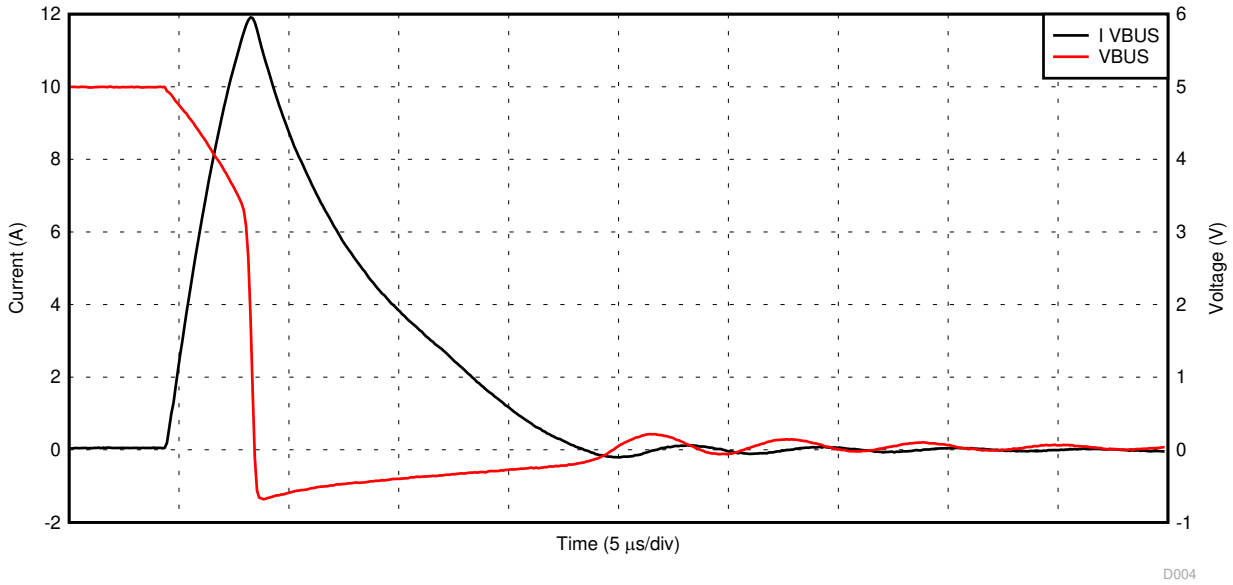


图 9-13. PP_5V0 Current Limit with a Hard Short

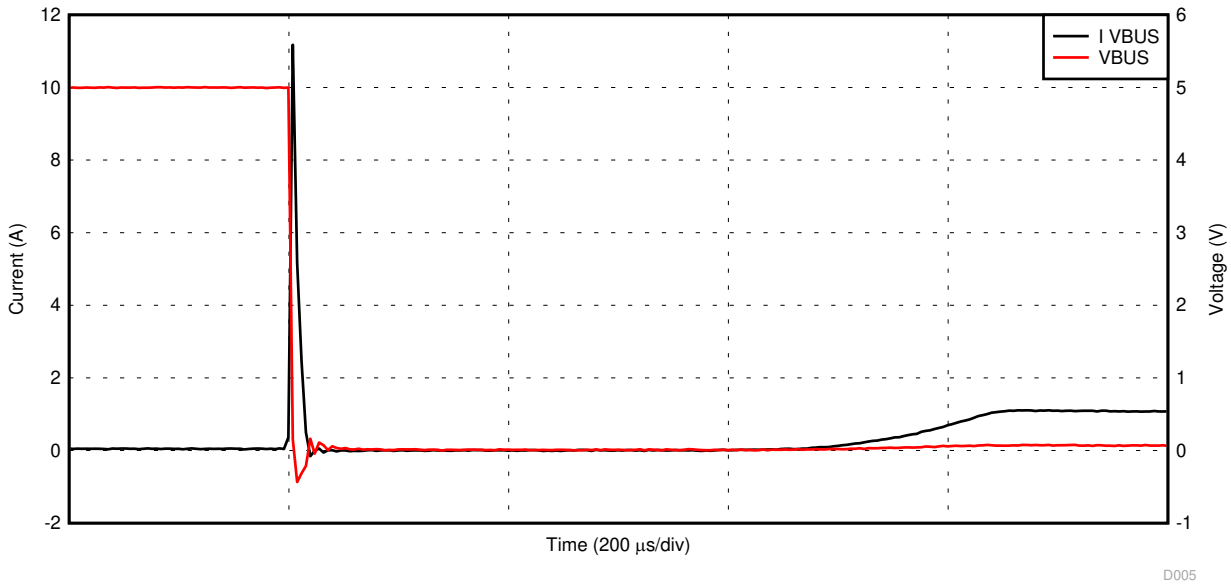


图 9-14. PP_5V0 Current Limit with a Hard Short (Extended Time Base)

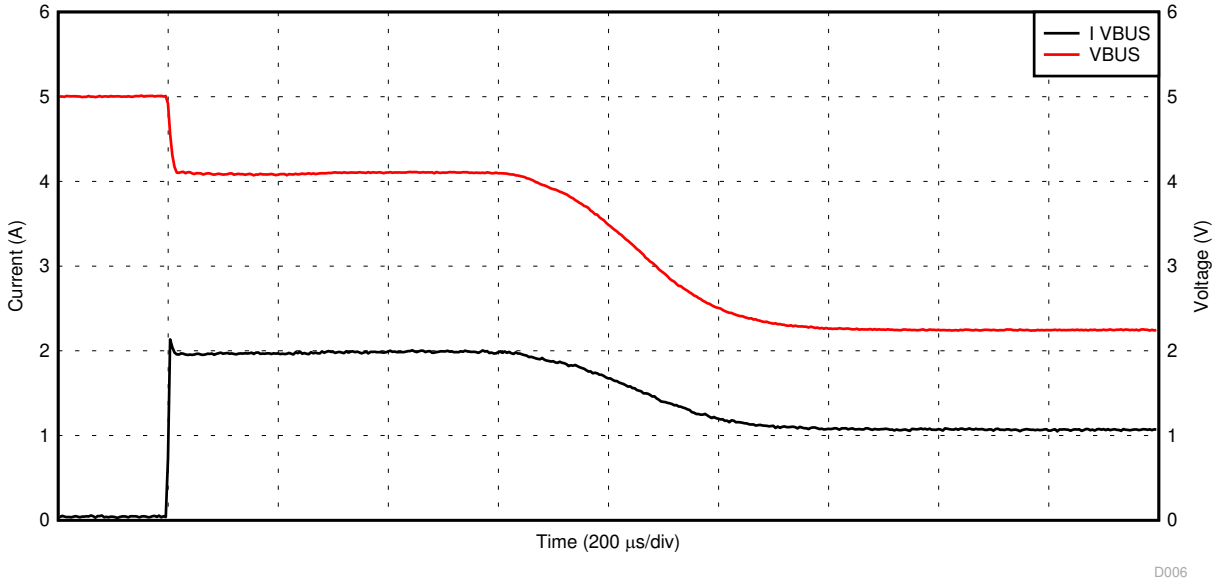


图 9-15. PP_5V0 Current Limit with a Soft Short (2 Ω)

9.3.3.5 Internal HV Power Delivery

The TPS65981 has an integrated, bi-directional high-voltage switch that is rated for up to 3 Amps of current. The TPS65981 is capable of sourcing or sinking high-voltage power through an internal switch path designed to support USB-PD power up to 20 V at 3 A of current. VBUS and PP_HV are both rated for up to 22 V as determined by *Recommended Operating Conditions*, and operate down to 0 V as determined by *Absolute Maximum Ratings*. In addition, VBUS is tolerant to voltages up to 22 V even when PP_HV is at 0 V. Similarly, PP_HV is tolerant up to 22 V while VBUS is at 0 V. The switch structure is designed to tolerate a constant operating voltage differential at either of these conditions. 图 9-11 shows a simplified circuit for the switch from PP_HV to VBUS.

9.3.3.6 Internal HV Power Switch as a Source

The TPS65981 provides power from PP_HV to VBUS at the USB Type-C port as an output when operating as a source. When the switch is on as a source, the path behaves resistively until the current reaches the amount

calculated by 方程式 3 and then blocks reverse current from VBUS to PP_HV. 图 9-16 shows the diode behavior of the switch as a source.

$$IREVHV = VREVHV/RPPHV \quad (3)$$

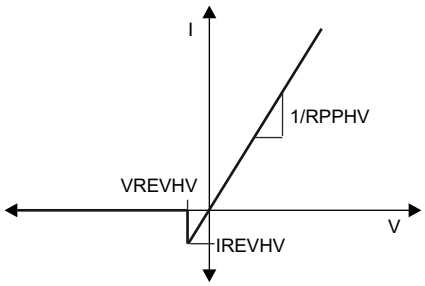


图 9-16. Internal HV Switch I-V Curve as a Source

9.3.3.7 Internal HV Power Switch as a Sink

The TPS65981 can also receive power from VBUS to PP_HV when operating as a sink. When the switch is on as a sink the path behaves as an ideal diode and blocks reverse current from PP_HV to VBUS. 图 9-17 shows the diode behavior of the switch as a sink.

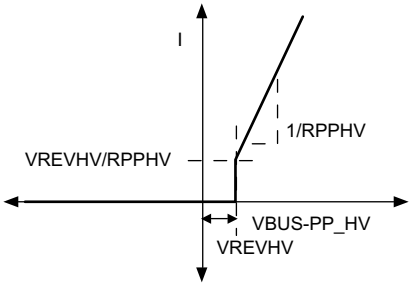


图 9-17. Internal HV Switch I-V Curve as a Sink

9.3.3.8 Internal HV Power Switch Current Sense

The current from PP_HV to VBUS is sensed through the switch and is available to be read digitally through the ADC only when the switch is sourcing power. When sinking power, the readout from the ADC will not reflect the current.

9.3.3.9 Internal HV Power Switch Current Limit

The current through PP_HV to VBUS is current limited to ILIMPPHV (only when operating as a source) and is controlled automatically by the digital core. When the current exceeds ILIMPPHV, the current-limit circuit activates. Depending on the severity of the over-current condition, the transient response will react in one of two ways: 图 9-18 shows the approximate response time and clamping characteristics of the circuit for a hard short while 图 9-19 shows the approximate response time and clamping characteristics for a soft short of 7 Ω.

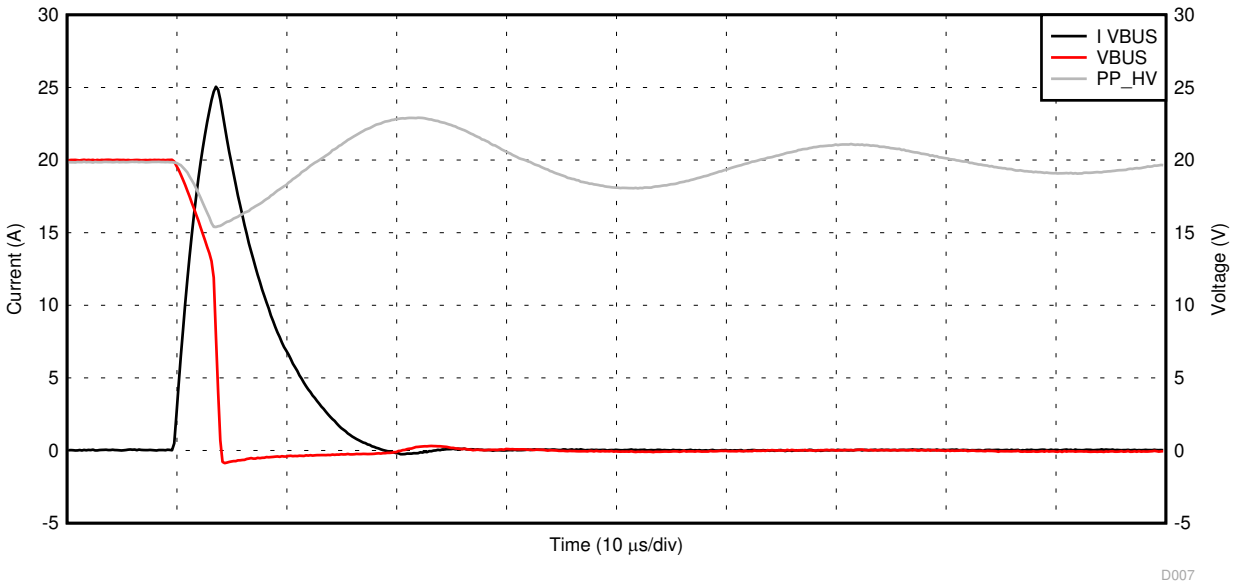


图 9-18. PP_HV Current Limit Response with a Hard Short

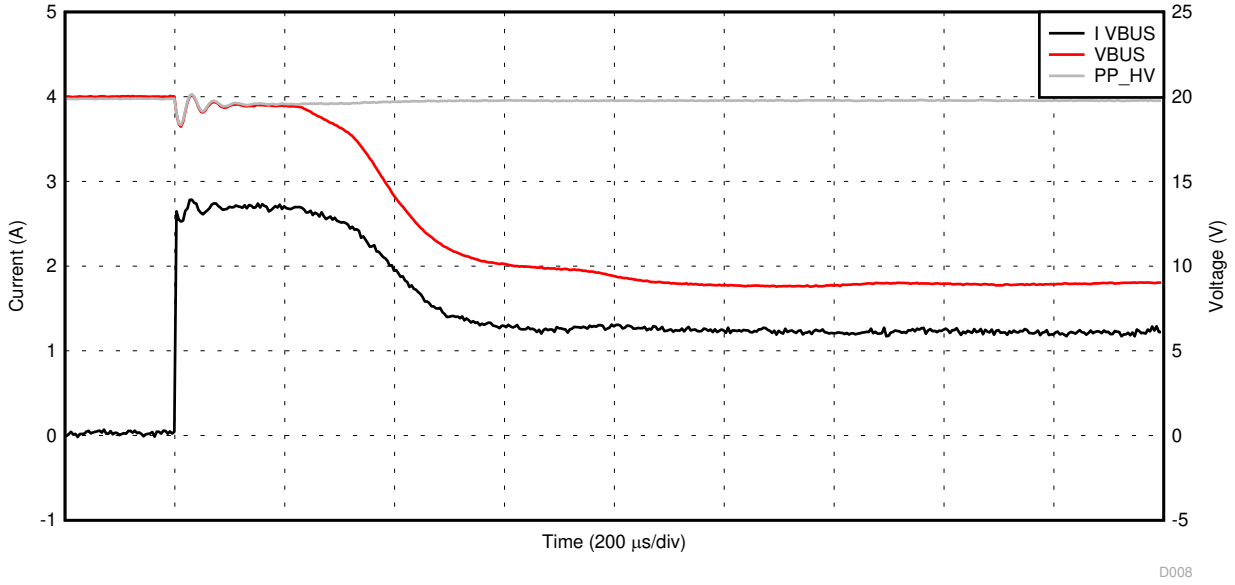


图 9-19. PP_HV Current Limit Response with a Soft Short (7 Ω)

9.3.3.10 External HV Power Delivery

The TPS65981 is capable of controlling an external high-voltage, common-drain back-to-back NMOS FET switch path to source or sink power up to the maximum limit of the USB PD specification: 20 V at 5 A of current. The TPS65981 provides external control and sense to external NMOS power switches for currents greater than 3 A. This path is bi-directional for either sourcing current to VBUS or sinking current from VBUS. The external NMOS switches are back-to-back to protect the system from large voltage differential across the FETs as well as blocking reverse current flow. Each NFET has a separate gate control. HV_GATE2 is always connected to the VBUS side and HV_GATE1 is always connected to the opposite side, referred to as PP_EXT. Two sense pins, SENSEP and SENSEN, are used to implement reverse current blocking, over-current protection, and current sensing. The external path may be used in conjunction with the internal path. For example, the internal path may be used to source current from PP_HV to VBUS when the TPS65981 is acting as a power source and the external path may be used to sink current from VBUS to PP_EXT to charge a battery when the TPS65981 is acting as a sink. The internal and external paths must never be used in parallel to source current at the same

time or sink current at the same time. The current limiting function will not function properly in this case and may become unstable.

9.3.3.11 External HV Power Switch as a Source with RSENSE

图 9-11 shows the configuration when the TPS65981 is acting as a source for the external switch path. The external FETs must be connected in a common-drain configuration and will not work in a common source configuration. In this mode, current is sourced to VBUS. RSENSE provides an accurate current measurement and is used to initiate the current limiting feature of the external power path. The voltage between SENSEP (PP_EXT) and SENSEN (VBUS) is sensed to block reverse current flow. This measurement is also digitally readable via the ADC.

9.3.3.12 External HV Power Switch as a Sink With RSENSE

图 9-20 shows the configuration when the TPS65981 is acting as a sink for the external switch path with RSENSE used to sense current. Acting as a sink, the voltage between SENSEP (VBUS) and SENSEN (PP_EXT) is sensed to provide an accurate current measurement and initiate the current limiting feature of the external power path. This measurement is also digitally readable via the ADC.

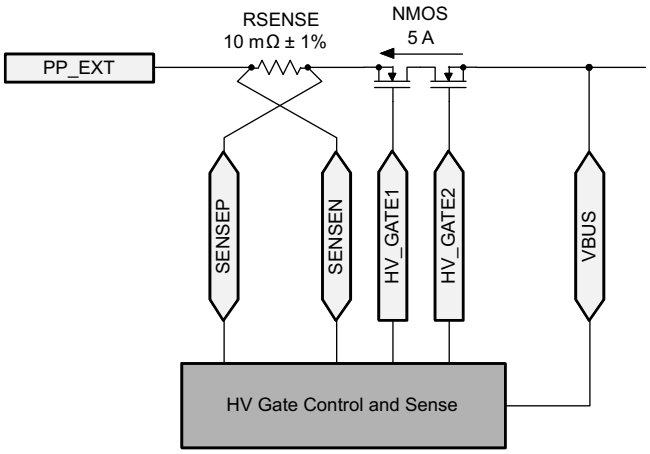


图 9-20. External HV Switch as a Sink With RSENSE

9.3.3.13 External HV Power Switch as a Sink Without RSENSE

图 9-21 shows the configuration when the TPS65981 is acting as a sink for the external switch path without an RSENSE resistor. In this mode, current is sunk from VBUS to an internal system power node, referred to as PP_EXT. This is used for charging a battery or for providing a supply voltage for a bus-powered device. To block reverse current, the VBUS and SENSEP pins monitor the voltage across the NFETs. To ensure that SENSEN does not float, tie SENSEP to SENSEN in this configuration. When configured in this mode, the digital readout from current from the ADC will be approximately zero.

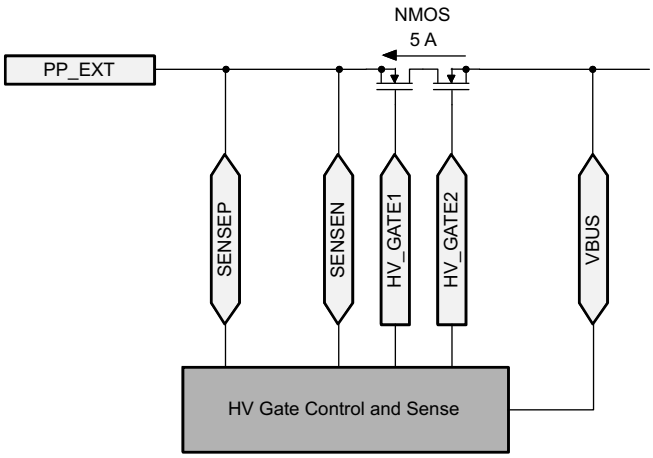


图 9-21. External HV Switch as a Sink Without RSENSE

9.3.3.14 External Current Sense

The current through the external NFETs to VBUS is sensed through the RSENSE resistor and is available to be read digitally through the ADC. When acting as a source, the readout from the ADC will only accurately reflect the current through the external NFETs when the connection of SENSEP and SENSEN adheres to 图 9-11. When acting as a sink, the readout from the ADC will only accurately reflect the current through the external NFETs when the connection of SENSEP and SENSEN adheres to 图 9-20.

9.3.3.15 External Current Limit

The current through the external NFETs to VBUS is current limited when acting as a source or a sink. The current is sensed across the external RSENSE resistance. The current limit is set by a combination of the RSENSE magnitude and configuration settings for the voltage across the resistance. When the voltage across the RSENSE resistance exceeds the automatically set voltage limit, the current-limit circuit is activated.

9.3.3.16 Soft Start

When configured as a sink, the SS pin provides a soft start function for each of the high-voltage power path supplies (P_HV and external PP_EXT path) up to 5.5 V. The SS circuitry is shared for each path and only one path will turn on as a sink at a time. The soft start is enabled by application code or via the host processor. The SS pin is initially discharged through a resistance RSS_DIS. When the switch is turned on, a current ISS is sourced from the pin to a capacitance CSS. This current into the capacitance generates a slow ramping voltage. This voltage is sensed and the power path FETs turn on and the voltage follows this ramp. When the voltage reaches the threshold VTHSS, the power path FET will be near being fully turned on, the output voltage will be fully charged. At time TSSDONE, a signal to the digital core indicates that the soft start function has completed. The ramp rate of the supply is given by 方程式 4:

$$\text{Ramp Rate} = 9 \times \frac{\text{ISS}}{\text{CSS}} \tag{4}$$

The maximum ramp voltage for the supply is approximately 16.2 V. For any input voltage higher than this, the ramp will stop at 16.2 V until the firmware disables the soft start. At this point, the voltage will step to the input voltage at a ramp rate defined by approximately 7 μA into the gate capacitance of the switch. The TSSDONE time is independent of the actual final ramp voltage.

9.3.3.17 BUSPOWERZ

At power-up, when VIN_3V3 is not present and a dead-battery condition is supported as described in *Dead-Battery or No-Battery Support*, the TPS65981 will appear as a USB Type-C sink (device) causing a connected USB Type-C source (host) to provide 5 V on VBUS. The TPS65981 receives power from the 5-V VBUS rail (see *Power MAnagement*) and execute boot code (see *Boot Code*). The boot code will observe the BUSPOWERZ voltage, which will fall into one of three voltage ranges: VBPZ_DIS, VBPZ_HV, and VBPZ_EXT (defined in

BUSPOWERZ Configuration Requirements). These three voltage ranges configure how the TPS65981 routes the 5 V present on VBUS to the system in a dead-battery or no-battery scenario.

When the voltage on BUSPOWERZ is in the VBPZ_DIS range (when BUSPOWERZ is tied to LDO_3V3 as in 图 9-22), this indicates that the TPS65981 will not route the 5 V present on VBUS to the entire system. In this case, the TPS65981 will load SPI-connected flash memory and execute this application code. This configuration will disable both the PP_HV and PP_EXT high voltage switches and only use VBUS to power the TPS65981.

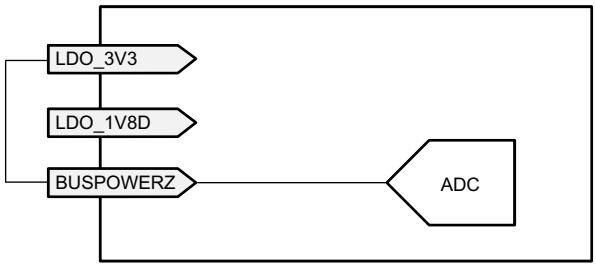


图 9-22. BUSPOWERZ Configured to Disable Power from VBUS

The BUSPOWERZ pin can alternately configure the TPS65981 to power the entire system through the PP_HV internal load switch when the voltage on BUSPOWERZ is in the VBPZ_HV range (when BUSPOWERZ is tied to LDO_1V8D as in 图 9-23).

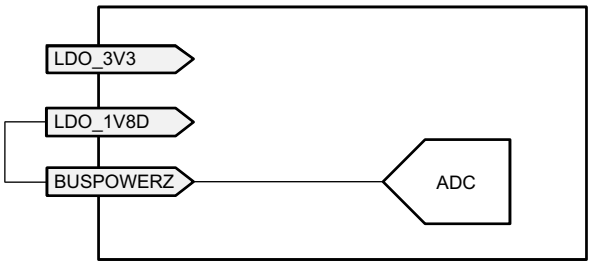


图 9-23. BUSPOWERZ Configured With PP_HV as Input Power Path

The BUSPOWERZ pin can also alternately configure the TPS65981 to power the entire system through the PP_EXT external load switch when the voltage on BUSPOWERZ is in the VBPZ_EXT range (when BUSPOWERZ is tied to GND as in 图 9-24).

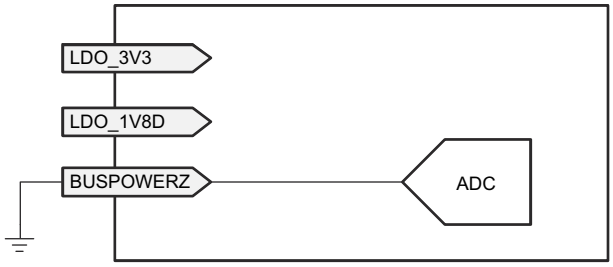


图 9-24. BUSPOWERZ Configured With PP_EXT as Input Power Path

9.3.3.18 Voltage Transitions on VBUS through Port Power Switches

图 9-25 shows the waveform for a positive voltage transition. The timing and voltages apply to both a transition from 0 V to PP_5V0 and a transition from PP_5V0 to PP_HV as well as a transition from PP_5V0 to an PP_EXT. A transition from PP_HV to PP_EXT is possible and vice versa, but does not necessarily follow the constraints in 图 9-25. When a switch is closed to transition the voltage, a maximum slew-rate of SRPOS occurs on the transition. The voltage ramp will remain monotonic until the voltage reaches VSRCVALID within the final voltage. The voltage may overshoot the new voltage by VSRCVALID. After time TSTABLE from the start of the transition,

the voltage will fall to within VSRCNEW of the new voltage. During the time TSTABLE, the voltage may fall below the new voltage, but will remain within VSRCNEW of this voltage.

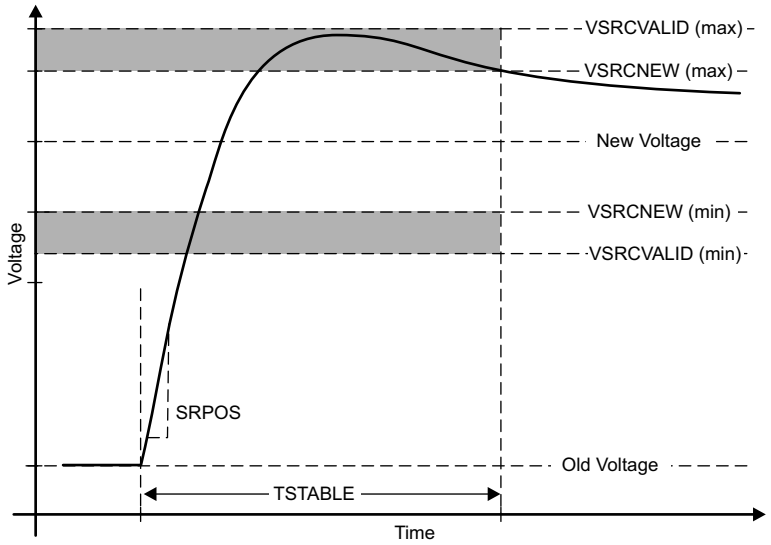


图 9-25. Positive Voltage Transition on VBUS

图 9-26 shows the waveform for a negative voltage transition. The timing and voltages apply to both a transition from PP_HV to PP_5V0 and a transition from PP_5V0 to 0V as well as a transition from PP_EXT to PP_5V0. A transition from PP_HV to PP_EXT is possible and vice versa, but does not necessarily follow the constraints in 图 9-26. When a switch is closed to transition the voltage, a maximum slew-rate of SRNEG occurs on the transition. The voltage ramp will remain monotonic until the voltage reaches TOLTRANUN within the final voltage. The voltage may overshoot the new voltage by TOLTRANLN. After time TSTABLE from the start of the transition, the voltage will fall to within VSRCNEW of the new voltage. During the time TSTABLE, the voltage may fall below the new voltage, but will remain within VSRCNEW of this voltage.

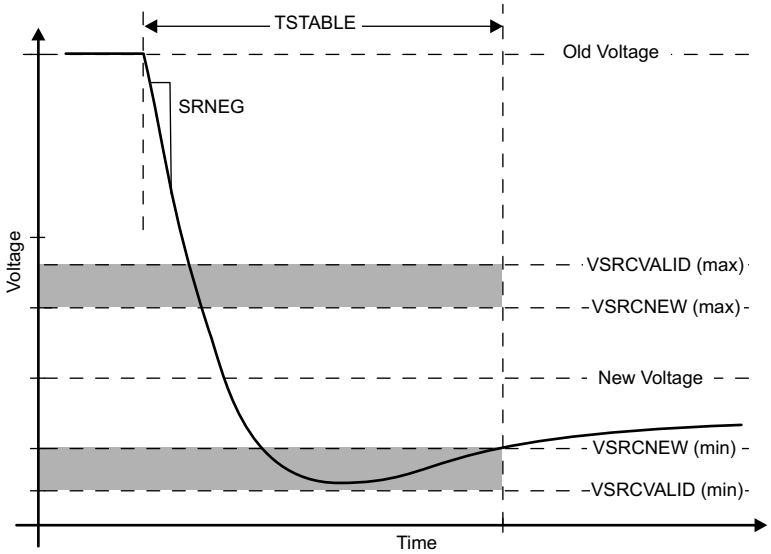


图 9-26. Negative Voltage Transition on VBUS

9.3.3.19 HV Transition to PP_RV0 Pull-down on VBUS

The TPS65981 has an integrated active pull-down on VBUS when transitioning from PP_HV to PP_5V0, shown in 图 9-27. When the PP_HV switch is disabled and VBUS > PP_5V0 + VHVDISPD, amplifier turns on a current source and pulls down on VBUS. The amplifier implements active slew rate control by adjusting the pull-down

current to prevent the slew rate from exceeding specification. When VBUS falls to within VHVDISPD of PP_5V0, the pull-down is turned off. The load on VBUS will then continue to pull VBUS down until the ideal diode switch structure turns on connecting it to PP_5V0. When switching from PP_HV or PP_EXT to PP_5V0, PP_HV or PP_EXT must be above VSO_HV to follow the switch-over shown in 图 9-26.

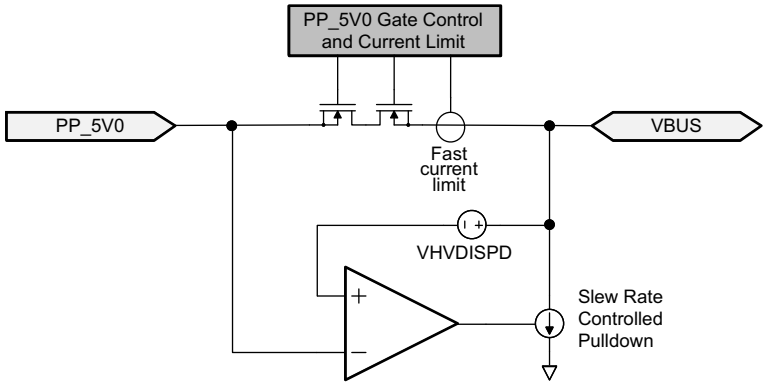


图 9-27. PP_5V0 Slew-Rate Control

9.3.3.20 VBUS Transition to VSAFE0V

When VBUS transitions to near 0 V (VSAFE0V), the pull-down circuit in 图 9-27 is turned on until VBUS reaches VSAFE0V. This transition will occur within time TSAFE0V.

9.3.3.21 C_CC1 and C_CC2 Power Configuration and Power Delivery

The C_CC1 and C_CC2 pins are used to deliver power to active circuitry inside a connected cable and output USB-PD data to the cable and connected device. 图 9-11 shows the C_CC1, and C_CC2 outputs to the port. Only one of these pins will be used to deliver power at a time depending on the cable orientation. The other pin will be used to transmit USB-PD data through the cable to a connected device.

图 9-28 shows a high-level flow of connecting these pins based on the cable orientation. See the *节 9.3.2* section for more detailed information on plug and orientation detection.

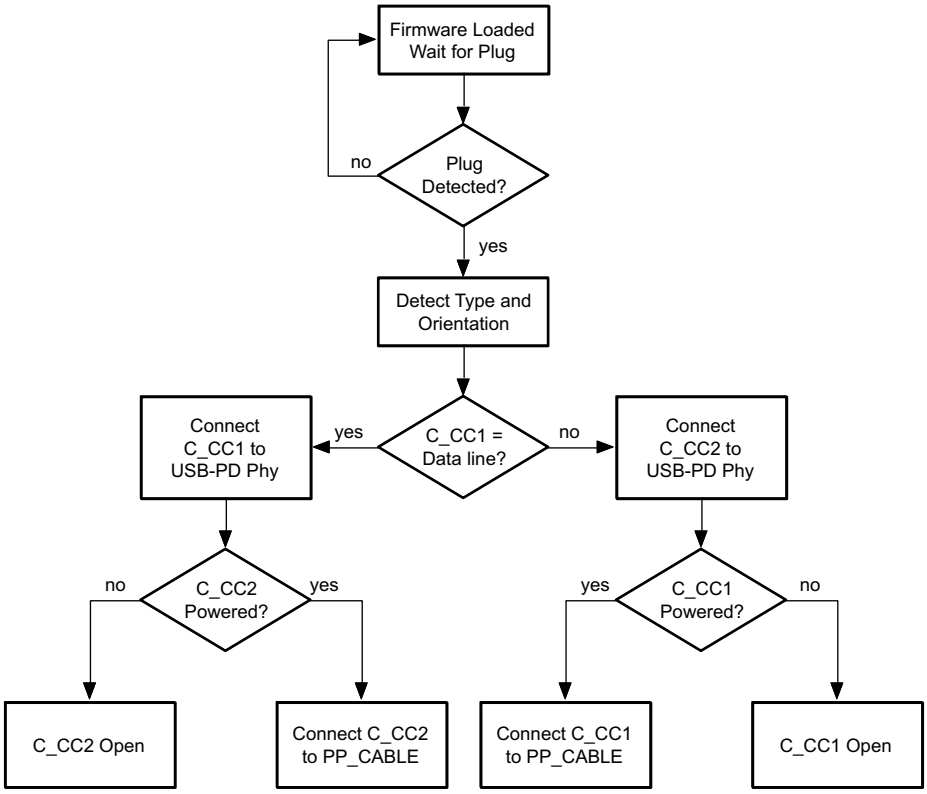


图 9-28. Port C_CC and VCONN Connection Flow

图 9-29 and 图 9-30 show the two paths from PP_CABLE to the C_CCn pins. When one C_CCn pin is powered from PP_CABLE, the other is connected to the USB-PD BMC modem. The red line shows the power path and the green line shows the data path.

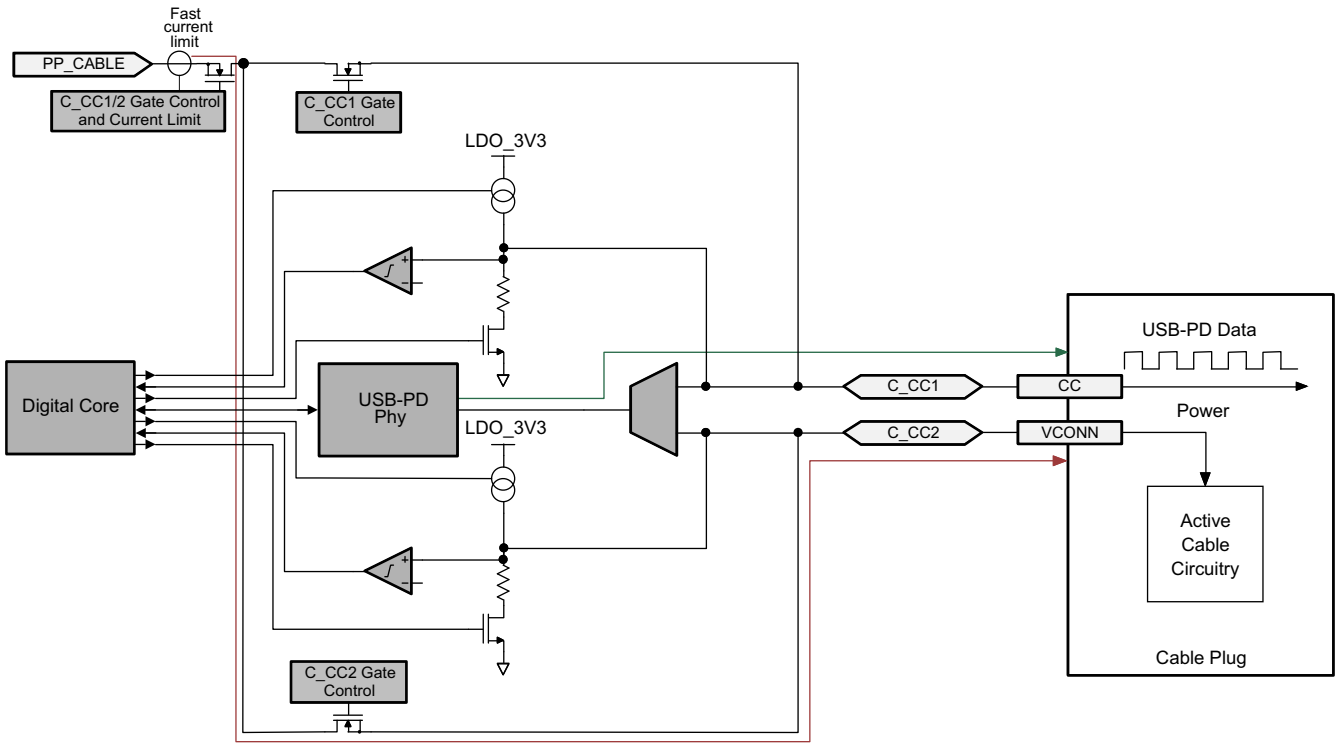


图 9-29. Port C_CC1 and C_CC2 Normal Orientation Power from PP_CABLE

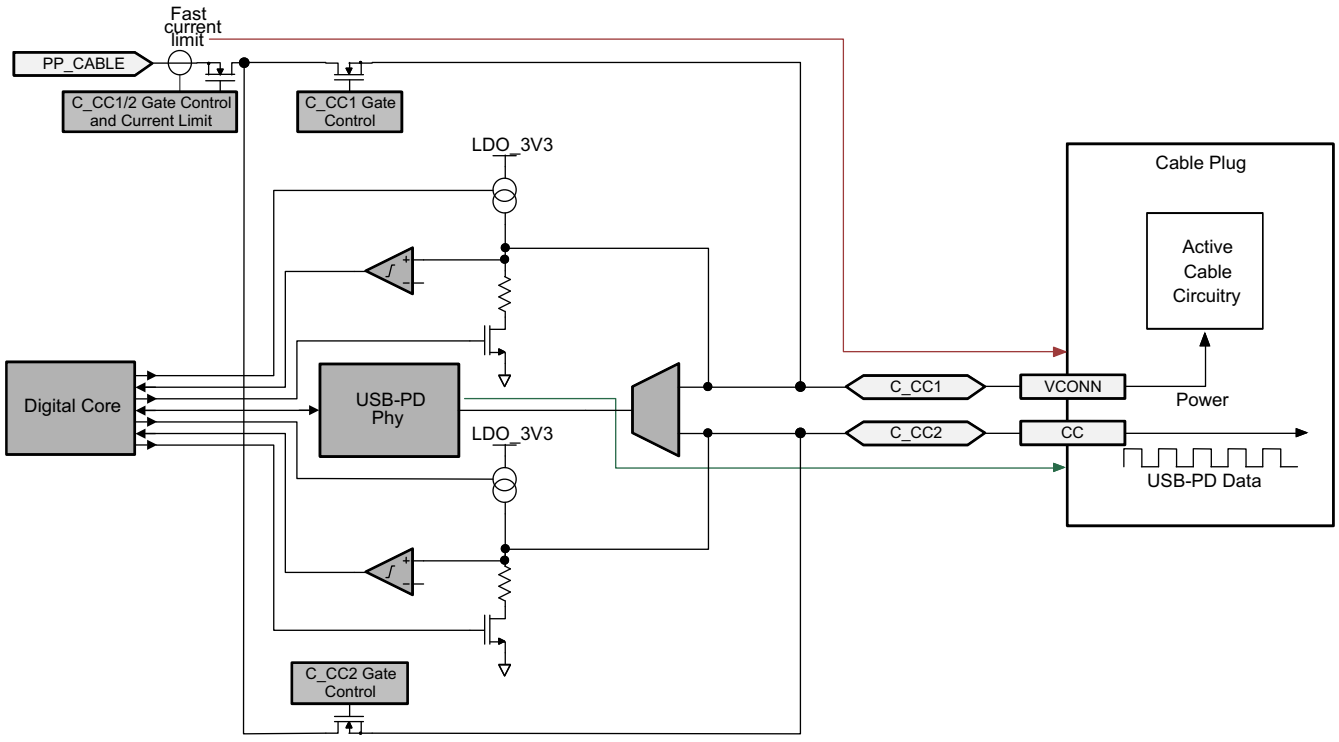


图 9-30. Port C_CC1 and C_CC2 Reverse Orientation Power from PP_CABLE

9.3.3.22 PP_CABLE to C_CC1 and C_CC2 Switch Architecture

图 9-11 shows the switch architecture for the PP_CABLE switch path to the C_CCc pins. Each path provides a unidirectional current from PP_CABLE to C_CC1 and C_CC2. The switch structure blocks reverse current from C_CC1 or C_CC2 to PP_CABLE.

9.3.3.23 PP_CABLE to C_CC1 and C_CC2 Current Limit

The PP_CABLE to C_CC1 and C_CC2 share current limiting through a single FET on the PP_CABLE side of the switch. The current limit ILIMPPCC is adjustable between two levels. When the current exceeds ILIMPPCC, the current-limit circuit activates. Depending on the severity of the over-current condition, the transient response will react in one of two ways: 图 9-31 and 图 9-32 show the approximate response time and clamping characteristics of the circuit for a hard short while 图 9-33 shows the approximate response time and clamping characteristics for a soft short. The switch does not have reverse current blocking when the switch is enabled and current is flowing to either C_CC1 or C_CC2.

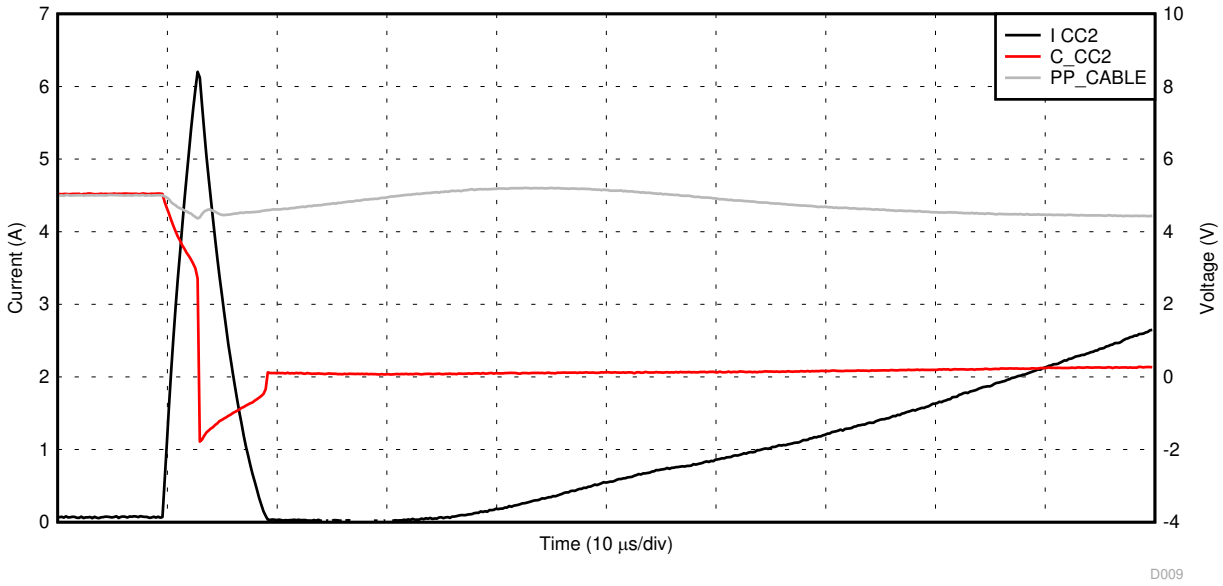


图 9-31. PP_CABLE to C_CCn Current Limit With a Hard Short

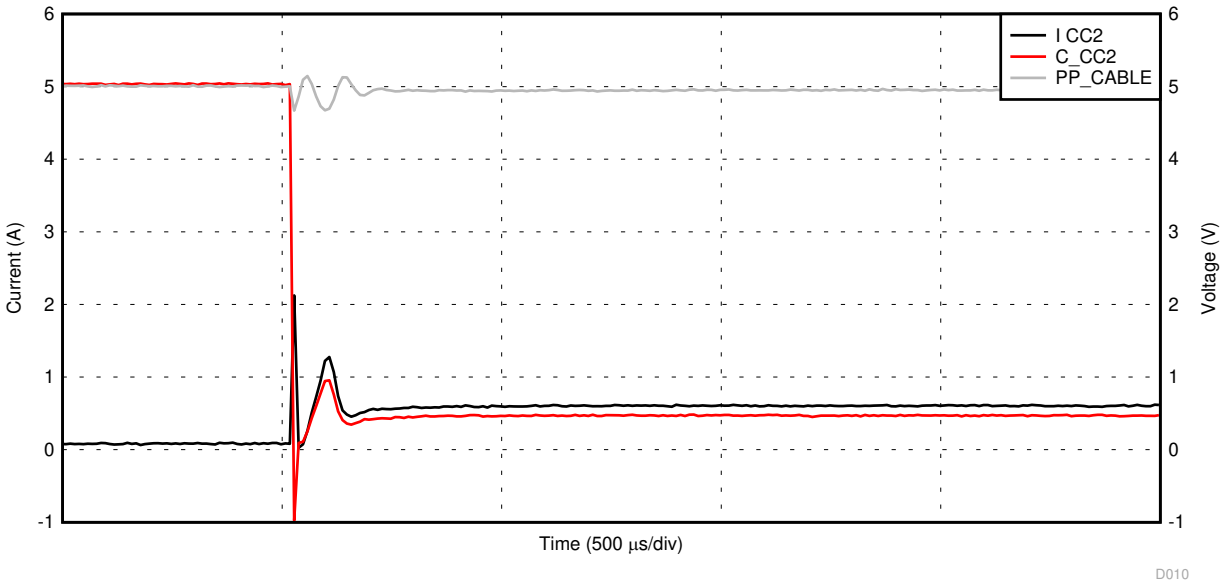


图 9-32. PP_CABLE to C_CCn Current Limit With a Hard Short (Extended Time Base)

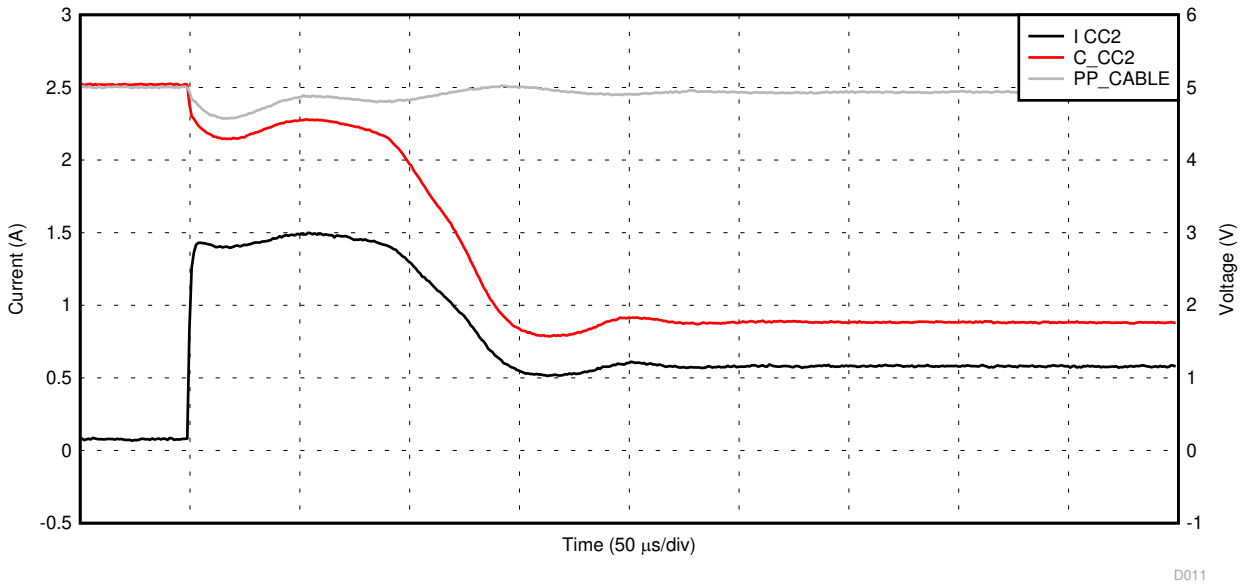


图 9-33. PP_CABLE to C_CCn Current Limit Response With a Soft Short (2 Ω)

9.3.4 USB Type-C® Port Data Multiplexer

The USB Type-C receptacle pin configuration is show in 图 9-34. Not all signals shown are required for all platforms or devices. The basic functionality of the pins deliver USB 2.0 (D+ and D –) and USB 3.1 (TX and RX pairs) data buses, USB power (VBUS) and ground (GND). Configuration Channel signals (CC1 and CC2), and two Reserved for Future Use (SBU) signal pins. The data bus pins (Top and Bottom D+/D – and the SBU pins) are available to be used in non-USB applications as an Alternate Mode (for example, DisplayPort).

图 9-34. USB Type-C® Receptacle Pin Configuration

A1	A2	A3	A4	A5	A6	A7	A8	A9	A11	A11	A12
GND	TX1+	TX1 –	VBUS	CC1	D+	D –	SBU1	VBUS	RX2 –	RX2+	GND
GND	RX1+	RX1 –	VBUS	SBU2	D –	D+	CC2	VBUS	TX2 –	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

The TPS65981 USB Type-C interface multiplexers are shown in 表 9-2. The outputs are determined based on detected cable orientation as well as the identified interface that is connected to the port. There are two USB output ports that may or may not be passing USB data. When an Alternate Mode is connected, these same ports may also pass that data (for example, DisplayPort). Note, the TPS65981 pin to receptacle mapping is shown in 表 9-2. The high-speed RX and TX pairs are not mapped through the TPS65981 as this would place extra resistance and stubs on the high-speed lines and degrade signal performance.

表 9-2. TPS65981 to USB Type-C® Receptacle Mapping

DEVICE PIN	Type-C RECEPTACLE PIN
VBUS	VBUS (A4, A9, B4, B9)
C_CC1	CC1 (A5)
C_CC2	CC2 (B5)
C_USB_TP	D+ (A6)
C_USB_TN	D – (A7)
C_USB_BP	D+ (B6)
C_USB_BN	D – (B7)
C_SBU1	SBU1 (A8)

表 9-2. TPS65981 to USB Type-C® Receptacle Mapping (continued)

DEVICE PIN	Type-C RECEPTACLE PIN
C_SBU2	SBU2 (B8)

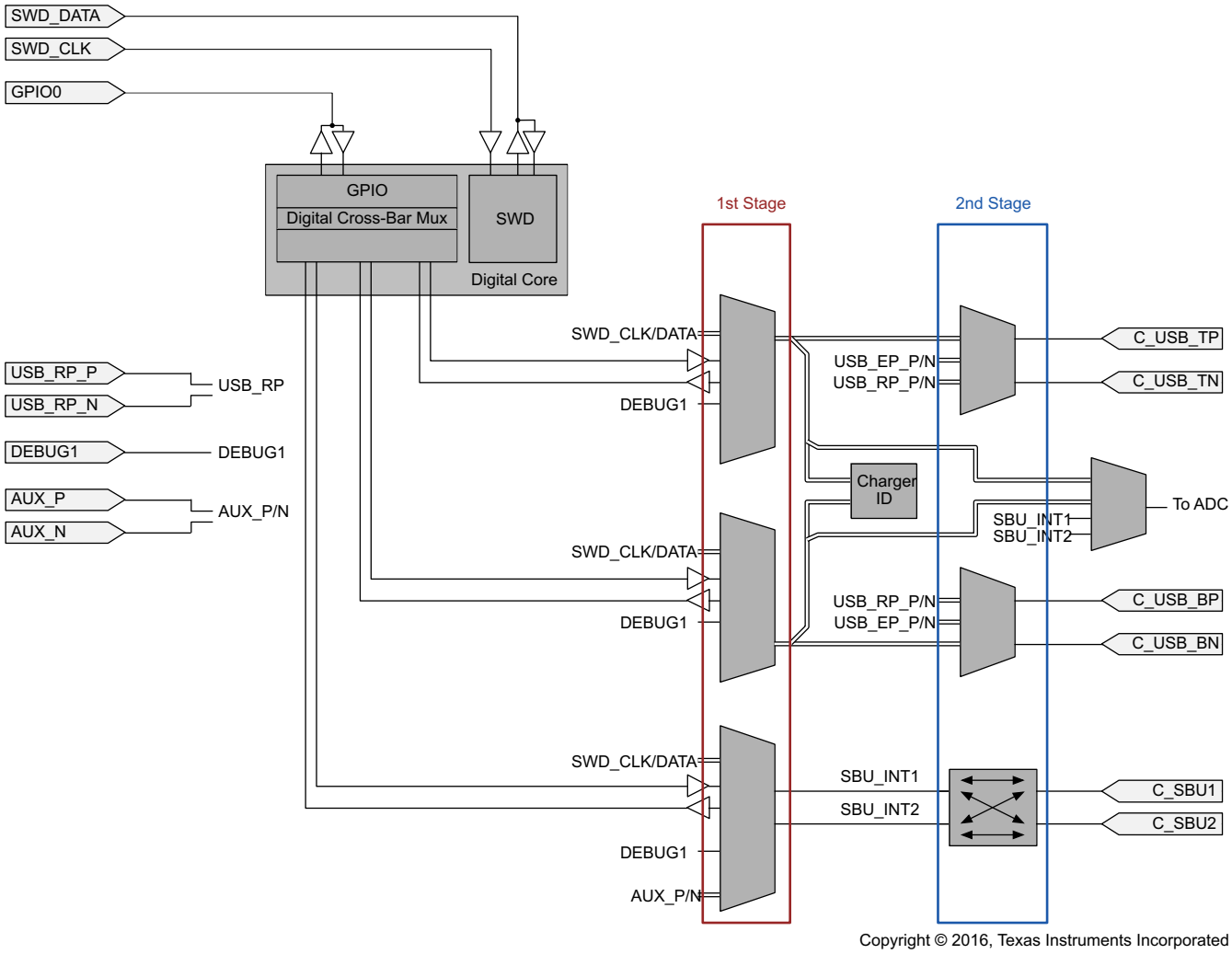


图 9-35. Port Data Multiplexers

表 9-3 shows the typical signal types through the switch path. All switches are analog pass switches. These switch paths are not limited to the specified signal type. For the signals that interface with the digital core, the maximum data rate is dictated by the clock rate at which the core is running.

表 9-3. Typical Signals through Analog Switch Path

INPUT PATH	SIGNAL TYPE	SIGNAL FUNCTION
SWD_DATA/CLK	Single Ended	Data, Clock
DEBUG1	Single Ended	Debug
AUX_P/N	Differential	DisplayPort AUX channel
USB_EP_P/N	Differential	USB 2.0 Low Speed Endpoint
USB_RP_P/N	Differential	USB 2.0 High Speed Data Root Port

9.3.4.1 USB Top and Bottom Ports

The Top (C_USB_TP and C_USB_TN) and Bottom (C_USB_BP and C_USB_BN) ports that correspond to the Type-C top and bottom USB D+/D– pairs are swapped based on the detected cable orientation. The symmetric

pin order shown in 图 9-34 from the A-side to the B-side allows the pins to connect to equivalent pins on the opposite side when the cable orientation is reversed.

9.3.4.2 Multiplexer Connection Orientation

表 9-4 shows the multiplexer connection orientation. For the USB D+/D – pair top and bottom port connections, these connections are fixed. For the SBU port connections, the SBU crossbar multiplexer enables flipping of the signal pair and the connections shown are for the upside-up orientation.

表 9-4. Data Multiplexer Connections

SYSTEM PIN	USB TOP PIN	USB BOTTOM PIN	SBU MULTIPLEXER PIN
USB_RP_P	C_USB_TP	C_USB_BP	
USB_RP_N	C_USB_TN	C_USB_BN	
USB_EP_P	C_USB_TP	C_USB_BP	
USB_EP_N	C_USB_TN	C_USB_BN	
SWD_CLK	C_USB_TP	C_USB_BP	SBU1
SWD_DATA	C_USB_TN	C_USB_BN	SBU2
DEBUG1	C_USB_TP	C_USB_BP	SBU1
AUX_P	C_USB_TP	C_USB_BP	SBU1
AUX_N	C_USB_TN	C_USB_BN	SBU2

9.3.4.3 SBU Crossbar Multiplexer

The SBU Crossbar Multiplexer provides pins (C_SBU1 and C_SBU2) for future USB functionality as well as Alternate Modes. The multiplexer swaps the output pair orientation based on the cable orientation. For more information on Alternate Modes, refer to the USB PD Specification.

9.3.4.4 Signal Monitoring and Pull-up and Pull-down

The TPS65981 has comparators that may be enabled to interrupt the core when a switching event occurs on any of the port inputs. The input parameters for the detection are shown in *Port Data Multiplexer Signal Monitoring Pullup and Pulldown Characteristics*. These comparators are disconnected by application code when these pins are not digital signals but an analog voltage.

The TPS65981 has pull-ups and pull-downs between the first and second stage multiplexers of the port switch for each port output: C_SBU1/2, C_USB_TP/N, C_USB_BP/N. The configurable pull-up and pull-down resistances between each multiplexer are shown in 图 9-36.

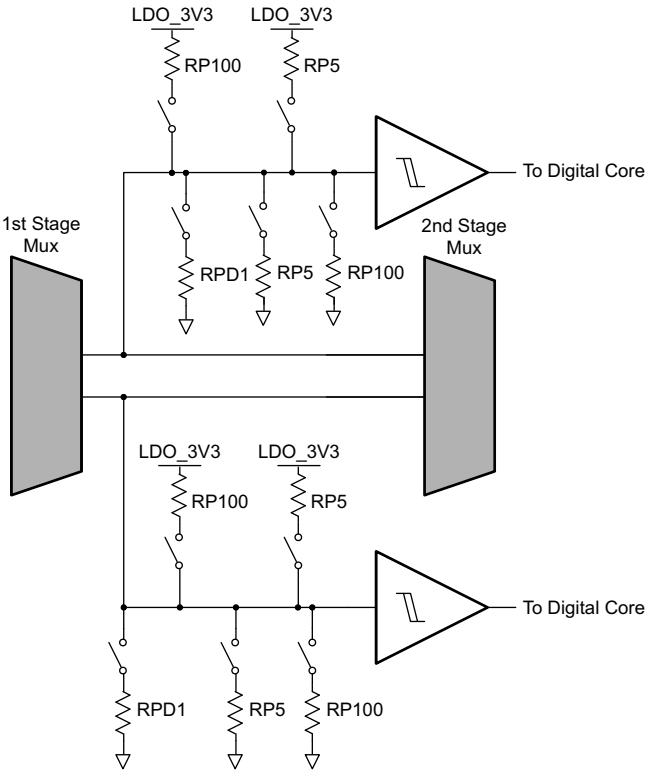


图 9-36. Port Detect and Pull-up and Pull-down

9.3.4.5 Port Multiplexer Clamp

Each input to the 2nd stage multiplexer is clamped to prevent voltages on the port from exceeding the safe operating voltage of circuits attached to the System-side of the Port Data Multiplexer. 图 9-37 shows the simplified clamping circuit. When a path through the 2nd stage multiplexer is closed, the clamp is connected to the one of the port pins (C_USB_TP/N, C_USB_BP/N, C_SBU1/2). When a path through the 2nd stage multiplexer is not closed, then the port pin is not clamped. As the pin voltage rises above the VCLMP_IND voltage, the clamping circuit activates, and sinks current to ground, preventing the voltage from rising further.

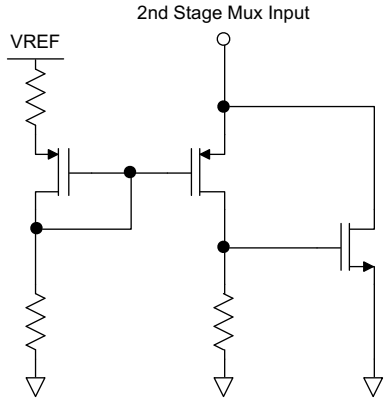


图 9-37. Port Multiplexer Clamp

9.3.4.6 USB2.0 Low-Speed Endpoint

The USB low-speed Endpoint is a USB 2.0 low-speed (1.5 Mbps) interface used to support HID class based accesses. The TPS65981 supports control of endpoint EP0. This endpoint enumerates to a USB 2.0 bus to provide USB-Billboard information to a host system as defined in the USB Type-C standard. EP0 is used for advertising the Billboard Class. When a host is connected to a device that provides Alternate Modes which

cannot be supported by the host, the Billboard class allows a means for the host to report back to the user without any silent failures.

图 9-38 shows the USB Endpoint physical layer. The physical layer consists of the analog transceiver, the Serial Interface Engine, and the Endpoint FIFOs and supports low speed operation.

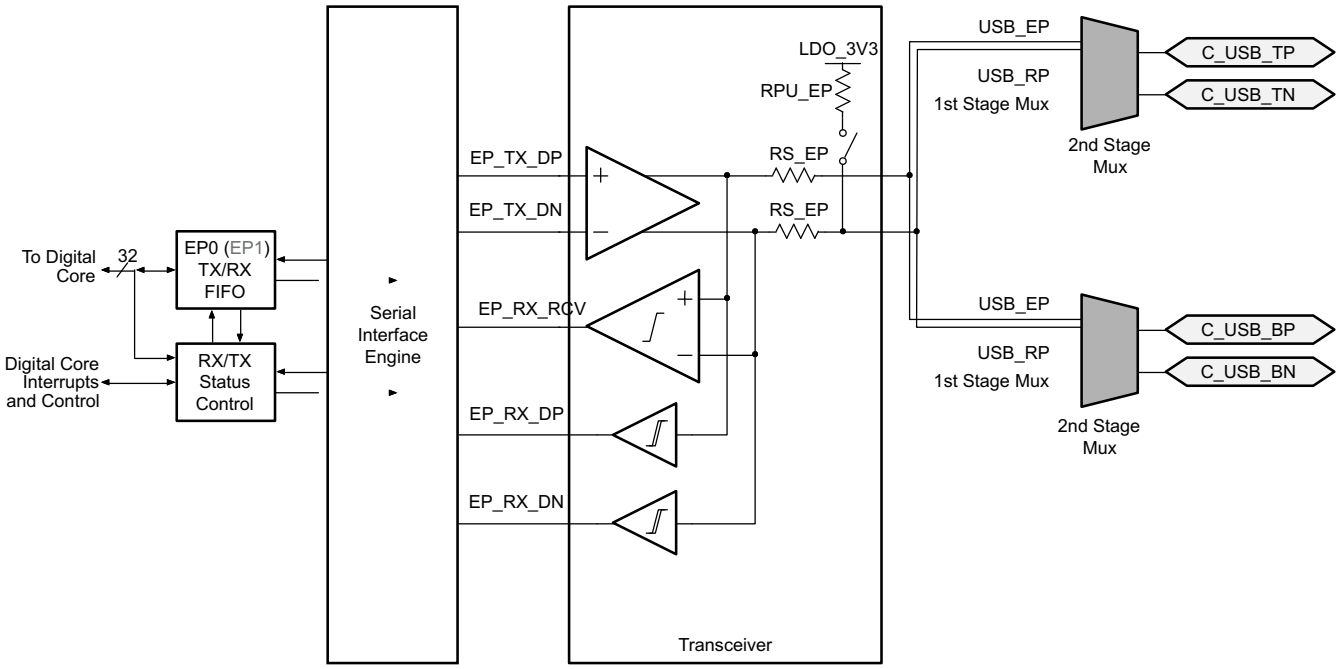


图 9-38. USB Endpoint Phy

The transceiver is made up of a fully differential output driver, a differential to single-ended receive buffer and two single-ended receive buffers on the D+/D – independently. The output driver drives the D+/D – of the selected output of the Port Multiplexer. The signals pass through the 2nd Stage Port Data Multiplexer to the port pins. When driving, the signal is driven through a source resistance RS_EP. RS_EP is shown as a single resistor in USB Endpoint Phy but this resistance also includes the resistance of the 2nd Stage Port Data Multiplexer defined in Port Data Multiplexer Requirements and Characteristics. RPU_EP is disconnected during transmit mode of the transceiver.

When the endpoint is in receive mode, the resistance RPU_EP is connected to the D – pin of the top or bottom port (C_USB_TN or C_USB_BN) depending on the detected orientation of the cable. The RPU_EP resistance advertises low speed mode only.

9.3.4.7 Battery Charger (BC1.2) Detection Block

The battery charger (BC1.2) detection block integrates circuitry to detect when the connected entity on the USB D+/D – pins is a charger. To enable the required detection mechanisms, the block integrates various voltage sources, currents, and resistances to the Port Data Multiplexers. 图 9-39 shows the connections of these elements to the Port Data Multiplexers.

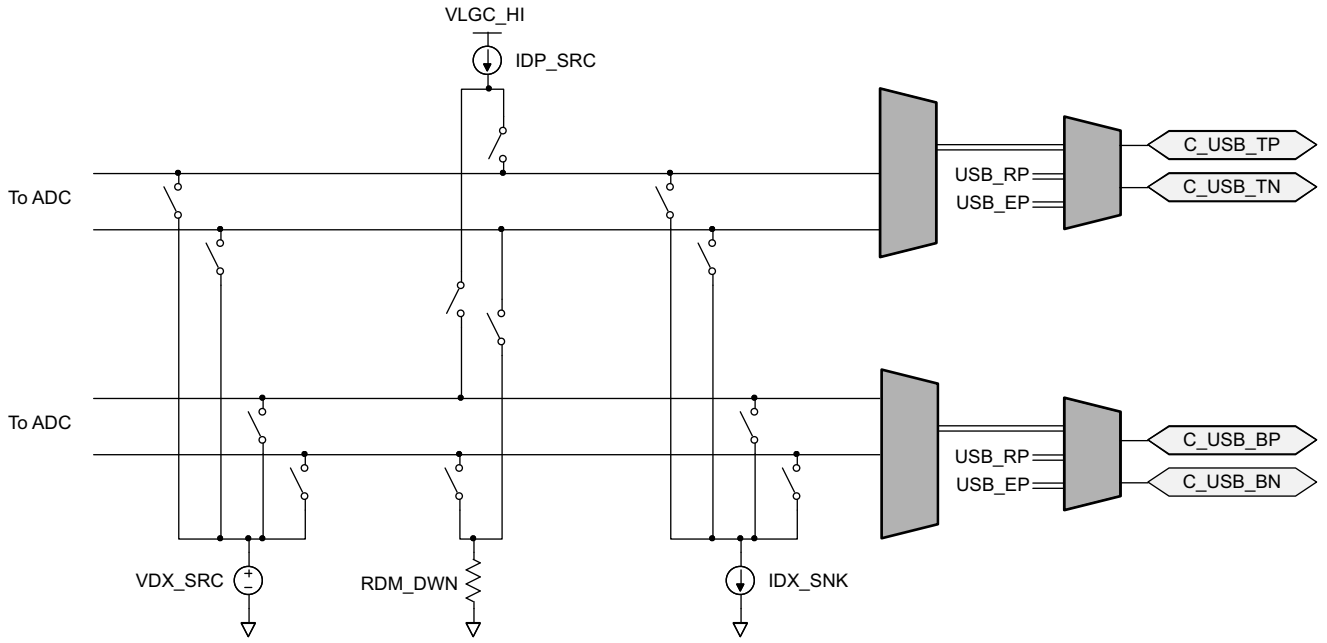


图 9-39. BC1.2 Detection Circuitry

9.3.4.8 BC1.2 Data Contact Detect

Data Contact Detect follows the definition in the USB BC1.2 specification. The detection scheme sources a current IDP_SRC into the D+ pin of the USB connection. The current is sourced into either the C_USB_TP (top) or C_USB_BP (bottom) D+ pin based on the determined cable/device orientation. A resistance RDM_DWN is connected between the D – pin and GND. Again, this resistance is connected to either the C_USB_TN (top) or C_USB_BN (bottom) D – pin based on the determined cable/device orientation. The middle section of 图 9-39, the current source IDP_SRC and the pull-down resistance RDM_DWN, is activated during data contact detection.

9.3.4.9 BC1.2 Primary and Secondary Detection

The Primary and Secondary Detection follow the USB BC1.2 specification. This detection scheme looks for a resistance between D+ and D – lines by forcing a known voltage on the first line, forcing a current sink on the second line and then reading the voltage on the second line using the general purpose ADC integrated in the TPS65981. To provide complete flexibility, 12 independent switches are connected to allow firmware to force voltage, sink current, and read voltage on any of the C_USB_TP, C_USB_TN, C_USB_BP, and C_USB_BN. The left and right sections of 图 9-39, the voltage source VDX_SRC and the current source IDX_SNK, are activated during primary and secondary detection.

9.3.5 Power Management

The TPS65981 Power Management block receives power and generates voltages to provide power to the TPS65981 internal circuitry. These generated power rails are LDO_3V3, LDO_1V8A, and LDO_1V8D. LDO_3V3 is also a low power output to load flash memory. VRSTZ_3V3 (formerly referred to as VOUT_3V3 on the TPS65982) is an internal reference voltage that is enabled when VIN_3V3 rises above the under-voltage threshold and application code is executing, causing RESETZ to be de-asserted. 图 9-40 shows the power supply path.

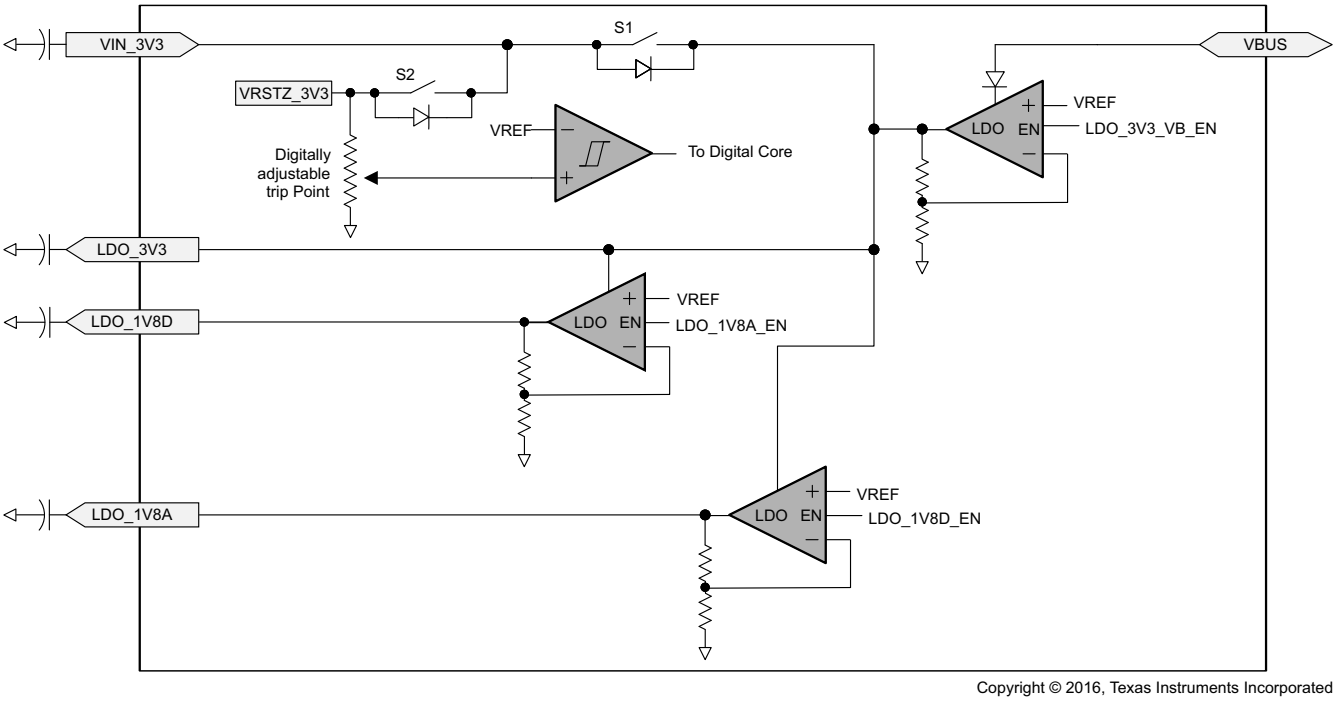


图 9-40. Power Supply Path

The TPS65981 is powered from either VIN_3V3 or VBUS. The normal power supply input is VIN_3V3. In this mode, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and the 3.3-V I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V8D and LDO_1V8A to power the 1.8-V core digital circuitry and 1.8-V analog circuits. When VIN_3V3 power is unavailable and power is available on the VBUS, the TPS65981 will be powered from VBUS. In this mode, the voltage on VBUS is stepped down through an LDO to LDO_3V3. Switch S1 in 图 9-40 is unidirectional and no current will flow from LDO_3V3 to VIN_3V3. When VIN_3V3 is unavailable, this is an indicator that there is a dead-battery or no-battery condition.

9.3.5.1 Power-On and Supervisory Functions

A power-on-reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present. In addition to the POR and supervisory circuits for the internal supplies, a separate programmable voltage supervisor monitors the VRSTZ_3V3 voltage.

9.3.5.2 Supply Switch-Over

VIN_3V3 takes precedence over VBUS, meaning that when both supply voltages are present the TPS65981 will power from VIN_3V3. Refer to The 图 9-40 for a diagram showing the power supply path block. There are two cases in with a power supply switch-over will occur. The first is when VBUS is present first and then VIN_3V3 becomes available. In this case, the supply will automatically switch-over to VIN_3V3 and brown-out prevention is verified by design. The other way a supply switch-over will occur is when both supplies are present and VIN_3V3 is removed and falls below 2.85 V. In this case, a hard reset of the TPS65981 occurs prompting a re-boot.

9.3.5.3 RESETZ and MRESET

The VIN_3V3 voltage is connected to VRSTZ_3V3 by a single FET switch (S2 in 图 9-40).

The enabling of the switch is controlled by the core digital circuitry and the conditions are programmable. A supervisor circuit monitors the voltage at VRSTZ_3V3 for an under-voltage condition and sets the external indicator RESETZ. The RESETZ pin is active low (low when an under-voltage condition occurs). The RESETZ output is also asserted when the MRESET input is asserted. The MRESET input is active-high by default, but is configurable to be active low. 图 8-1 shows the RESETZ timing with MRESET set to active high. When VRSTZ_3V3 is disabled in application code, a resistance of RPDOUT_3V3 pulls down on the pin.

9.3.6 Digital Core

图 9-41 shows a simplified block diagram of the digital core. This diagram shows the interface between the digital and analog portions of the TPS65981.

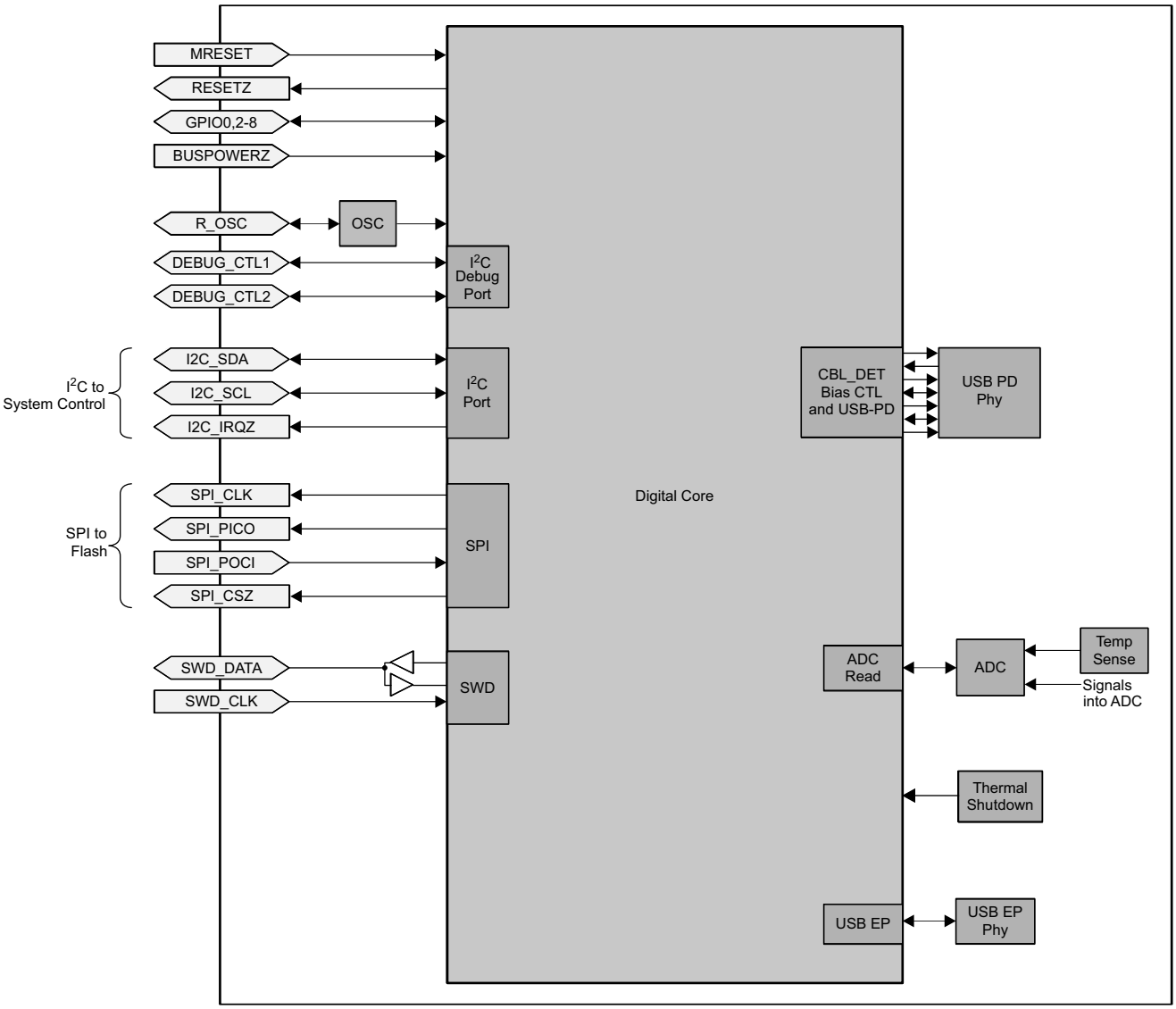


图 9-41. Digital Core Block Diagram

9.3.7 USB-PD BMC Modem Interface

The USB-PD BMC modem interface is a fully USB-PD compliant Type-C interface. The modem contains the BMC encoder and decoder, the TX/Rx FIFOs, the packet engine for construction and deconstruction of the USB-PD packet. This module contains programmable SOP values and processes all SOP headers.

9.3.8 System Glue Logic

The system glue logic module performs various system interface functions such as control of the system interface for RESETZ, MRESET, and VRSTZ_3V3. This module supports various hardware timers for digital control of analog circuits.

9.3.9 Power Reset Congrol Module (PRCM)

The PRCM implements all clock management, reset control, and sleep-mode control.

9.3.10 Interrupt Monitor

The Interrupt Control module handles all interrupt from the external GPIO as well as interrupts from internal analog circuits.

9.3.11 ADC Sense

The ADC Sense module is a digital interface to the SAR ADC. The ADC converts various voltages and currents from the analog circuits. The ADC converts up to 11 channels from analog levels to digital signals. The ADC can be programmed to convert a single sampled value.

9.3.12 I²C Slave

One I²C interface provides interface to the digital core from the system. This interface is an I²C slave and supports low-speed and full-speed signaling. See the *I²C Slave Interface* section for more information.

9.3.13 SPI Controller

The SPI controller provides a serial interface to an external flash memory. The recommended memory is the W25Q80DV 8-Mbit serial-flash memory. A memory of at least 2 Mbit is required. See the *SPI Controller Interface* section for more information.

9.3.14 Single-Wire Debugger Interface

The SWD interface provides a mechanism to directly master the digital core.

9.3.15 DisplayPort HPD Timers

To enable DisplayPort HPD signaling through PD messaging, two GPIO pins (GPIO4, GPIO5) are used as the HPD input and output. When events occur on this pins during a DisplayPort connection through the Type-C connector (configured in firmware), hardware timers trigger and interrupt the digital core to indicated needed PD messaging. 表 9-5 shows each I/O function when GPIO4/5 are configured in HPD mode. When HPD is not enabled via firmware, both GPIO4 and GPIO5 remain generic GPIO and may be programmed for other functions. 图 9-42 and 图 9-43.

表 9-5. HPD GPIO Configuration

HPD (Binary) Configuration	GPIO4	GPIO5
00	HPD TX	Generic GPIO
01	HPD RX	Generic GPIO
10	HPD TX	HPD RX
11	HPD TX/RX (bidirectional)	Generic GPIO

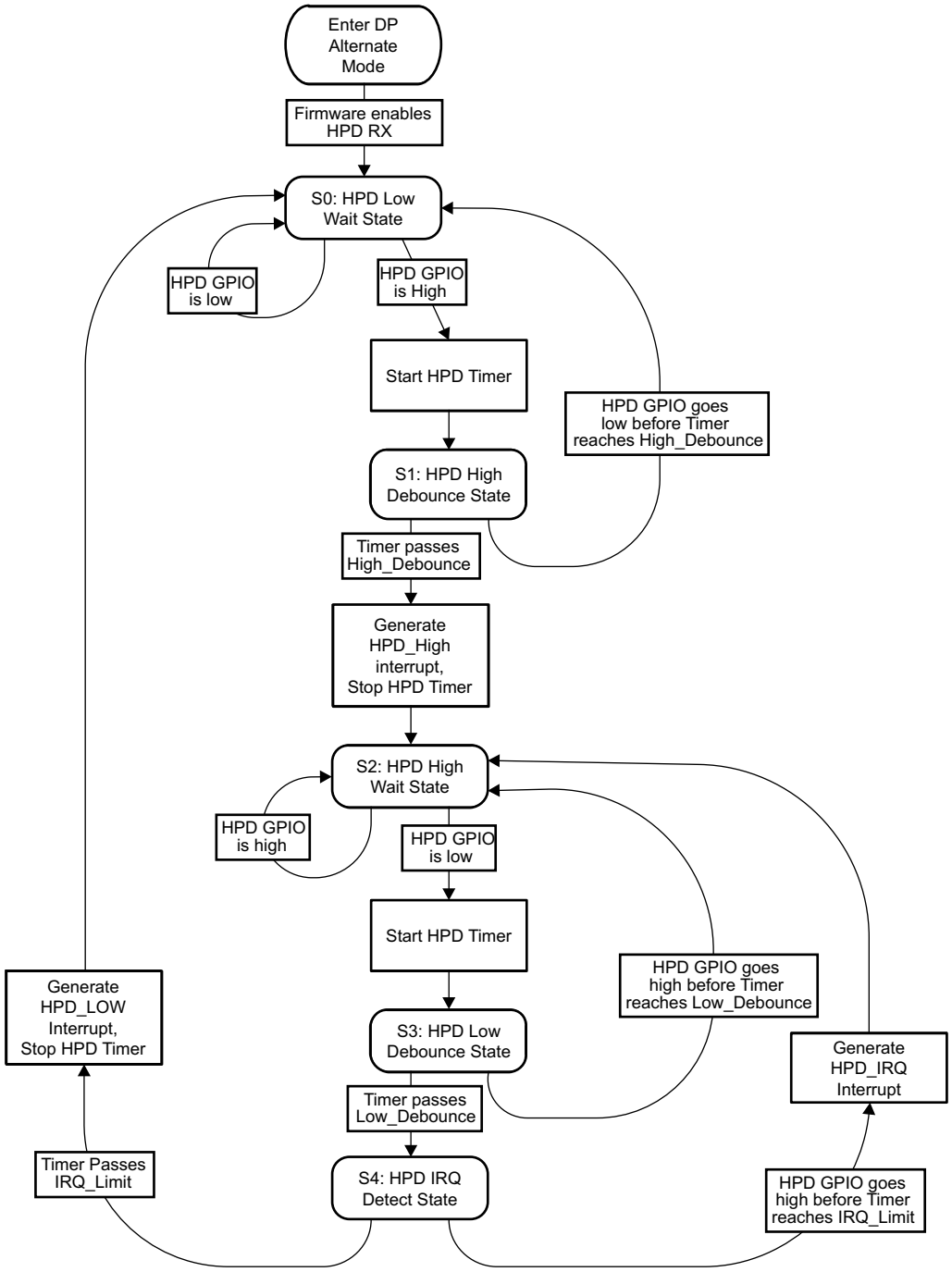


图 9-42. HPD RX Flow

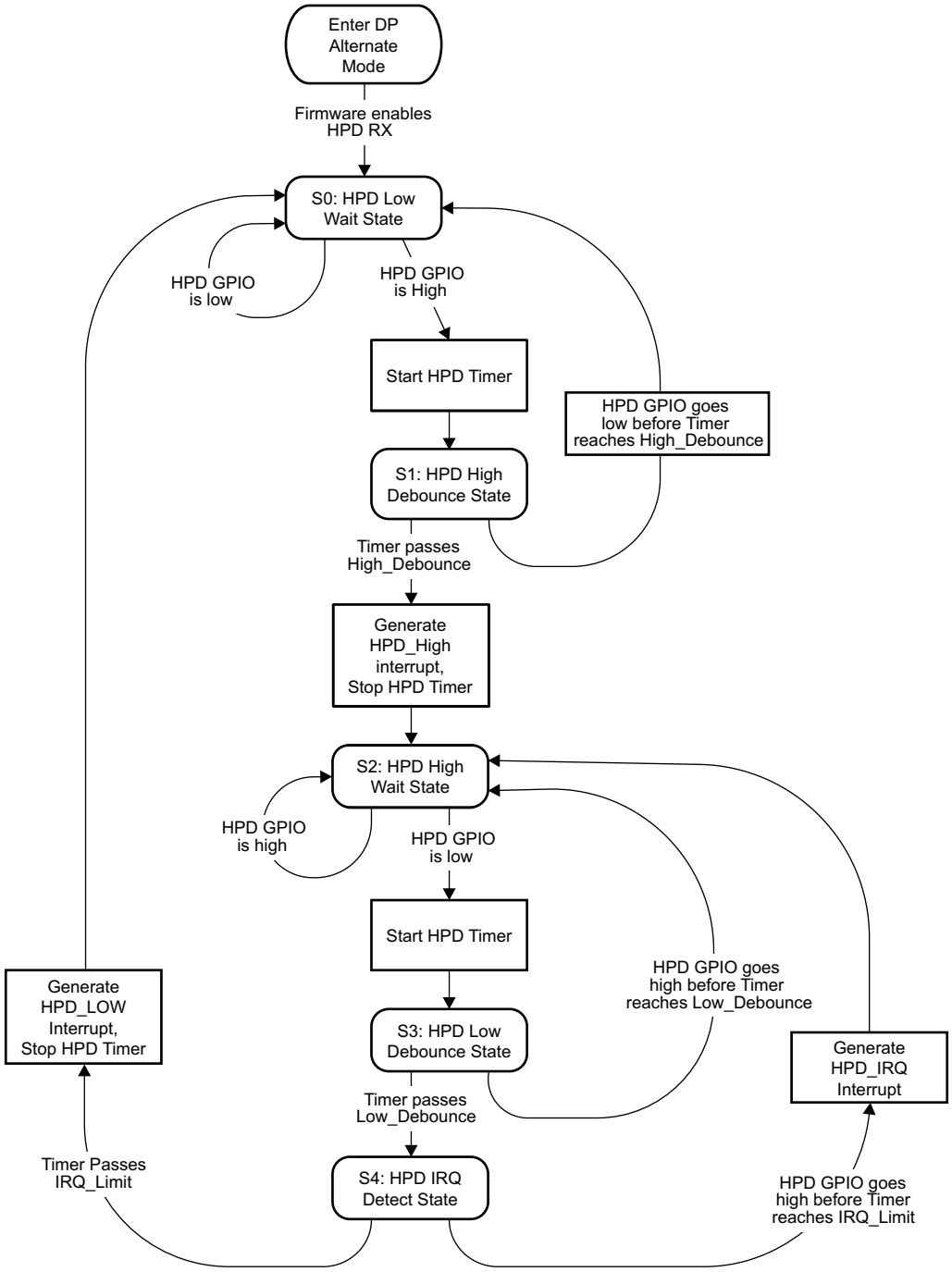


图 9-43. HPD TX Flow Diagram

9.3.16 ADC

The TPS65981 ADC is shown in 图 9-44. The ADC is a 10-bit successive approximation ADC. The input to the ADC is an analog input multiplexer that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware. Each supply voltage into the TPS65981 is available to be converted including the port power path inputs and outputs. All GPIO, the C_CCn pins, the charger detection voltages are also available for conversion. To read the port power path current sourced to VBUS, the high-voltage and low-voltage power paths are sensed and converted to voltages to be read by the ADC. For the external FET path, the difference in the SENSEP and SENSEN voltages is converted to detect the current (I_PP_EXT) that is sourced through this path.

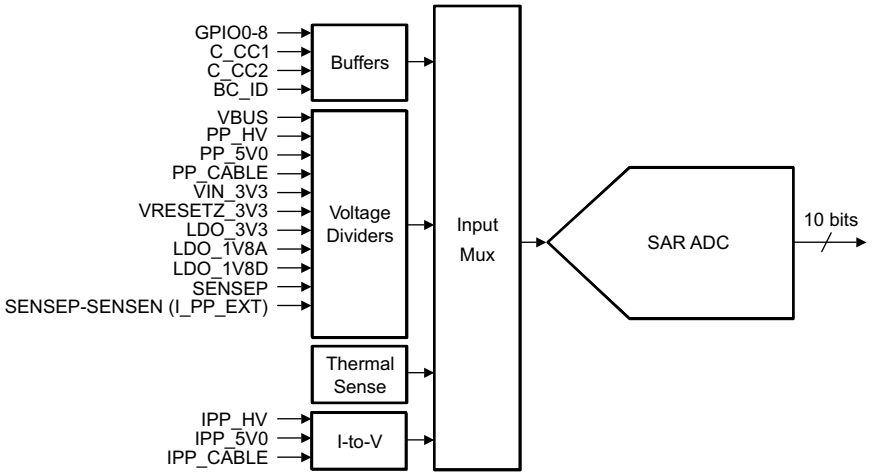


图 9-44. SAR ADC

9.3.16.1 ADC Divider Ratios

The ADC voltage inputs are each divided down to the full-scale input of 1.2 V. The ADC current sensing elements are not divided.

表 9-6 lists the divider ratios for each ADC input. The table also shows which inputs are auto-sequenced in the round-robin automatic readout mode. The C_CC1 and C_CC2 pin voltages each have two conversions values. The divide-by-5 (CCn_BY5) conversion is intended for use when the C_CCn pin is configured as VCONN output and the divide-by-2 (CCn_BY2) conversion is intended for use when C_CCn pin is configured as the CC data pin.

表 9-6. ADC Divider Ratios

CHANNEL #	SIGNAL	TYPE	AUTO-SEQUENCED	DIVIDER RATIO	BUFFERED
0	Thermal Sense	Temperature	Yes	N/A	No
1	VBUS	Voltage	Yes	25	No
2	SENSEP	Voltage	Yes	25	No
3	IPP_EXT	Current	Yes	N/A	No
4	PP_HV	Voltage	Yes	25	No
5	IPP_HV	Current	Yes	N/A	No
6	PP_5V0	Voltage	Yes	5	No
7	IPP_5V0	Current	Yes	N/A	No
8	CC1_BY5	Voltage	Yes	5	Yes
9	IPP_CABLE	Current	Yes	N/A	No
10	CC2_BY5	Voltage	Yes	5	Yes
11	GPIO5	Voltage	No	1	No
12	CC1_BY2	Voltage	No	2	Yes
13	CC2_BY2	Voltage	No	2	Yes
14	PP_CABLE	Voltage	No	5	No
15	VIN_3V3	Voltage	No	3	No
16	VRSTZ_3V3	Voltage	No	3	No
17	BC_ID	Voltage	No	3	Yes
18	LDO_1V8A	Voltage	No	2	No
19	LDO_1V8D	Voltage	No	2	No
20	LDO_3V3	Voltage	No	3	No
21	Unused	Voltage	No	3	Yes

表 9-6. ADC Divider Ratios (continued)

CHANNEL #	SIGNAL	TYPE	AUTO-SEQUENCED	DIVIDER RATIO	BUFFERED
22	GPIO0	Voltage	No	3	Yes
23	Unused	Voltage	No	3	Yes
24	GPIO2	Voltage	No	3	Yes
25	GPIO3	Voltage	No	3	Yes
26	GPIO4	Voltage	No	3	Yes
27	GPIO5	Voltage	No	3	Yes
28	GPIO6	Voltage	No	3	Yes
29	GPIO7	Voltage	No	3	Yes
30	GPIO8	Voltage	No	3	Yes
31	BUSPOWERZ	Voltage	No	3	Yes

9.3.16.2 ADC Operating Modes

The ADC is configured into one of three modes: single channel readout, round-robin automatic readout and one time automatic readout.

9.3.16.3 Single Channel Readout

In Single Channel Readout mode, the ADC reads a single channel only. Once the channel is selected by firmware, a conversion takes place followed by an interrupt back to the digital core. 图 8-2 shows the timing diagram for a conversion starting with an ADC enable. When the ADC is disabled and then enabled, there is an enable time T_ADC_EN (programmable) before sampling occurs. Sampling of the input signal then occurs for time T_SAMPLE (programmable) and the conversion process takes time T_CONVERT (12 clock cycles). After time T_CONVERT, the output data is available for read and an Interrupt is sent to the digital core for time T_INTA (2 clock cycles).

In Single Channel Readout mode, the ADC can be configured to continuously convert that channel. 图 8-3 shows the ADC repeated conversion process. In this case, once the interrupt time has passed after a conversion, a new sample and conversion occurs.

9.3.16.4 Round-Robin Automatic Readout

When this mode is enabled, the ADC state machine will read from channel 0 to channel 11 and place the converted data into registers. The host interface can request to read from the registers at any time. During Round-Robin Automatic Readout, the channel averaging must be set to 1 sample.

When the TPS65981 is running a Round Robin Readout, it will take approximately 696 µs (11 channels × 63.33 µs conversion) to fully convert all channels. Since the conversion is continuous, when a channel is converted, it will overwrite the previous result. Therefore, when all channels are read, any given value may be 649 µs out of sync with any other value.

9.3.16.5 One Time Automatic Readout

The One Time Automatic Readout mode is identical to the Round-Robin Automatic Readout except the conversion process halts after the final channel is converted. Once all 11 channels are converted, an interrupt occurs to the digital core.

9.3.17 I/O Buffers

表 9-7 lists the I/O buffer types and descriptions. 表 9-8 lists the pin to I/O buffer mapping for cross-referencing the particular I/O structure of a pin. The following sections show a simplified version of the architecture of each I/O buffer type.

表 9-7. I/O Buffer Type Description

BUFFER TYPE	DESCRIPTION
IOBUF_GPIOHSSWD	General purpose high-speed I/O
IOBUF_GPIOHSSPI	General purpose high-speed I/O
IOBUF_GPIOLS	General purpose low-speed I/O
IOBUF_GPIOLSI2C	General purpose low-speed I/O with I^2C de-glitch time
IOBUF_I2C	I^2C compliant clock and data buffers
IOBUF_OD	Open-drain output
IOBUF_PORT	Input buffer between 1st and 2nd stage port-data multiplexer

表 9-8. Pin to I/O Buffer Mapping

I/O GROUP/PIN	BUFFER TYPE	SUPPLY CONNECTION (DEFAULT FIRST)
DEBUG1	IOBUF_GPIOLS	LDO_3V3, VDDIO
DEBUG_CTL1/2	IOBUF_GPIOLSI2C	LDO_3V3, VDDIO
BUSPOWERZ	IOBUF_GPIOLS	LDO_3V3, VDDIO
GPIO0,GPIO2-8	IOBUF_GPIOLS	LDO_3V3, VDDIO
I2C_IRQZ	IOBUF_OD	LDO_3V3, VDDIO
I2C_SDA/SCL	IOBUF_I2C	LDO_3V3, VDDIO
MRESET	IOBUF_GPIOLS	LDO_3V3, VDDIO
RESETZ	IOBUF_GPIOLS	LDO_3V3, VDDIO
PORT_INT	IOBUF_PORT	LDO_3V3
SPI_PICO/POCI/CLK/CSZ	IOBUF_GPIOHSSPI	LDO_3V3
SWD_CLK/DATA	IOBUF_GPIOHSSWD	LDO_3V3

9.3.17.1 IOBUF_GPIOLS and IOBUF_GPIOLSI2C

图 9-45 shows the GPIO I/O buffer for all GPIOn pins listed GPIO0-GPIO17 in *Pin Configuration and Functions*. GPIOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input or an analog input to the ADC. The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to this buffer is configurable to be LDO_3V3 by default or VDDIO. For simplicity, the connection to VDDIO is not shown in 图 9-45, but the connection to VDDIO is fail-safe and a diode will not be present from GPIOn to VDDIO in this configuration. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

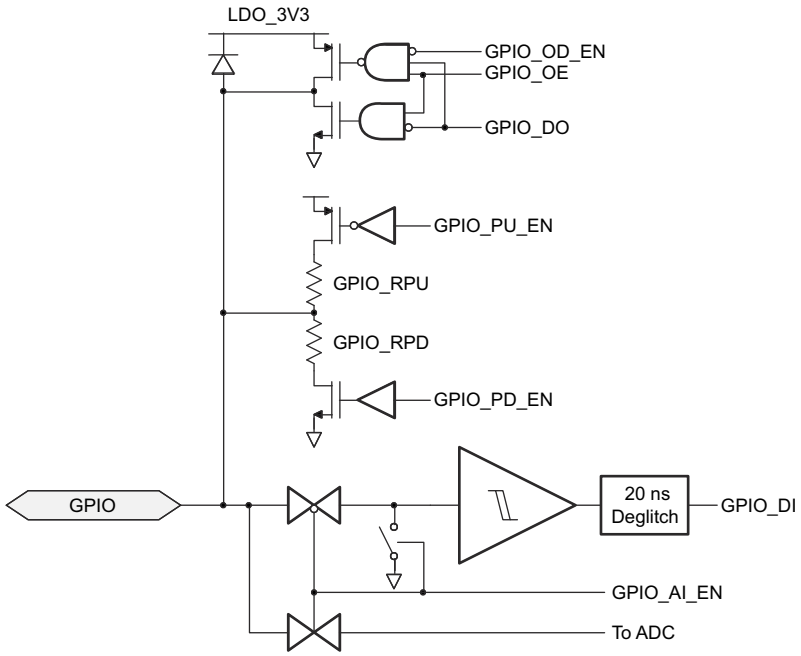


图 9-45. IOBUF_GPIOLS (General GPIO) I/O

图 9-46 shows the IOBUF_GPIOLSI2C that is identical to IOBUF_GPIOLS with an extended de-glitch time.

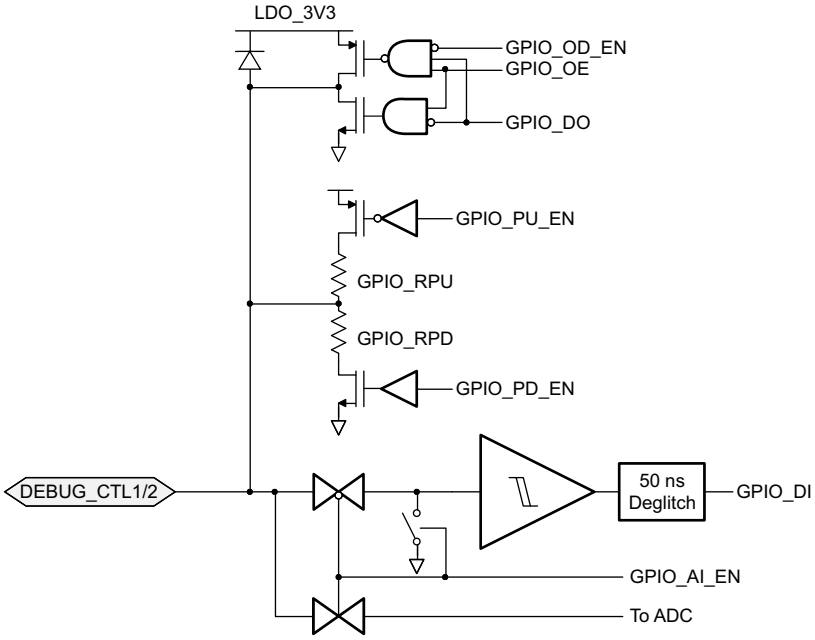


图 9-46. IOBUF_GPIOLSI2C (General GPIO) I/O with I^2C De-glitch

9.3.17.2 IOBUF_OD

The open-drain output driver is shown in 图 9-47 and is the same push-pull CMOS output driver as the GPIO buffer. The output has independent pull-down control allowing open-drain connections.

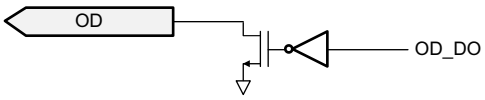


图 9-47. IOBUF_OD Output Buffer

9.3.17.3 IOBUF_PORT

The input buffer is shown in 图 9-48. This input buffer is connected to the intermediate nodes between the 1st stage switch and the 2nd stage switch for each port output (C_SBU1/2, C_USB_TP/N, C_USB_BN/P). The input buffer is enabled through firmware when monitoring digital signals and disabled when an analog signal is desired. See the 图 9-36 section for more detail on the pull-up and pull-down resistors of the intermediate node.

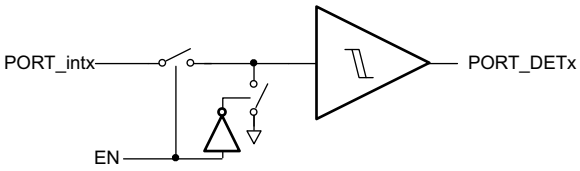


图 9-48. IOBUF_PORT Input Buffer

9.3.17.4 IOBUF_I2C

The I2C I/O driver is shown in 图 9-49. This I/O consists of an open-drain output and an input comparator with de-glitching. The supply voltage to this buffer is configurable to be LDO_3V3 by default or VDDIO. This is not shown in 图 9-49. Parameters for the I2C clock and data I/Os are found in 节 7.20.

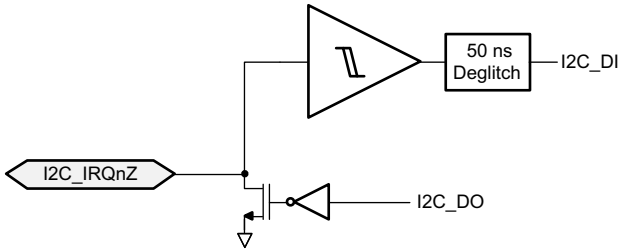


图 9-49. IOBUF_I2C I/O

9.3.17.5 IOBUF_GPIOHSPI

图 9-50 shows the I/O buffers for the SPI interface.

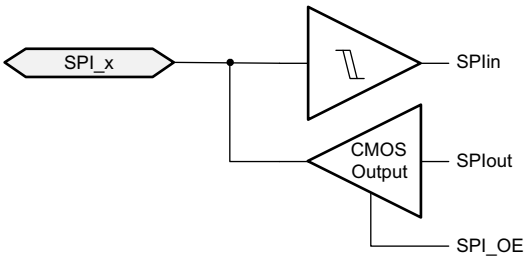


图 9-50. IOBUF_GPIOHSSPI

9.3.17.6 IOBUF_GPIOHSSWD

图 9-51 shows the I/O buffers for the SWD interface. The CLK input path is a comparator with a pull-up SWD_RPU on the pin. The data I/O consists of an identical input structure as the CLK input but with a tri-state CMOS output driver.

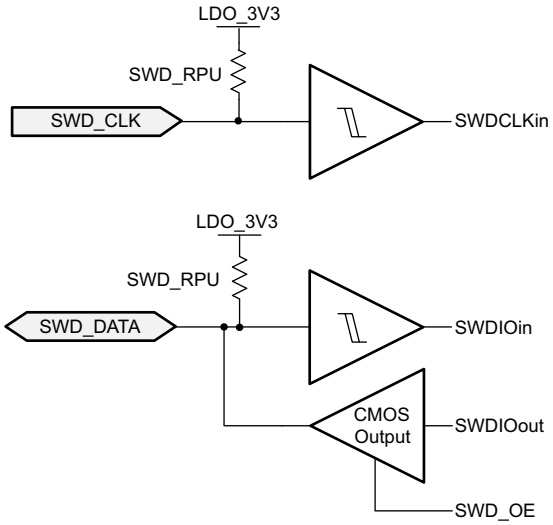


图 9-51. IOBUF_GPIOHSSWD

9.3.18 Thermal Shutdown

The TPS65981 has both a central thermal shutdown to the chip and a local thermal shutdown for the power path block. The central thermal shutdown monitors the temperature of the center of the die and disables all functions except for supervisory circuitry and halts digital core when die temperature goes above a rising temperature of TSD_MAIN. The temperature shutdown has a hysteresis of TSDH_MAIN and when the temperature falls back below this value, the device resumes normal operation. The power path block has a local thermal-shutdown circuit to detect an over temperature condition because of over current and quickly turn off the power switches. The power path thermal shutdown values are TSD_PWR and TSDH_PWR. The output of the thermal-shutdown circuit is de-glitched by TSD_DG before triggering. The thermal-shutdown circuits interrupt to the digital core.

9.3.19 Oscillators

The TPS65981 has two independent oscillators for generating internal clock domains. A 48-MHz oscillator generates clocks for the core during normal operation and clocks for the USB 2.0 endpoint physical layer. An external resistance is placed on the R_OSC pin to set the oscillator accuracy. A 100-kHz oscillator generates clocks for various timers and clocking the core during low-power states.

9.4 Device Functional Modes

9.4.1 Boot Code

The TPS65981 has a Power-on-Reset (POR) circuit that monitors LDO_3V3 and issues an internal reset signal. The digital core, memory banks, and peripherals receive clock and RESET interrupt is issued to the digital core and the boot code starts executing. 图 9-52 provides the TPS65981 boot code sequence.

The TPS65981 boot code is loaded from OTP on POR, and begins initializing TPS65981 settings. This initialization includes enabling and resetting internal registers, loading trim values, waiting for the trim values to settle, and configuring the device I^2C addresses.

The unique I^2C address is based on the digital input read on the DEBUG_CTL1/2 pins, which can be tied to GND through a pull-down resistor or to LDO_3V3 through a pull-up resistor.

Once initial device configuration is complete the boot code determines if the TPS65981 is booting under dead battery condition (VIN_3V3 invalid, VBUS valid). If the boot code determines the TPS65981 is booting under

dead battery condition, the BUSPOWERZ pin is sampled to determine the appropriate path for routing VBUS power to the system.

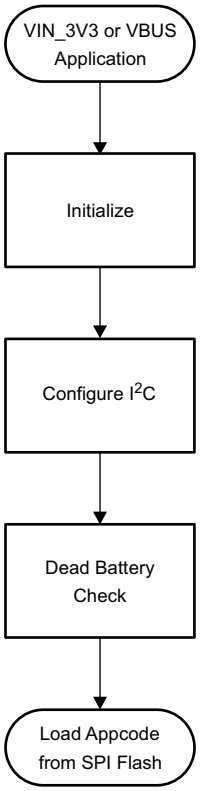


图 9-52. Flow Diagram for Boot Code Sequence

9.4.2 Initialization

During initialization the TPS65981 enables device internal hardware and loads default configurations. The 48-MHz clock is enabled and the TPS65981 persistence counters begin monitoring VBUS and VIN_3V3. These counters ensure the supply powering the TPS65981 is stable before continuing the initialization process. The initialization concludes by enabling the thermal monitoring blocks and thermal shutdown protection, along with the ADC, CRC, GPIO and NVIC blocks.

9.4.3 I²C Configuration

The TPS65981 features dual I²C busses with configurable addresses. The I²C addresses are determined according to the flow depicted in 图 9-53. The address is configured by reading device GPIO states at boot (refer to the *I²C Pin Address Setting* section for details). Once the I²C addresses are established the TPS65981 enables a limited host interface to allow for communication with the device during the boot process.

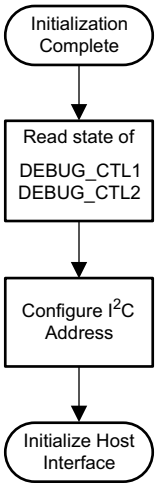


图 9-53. I²C Address Configuration

9.4.4 Dead-Battery Condition

After I²C configuration concludes the TPS65981 checks VIN_3V3 to determine the cause of device boot. If the device is booting from a source other than VIN_3V3, the dead battery flow is followed to allow for the rest of the system to receive power. The state of the BUSPOWERZ pin is read to determine power path configuration for dead battery operation. After the power path is configured, the TPS65981 will continue through the boot process. 图 9-54 depicts the full dead battery process.

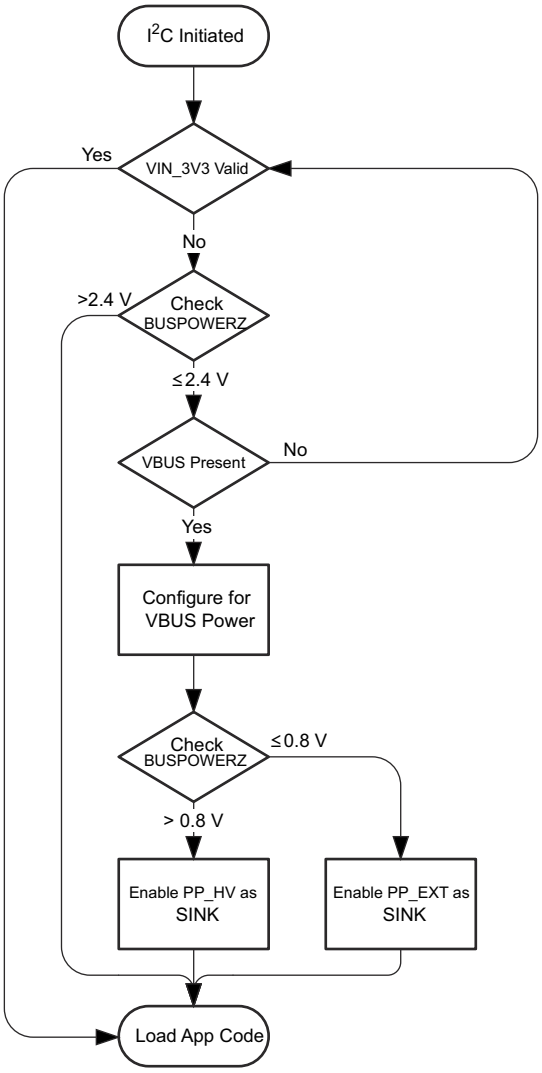


图 9-54. Dead-Battery Condition Flow Diagram

9.4.5 Application Code

The TPS65981 application code is stored in an external flash memory. The flash memory used for storing the TPS65981 application code may be shared with other devices in the system. The flash memory organization shown in 图 9-55 supports the sharing of the flash as well as the TPS65981 using the flash without sharing.

The flash is divided into two separate regions, the Low Region and the High Region. The size of this region is flexible and only depends on the size of the flash memory used. The two regions are used to allow updating the application code in the memory without over-writing the previous code. This ensures that the new updated code is valid before switching to the new code. For example, if a power loss occurred while writing new code, the original code is still in place and used at the next boot.

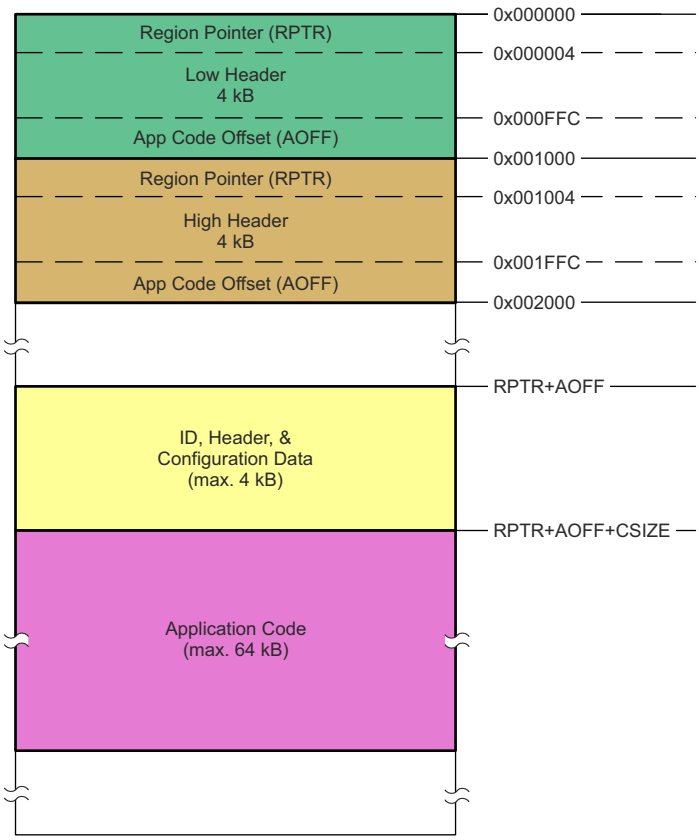


图 9-55. Flash Memory Organization

Two 4-kB header blocks start at address 0x000000h. The low-header 4-kB block is at address 0x000000h and the High Header 4 kB block is at 0x001000h. Each header contains a Region Pointer (RPTR) that holds the address of the physical location in memory where the low region application code resides. Each also contains an application code offset (AOFF) that contains the physical offset inside the region where the TPS65981 application code resides. The TPS65981 firmware physical location in memory is RPTR + AOFF. The first sections of the TPS65981 application code contain device configuration settings. This configuration determines the devices default behavior after power-up and can be customized using the TPS65981 Configuration Tool. These pointers may be valid or invalid. The Flash Read flow handles reading and determining whether a region is valid and contains good application code.

9.4.6 Flash Memory Read

The TPS65981 first attempts to load application code from the low region of the attached flash memory. If any part of the read process yields invalid data, the TPS65981 will abort the low region read and attempt to read from the high region. If both regions contain invalid data the device carries out the Invalid Memory flow. 图 9-56 shows the flow of the flash memory read.

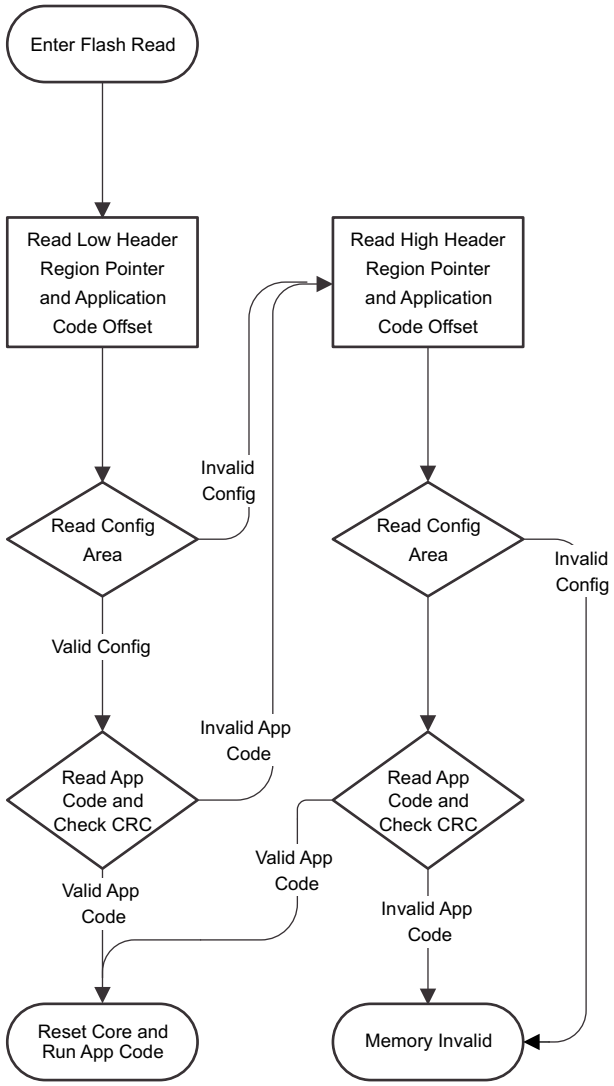


图 9-56. Flash Read Flow

9.4.7 Invalid Flash Memory

If the flash memory read fails because of invalid data, the TPS65981 carries out the memory invalid flow and presents the SWD interface on the USB Type-C SBU pins.

Memory Invalid Flow depicts the invalid memory process.

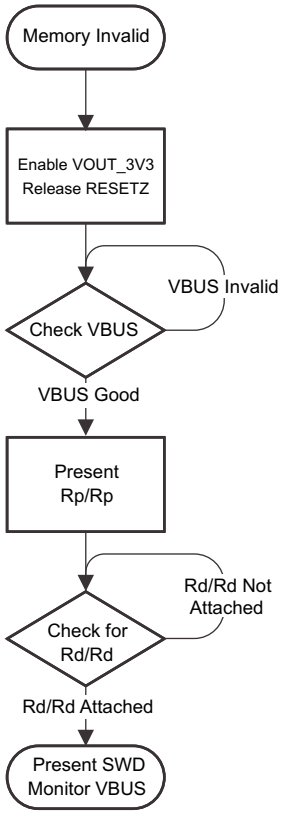


图 9-57. Memory Invalid Flow

9.5 Programming

9.5.1 SPI Controller Interface

The TPS65981 loads flash memory during the *Boot Code* sequence. The SPI controller electrical characteristics are defined in *SPI Controller Characteristics* and timing characteristics are defined in 图 8-4. The TPS65981 is designed to power the flash from LDO_3V3 to support dead-battery or no-battery conditions, and therefore pull-up resistors used for the flash memory must be tied to LDO_3V3. The flash memory IC must support 12 MHz SPI clock frequency. The size of the flash must be at least 1 Mbyte (equivalent to 8 Mbit) to hold the standard application code outlined in *Application Code*. The SPI controller of the TPS65981 supports SPI Mode 0. For Mode 0, data delay is defined such that data is output on the same cycle as chip select (SPI_CSZ pin) becomes active. The chip select polarity is active-low. The clock phase is defined such that data (on the SPI_POCI and SPI_PICO pins) is shifted out on the falling edge of the clock (SPI_CLK pin) and data is sampled on the rising edge of the clock. The clock polarity for chip select is defined such that when data is not being transferred the SPI_CLK pin is held (or idling) low. The minimum erasable sector size of the flash must be 4 kB. The W25Q80 flash memory IC is recommended. Refer to TPS65981 I^{2}C Host Interface Specification for instructions for interacting with the attached flash memory over SPI using the host interface of the TPS65981.

9.5.2 I^{2}C Slave Interface

The TPS65981 has one I^{2}C interface port. The I^{2}C Port is comprised of the I2C_SDA, I2C_SCL, and I2C_IRQZ pins. This interface provide general status information about the TPS65981, as well as the ability to control the TPS65981 behavior, as well as providing information about connections detected at the USB-C receptacle and supporting communications to and from a connected device and/or cable supporting BMC USB-PD.

The port is an I^{2}C slave. An interrupt mask is set for the I^{2}C port that determines what events are interrupted on the port. The interrupt mask is configurable in application code.

9.5.2.1 I²C Interface Description

The TPS65981 support Standard and Fast mode I²C interface. The bi-directional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

图 9-58 shows the start and stop conditions of the transfer. 图 9-59 shows the SDA and SCL signals for transferring a bit. 图 9-60 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

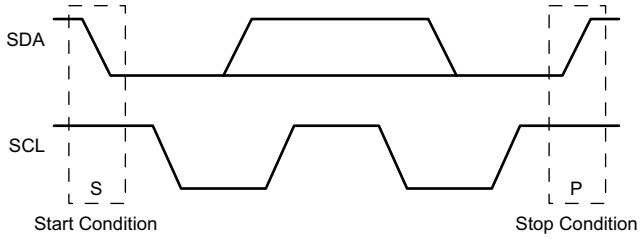


图 9-58. I²C Definition of Start and Stop Conditions

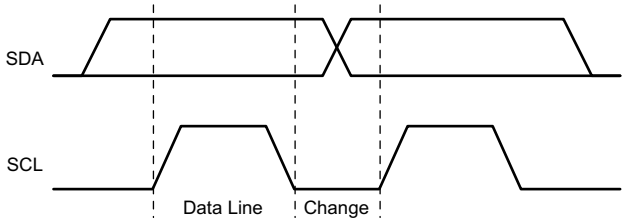


图 9-59. I²C Bit Transfer

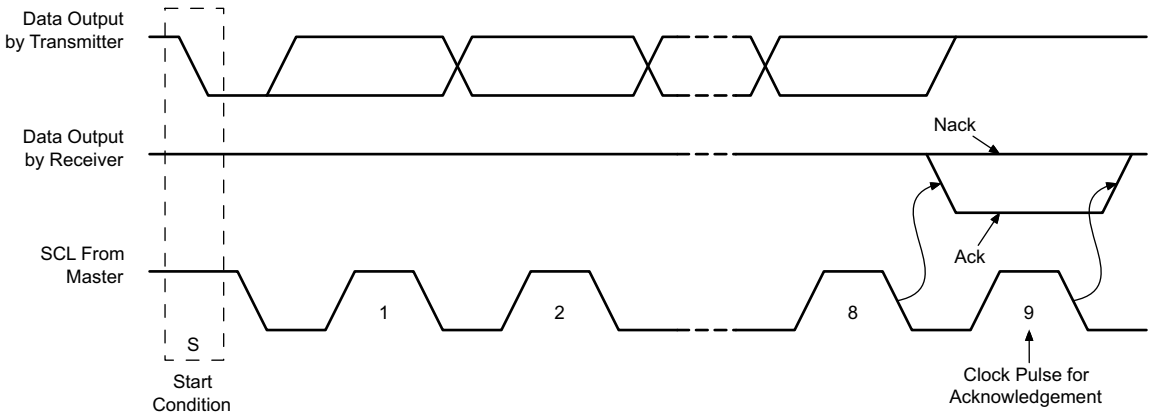


图 9-60. I²C Acknowledgment

9.5.2.2 I²C Clock Stretching

The TPS65981 features clock stretching for the I²C protocol. The TPS65981 slave I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line will remain low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 μs for standard 100 kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

9.5.2.3 I²C Address Setting

The boot code sets the hardware configurable unique I²C address of the TPS65981 before the port is enabled to respond to I²C transactions. The unique I²C address is determined by a combination of the digital level on the DEBUG_CTL1/DEBUG_CTL2 pins (two bits) as shown in 表 9-9.

表 9-9. I²C Default Unique Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	DEBUG_CTL2	DEBUG_CTL1	1	1	1	R/$\overline{W}$

9.5.2.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS65981. The I²C Slave sub-address is used to receive or respond to Host Interface protocol commands. 图 9-61 and 图 9-62 show the write and read protocol for the I²C slave interface, and a key is included in 图 9-63 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

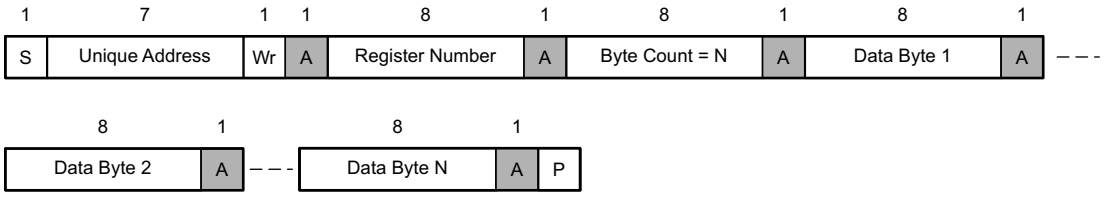


图 9-61. I²C Unique Address Write Register Protocol

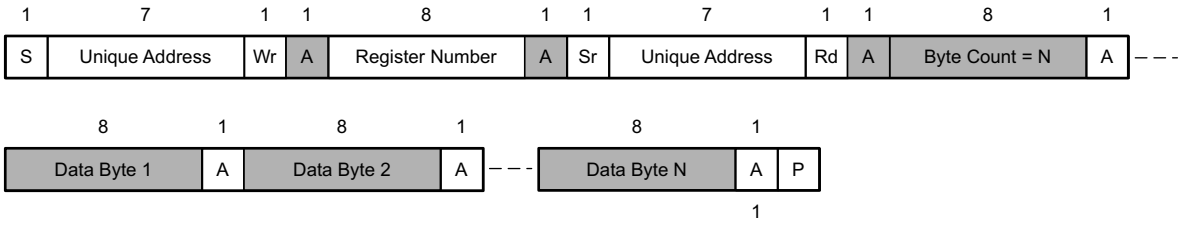


图 9-62. I²C Unique Address Read Register Protocol

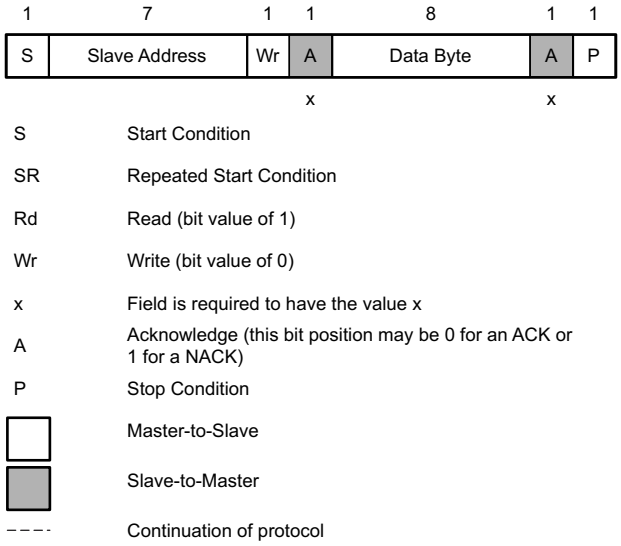


图 9-63. I²C Read/Write Protocol Key

9.5.2.5 I²C Pin Address Setting

图 9-64 shows the decoding of the I²C address. DEBUG_CTL1/2 are checked for the DC condition on these pins (high or low) for setting the two configurable bits of the I²C address described previously. DEBUG_CTL1/2 are GPIO and the address decoding is done by firmware in the digital core.

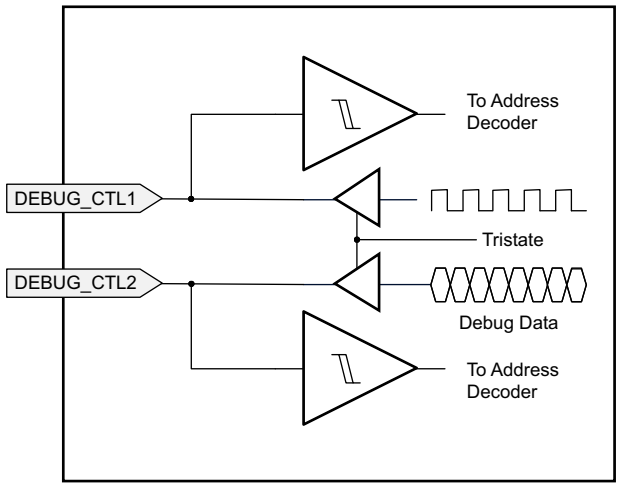


图 9-64. I²C Address Decode

10 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

The typical applications of the TPS65981 include chargers, docking systems, monitors, notebooks, tablets, ultrabooks, and any other product supporting USB Type-C, USB-PD, or both as a power source, power sink, data DFP, data UFP, or dual-role port (DRP). The typical applications outlined in the following sections detail a *Fully-Featured USB Type-C and PD Charger Application* and a *USB Type-C and PD Dock or Monitor Application*.

10.2 Typical Applications

10.2.1 Fully-Featured USB Type-C® and PD Charger Application

The TPS65981 controls three separate power paths making it a flexible option for Type C PD charger applications. In addition, the TPS65981 supports VCONN power for *e-marked* cables which are required for applications which require greater than 3 A of current on VBUS. 图 10-1 shows the high level block diagram of a Type-C and PD charger that is capable of supporting 5 V at 3 A, 9 V at 3 A, 12 V at 3 A (optional), 15 V at 3 A, and 20 V at 5 A. The 5-V , 9-V, 12-V and 15-V outputs are supported by the TPS65981 internal FETs and the 20-V output uses the external FET path controlled by the TPS65981 NFET drive. This Type-C PD charger uses a receptacle for flexibility on cable choice.

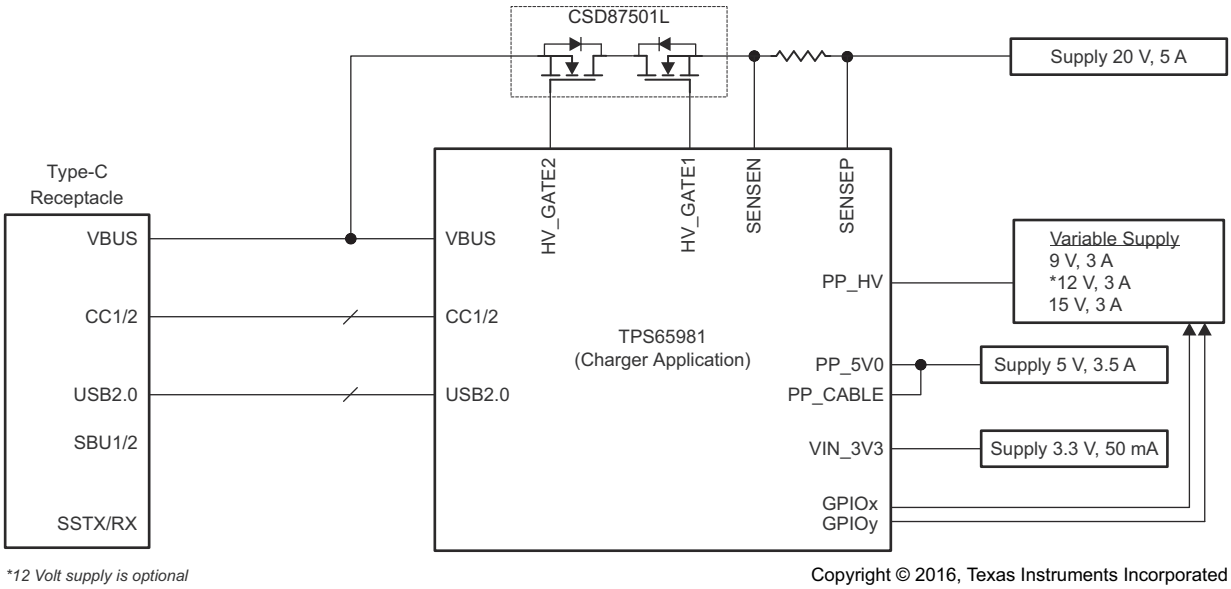


图 10-1. Type-C and PD Charger Application

10.2.1.1 Design Requirements

For a USB Type-C and PD charger application, 表 10-1 lists the input voltage requirements and expected current capabilities.

表 10-1. Charging Application Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE	DIRECTION OF CURRENT
PP_5V0 Input Voltage and Current Capabilities	5 V, 3 A	Sourcing to VBUS
PP_CABLE Input Voltage and Current Capabilities	5 V, 500 mA	Sourcing to VCONN
PP_HV Input Voltage and Current Capabilities	9 V/12 V/15 V, 3 A	Sourcing to VBUS
EXT FET Path Input Voltage and Current Capabilities	20 V, 5 A	Sourcing to VBUS
VIN_3V3 Voltage and Current Requirements	2.85 - 3.45 V, 50 mA	Internal TPS65981 Circuitry

10.2.1.1.1 External FET Path Components (PP_EXT and RSENSE)

The external FET path allows for the maximum PD power profile (20 V at 5 A) and design considerations must be taken into account for choosing the appropriate components to optimize performance.

Although a Type C PD charger will be providing power there could be a condition where a non-compliant device can be connected to the charger and force voltage back into the charger. To protect against this the external FET path detects reverse current in both directions of the current path. The TPS65981 uses two *back-to-back* NFETs to protect both sides of the system. Another design consideration is to rate the external NFETs above the Type C and PD specification maximum which is 20 V. In this specific design example, 30-V NFETs are used that have an average combined source-to-source on-resistance $R_{SS,ON}$ of 9.3 mΩ to reduce losses. The CSD87501L is recommended.

The TPS65981 supports either a 10-mΩ or a 5-mΩ sense resistor on the external FET path. This RSENSE resistor is used for current limiting and is used for the reverse current protection of the power path. A 5 mΩ sense resistor is used in the design to minimize losses and I-R voltage drop. Recommended NFET Capabilities summarizes the recommended parameters for the external NFET used. The total voltage drop seen across RSENSE and the external NFET could be determined by 方程式 5. The drop in the entire system must be considered and regulated accordingly to ensure that the output voltage is within the specification. Use 方程式 6 to calculate the power lost through the external FET path.

表 10-2. Recommended NFET Capabilities

VOLTAGE RATING	CURRENT RATING	$R_{DS,ON}$, $R_{SS,ON}$
30 V (minimum)	10 A (peak current)	< 10 mΩ , < 20 mΩ

$$\text{Voltage Drop} = \text{DC Current} \times (R_{SENSE} + \text{NFET1 } R_{DS,ON} + \text{NFET2 } R_{DS,ON}) \quad (5)$$

$$\text{Power Loss} = \text{Voltage Drop} \times \text{DC Current} \quad (6)$$

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 TPS65981 External Flash

The external flash contains the TPS65981 application firmware and must be sized to 2M-bit (256k-Byte) minimum. This size allows for pointers and two copies of the firmware image to reside on the flash along with the needed headers. The recommended flash IC is the W25Q20CL which is a 3.3 V flash and is powered from the LDO_3V3 output from the TPS65981.

10.2.1.2.2 Debug Control (DEBUG_CTL) and I²C (I2C) Resistors

DEBUG_CTL1/2 pins must be tied to GND through a 0-Ω resistor tied to GND directly if needed to reduce solution size. Pull-ups on the I2C_CLK, I2C_SDA, and I2C_IRQZ are used for debugging purposes. In most simple charger designs, I²C communication is not needed in the final application.

10.2.1.2.3 Oscillator (R_OSC) Resistor

A 15-kΩ 0.1% resistor is needed for key PD BMC communication timing and the USB2.0 endpoint. A 1% 15-kΩ resistor is not recommended to be used because the internal oscillators are not controlled well enough by this loose resistor tolerance.

10.2.1.2.4 VBUS Capacitor and Ferrite Bead

A 1-µF ceramic capacitor is placed close to the TPS65981 VBUS pins. A 6-A ferrite bead is used in this design along with four high frequency noise 10-nF capacitors placed close to the Type-C connector to minimize noise.

10.2.1.2.5 Soft Start (SS) Capacitor

The recommended 0.22-µF capacitor is placed on the TPS65981 SS pin.

10.2.1.2.6 USB Top (C_USB_T), USB Bottom (C_USB_B), and Sideband-Use (SBU) Connections

Although the charger is configured to be only a power source, SBU1/2, USB top and bottom must be routed to the Type C connector. This allows for debugging or for any specific alternate modes for power to be configured if needed. ESD protection is used in the design on all of these nets as good design practice.

10.2.1.2.7 Port Power Switch (PP_EXT, PP_HV, PP_5V0, and PP_CABLE) Capacitors

The design assumes that a DC-DC converter is connected to the paths where there is significant output capacitance on the DC-DCs to provide the additional capacitance for load steps. TI recommends for the DC-DC converters to be capable of supporting current spikes which can occur with certain PD configurations.

The PP_EXT path is capable of supporting up to 5 A which requires additional capacitance to support system loading by the device connected to the charger. A ceramic 10-µF (X7R/X5R) capacitor is used in this design. This capacitor must at least have a 25 V rating and TI recommends to have 30 V or greater rated capacitor.

The PP_HV path is capable of supporting up to 3 A which requires additional capacitance to support system loading by the device connected to the charger. A ceramic 10-µF (X7R/X5R) capacitor coupled with a 0.1 µF high frequency capacitor is placed close to the TPS65981.

The PP_5V0 and PP_CABLE supplies are connected together therefore a ceramic 22-µF (X7R/X5R) capacitor coupled with a 0.1-µF high-frequency capacitor is placed close to the TPS65981. The PP_5V0 path can support 3 A and the PP_CABLE path supports 600 mA for active Type C PD cables.

The design assumes that a DC-DC converter is connected to the paths where there is significant output capacitance on the DC-DCs to provide the additional capacitance. TI recommends that the DC-DC converters are capable of supporting current spikes which can occur with certain PD configurations.

10.2.1.2.8 Cable Connection (CCn) Capacitors and RPD_Gn Connections

This charger application is designed to only be a source of power and does not support dead battery. RPD_G1 and RPD_G2 must be tied to GND and not connected to the CC1 and CC2 respectively. For CC1 and CC2 lines, they require a 330-pF capacitor to GND.

10.2.1.2.9 LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, and VDDIO

For all capacitances, consider the DC-voltage derating of ceramic capacitors. Generally the effective capacitance is halved with voltage applied.

VIN_3V3 is connected to VDDIO which ensures that the I/Os of the TPS65981 will be configured to 3.3 V. A 1-µF capacitor is used and is shared between VDDIO and VIN_3V3. LDO_1V8D, LDO_1V8A, and LDO_BMC each have a 1-µF capacitor. In this design LDO_3V3 powers the external flash and various pull-ups of the TPS65981 device. A 10-µF capacitor was chosen to support these additional connections.

10.2.1.3 Application Curve

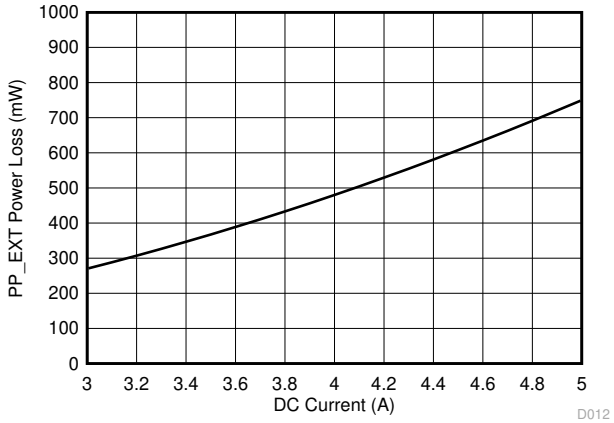


图 10-2. PP_EXT Power Loss (R_{NFETS} + R_{SENSE} = 30 mΩ)

10.2.2 USB Type-C® and PD Dock or Monitor Application

The TPS65981 controls two separate power paths making it a flexible option for Type-C and PD dock application that simultaneously charges a USB PD DisplayPort video source (for example, a notebook computer). The dock or monitor application of the TPS65981, shown in 图 10-3, uses a GPIO to sense when a power supply is present on the system-side of the TPS65981. When external power is applied from an AC-DC power supply first, the TPS65981 shall be configured to automatically attempt to become the USB Type-C or PD power source. When a notebook computer or other USB PD source is connected first and the AC-DC supply is not present, the dock or monitor supports booting from VBUS in No Battery Mode, provides power to the SPI Flash to load application code, and can optionally power the entire system by enabling the PP_EXT path as a sink. If the AC-DC power supply is applied at a later time, the TPS65981 will detect the new power supply, automatically enable one of more Source PDOs, and initiate a Power Role Swap PD message to offer power to the system at the far-end of the Type-C cable. Refer to 图 10-6 for a timing diagram of the GPIO-controlled variable buck regulator voltage output at PP_HV and the voltage at VBUS during a Type-C connection and throughout an intial USB PD power negotiation where the dock or monitor is the power source. The video receptacle can be DisplayPort, HDMI, or VGA although only DisplayPort is shown in 图 10-3. The dock or monitor application uses a Type-C receptacle and an HD3SS460 SuperSpeed multiplexer that is controlled by the TPS65981. The CC1/2 pins of the TPS65981 will detect cable orientation and automatically configure the HD3SS460 SuperSpeed signal pairs for 2-lanes of USB3 data and 2-lanes of DisplayPort video or 4-lanes of DisplayPort video depending on the Alternate Mode configured by the downstream-facing port (DFP).

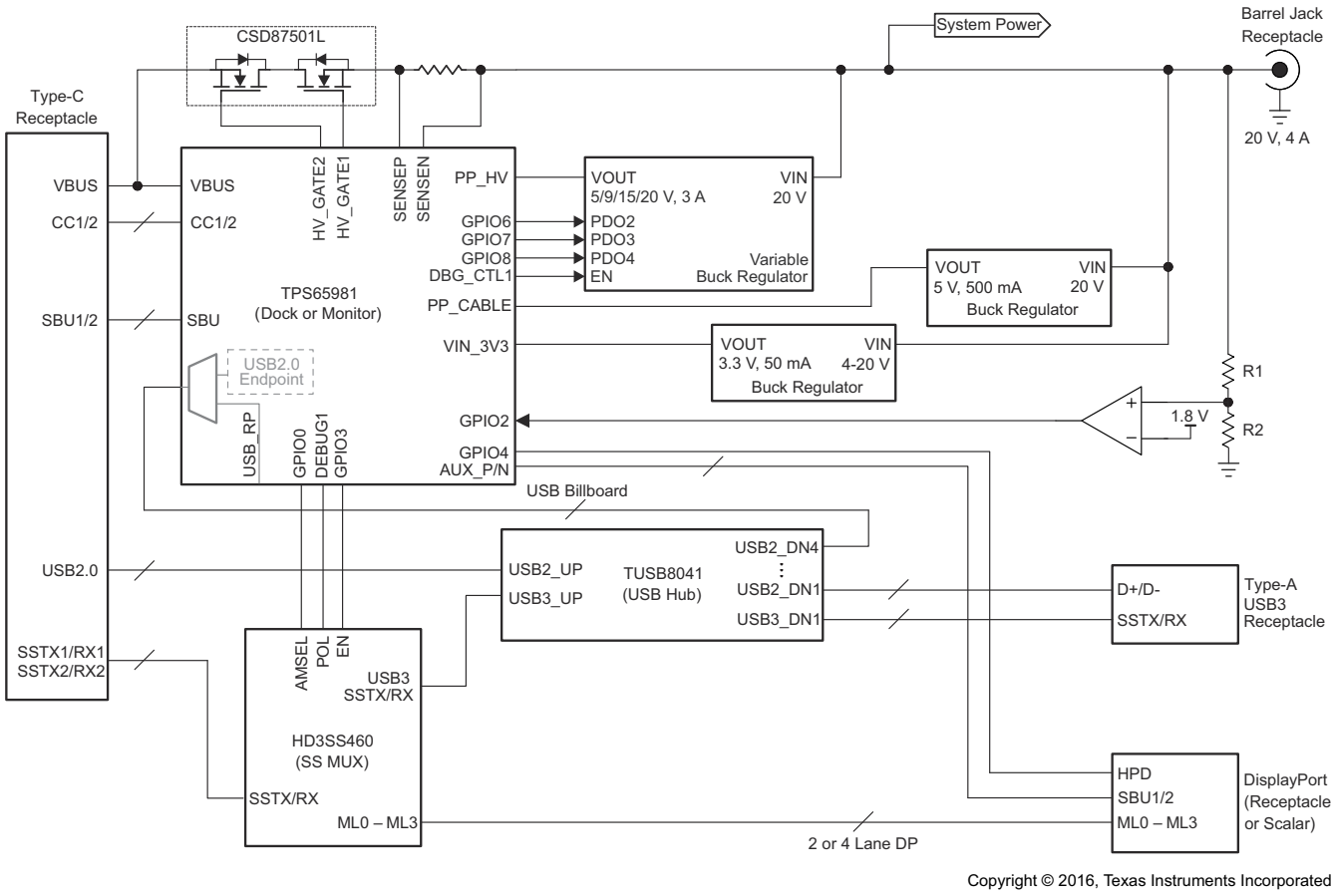


图 10-3. Type-C and PD Dock or Monitor Application

10.2.2.1 Design Requirements

For a USB Type-C and PD dock application, 表 10-3 shows the input/output voltage requirements and expected current capabilities for the TPS65981

表 10-3. Dock Application Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE	DIRECTION OF CURRENT
PP_CABLE Input Voltage and Current Capabilities	5 V, 500 mA	Sourcing to VCONN (CC2 or CC1)
PP_HV Output Voltage and Current Capabilities	5 V/9 V/15 V/20 V, 3 A	Sourcing to VBUS
PP_EXT Input Voltage and Current Capabilities	12-20 V, 5 A	Sinking from VBUS
VIN_3V3 Voltage and Current Requirements	2.85 - 3.45 V, 50 mA	Internal TPS65981 Circuitry

10.2.2.2 Detailed Design Procedure

The same passive components used in the *Fully-Featured USB Type-C and PD Charger Application* are also applicable in this design to support all of the features of the TPS65981. Additional design information is provided below for changes in passive components required by the dock or monitor application. The TPS65981 control of the HD3SS460 SuperSpeed multiplexer is explained in *HD3SS460 Control and DisplayPort Configuration*.

10.2.2.2.1 Port Power Switch (PP_5V0 and PP_CABLE) Capacitors

The PP_5V0 supply is un-used in this application because 5 Volts is the default output voltage of the variable buck regulator and is sourced to VBUS from PP_HV. PP_CABLE is still used and can supply up to 500 mA to provide power to e-marked or active Type-C cables for SuperSpeed data signal conditioning. The PP_CABLE

supply, when PP_5V0 is un-used, is connected to a 4.7-µF ceramic (X7R/X5R) capacitor coupled with a 0.1-µF high-frequency capacitor that must be placed close to the TPS65981.

10.2.2.2.2 HD3SS460 Control and DisplayPort Configuration

The Type-C port in this design supports DisplayPort and/or USB3.1 SuperSpeed data by adding the HD3SS460 multiplexer with GPIO input signals controlled by the TPS65981. 表 10-4 shows the DisplayPort configurations supported in the system. 表 10-5 shows the summary of the TPS65981 GPIO signals control for the HD3SS460. The HD3SS460 is also capable of multiplexing the required signals to the SBU_1/2 pins at the Type-C port.

表 10-4. Supported DisplayPort Configurations

	DisplayPort Role	Display Port Pin Assignment	DisplayPort Lanes
Configuration 1	UFP_D	Pin Assignment C	4-Lane
Configuration 2	UFP_D	Pin Assignment D	2-Lane and USB 3.1 data

表 10-5. TPS65981 and HD3SS460 GPIO Control(1)

TPS65981 GPIO	HD3SS460 Control Pin	Description
GPIO0	AMSEL	Alternate Mode Selection (4-Lane DP/2-Lane DP + USB3.1)
GPIO3	EN	Super Speed Multiplexer Enable
DEBUG1	POL	Type-C Cable Orientation

(1) Specific GPIO pins are used for simplicity, but the configurable firmware settings allow the HD3SS460 GPIO Events to be mapped to any GPIO pin of the TPS65981.

10.2.2.2.3 AC-DC Power Supply (Barrel Jack) Detection Circuitry

The system is design to either operate bus-powered over Type-C/PD or line-powered from the DC barrel jack. The TPS65981 detects that the DC barrel jack is connected to GPIOn. In the simplest form, a voltage divider could be set to the GPIO I/O level when the DC Barrel jack voltage is present, as shown in 图 10-4. A comparator circuit is recommend and used in this design for design robustness, as shown in 图 10-5. 图 10-3 shows the barrel jack detection circuitry used in the dock or monitor application connected to GPIO2 configured as an input.

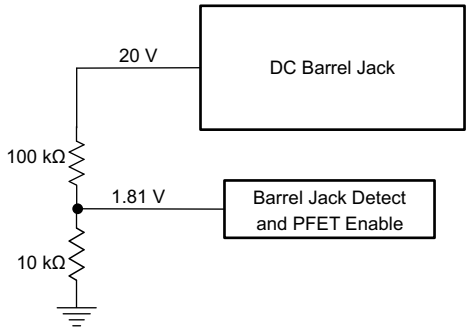


图 10-4. DC Barrel Jack Voltage Divider

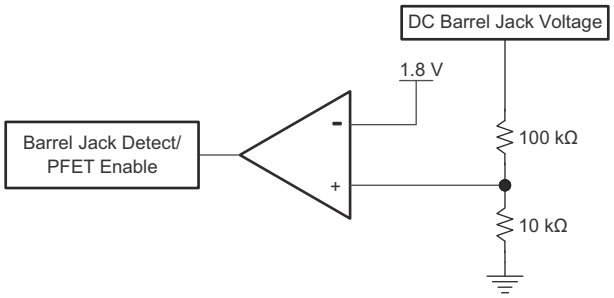


图 10-5. Barrel Jack Detect Comparator

This detect signal is used to determine if the barrel jack is present to support the 20 V PD power contracts and to hand-off charging from barrel jack to Type-C or Type-C to barrel jack. When the DC barrel jack is detected the TPS65981 at the Type-C port will not request power as a USB PD sink and the system will be able to support a 5-20 V source power contract to another device. When the DC Barrel Jack is disconnected the TPS65981 will exit any 20 V source power contract and re-negotiate a power contract as a sink. When the DC Barrel Jack is re-connected the TPS65981 will send updated source capabilities and re-negotiate a power contract if possible.

10.2.2.2.4 TPS65981 Control of Variable Buck Regulator Output Voltage (PP_HV)

The Type-C port in this design supports the 4 standard discrete source voltages in USB PD (5 V, 9 V, 15 V, and 20 V) by adding the LM3489 DC-DC hysteretic PFET buck controller with GPIOs controlled by the TPS65981 that enables the LM3489 and modifies the output voltage that is supplied to VBUS through the internal PP_HV power switch. In 图 10-3, the enabled (EN) pin of the LM3489 is controlled by DBG_CTL1 which is mapped to the Plug Event GPIO so that whenever a Type-C plug occurs the voltage regulator will generate the 5-V default output voltage for sourcing Type-C and PDO1 power. The default voltage is set by a resistor divider (R_{FB1} and R_{FB2}) with the center tap connected to the feedback pin (FB) of the LM3489. The TPS65981 modifies the output voltage when a high voltage PD contract is negotiated by forcing a GPIO output high and switching in a third resistor in parallel with R_{FB2} in the feedback circuit. In 图 10-3, GPIO6 indicates a 9-V PD contract (PDO2), GPIO7 indicates a 15-V contract (PDO3), and GPIO8 indicates a 20-V contract (PDO4). The LM3489 was selected because the architecture allows 100% duty-cycle operation, where the only additional power loss in the system is from the $R_{DS,ON}$ of the PFET used in the regulator circuit.

10.2.2.2.5 TPS65981 and System Controller Interaction

The TPS65981 features an I^2C slave port, where a system controller has the ability to write to the I^2C slave port. The I^2C port has an I^2C interrupt that will inform the system controller that a change has happened in the system. This allows the system controller to dynamically budget power and reconfigures a port’s capabilities dependent on current state of the system. The system controller is also used for updating the TPS65981 firmware over I^2C, where a connected host or the application processor loads the Firmware update to the system controller and then the system controller updates firmware stored in the SPI Flash memory via I^2C writes to the TPS65981. In a dock or monitor application, the video scalar is commonly a processor and the I^2C master capable of acting as the system controller for the TPS65981.

10.2.2.3 Application Curves

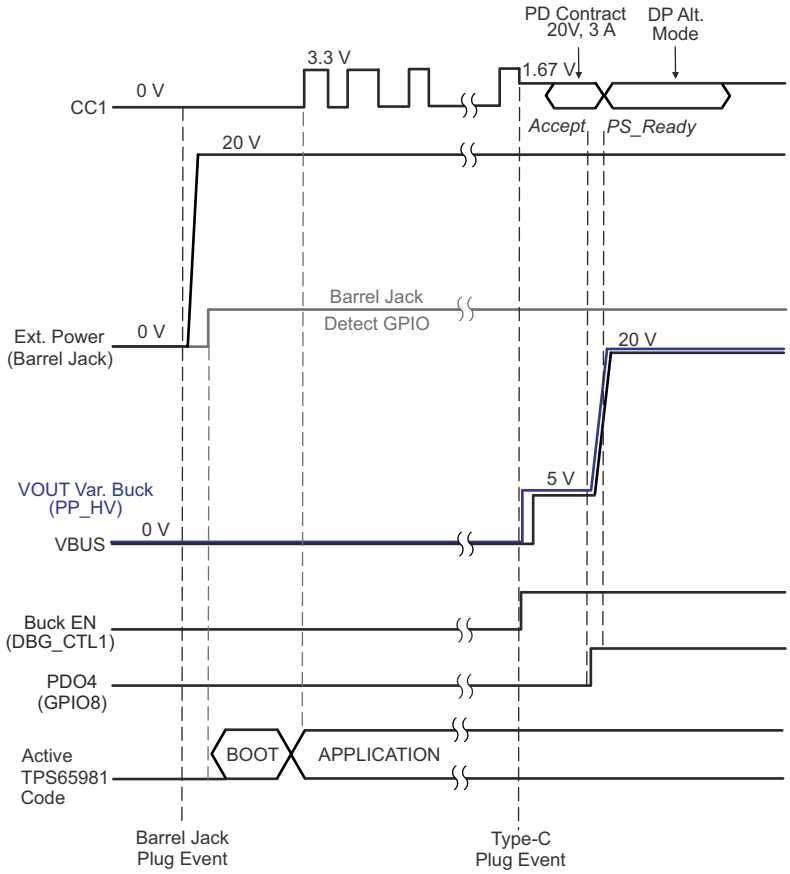


图 10-6. TPS65981 Variable Buck Regulator in Dock or Monitor Application Timing Diagram

11 Power Supply Recommendations

11.1 3.3 V Power

11.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply to the TPS65981. The VIN_3V3 switch (S1 in 图 9-40) is a unidirectional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when 3.3 V is available. See 表 11-1 for the recommended external capacitance on the VIN_3V3 pin.

11.1.2 VBUS 3.3-V LDO

The 3.3 V LDO from VBUS steps down voltage from VBUS to LDO_3V3. This allows the TPS65981 to be powered from VBUS when VIN_3V3 is not available. This LDO steps down any recommended voltage on the VBUS pin. When VBUS is 20 V, as is allowable by USB PD, the internal circuitry of the TPS65981 will operate without triggering thermal shutdown; however, a significant external load on the LDO_3V3 pin may increase temperature enough to trigger thermal shutdown. The VBUS 3.3-V LDO blocks reverse current from LDO_3V3 back to VBUS allowing VBUS to be unpowered when LDO_3V3 is driven from another source. See 表 11-1 for the recommended external capacitance on the VBUS and LDO_3V3 pins.

11.2 1.8 V Core Power

Internal circuitry is powered from 1.8 V. There are two LDOs that step the voltage down from LDO_3V3 to 1.8 V. One LDO powers the internal digital circuits. The other LDO powers internal low voltage analog circuits.

11.2.1 1.8 V Digital LDO

The 1.8 V digital LDO provides power to all internal low voltage digital circuits. This includes the digital core, memory, and other digital circuits. See 表 11-1 for the recommended external capacitance on the LDO_1V8D pin.

11.2.2 1.8 V Analog LDO

The 1.8 V analog LDO provides power to all internal low voltage analog circuits. See 表 11-1 for the recommended external capacitance on the LDO_1V8A pin.

11.3 VDDIO

The VDDIO pin provides a secondary input allowing some I/Os to be powered by a source other than LDO_3V3. The default state is power from LDO_3V3. The memory stored in the flash will configure the I/O’s to use LDO_3V3 or VDDIO as a source and application code will automatically scale the input and output voltage thresholds of the I/O buffer accordingly. See *I/O Buffers* for more information on the I/O buffer circuitry. See 表 11-1 for the recommended external capacitance on the VDDIO pin.

11.3.1 Recommended Supply Load Capacitance

表 11-1 lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

表 11-1. Recommended Supply Load Capacitance

PARAMETER	DESCRIPTION	VOLTAGE RATING	CAPACITANCE		
			MIN (ABSOLUTE)	TYP (PLACED)	MAX (ABSOLUTE)
CVIN_3V3	Capacitance on VIN_3V3	6.3 V	5 µF	10 µF	
CLDO_3V3	Capacitance on LDO_3V3	6.3 V	5 µF	10 µF	25 µF
CLDO_1V8D	Capacitance on LDO_1V8D	4 V	500 nF	2.2 µF	12 µF
CLDO_1V8A	Capacitance on LDO_1V8A	4 V	500 nF	2.2 µF	12 µF
CLDO_BMC	Capacitance on LDO_BMC	4 V	1 µF	2.2 µF	4 µF
CVDDIO	Capacitance on VDDIO. When shorted to LDO_3V3, the CLDO_3V3 capacitance may be shared.	6.3 V	0.1 µF	1 µF	
CVBUS	Capacitance on VBUS 1	25 V	0.5 µF	1 µF	12 µF
CPP_5V0	Capacitance on PP_5V0	10 V	2.5 µF	4.7 µF	
CPP_HV	Capacitance on PP_HV (Source to VBUS)	25 V	2.5 µF	4.7 µF	
	Capacitance on PP_HV (Sink from VBUS)	25 V		47 µF	120 µF
CPP_CABLE	Capacitance on PP_CABLE. When shorted to PP_5V0, the CPP_5V0 capacitance may be shared.	10 V	2.5 µF	4.7 µF	
CPP_HVEXT	Capacitance on external high voltage source to VBUS	25 V	2.5 µF	4.7 µF	
	Capacitance on external high voltage sink from VBUS	25 V		47 µF	120 µF
CSS	Capacitance on soft start pin	6.3 V		220 nF	
CC_CC1	Capacitance on C_CC1 pin	25 V	220 pF	330 pF	470 pF
CC_CC2	Capacitance on C_CC2 pin	25 V	220 pF	330 pF	470 pF

11.3.2 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS65981 during sudden disconnects because of inductive effects in a cable, TI recommends that a Schottky be placed from VBUS to GND as shown in 图 11-1. The NSR20F30NXT5G is recommended.

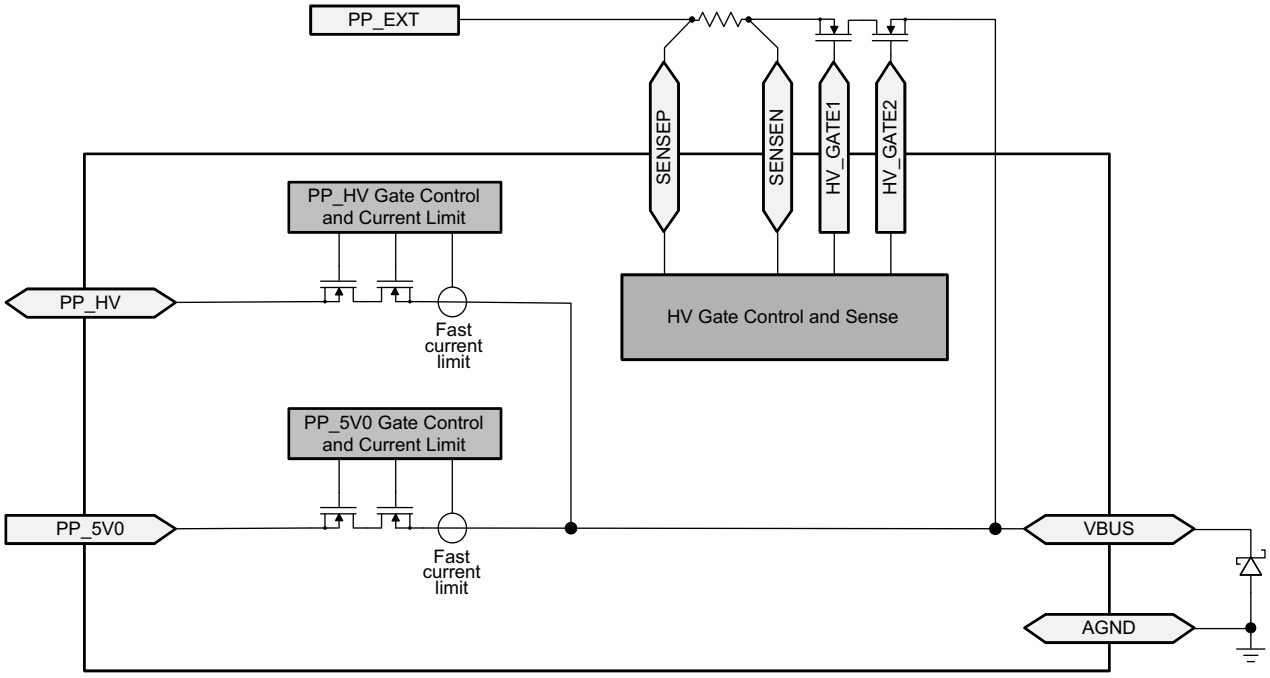


图 11-1. Schottky on VBUS for Current Surge Protection

12 Layout

12.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high-speed signals and improve the thermal dissipation from the TPS65981 power path. The combination of power and high-speed data signals are easily routed if the following guidelines are followed. Consult with a printed circuit board (PCB) manufacturer to verify manufacturing capabilities.

12.1.1 TPS65981 Recommended Footprint

图 12-1 shows the TPS65981 footprint with 56 0.6-mm long by 0.25-mm wide rectangular pads and 1 5.9-mm by 5.9-mm square, grounded Thermal Pad. This footprint is applicable to boards that will be using a non-HDI process using all through-hole vias or an HDI PCB process using smaller vias to fan-out into the inner layers of the PCB. Via fills and via tenting is recommended for size-constrained applications. The footprint allows for easy fan-out into other layers of the PCB and thermal dissipation into the GND plane(s) from vias placed directly under the large, square grounded Thermal Pad. 图 12-2 shows the minimum recommended via sizing for use under the thermal pad. The size is 8-mil hole and 16-mil diameter. This via size will allow for approximately 1.8-A of DC current rating at 1.5 mΩ of resistance with 1.3 nH of inductance. Some board manufacturers can guarantee vias with a 6-mile hole and 12-mil diameter using a standard mechanical drill. TI recommends to verify these numbers with board manufacturing processes used in fabrication of the PCB. This footprint is available for download on the TPS65981 product folder on the TPS65981 product folder.

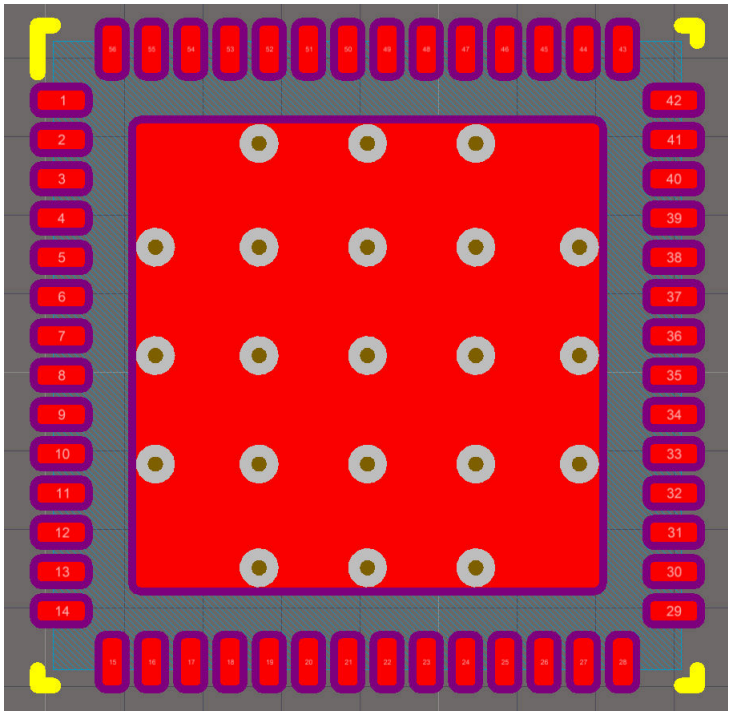


图 12-1. Top View Standard TPS65981 Footprint

图 12-2. Recommended Minimum Via Size

12.1.2 Top TPS65981 Placement and Bottom Component Placement and Layout

When the TPS65981 is placed on top and the components on bottom the solution size will be the smallest. For systems that do not use the optional external FET path the solution size will average less than 100 mm^2 (10 mm × 10 mm). Systems that implement the optional external FET path will average a solution size of less than 121 mm^2 (11 mm × 11 mm). These averages will vary with component selection (NFETs, Passives, etc.). The CSD87501L is used for back-to-back NFETs in a single WCSP package to reduce total solution size.

12.1.3 Component Placement

Placement of components on the top and bottom layers is used for this example to minimize solution size. The TPS65981 is placed on the top layer of the board and the majority of the components are placed on the bottom layer. When placing the components on the bottom layer, place them directly under the TPS65981 in a manner where the pads of the components are not directly under the void on the top layer. 图 12-3 and 图 12-4 show the placement in 2-D. 图 12-5 and 图 12-6 show the placement in 3-D.

12.1.4 Designs Rules and Guidance

When starting to route nets, start with 4 mil clearance spacing. The designer may have to adjust the 4mil clearance to 3.5 mil when fanning out the top layer routes. With the routing of the top layer having a tight clearance, TI recommends to have the layout grid snapped to 1 mil. For component spacing this design used 20 mil clearance between components. The silk screen around certain passive components may be deleted to allow for closer placement of components.

12.1.5 Routing PP_HV, PP_EXT, PP_5V0, and VBUS

On the top layer, create pours for PP_HV, PP_5V0 and VBUS to extend area to place 8 mil hole and 16 mil diameter vias to connect to the bottom layer. A minimum of 4 vias is needed to connect between the top and

bottom layer. For the bottom layer, place pours that will connect the PP_HV, PP_5V0, and VBUS capacitors to their respective vias. The external FETS connected from PP_EXT to VBUS (SENSEP, SENSEN, HV_GATE1, and HV_GATE2 pins of the TPS65981) must also be connected through pours and place vias for the external FET gates. For 5 A systems, special consideration must be taken for ensuring enough copper is used to handle the higher current. For 0.5 oz copper top or bottom pours with 0.5-oz plating use approximately a 120-mil pour width for 5-A support. When routing the 5 A through a 0.5 oz internal layer, more than 200 mil is required to carry the current. 图 12-7 and 图 12-8 show the pours used in this example.

12.1.6 Routing Top and Bottom Passive Components

The next step is to route the connections to the passive components on the top and bottom layers. For the top layer only CC1 and CC2 capacitors will be placed on top. Routing the CC1 and CC2 lines with a 8 mil trace will facilitate the needed current for supporting powered Type C cables through VCONN. For more information on VCONN please refer to the Type C specification. 图 12-9 shows how to route to the CC1 and CC2 to their respective capacitors. For capacitor GND pin use a 10 mil trace if possible. This particular system support Dead Battery, which has RPD_G1/2 connected to CC1/2.

The top layer pads will have to be connected the bottom placed component through Vias (8 mil hole and 16 mil diameter recommended). For the VIN_3V3, VDDIO, LDO_3V3, LDO_1V8A, LDO1 V8D, and LDO_BMC use 6mil traces to route. For PP_CABLE route using an 8 mil trace and for all other routes 4 mil traces may be used. To allow for additional space for routing, stagger the component vias to leave room for routing other signal nets. 图 12-10 and 图 12-11 show the top and bottom routing. 表 12-1 provides a summary of the trace widths.

表 12-1. Routing Trace Widths

ROUTE	WIDTH (mil)
CC1, CC2, PP_CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Thermal Pad (GND)	10

12.1.7 Thermal Pad Via Placement

The Thermal Pad under the TPS65981 is populated with 20 for thermal relief vias that must be electrically connected to GND. This can be seen in the 图 12-1 that is not connected to a PCB project. If any of the vias in the footprint are removed for placing components closer to the TPS65981, a minimum of 6 vias must be used for thermal dissipation to the GND planes. If the number of Thermal Relief vias is reduced, the majority of these vias must be placed on the right side of the device by the power path.

12.1.8 Top Layer Routing

Once the components are routed, the rest of the area can be used to route all of the additional I/O. After all nets have been routed place polygonal pours around the PP_5V0, PP_HV, and VBUS pins of the TPS65981 GND pins to the GND vias. Refer to 图 12-12 for the final top routing.

12.1.9 Inner Signal Layer Routing

The inner signal layer is used to route the I/O, low-speed data signals, and the external FET control and sensing of the TPS65981 away from the critical thick power traces and length-sensitive high-speed data 图 12-13 shows how to route the internal layer.

12.1.10 Bottom Layer Routing

The bottom layer has most of the components placed and routed already. Place a polygon pour to connect all of the GND nets and vias on the bottom layer, refer to 图 12-14.

12.2 Layout Example

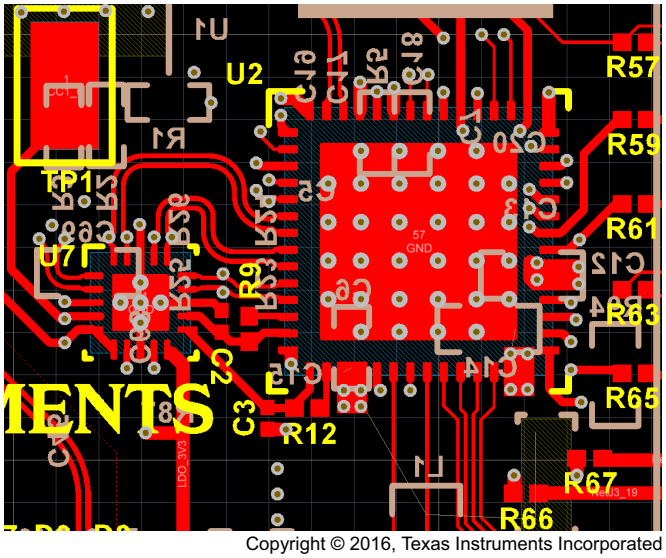


图 12-3. Example Layout (Top View in 2-D)

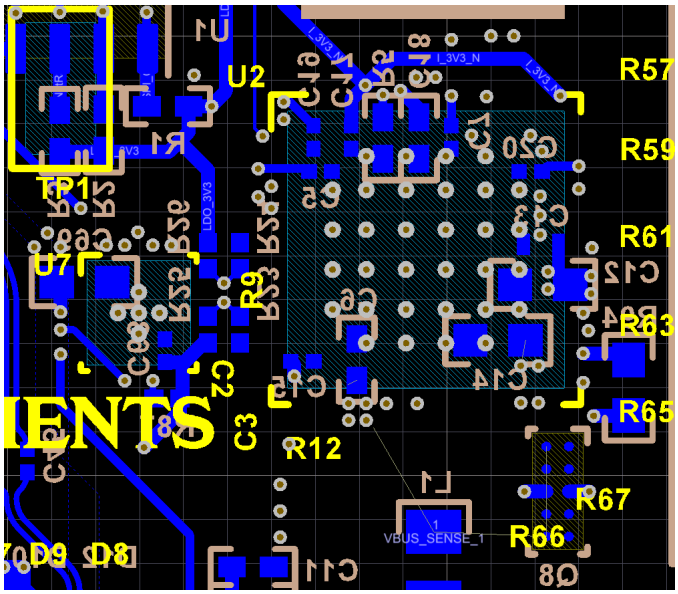


图 12-4. Example Layout (Bottom View in 2-D)

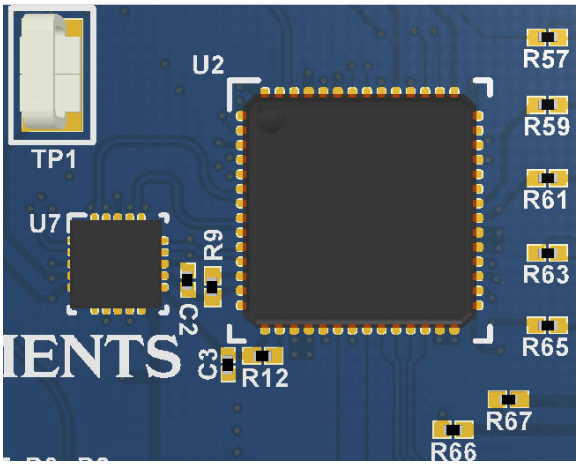


图 12-5. Example Layout (Top View in 3-D)

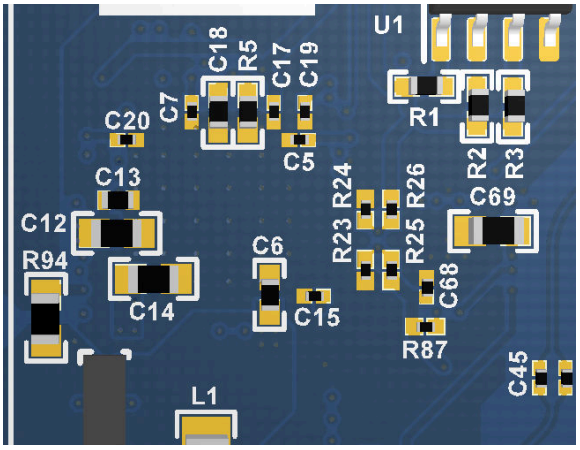


图 12-6. Example Layout (Bottom View in 3-D)

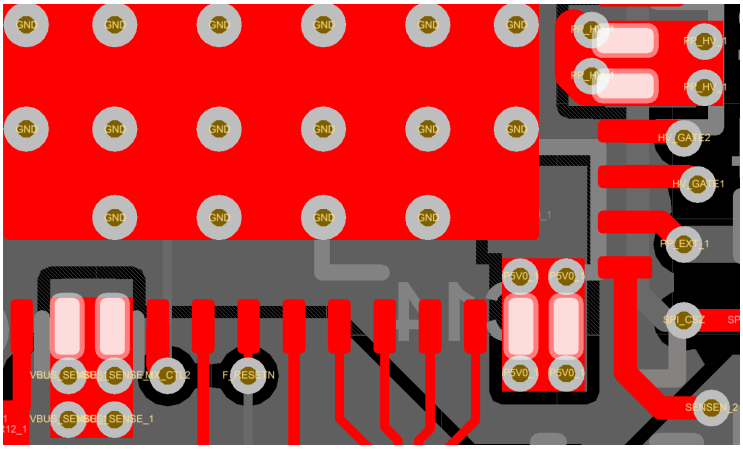


图 12-7. Top Polygonal Pours

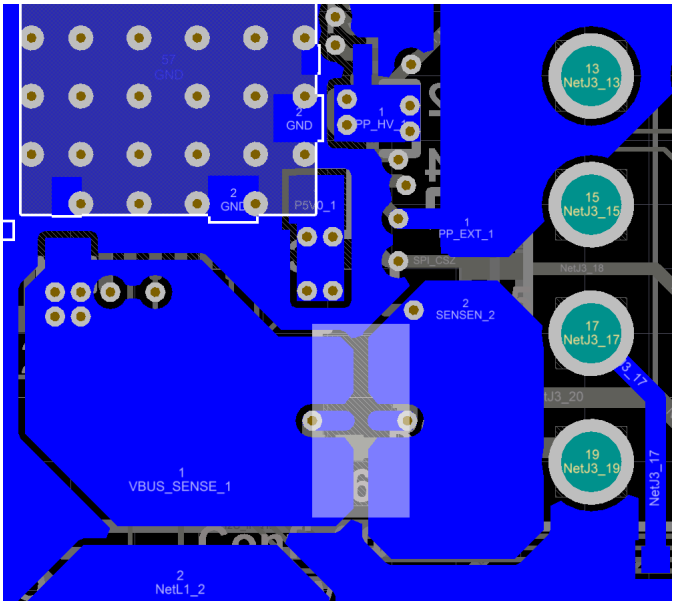


图 12-8. Bottom Polygonal Pours

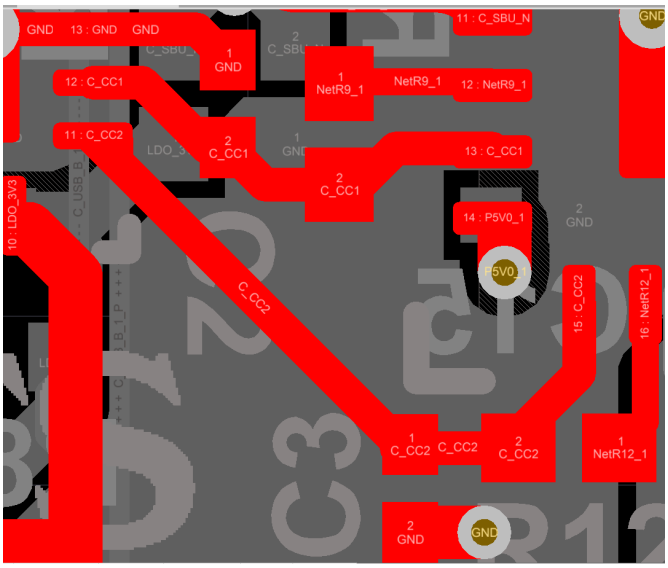


图 12-9. CC1 and CC2 Capacitor Routing

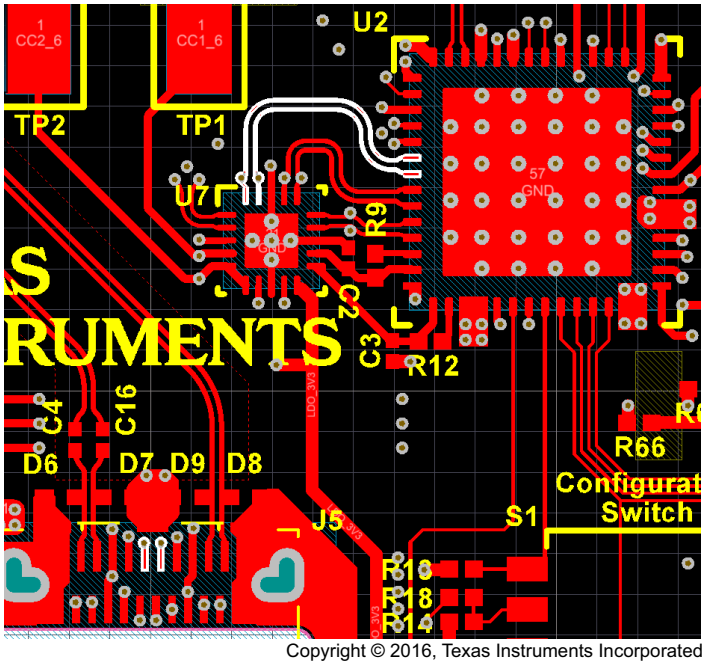


图 12-10. Top Layer Component Routing

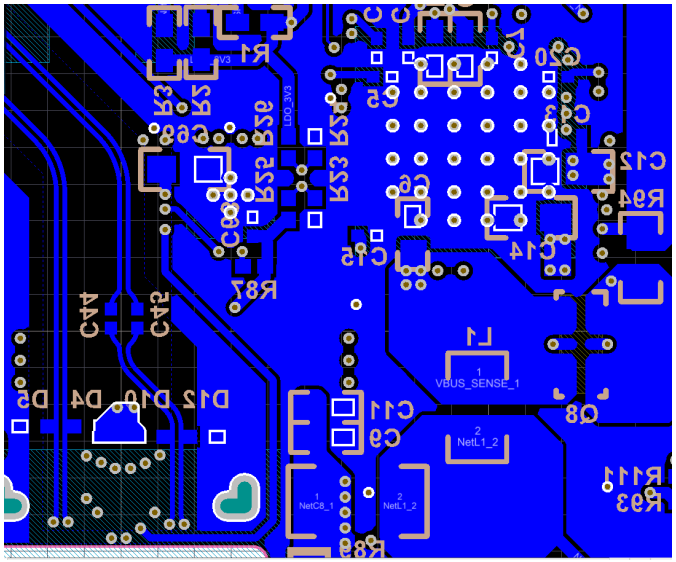


图 12-11. Bottom Layer Component Routing

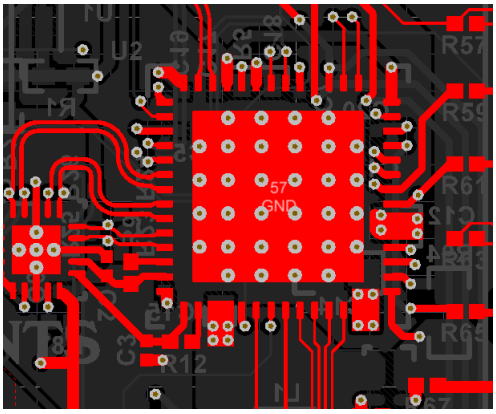


图 12-12. Final Routing (Top Layer)

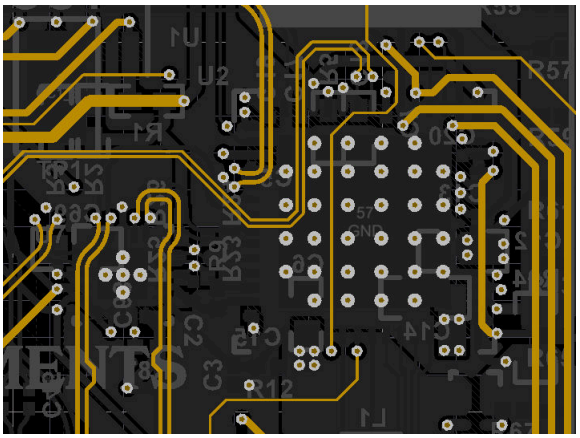


图 12-13. Final Routing (Inner Signal Layer)

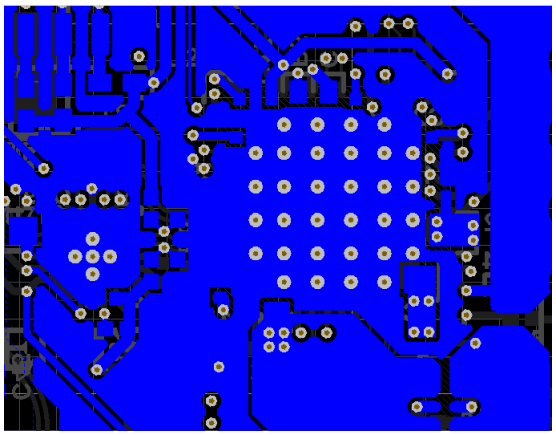


图 12-14. Final Routing (Bottom Layer)

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

TPS65981 Tools and Software: http://www.ti.com/product/TPS65981/toolssoftware

For the TPS65981ABZQZR IBIS Model, see SLVMBQ9

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

- USB Power Delivery Specification, Revision 2.0, Version 1.2 (March 25th, 2016)
- USB Type-C Specification, Revision 1.2 (March 25th, 2016)
- USB Battery Charging Specification, Revision 1.2 (December 7th, 2010)
- *TPS65981, TPS65982, and TPS65986 Firmware User's Guide* (SLVUAH7)
- *TPS65981, TPS65982, and TPS65986 Host Interface Technical Reference Manual* (SLVUAN1)
- W25Q20CL data sheet, *8M-Bit, 16M-Bit and 32M-Bit Serial Flash Memory With Dual and Quad SPI*
- NSR20F30NXT5G data sheet, *Schottky Barrier Diode*

13.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.5 Trademarks

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

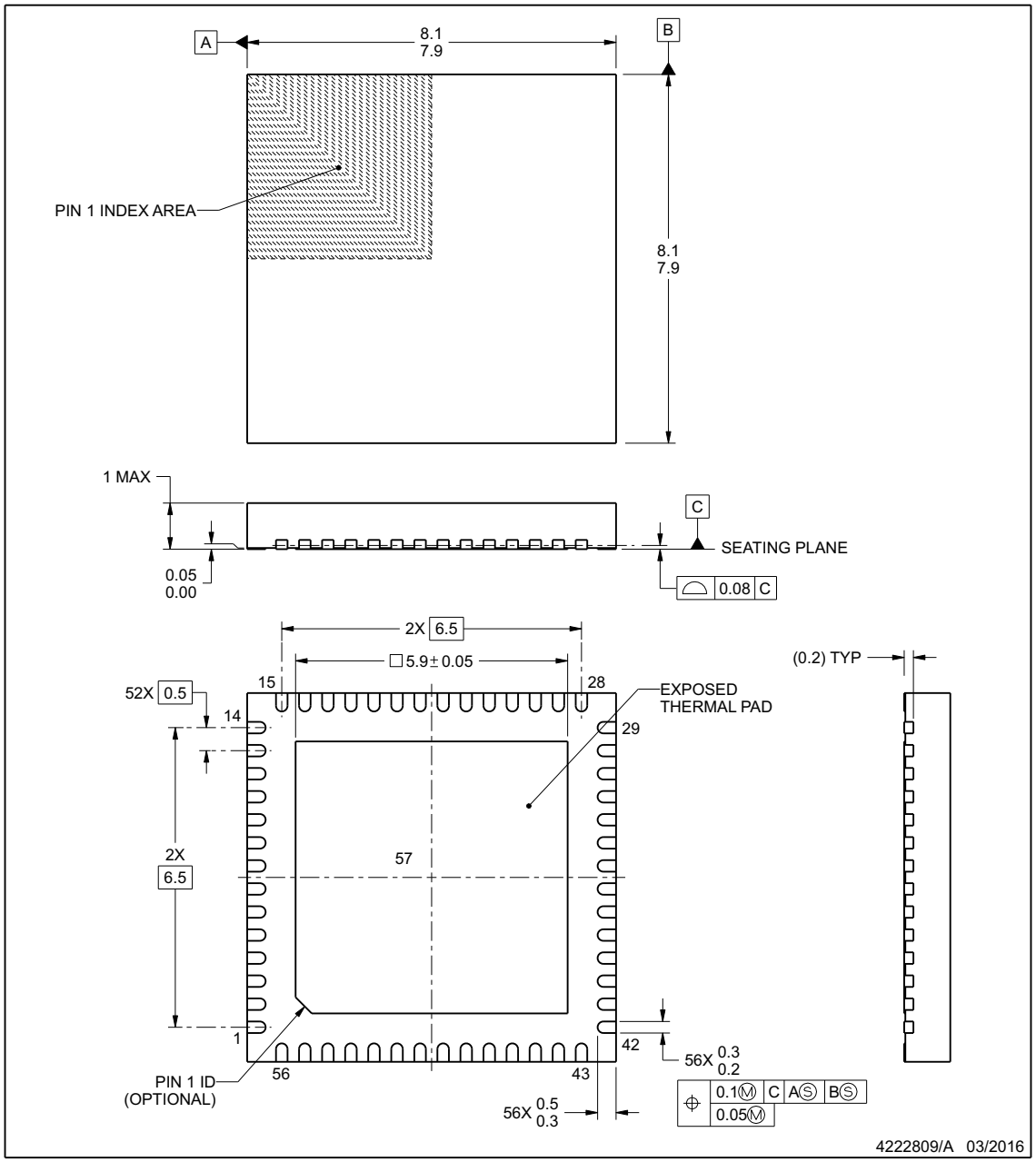
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RTQ0056H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

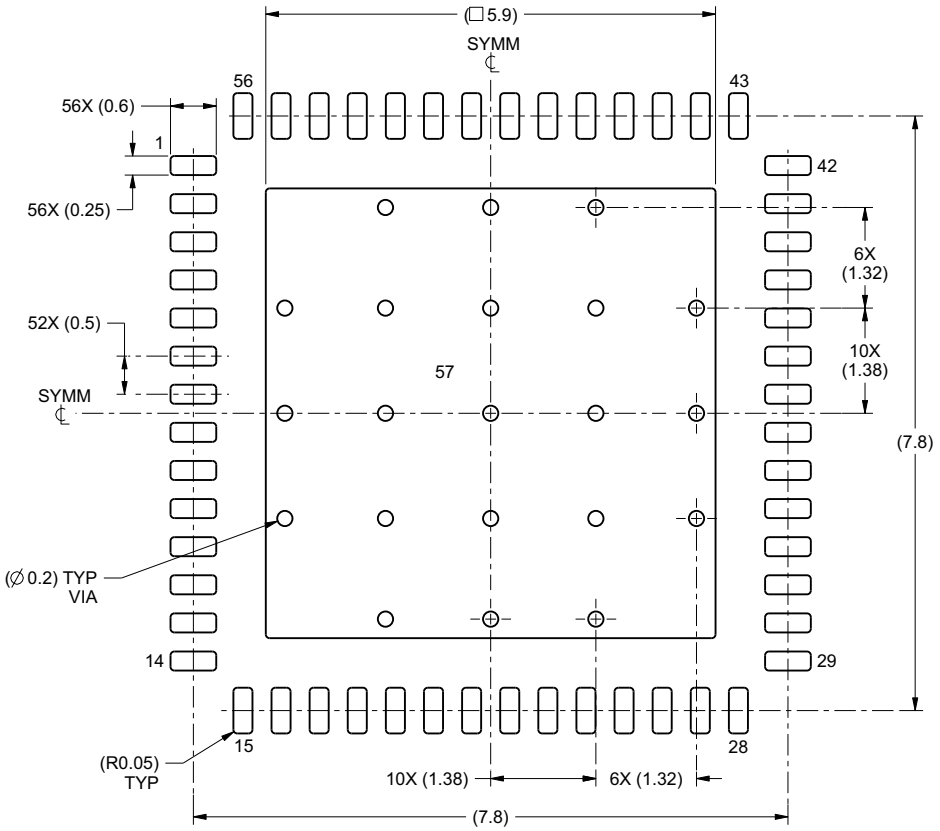
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

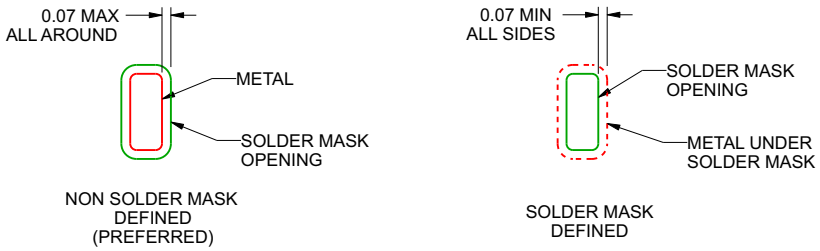
RTQ0056H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

4222809/A 03/2016

NOTES: (continued)

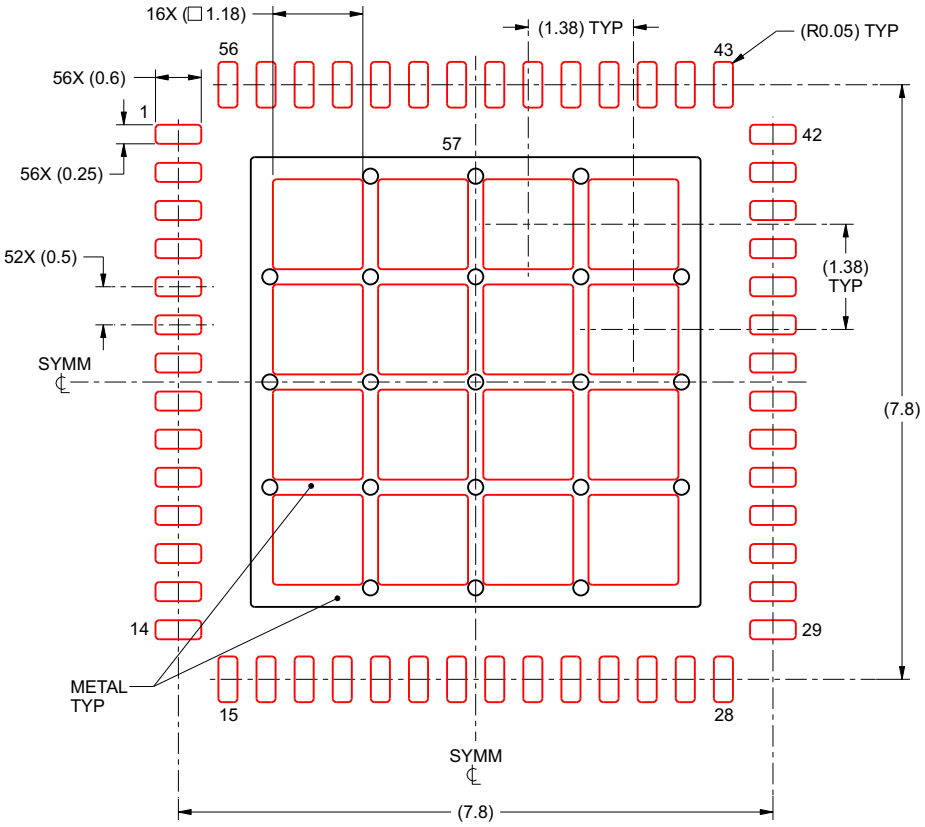
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTQ0056H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
64% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

4222809/A 03/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65981ABIRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	65981ABI	Samples
TPS65981ABIRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	65981ABI	Samples
TPS65981ABTRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	65981ABT	Samples
TPS65981ABTRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	65981ABT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

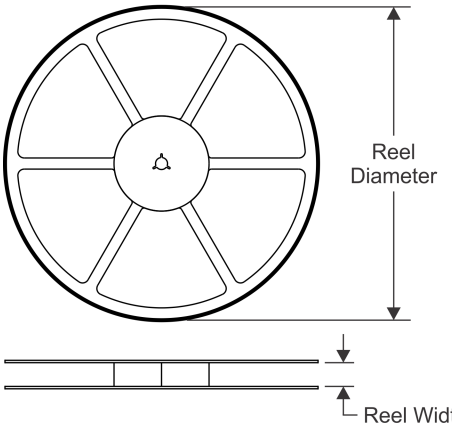
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

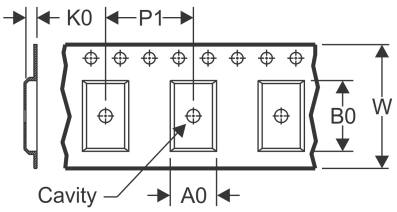
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

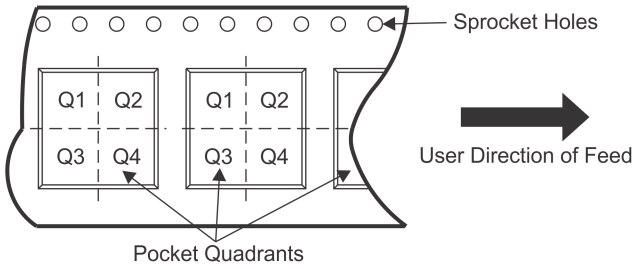


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

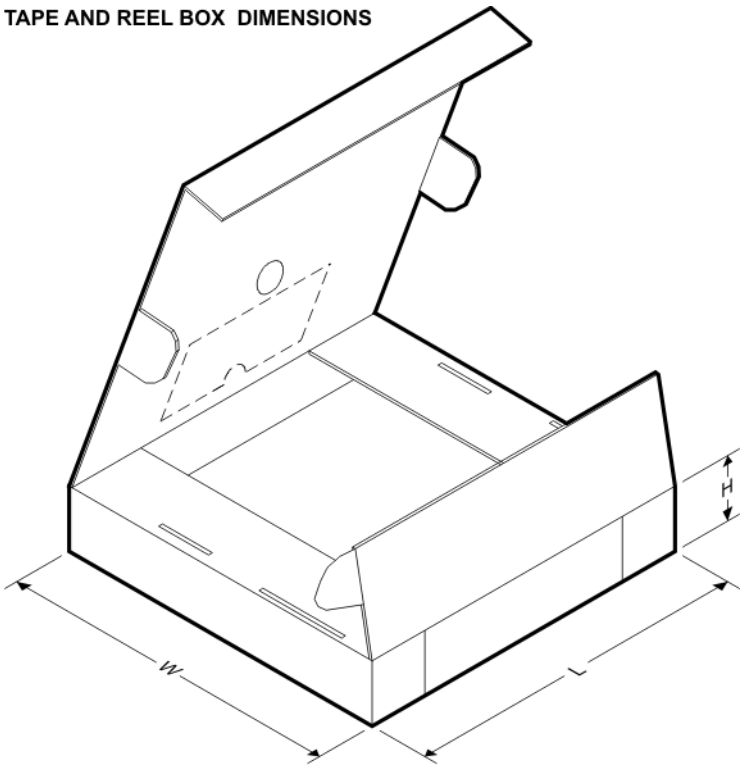
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65981ABIRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS65981ABIRTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS65981ABTRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS65981ABTRTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65981ABIRTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
TPS65981ABIRTQT	QFN	RTQ	56	250	210.0	185.0	35.0
TPS65981ABTRTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
TPS65981ABTRTQT	QFN	RTQ	56	250	210.0	185.0	35.0

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