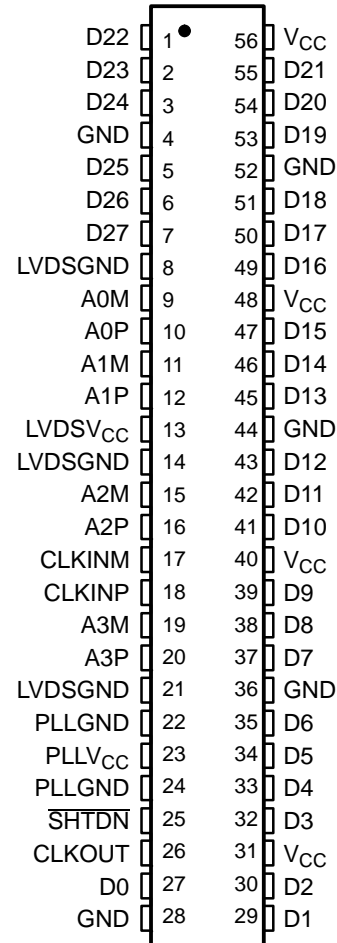


## LVDS SERDES RECEIVER

### FEATURES

- 4:28 Data Channel Expansion at up to 1.904 Gigabits per Second Throughput
- Suited for Point-to-Point Subsystem Communication With Very Low EMI
- 4 Data Channels and Clock Low-Voltage Differential Channels in and 28 Data and Clock Out Low-Voltage TTL Channels Out
- Operates From a Single 3.3-V Supply and 250 mW (Typ)
- 5-V Tolerant  $\overline{\text{SHTDN}}$  Input
- Rising Clock Edge Triggered Outputs
- Bus Pins Tolerate 4-kV HBM ESD
- Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch
- Consumes <1 mW When Disabled
- Wide Phase-Lock Input Frequency Range 20 MHz to 68 MHz
- No External Components Required for PLL
- Meets or Exceeds the Requirements of ANSI EIA/TIA-644 Standard
- Industrial Temperature Qualified  
 $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$
- Replacement for the DS90CR286

**DGG PACKAGE  
(TOP VIEW)**



### DESCRIPTION

The SN65LVDS94 LVDS serdes (serializer/deserializer) receiver contains four serial-in 7-bit parallel-out shift registers, a 7x clock synthesizer, and five low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN65LVDS93 and SN65LVDS95, over five balanced-pair conductors and expansion to 28 bits of single-ended LVTTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at the rate seven times the LVDS input clock (CLKIN). The data is then unloaded to a 28-bit wide LVTTTL parallel bus at the CLKIN rate. A phase-locked loop clock synthesizer circuit generates a 7x clock for internal clocking and an output clock for the expanded data. The SN65LVDS94 presents valid data on the rising edge of the output clock (CLKOUT).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



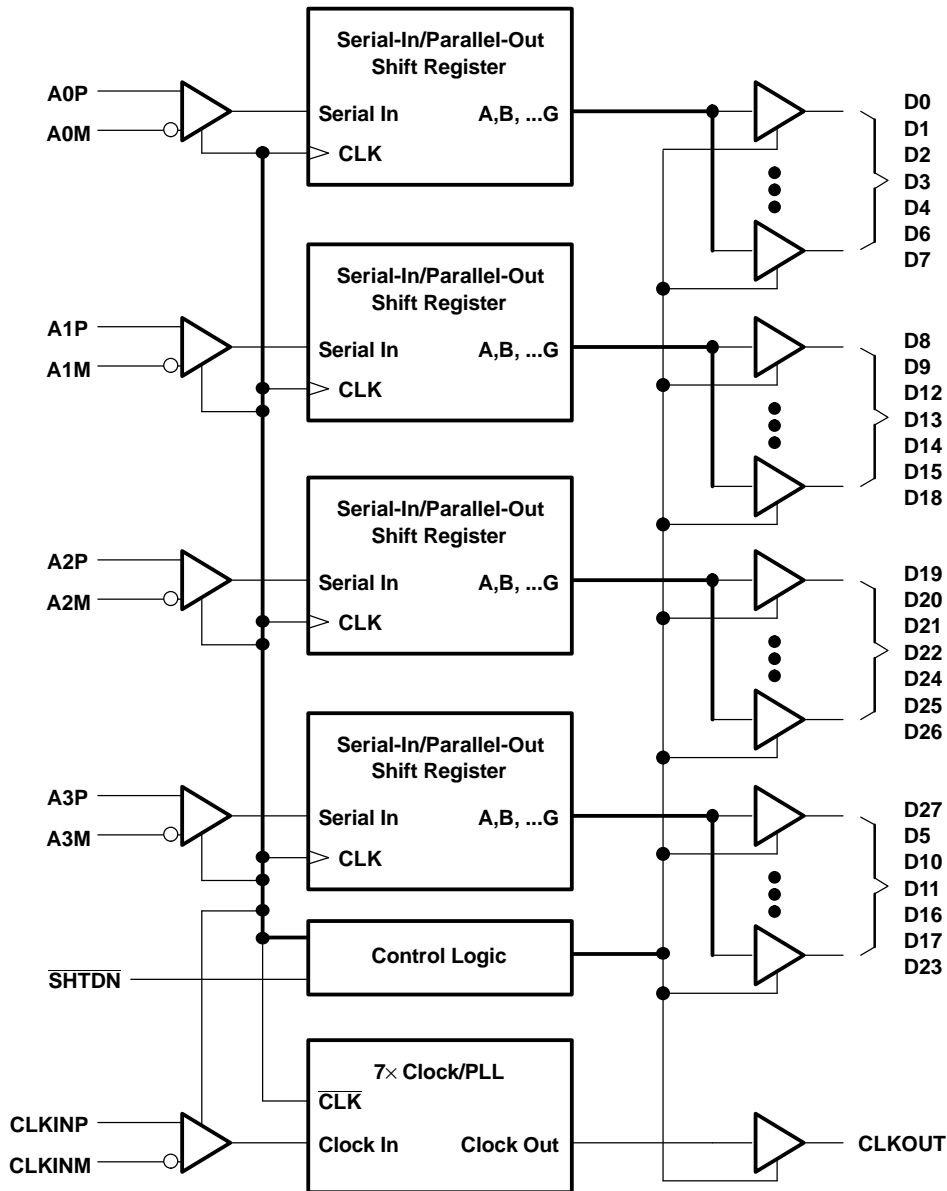
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

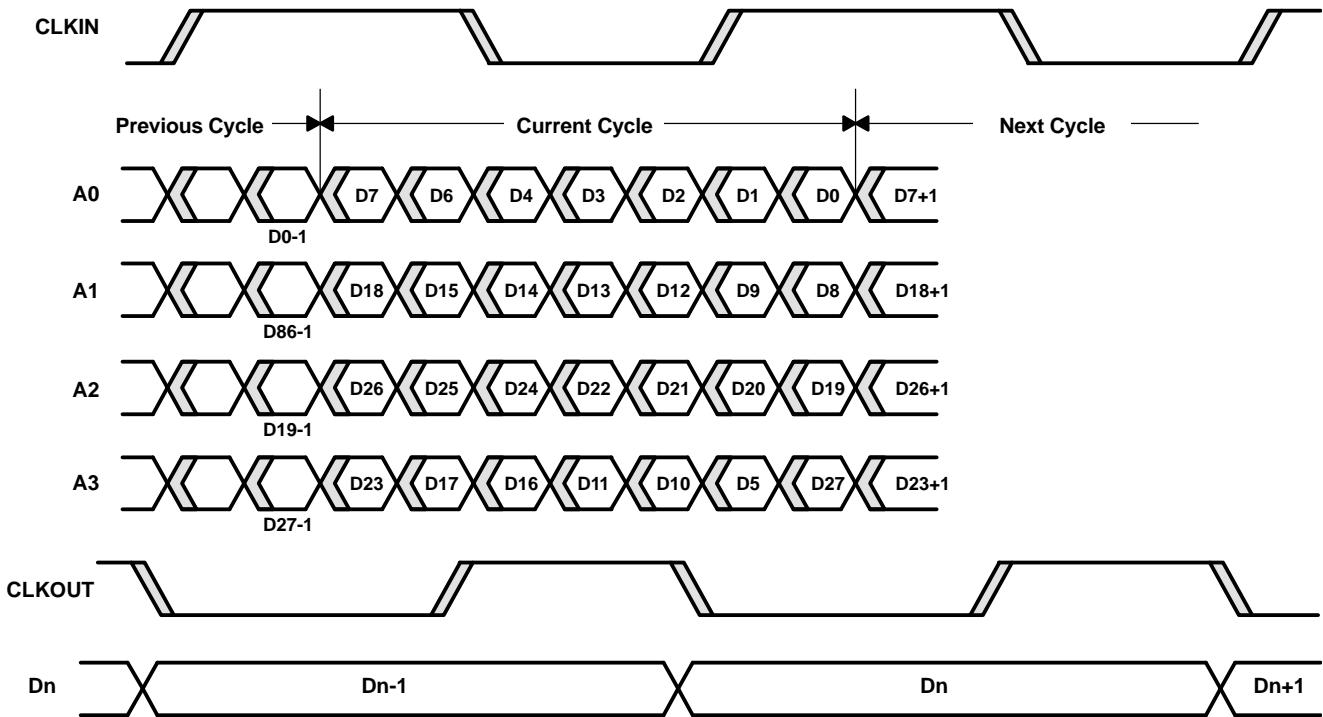
**DESCRIPTION (CONTINUED)**

The SN65LVDS94 requires only five line termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear (SHTDN) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN65LVDS94 is characterized for operation over ambient air temperatures of -40°C to 85°C.

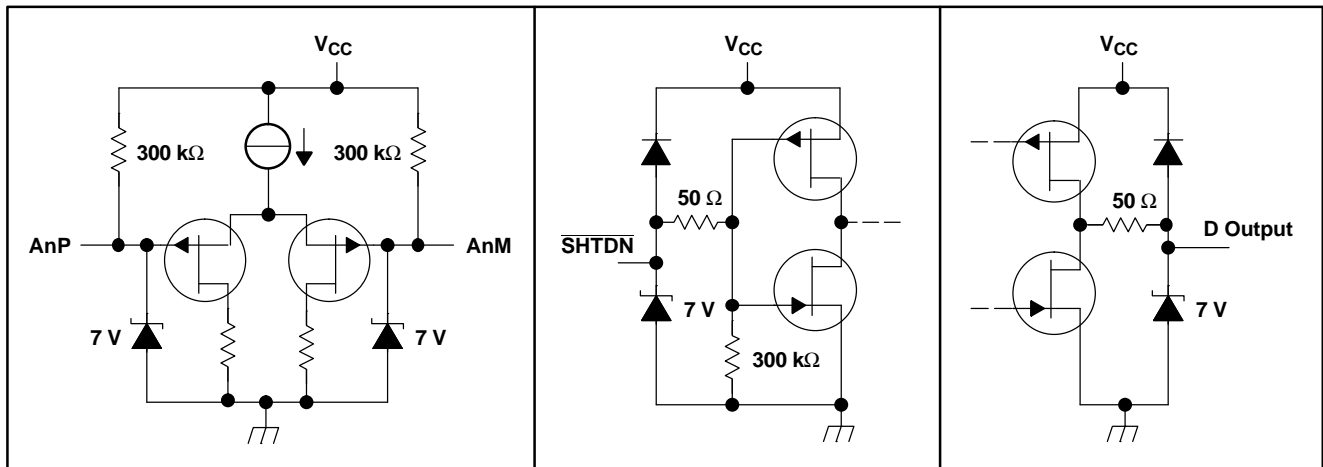
**FUNCTIONAL BLOCK DIAGRAM**





**Figure 1. SN65LVDS94 Load and Shift Sequences**

**EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**



**ABSOLUTE MAXIMUM RATINGS**over operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

		UNIT
$V_{CC}^{(2)}$	Supply voltage range	-0.3 V to 4 V
	Voltage range at any terminal (except $\overline{SHTDN}$ )	-0.5 V to $V_{CC} + 0.5$ V
	Voltage range at $\overline{SHTDN}$ terminal	-0.5 V to $V_{CC} + 3$ V
	Electrostatic discharge <sup>(3)</sup>	Bus pins (Class 3A)
		Bus pins (Class 2B)
		All pins (Class 3A)
		All pins (Class 2B)
	Continuous total power dissipation	(see Dissipation Rating Table)
$T_A$	Operating free-air temperature range	-40°C to 85°C
$T_{stg}$	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals unless otherwise noted.
- (3) This rating is measured using MIL-STD-883C Method, 3015.7.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGG	1377 mW	11 mW/°C	882 mW	717 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.3	3.6	V
$V_{IH}$	High-level input voltage ( $\overline{SHTDN}$ )	2			
$V_{IL}$	Low-level input voltage ( $\overline{SHTDN}$ )			0.8	
$ V_{ID} $	Magnitude of differential input voltage	0.1		0.6	
$V_{IC}$ , see Figure 2 and Figure 3	Common-mode input voltage	$\frac{ V_{ID} }{2}$	$2.4 - \frac{ V_{ID} }{2}$	$V_{CC} - 0.8$	
$T_A$	Operating free-air temperature	-40		85	°C

**TIMING REQUIREMENTS**

		MIN	NOM	MAX	UNIT
$t_c^{(1)}$	Input clock period	14.7	$t_c$	50	ns

- (1)  $t_c$  is defined as the mean duration of a minimum of 32,000 clock periods.

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IT+</sub> Positive-going differential input voltage threshold				100	mV
V <sub>IT-</sub> Negative-going differential input voltage threshold <sup>(2)</sup>		-100			
V <sub>OH</sub> High-level output voltage	I <sub>OH</sub> = -4 mA	2.4			V
V <sub>OL</sub> Low-level output voltage	I <sub>OL</sub> = 4 mA			0.4	V
I <sub>CC</sub> Quiescent current (average)	Disabled, all inputs open			280	μA
	Enabled, AnP at 1 V and AnM at 1.4 V, t <sub>c</sub> = 15.38 ns		62	84	mA
	Enabled, C <sub>L</sub> = 8 pF (5 places), Worst-case pattern, see Figure 4, t <sub>c</sub> = 15.38 ns			107	mA
I <sub>IH</sub> High-level input current ( $\overline{\text{SHTDN}}$ )	V <sub>IH</sub> = V <sub>CC</sub>			±20	μA
I <sub>IL</sub> Low-level input current ( $\overline{\text{SHTDN}}$ )	V <sub>IL</sub> = 0 V			±20	μA
I <sub>IN</sub> Input current (A and CLKIN inputs)	0 V ≤ V <sub>I</sub> ≤ 2.4 V			±20	μA
I <sub>OZ</sub> High-impedance output current	V <sub>O</sub> = 0 V or V <sub>CC</sub>			±10	μA

(1) All typical values are V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>su</sub> Data setup time, D0 through D27 to CLKOUT	C <sub>L</sub> = 8 pF See Figure 5	4	6		ns
t <sub>h</sub> Data hold time, CLKOUT to D0 through D27		4	6		
t <sub>RSKM</sub> Receiver input skew margin <sup>(1)</sup> , see Figure 6	t <sub>c</sub> = 15.38 ns (±0.2%),  Input clock jitter  < 50 ps <sup>(2)</sup>	490	800		ps
	T <sub>A</sub> = 0°C to 85°C T <sub>A</sub> = -40°C to 0°C	390			
t <sub>d</sub> Delay time, input clock to output clock, see Figure 6	t <sub>c</sub> = 15.38 ns (±0.2%)		3.7		ns
Δt <sub>C(O)</sub> Change in output clock period from cycle to cycle <sup>(3)</sup>	t <sub>c</sub> = 15.38 + 0.75 sin(2π500E3t) ± 0.05 ns, See Figure 7		±80		ps
	t <sub>c</sub> = 15.38 + 0.75 sin(2π3E6t) ± 0.05 ns, See Figure 7		±300		
t <sub>en</sub> Enable time, $\overline{\text{SHTDN}}$ to phase lock	See Figure 8		1		ms
t <sub>dis</sub> Disable time, $\overline{\text{SHTDN}}$ to Off state	See Figure 9		400		ns
t <sub>t</sub> Output transition time (t <sub>r</sub> or t <sub>f</sub> )	C <sub>L</sub> = 8 pF		3		ns
t <sub>w</sub> Output clock pulse duration			0.43 t <sub>c</sub>		ns

- (1) t<sub>RSKM</sub> is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. It is defined by  $\frac{t_c}{14} - t_s/h$ .
- (2) |Input clock jitter| is the magnitude of the change in the input clock period.
- (3) Δt<sub>C(O)</sub> is the change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.

PARAMETER MEASUREMENT INFORMATION

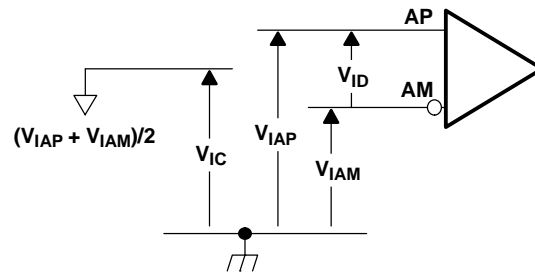


Figure 2. Voltage Definitions

COMMON-MODE INPUT VOLTAGE  
vs  
DIFFERENTIAL INPUT VOLTAGE AND  $V_{CC}$

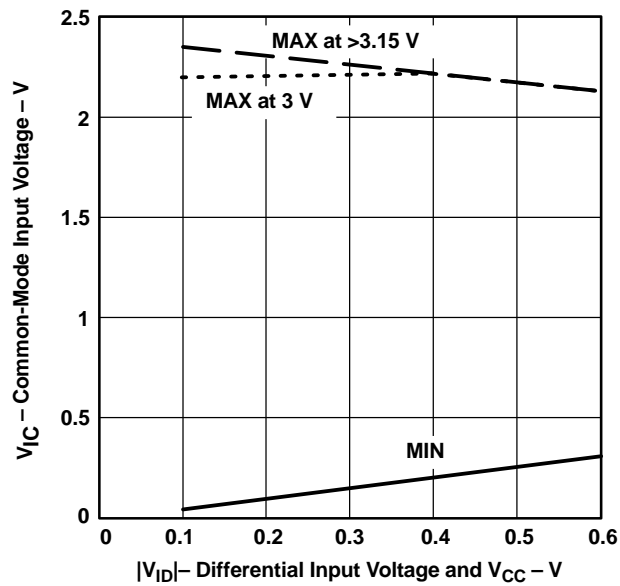
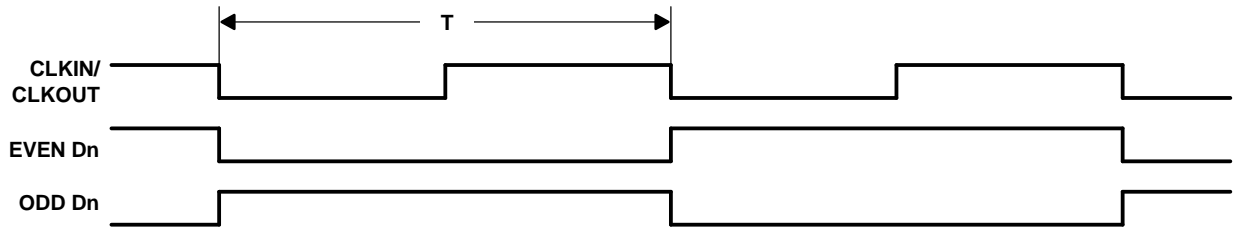
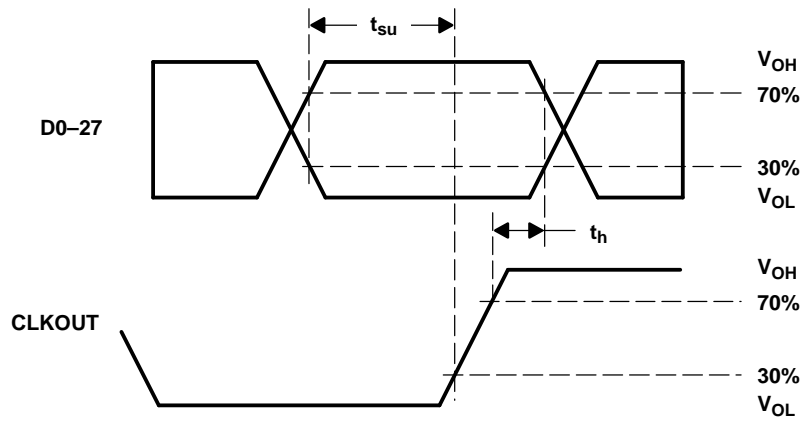


Figure 3. Recommended  $V_{IC}$  Versus  $V_{ID}$  and  $V_{CC}$

**PARAMETER MEASUREMENT INFORMATION (continued)**

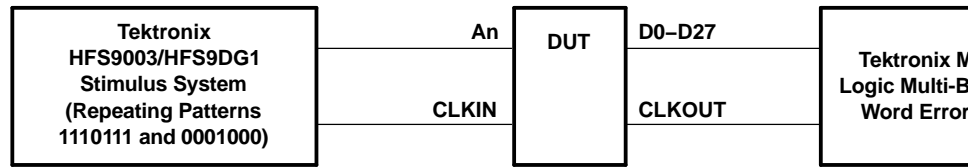


**Figure 4. Worst-Case Power Test Pattern**



**Figure 5. Setup and Hold Time Measurements**

PARAMETER MEASUREMENT INFORMATION (continued)



CLKIN is advanced or delayed with respect to data until errors are observed at the receiver output. The magnitude of the advance or delay is  $t_{RSKM}$ .

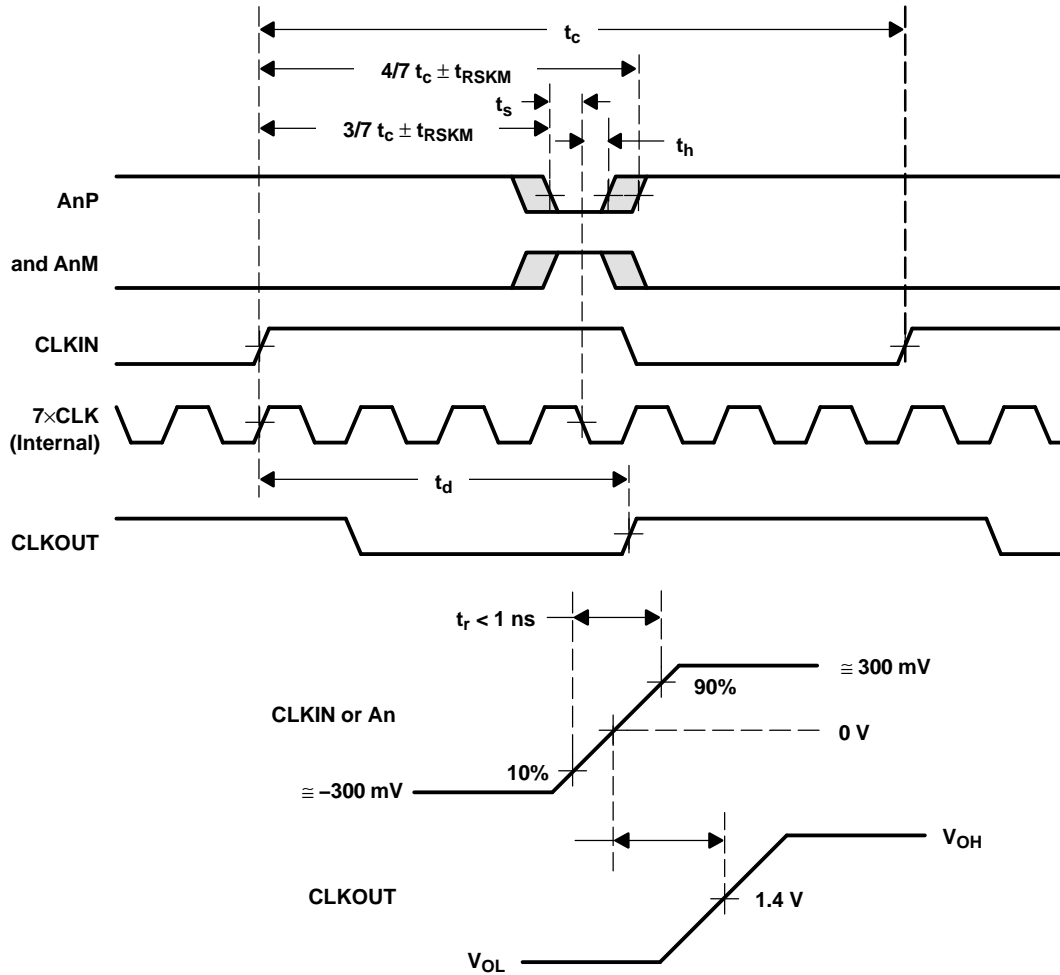


Figure 6. Receiver Input Skew Margin and  $t_d$  Definitions



PARAMETER MEASUREMENT INFORMATION (continued)

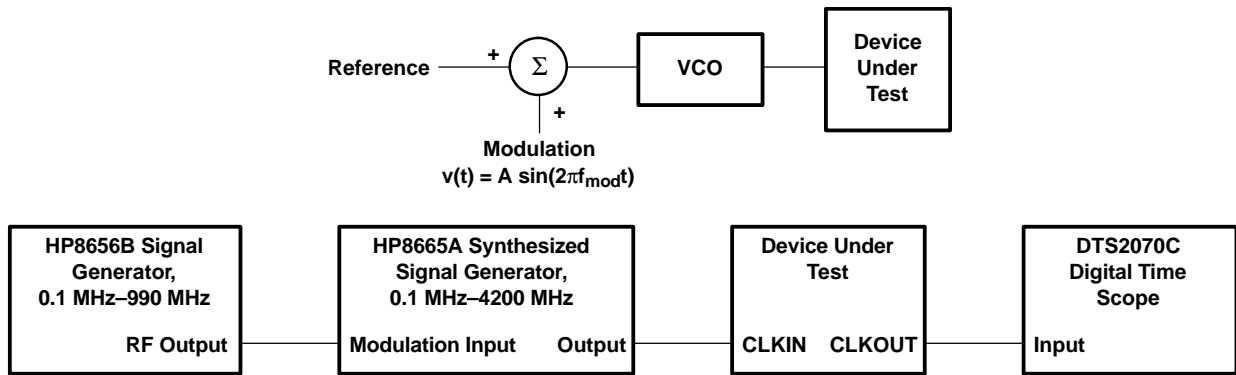


Figure 7. Output Clock Jitter Test Setup

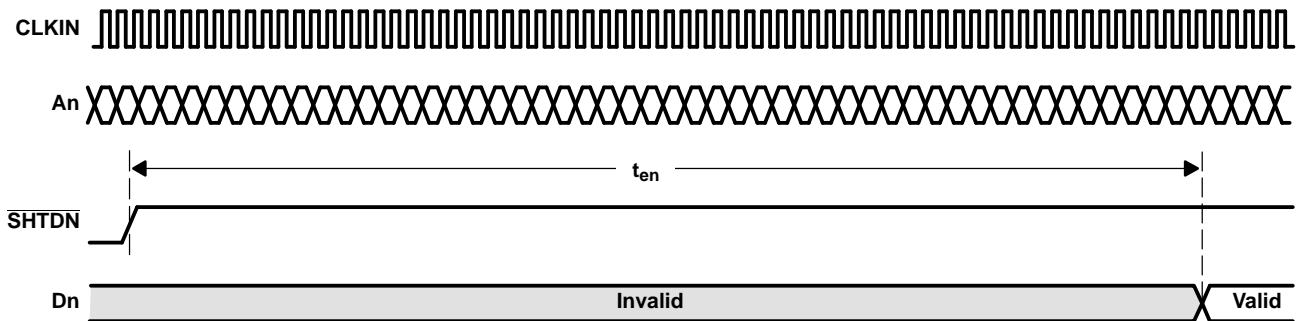


Figure 8. Enable Time Waveforms

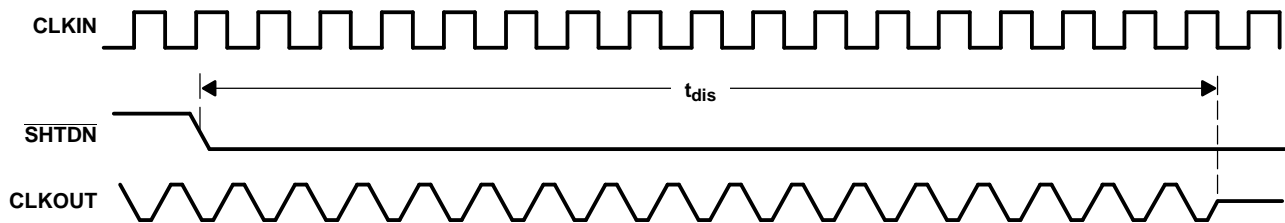


Figure 9. Disable Time Waveforms

**TYPICAL CHARACTERISTICS**  
**WORST-CASE SUPPLY CURRENT**  
**vs**  
**FREQUENCY**

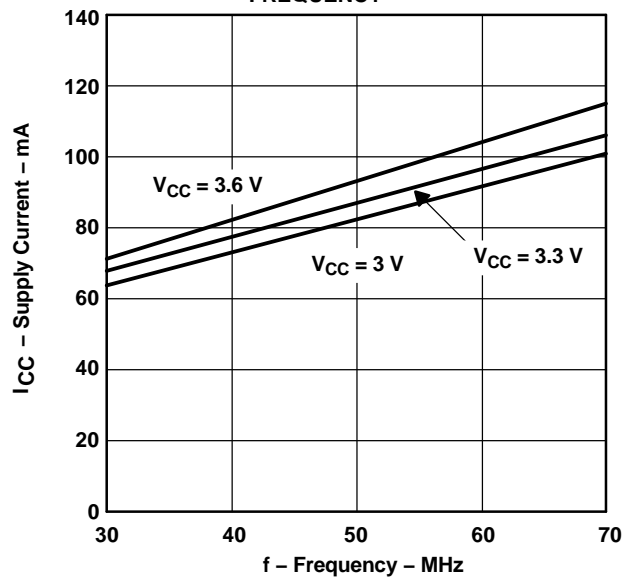
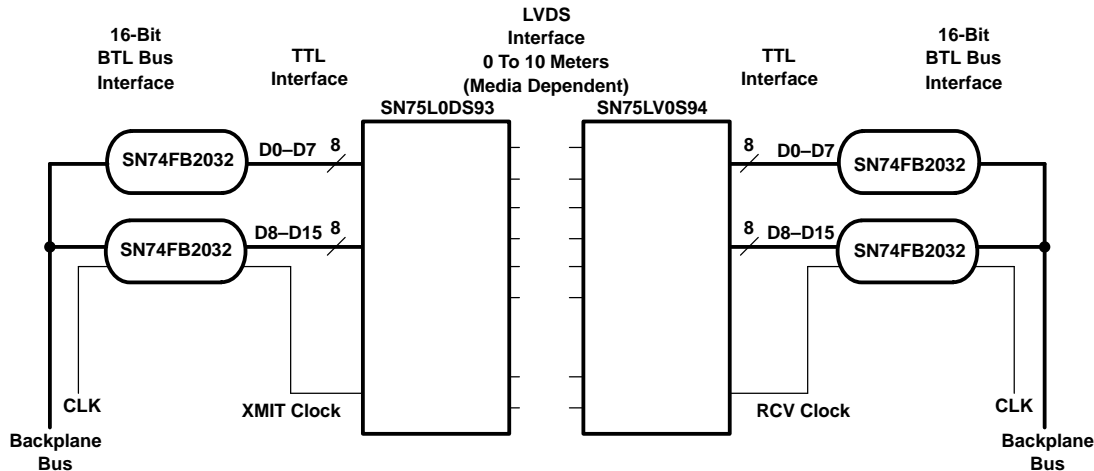


Figure 10.

**APPLICATION INFORMATION**

**16-BIT BUS EXTENSION**

In a 16-bit bus application (Figure 11), TTL data and clock coming from bus transceivers that interface the backplane bus arrive at the Tx parallel inputs of the LVDS serdes transmitter. The clock associated with the bus is also connected to the device. The on-chip PLL synchronizes this clock with the parallel data at the input. The data is then multiplexed into three different line drivers which perform the TTL to LVDS conversion. The clock is also converted to LVDS and presented to a separate driver. This synchronized LVDS data and clock at the receiver, which recovers the LVDS data and clock, performs a conversion back to TTL. Data is then demultiplexed into a parallel format. An on-chip PLL synchronizes the received clock with the parallel data, and then all are presented to the parallel output port of the receiver.



**Figure 11. 16-Bit Bus Extension**

**16-BIT BUS EXTENSION WITH PARITY**

In the previous application we did not have a checking bit that would provide assurance that the data crosses the link. If we add a parity bit to the previous example, we would have a diagram similar to the one in Figure 12. The device following the SN74FB2032 is a low cost parity generator. Each transmit-side transceiver/parity generator takes the LVTTTL data from the corresponding transceiver, performs a parity calculation over the byte, and then passes the bits with its calculated parity value on the parallel input of the LVDS serdes transmitter. Again, the on-chip PLL synchronizes this transmit clock with the eighteen parallel bits (16 data + 2 parity) at the input. The synchronized LVDS data/parity and clock arrive at the receiver.

The receiver performs the conversion from LVDS to LVTTTL and the transceiver/parity generator performs the parity calculations. These devices compare their corresponding input bytes with the value received on the parity bit. The transceiver/parity generator will assert its parity error output if a mismatch is detected.

APPLICATION INFORMATION (continued)

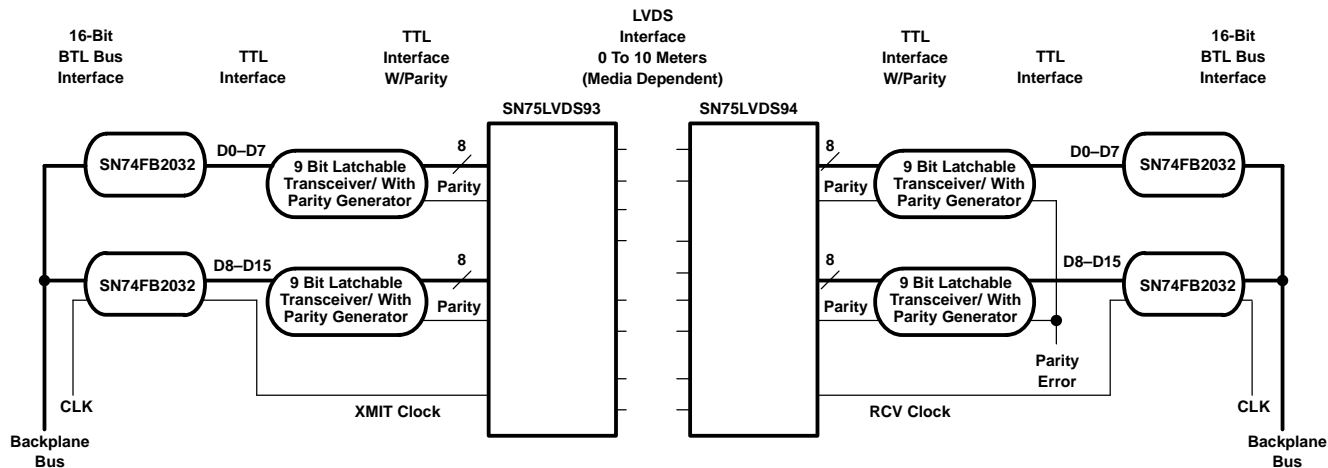


Figure 12. 16-Bit Bus Extension With Parity

LOW COST VIRTUAL BACKPLANE TRANSCEIVER

Figure 13 represents LVDS serdes in an application as a virtual backplane transceiver (VBT). The concept of a VBT can be achieved by implementing individual LVDS serdes chipsets in both directions of subsystem serialized links.

Depending on the application, the designer will face varying choices when implementing a VBT. In addition to the devices shown in Figure 13, functions such as parity and delay lines for control signals could be included. Using additional circuitry, half-duplex or full-duplex operation can be achieved by configuring the clock and control lines properly.

The designer may choose to implement an independent clock oscillator at each end of the link and then use a PLL to synchronize LVDS serdes's parallel I/O to the backplane bus. Resynchronizing FIFOs may also be required.

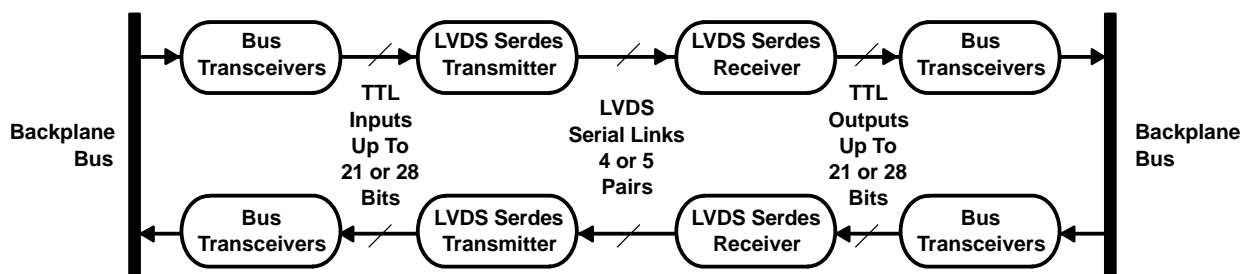


Figure 13. Virtual Backplane Transceiver

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS94DGG	ACTIVE	TSSOP	DGG	56	35	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		SN65LVDS94	<b>Samples</b>
SN65LVDS94DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN65LVDS94	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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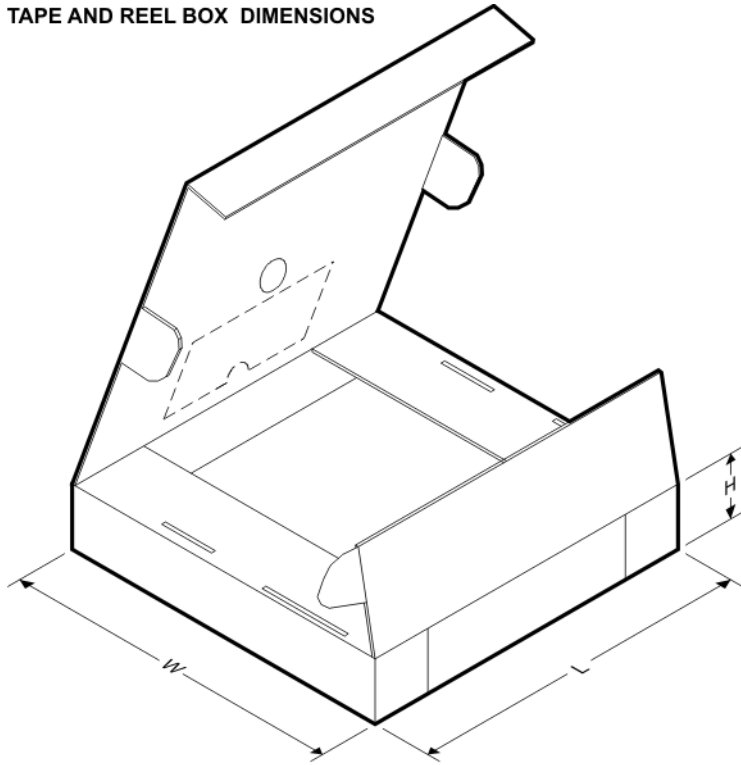


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

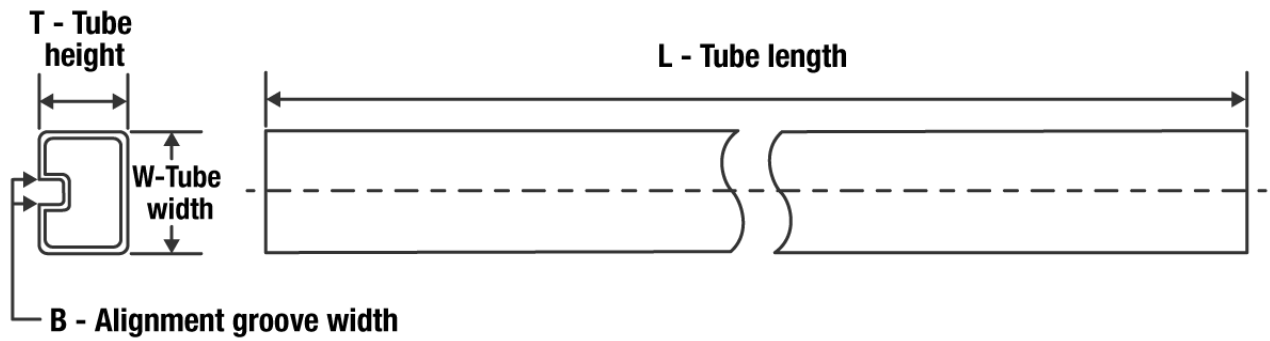
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS94DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS94DGGR	TSSOP	DGG	56	2000	350.0	350.0	43.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LVDS94DGG	DGG	TSSOP	56	35	530	11.89	3600	4.9

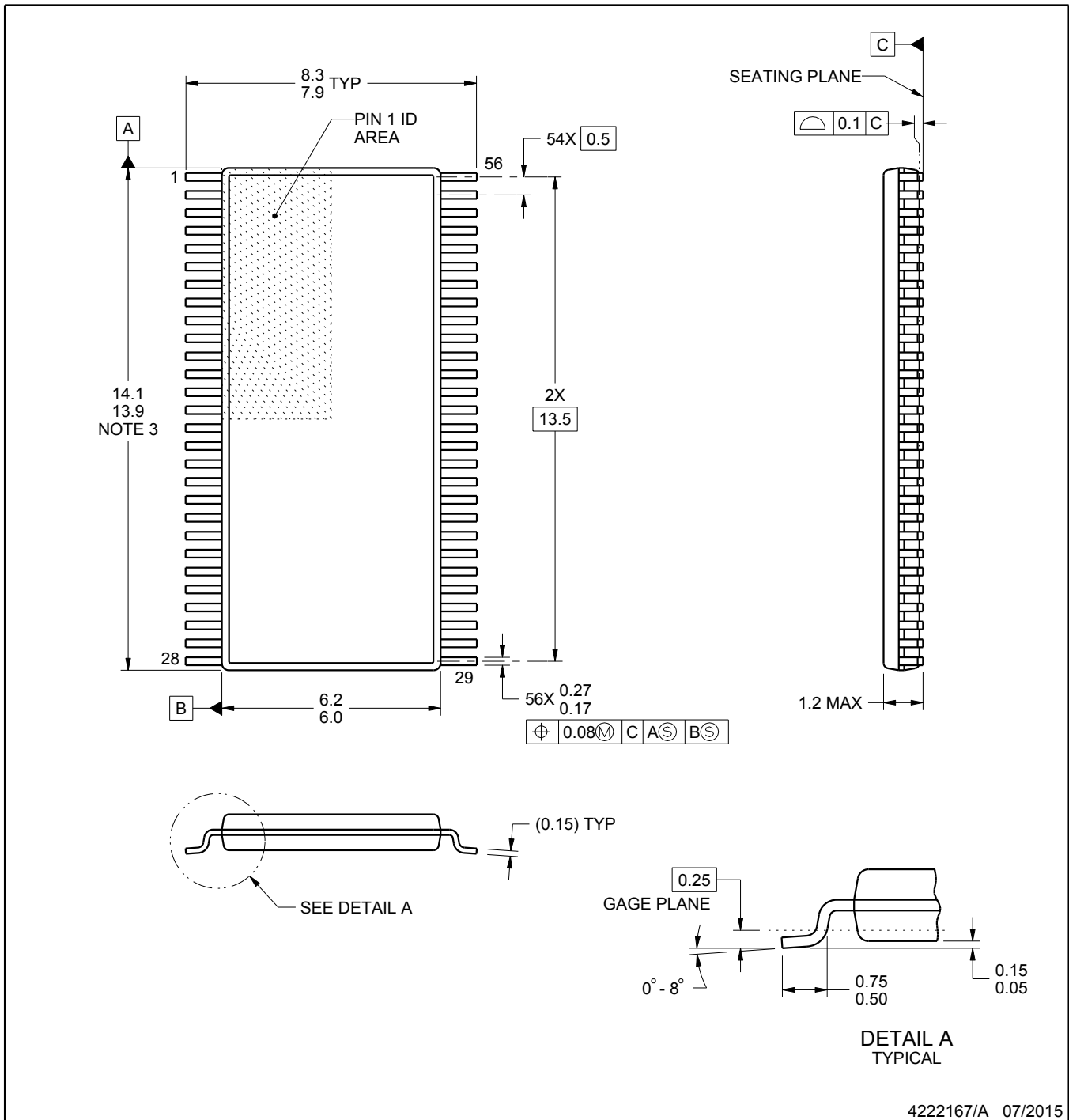
# DGG0056A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

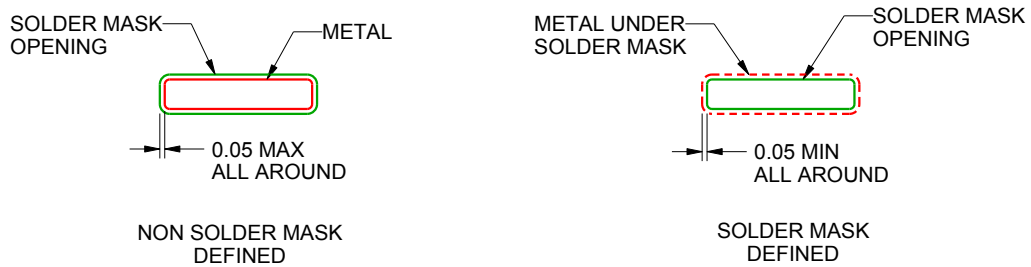
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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